

iSBC 534

FOUR CHANNEL COMMUNICATION EXPANSION BOARD

iSBC 80 serial I/O expansion through four programmable synchronous and asynchronous communications channels

Individual software programmable baud rate generation for each serial I/O channel

Two independent programmable 16-bit interval timers

Sixteen maskable interrupt request lines with priority encoded and programmable interrupt algorithms

Jumper selectable interface register addresses

16-Bit parallel I/O interface compatible with Bell 801 automatic calling unit

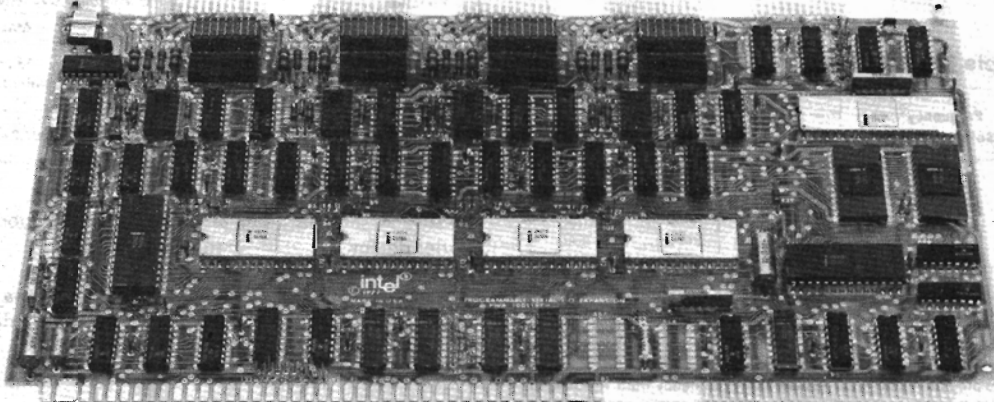
RS232C/CCITT V.24 interfaces plus 20 mA optically isolated current loop interfaces (sockets)

Programmable digital loopback for diagnostics

Interface control for auto answer and auto originate modems

The iSBC 534 Four Channel Communication Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 534 interfaces directly to any iSBC 80 single board computer via the system bus to provide expansion of system serial communications capability. Four fully programmable synchronous and asynchronous serial channels with RS232C buffering and provision for 20 mA optically isolated current loop buffering are provided. Baud rates, data formats, and interrupt priorities for each channel are individually software selectable. In addition to the extensive complement of EIA Standard RS232C signals provided, the iSBC 534 provides 16 lines of RS232C buffered programmable parallel I/O. This interface is configured to be directly compatible with the Bell Model 801 automatic calling unit. These capabilities provide a flexible and easy means for interfacing iSBC 80 and System 80 based systems to RS232C and optically isolated current loop compatible terminals, cassettes, asynchronous and synchronous modems, and distributed processing networks.

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output line may be jumper selected to drive any of the nine interrupt lines on the iSBC 80 bus.

Algorithm	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.

Table 2. Interrupt Priority Options

Interrupt Request Generation — As shown in Table 3, interrupt requests may originate from 16 sources. Two jumper selectable interrupt requests (8 total) can be automatically generated by each USART when a character is ready to be transferred to the iSBC 80 system bus (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). Jumper selectable requests can be generated by two of the programmable timers (PITs), and six lines are routed directly from peripherals to accept carrier detect (4 lines), ring indicator, and the Bell 801 present next digit request lines.

Systems Compatibility

The iSBC 534 provides 16 RS232C buffered parallel I/O lines implemented utilizing an Intel 8255 programmable

Interrupt Request Line	PIC 0	PIC 1
0	PORT 0 R _X RDY	PIT 1 counter 1
1	PORT 0 T _X RDY	PIT 2 counter 2
2	PORT 1 R _X RDY	Ring indicator (all ports)
3	PORT 1 T _X RDY	Present next digit
4	PORT 2 R _X RDY	Carrier detect port 0
5	PORT 2 T _X RDY	Carrier detect port 1
6	PORT 3 R _X RDY	Carrier detect port 2
7	PORT 3 T _X RDY	Carrier detect port 3

Table 3. Interrupt Assignments

peripheral interface (PPI) configured to operate in mode 0.* These lines are configured to be directly compatible with the Bell 801 automatic calling unit (ACU). This capability allows the iSBC 534 to interface iSBC 80 and System 80-based systems to Bell 801 type ACUs and up to four modems or other serial communications devices. For systems not requiring interface to an ACU, the parallel I/O lines may also be used as general purpose RS232C compatible control lines in system implementation.

*Complete operational details on the Intel 8251 USART, the Intel 8255 Programmable Interval Timer, the Intel 8255 Programmable Peripheral Interface, and the Intel 8259 Programmable Interrupt controller are contained in the Intel 8080 Microcomputer System User's Manual and 8085 Microcomputer System User's Manual.

SPECIFICATIONS

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Sample Baud Rates¹

Frequency ² (kHz, Software Selectable)	Baud Rate (Hz)	
	Synchronous	Asynchronous
		+ 16 + 64
153.6	—	9600 2400
76.8	—	4800 1200
38.4	38400	2400 600
19.2	19200	1200 300
9.6	9600	600 150
4.8	4800	300 75
6.98	6980	— 110

Notes:

1. Baud rates shown here are only a sample subset of possible software-programmable rates available. Any frequency from 18.75 Hz to 614.4 kHz may be generated utilizing on-board crystal oscillator and 16-bit programmable interval timer (used here as frequency divider).

2. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.

Interval Timer and Baud Rate Generator Frequencies

Input Frequency (On-Board Crystal Oscillator) — 1.2288 MHz ± 10% (0.813 µs period, nominal)

Function	Single Timer		Dual/Timer Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt Interval	1.63 µs	53.3 ms	3.26 µs	58.25 minutes
Rate Generator (Frequency)	18.75 Hz	614.4 kHz	0.0029 Hz	307.2 kHz

Interfaces — RS232C Interfaces

EIA Standard RS232C Signals provided and supported:

Carrier detect	Receive data
Clear to send	Ring indicator
Data set ready	Secondary receive data
Data terminal ready	Secondary transmit data
Request to send	Transmit clock
Receive clock	Transmit data

Parallel I/O — 8 input lines, 8 output lines, all signals RS232C compatible

Bus — All signals iSBC 80 bus compatible

I/O Addressing

The USART, interval timer, interrupt controller, and parallel interface registers of the iSBC 534 are configured as a block of 16 I/O address locations. The location of this block is jumper selectable to begin at any 16-byte I/O address boundary (i.e., 00H, 10H, 20H, etc.).

I/O Access Time

400 ns USART registers
 400 ns Parallel I/O registers
 400 ns Interval timer registers
 400 ns Interrupt controller registers

Compatible Connectors/Cable

Interface	Pins (qty)	Centers (in.)	Mating Connectors	Cable
Bus	86	0.156	Viking 3KH43/9AMK12	N/A
Serial and parallel I/O	26	0.1	3M 3462-000 or TI H312113	Intel ISBC 955

Compatible Opto-Isolators

Function	Supplier	Part Number
Driver	Fairchild General Electric Monsanto	4N33
Receiver	Fairchild General Electric Monsanto	4N37

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 14 oz (398 gm)

Electrical Characteristics**Average DC Current**

Voltage	Without Opto-Isolators	With Opto-Isolators ¹
V _{CC} = +5V	1.9 A, max	1.9 A, max
V _{DD} = +12V	275 mA, max	420 mA, max
V _{AA} = -12V	250 mA, max	400 mA, max

Note

1. With four 4N33 and four 4N37 opto-isolator packages installed in sockets provided to implement four 20 mA current loop interfaces.

Environmental Characteristics

Operating Temperature — 0°C to +55°C

Reference Manual

9800450-12 — iSBC 534 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

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ORDERING INFORMATION

Part Number	Description
SBC 534	Four Channel Communication Expansion Board