# iSBC 519
# PROGRAMMABLE I/O EXPANSION BOARD

**iSBC 80 I/O expansion via direct bus interface**

**72 programmable I/O lines with sockets for interchangeable line drivers and terminators**

**Jumper selectable I/O port addresses**

**Jumper selectable 0.5, 1.0, 2.0, or 4.0 ms interval timer**

**Eight maskable interrupt request lines with priority encoded and programmable interrupt algorithms**

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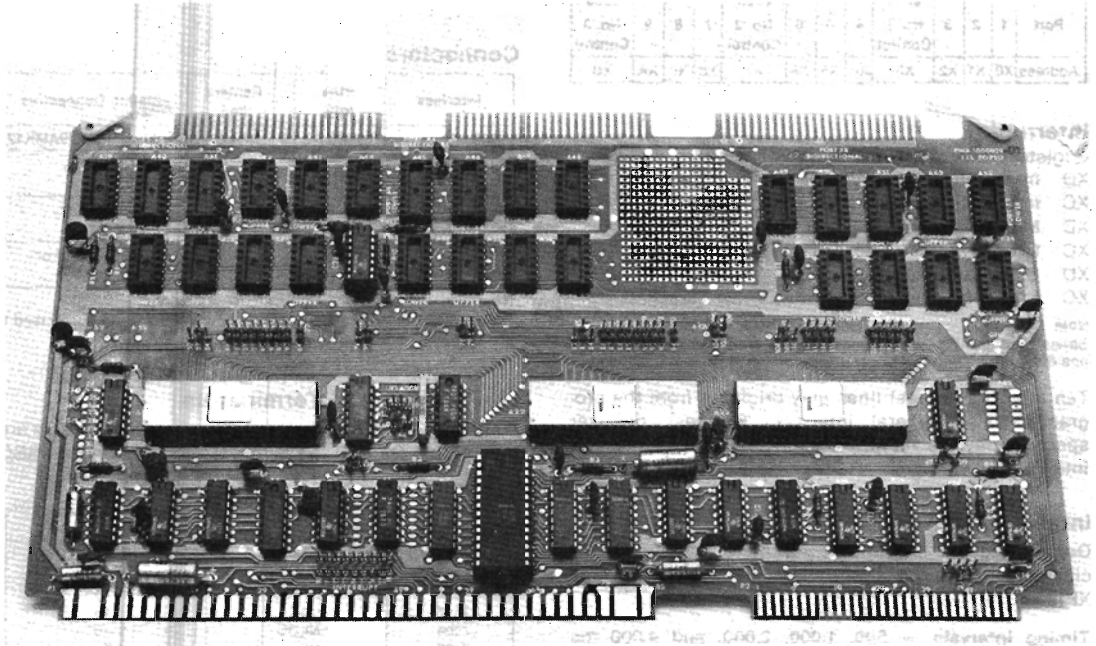
The iSBC 519 Programmable I/O Expansion Board is a member of Intel's complete line of iSBC 80 memory and I/O expansion boards. The iSBC 519 interfaces directly to any iSBC 80 single board computer via the system bus to expand input and output port capacity. The iSBC 519 provides 72 programmable I/O lines. The system software is used to configure the I/O lines to meet a wide variety of peripheral requirements. The flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. Address selection is accomplished by using wire-wrap jumbers to select one of 16 unique base addresses for the input and output ports. The board operates with a single +5V power supply.



## Interfaces

**Bus** — All signals TTL compatible
**Parallel I/O** — All signals TTL compatible
**Serial I/O** — RS232C
**Interrupt Requests** — All TTL compatible

## Connectors

| Interface | Pins (qty) | Centers (in.) | Mating Connectors |
|---|---|---|---|
| Bus | 86 | 0.156 | CDC VPB01E43A00A1 |
| Parallel I/O | 50 | 0.1 | 3M 3415-000 or TI H312125 |
| Serial I/O | 26 | 0.1 | 3M 3462-000 or TI H312113 |
| Auxiliary[1] | 60 | 0.1 | AMP PE5-14559 or TI H311130 |

**Note**

1. Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or system packaging. Auxiliary connector is used for test purposes only.

## Line Drivers and Terminators

**I/O Drivers** — The following line drivers and terminators are compatible with all the I/O driver sockets on the iSBC 517:

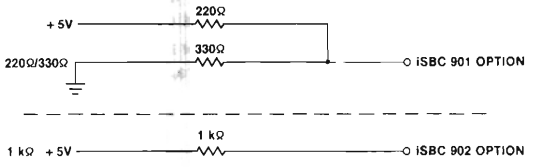
| Driver | Characteristic | Sink Current (mA) |
|---|---|---|
| 7438 | I,OC | 48 |
| 7437 | I | 48 |
| 7432 | NI | 16 |
| 7426 | I,OC | 16 |
| 7409 | NI,OC | 16 |
| 7408 | NI | 16 |
| 7403 | I,OC | 16 |
| 7400 | I | 16 |

**Note**

I = inverting; NI = non-inverting; OC = open-collector.

Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

**I/O Terminators** — 220Ω/330Ω divider or 1 kΩ pullup




## Bus Drivers

| Function | Characteristic | Sink Current (mA) |
|---|---|---|
| Data | Tri-state | 50 |
| Commands | Tri-state | 25 |

## Physical Characteristics

**Width** — 12.00 in. (30.48 cm)
**Height** — 6.75 in. (17.15 cm)
**Depth** — 0.50 in. (1.27 cm)
**Weight** — 14 oz (397. 3 gm)

## Electrical Characteristics

### Average DC Current

$V_{CC}$ = +5V ±5%
$V_{DD}$ = +12V ±5%
$V_{AA}$ = −12V ±5%
$I_{CC}$ = 2.4 mA max
$I_{DD}$ = 40 mA max
$I_{AA}$ = 60 mA max

**Note**

Does not include power required for optional I/O drivers and I/O terminators. With eight 220Ω/330Ω input terminators installed, all terminator inputs low.

## Environmental Characteristics

**Operating Temperature** — 0°C to +55°C

## Reference Manual

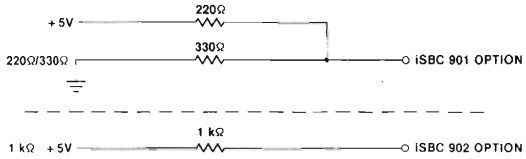
**9800388B** — iSBC 517 hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

## ORDERING INFORMATION

| Part Number | Description |
|---|---|
| SBC 517 | Combination I/O Expansion Board |

**I/O Terminators** — 220Ω/330Ω divider or 1 kΩ pullup




Ports 1, 4, and 7 may use any of the drivers or terminators shown above for unidirectional (input or output) port configurations. Either terminator and the following bidirectional drivers and terminators may be used for ports 1, 4, and 7 when these ports are used as bidirectional ports.

**Bidirectional Drivers**

| Driver | Characteristic | Sink Current (mA) |
|---|---|---|
| Intel 8216 | NI, TS | 25 |
| Intel 8226 | I, TS | 50 |

**Note**

I = inverting; NI = non-inverting; TS = three-state.

**Terminators** (for ports 1, 4, and 7 when used as bidirectional ports)

| Supplier | Product Series |
|---|---|
| CTS | 760- |
| Dale | LDP14k-02 |
| Beckman | 899-1 |

**Bus Drivers**

| Function | Characteristic | Sink Current (mA) |
|---|---|---|
| Data | Tri-state | 50 |
| Commands | Tri-state | 25 |

## Physical Characteristics

**Width** — 12.00 in. (30.48 cm)
**Height** — 6.75 in. (17.15 cm)
**Depth** — 0.50 in. (1.27 cm)
**Weight** — 14 oz (397.3 gm)

## Electrical Characteristics

**Average DC Current**

| Voltage | Without Termination[1] | With Termination[2] |
|---|---|---|
| $V_{CC}$ = +5V ±5% | $I_{CC}$ = 1.5A max | 3.5A max |

**Note**

1. Does not include power required for optional I/O drivers and I/O terminators.
2. With 18 220Ω/330Ω Input terminators installed, all terminator inputs low.

## Environmental Characteristics

**Operating Temperature** — 0°C to +55°C

## Reference Manual

**9800385B** — iSBC 519 hardware Reference Manual (NOT SUPPLIED)

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## ORDERING INFORMATION

| Part Number | Description |
|---|---|
| SBC 519 | Programmable I/O Expansion Board |

| Algorithm | Operation |
|---|---|
| Fully nested | Interrupt request line priorities fixed at 0 as highest, 7 as lowest. |
| Auto-rotating | Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs. |
| Specific priority | System software assigns lowest priority level. Priority of all other levels are based in sequence numerically on this assignment. |

**Table 2. Interrupt Priority Options**

manner in which requests are serviced may be configured to match system requirements. Priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel I/O interfaces, the interval timer, or direct from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the system master. Any combination of interrupt levels may be masked through storage, via software, of a single byte to the interrupt mask register of the PIC.

**Interrupt Request Generation** — Interrupt requests may originate from 10 sources. Six jumper selectable interrupt requests can be automatically generated by the programmable peripheral interfaces when a byte of information is ready to be transferred to the system master (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Three interrupt request lines may be interfaced to the PIC directly from user designated peripheral devices via the I/O edge connectors. One interrupt request may be generated by the interval timer.

**Bus Line Drivers** — The PIC interrupt request output line may be jumper selected to drive any of the nine interrupt lines on the iSBC 80 bus. Any of the on-board request lines may also drive any iSBC 80 bus interrupt line directly via jumpers and buffers on the board.

# SPECIFICATIONS

## Addressing

| Port | 1 | 2 | 3 | 8255 No. 1 Control | 4 | 5 | 6 | 8255 No. 2 Control | 7 | 8 | 9 | 8255 No. 3 Control |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | X0 | X1 | X2 | X3 | X4 | X5 | X6 | X7 | X8 | X9 | XA | XB |

## Interrupts

**Register Addresses** (hex notation, I/O address space)

XD Interrupt request register
XC In-service register
XD Mask register
XC Command register
XD Block address register
XC Status (polling register)

**Note**
Several registers have the same physical address; sequence of access and one data bit of control word determines which register will respond.

Ten interrupt request lines may originate from the programmable peripheral interface (6 lines), or user specified devices via the I/O edge connector (3 lines), or interval timer (1 line).

## Interval Timer

**Output Register** — Timer interrupt register output is cleared by an output instruction to I/O address XE or XF1.

**Timing Intervals** — 500, 1,000, 2,000, and 4,000 ms ± 1%; jumper selectable[2].

**Notes**

1. X is any hex digit assigned by jumper selection.
2. Assumes iSBC 80 constant clock (CCLK) frequency of 9.216 MHz ± 1%.

## Interfaces

**Bus** — All signals TTL compatible
**Parallel I/O** — All signals TTL compatible
**Interrupt Requests** — All TTL compatible

## Connectors

| Interface | Pins (qty) | Centers (in.) | Mating Connectors |
|---|---|---|---|
| Bus | 86 | 0.156 | Viking 3KH43/9AMK12 |
| Parallel I/O | 50 | 0.1 | 3M 3415-000 or TI H312125 |
| Serial I/O | 26 | 0.1 | 3M 3462-000 or TI H312113 |
| Auxiliary[1] | 60 | 0.1 | AMP PE5-14559 or TI H311130 |

**Note**
1. Connector heights and wirewrap pin lengths are not guaranteed to conform to Intel OEM or System packaging.

## Line Drivers and Terminators

**I/O Drivers** — The following line drivers and terminators are compatible with all the I/O driver sockets on the iSBC 519:

| Driver | Characteristic | Sink Current (mA) |
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| 7432 | NI | 16 |
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| 7409 | NI,OC | 16 |
| 7408 | NI | 16 |
| 7403 | I,OC | 16 |
| 7400 | I | 16 |

**Note**
I = inverting; NI = non-inverting; OC = open-collector.

| Port No. X = I/O Base Address | Type of I/O | Lines (qty) | Resistor Terminator Pac Rp 16-Pin DIP Bourns 4116R-00 or Equivalent | Dual Opto-Isolator 8-Pin Dip Monsanto MC T66 or Equivalent | Dual Opto-Isolator Darlington Pair 6-Pin DIP Monsanto 4N29, 30 31, 32 or Equivalent | Driver 7438 or Equivalent | Pull-Up iSBC 902 |
|---|---|---|---|---|---|---|---|
| X + 0 | Input | 8 | 1 | 4 | — | — | |
| X + 1 | Output | 8 | — | | 8 | — | |
| X + 2 | Input/ Control | 8 | 1 | | 8 | — | |
| X + 4 | Input | 8 | 1 | 4 | — | — | |
| X + 5 | Output | 8 | | | 8 | — | |
| X + 6 | Input/ Output | 8 | 1 if input | | 8 | 2 if output | 2 if input |
| X + 7 | Control | | | | | | |

Table 1. I/O Ports Opto-Isolator Receivers, Drivers, And Terminators

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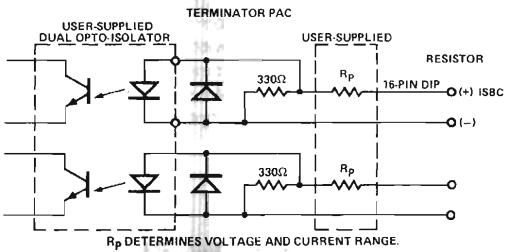
## SPECIFICATIONS

### Number of Lines

24 input lines
16 output lines
8 programmable lines: 4 input — 4 output

### I/O Interface Characteristics

**Line-to-Line Isolation** — 235V DC or peak AC
**Input/Output Isolation** — 500V DC or peak AC




### Bus Interface Characteristics

All data address and control commands are iSBC 80 bus compatible.

**I/O Addressing**

| Port | 8255 #1 | | | Control | 8255 #2 | | | Control |
|---|---|---|---|---|---|---|---|---|
| | A | B | C | | A | B | C | |
| Address | X + 0 | X + 1 | X + 2 | X + 3 | X + 4 | X + 5 | X + 6 | X + 7 |

Where:
base address is from 00H to 1FH (jumper selectable)

## ORDERING INFORMATION

| Part Number | Description |
|---|---|
| SBC 556 | Optically Isolated I/O Board |

### Connectors

| Interface | Pins (qty) | Centers | | Mating Connectors |
|---|---|---|---|---|
| | | in. | cm | |
| P1 iSBC bus | 86 | 0.156 | | Viking 3KH43/9AMK12 |
| J1 16 fixed input & 8 fixed output lines | 50 | 0.1 | | 3M 3415-000 or TI M312125 |
| J2 8 fixed output, 8 fixed output, & 8 programmable input/output lines | 50 | 0.1 | | 3M 3415-000 or TI M312125 |

### Physical Characteristics

**Width** — 12.00 in. (30.48 cm)
**Height** — 6.75 in. (17.15 cm)
**Depth** — 0.50 in. (1.27 cm)
**Weight** — 12 oz (397.3 gm)

### Electrical Characteristics

**Average DC Current**

$V_{CC} = +5V \pm 5\%$, 1.0A without user supplied isolated receiver/driver

$I_{CC} = 1.6A$ max with user supplied isolator receiver/driver

### Environmental Characteristics

**Temperature** — 0°C to 55°C
**Relative Humidity** — 0 to 90%, non-condensing

### Reference Manual

**9800489-02** — iSBC 556 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.