iSBC 501
DIRECT MEMORY ACCESS CONTROLLER

- **Directly compatible with Intel iSBC 80 single board computers**
- **Block length up to 65,536 words**
- **Directly addresses up to 65,536 memory locations**
- **Transfer rate up to 1 million words per second for block transfers**
- **Transfers initialized via software**
- **Transfers data up to 330K words per second for interleaved transfers**
- **Software selectable/maskable interrupt operations**
- **Interrupt priority switch selectable**

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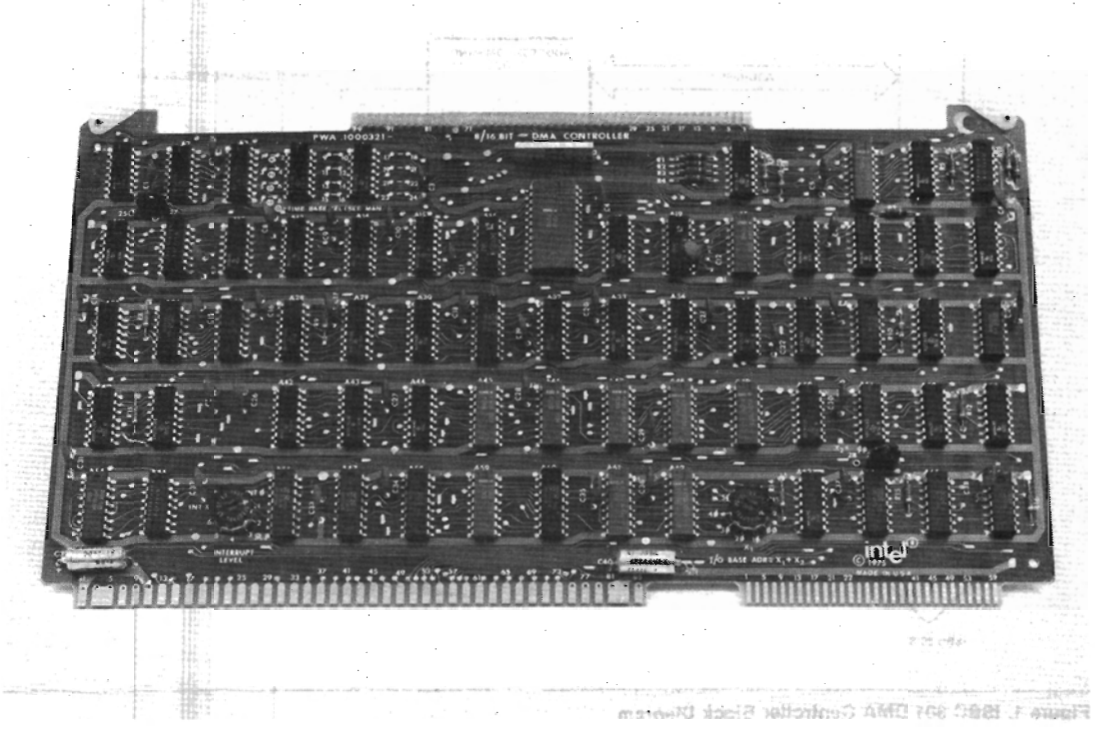
The iSBC 501 Direct Memory Access Controller is a member of Intel's complete line of iSBC 80 OEM computer systems. The iSBC 501 interfaces directly with any iSBC 80 single board computer based system via the system bus. High speed, direct memory access control and interfacing for transfers between iSBC 80 expansion board memory and up to 16 peripheral devices is provided.



FUNCTIONAL DESCRIPTION

Transfer Capability

Block lengths up to 65,536 bytes long may be transferred directly to or from RAM memory in iSBC 80 systems at rates up to 1 million words per second. The iSBC 501 16-bit addressing capability allows transfers to take place at any location within memory. It is designed to control the direct transfer of data to or from Intel iSBC 80 memory expansion or combination memory and I/O boards. Two transfer modes of operation are included. System software is used to select the desired mode. Transfer rates up to 330K words per second may be achieved in the shared bus mode, wherein the iSBC 501 requests access to the system bus for 600 ns to perform a transfer of one word to or from memory. The second mode, the override mode, establishes the DMA controller as the only master which may access the system bus during the transfer period, thereby providing rapid block transfer capability. This mode provides transfer rates up to 1 million words per second. The iSBC 80/10A single board computer may only interact with the iSBC 501 in the shared bus mode. Either mode may be used with the other iSBC single board computers. Four timing strobes are provided for the control of data input transfers and four timing strobes are provided for output transfer operations. Strobes are initiated and selected via system software, and strobe pulses are jumper selectable to 100, 200, 400, 800, or 1600 ns widths.

Interrupt Requests

Interrupt requests originating from the DMA controller are software maskable, active-low, and switch selectable to any one of eight priority levels. User selected DMA interrupt requests may originate automatically upon completion of a transfer operation, from an external DMA device, or from a software command to the DMA controller (for system testing purposes).

Peripheral Interface

A 4-bit tag register is provided which may be used as a device select port to provide selection for four (up to 16 with external decoding) high speed peripheral devices interfacing through the iSBC 501.

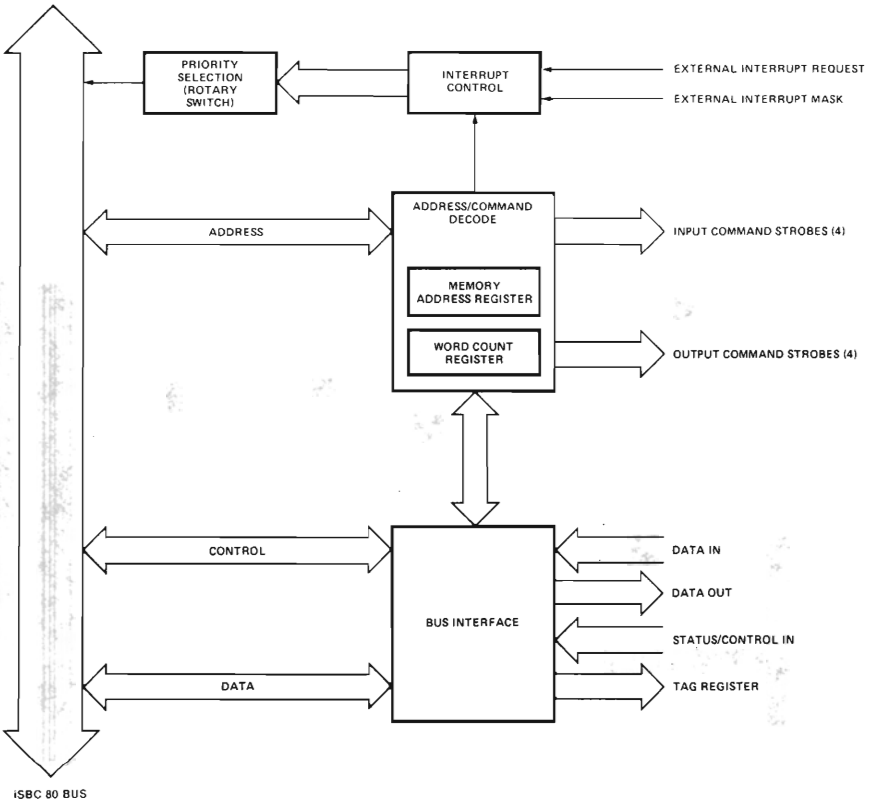


Figure 1. iSBC 501 DMA Controller Block Diagram

SPECIFICATIONS

Word Size

8 bits

Block Size

65,536 words, max

Address Capability

65,536 words

Transfer Rates

Mode	Transfer Rates (K bytes/sec)[1]			
	Memory Read Operations		Memory Write Operations	
	Typical	Worst Case[3]	Typical	Worst Case[3]
Shared bus, CPU halted[2]	330	270	330	270
Shared bus, CPU executing code[2]	180	160	180	160
Override	1000	660	1000	660

Notes

1. Transfer rates given are to and from RAM memory on iSBC 104 or iSBc 108 combination memory and I/O boards.

2. Shared bus mode may be used with Intel iSBC 80/10 or Intel iSBC 80/20. ISBC 80/20 may also operate in override mode.

3. Assumes every DMA transfer must wait for RAM refresh cycle to be completed, worst case memory cycle times.

Interrupts

Interrupt requests originating from the DMA controller are software maskable, active-low, and switch selectable to any one of eight priority levels. User selectable DMA interrupt requests may originate automatically upon completion of a transfer operation, from an external DMA device, or from a software command to the DMA controller (for system testing purposes).

Key Registers

Control Register (6 bits) — The contents of the control register specify the busy status of the DMA board, the type of operation to be performed (transfer or non-transfer), the transfer direction (to or from memory), the interrupt condition (enabled or disabled), and the means by which the DMA board is using the system bus (shared mode or override mode).

Memory Address Register (16 bits) — Contains the address of the next memory location to be accessed by the iSBC 501. Loaded from the CPU, prior to a transfer operation, with the address of the first memory location to be accessed. The address is gated onto the system address bus during each transfer, and incremented by one for each word transferred.

Length Register (16 bits) — Contents of this register specify the total number of words to be transferred. This word count is decremented by one after each word is transferred. The transfer stops when the word count equals zero.

Tag Register (4 bits) — The contents of the tag register are used as control/select lines to the external peripheral devices being interfaced by the iSBC 501 (e.g., as the "go" command line to each of four devices), or the tag register outputs may be used with external decoding to expand the maximum number of DMA peripherals to 16.

Status Register (8-bits) — Provides 4 bits of DMA controller status: software interrupt, memory read/write operation requested, external/end-of-transfer interrupt, and DMA controller busy. The status register also provides four status/control bits directly from user peripheral devices.

Address Selection

iSBC 501 registers are located in a jumber selectable block starting at any 16-word boundary in the I/O address space.

Register Locations

Address[1]	I/O Operation	Function
X0	Output	Output strobe 0
X1	Output	Output strobe 1
X2	Output	Output strobe 2
X3	Output	Output strobe 3
X4	Output	Output tag strobe
X8	Output	Set interrupt
X9	Output	Reset interrupt
XA	Output	Load control register
XB	Output	Load tag register
XC	Output	Load LSB length register
XD	Output	Load MSB length register
XE	Output	Load LSB memory address register
XF	Output	Load MSB memory address register
X0	Input	Input command strobe 0
X1	Input	Input command strobe 1
X2	Input	Input command strobe 2
X3	Input	Input command strobe 3
X4	Input	Read LSB length register
X5	Input	Read MSB length register
X6	Input	Read DMA status
X7	Input	Invalid command

Note

1. X is any hex digit, assigned by jumbers.

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
I/O	100	0.100	Intel MDS 990 Viking 3VH50/1JN5

Interface Characteristics

I/O Line Driver Sink Current — 48 mA

I/O Line Terminator Load — 150Ω pullup

Input — Data positive relative to data bus

Output — Data positive relative to data bus

Output Strobes — Jumper selectable to 100, 200, 400, 800, or 1600 ns pulse widths.

All I/O interface data and control signals are TTL compatible and iSBC 80 bus compatible.

Physical Characteristics

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12 oz (340.5 gm)

Electrical Characteristics

DC Power Requirements

V_{CC} = 5V ±5%
I_{CC} = 3.35A max; 2.70A typ

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Equipment Supplied

iSBC 501 DMA Controller Board

Reference Manuals

9800294A — iSBC 501 Hardware Reference Manual (NOT SUPPLIED)

iSBC 501 Schematic (SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 501	Direct Memory Access Controller