

Designing High Speed, Low Cost Memory Systems with the Intel 2105

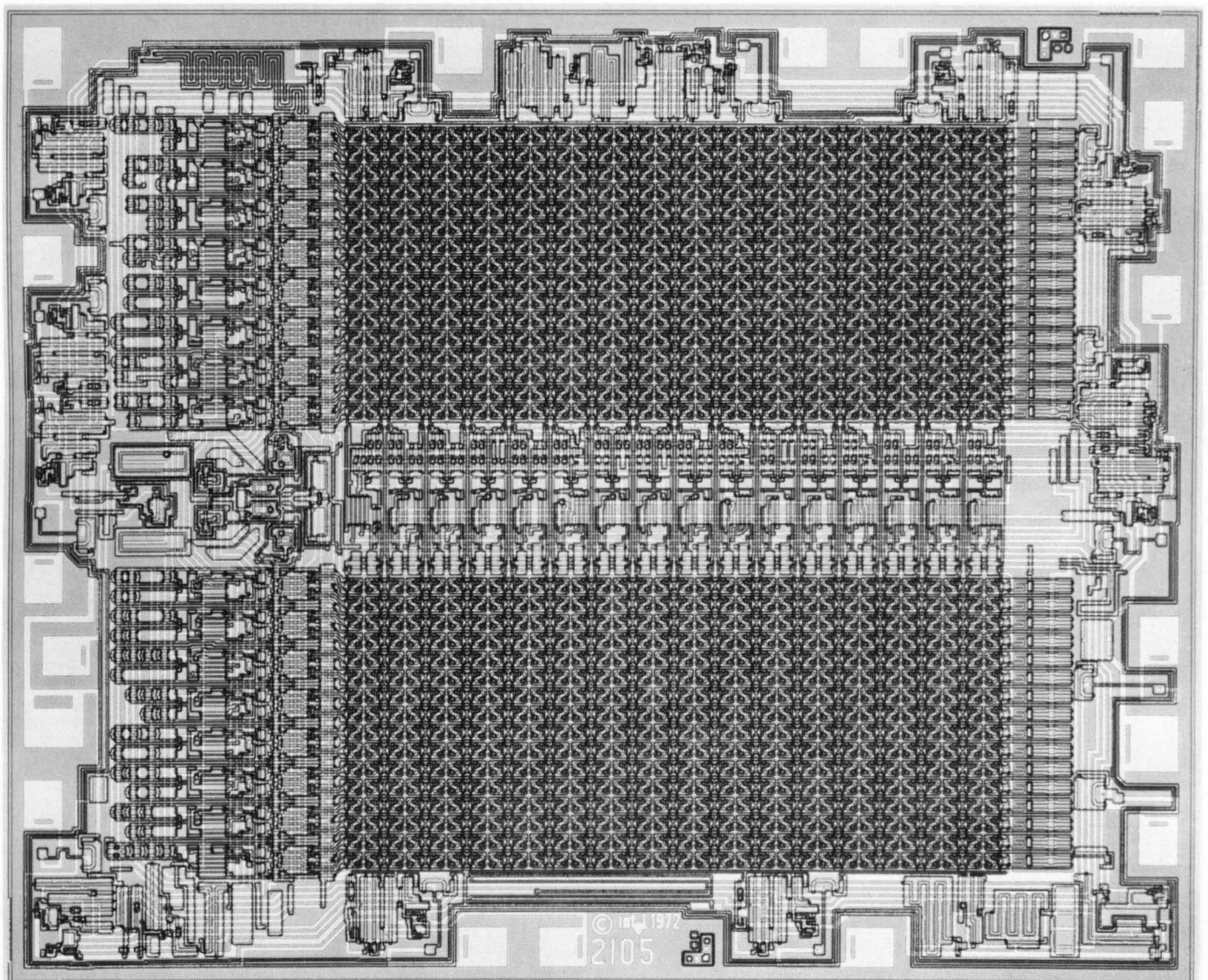
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Application Engineering

Designing High Speed, Low Cost Memory Systems with the Intel 2105

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Photomicrograph of N-channel 1024 bit 2105 memory element.



INTRODUCTION

The Intel 2105 is a 1024 bit, high speed, low cost, Random Access, read-write memory element. The high speed and high functional density of N-Channel silicon gate technology, combined with the superior performance of a stable four transistor cell, has produced a new industry price/performance leader. Easy system design is provided by the low voltage, low capacitance inputs, on-chip address registers, and hidden planar refresh.

System size is reduced by the use of a standard 18 pin Dual In-line Package, shown in Figure 1.

Figure 2 is a simplified block diagram of the 2105. The memory is organized as 32 rows of 32 cells each. The five low order address lines, A_0 through A_4 , are decoded to activate one of the 32 possible rows. The upper order address, A_5 through A_9 , are also decoded to activate one of a possible 32 column I/O circuits. Thus one of a possible 1024 cells in the 32 x 32 matrix is selected for reading by way of the read bus, or writing by way of the write bus.

All 1024 memory cells are refreshed at the same time by application of a single 100KHz to 1MHz, 12 volt signal to the low capacitance refresh pin

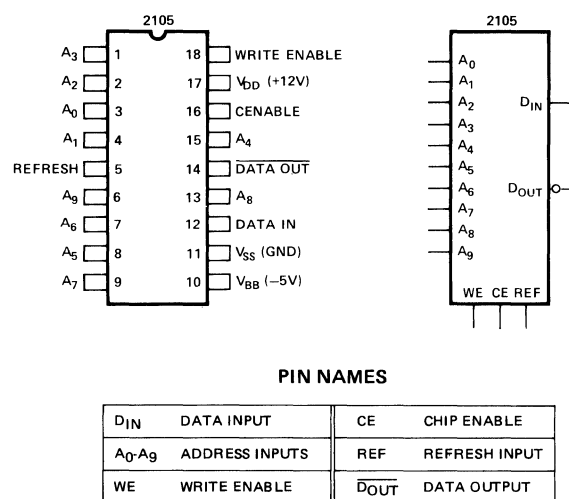


FIGURE 1—2105 pin configuration and logic symbol.

of each chip, thus eliminating the refresh counters and address multiplexers normally associated with MOS memories.

The address, data, and write enable pins are low capacitance, low voltage swing inputs. Only refresh

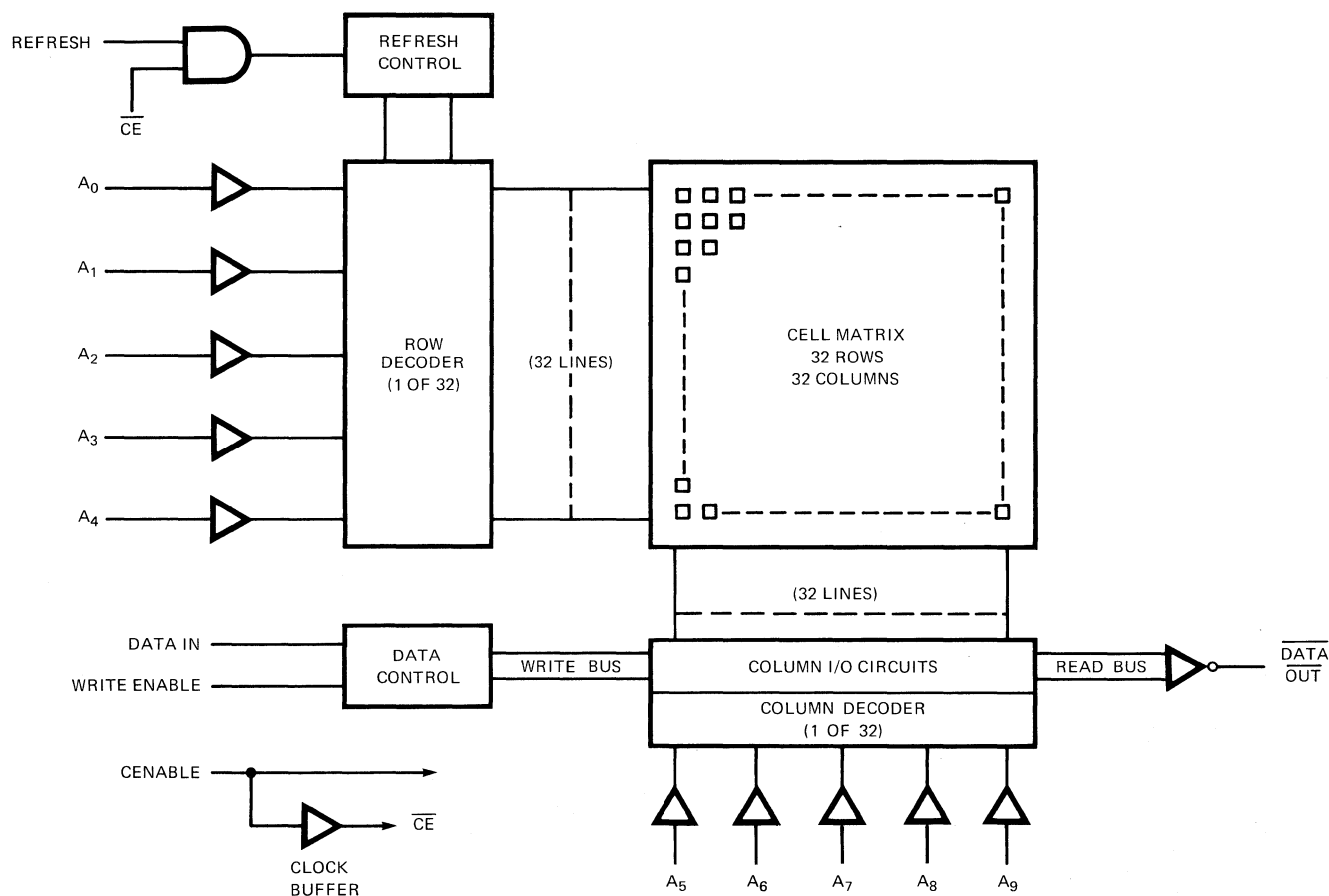
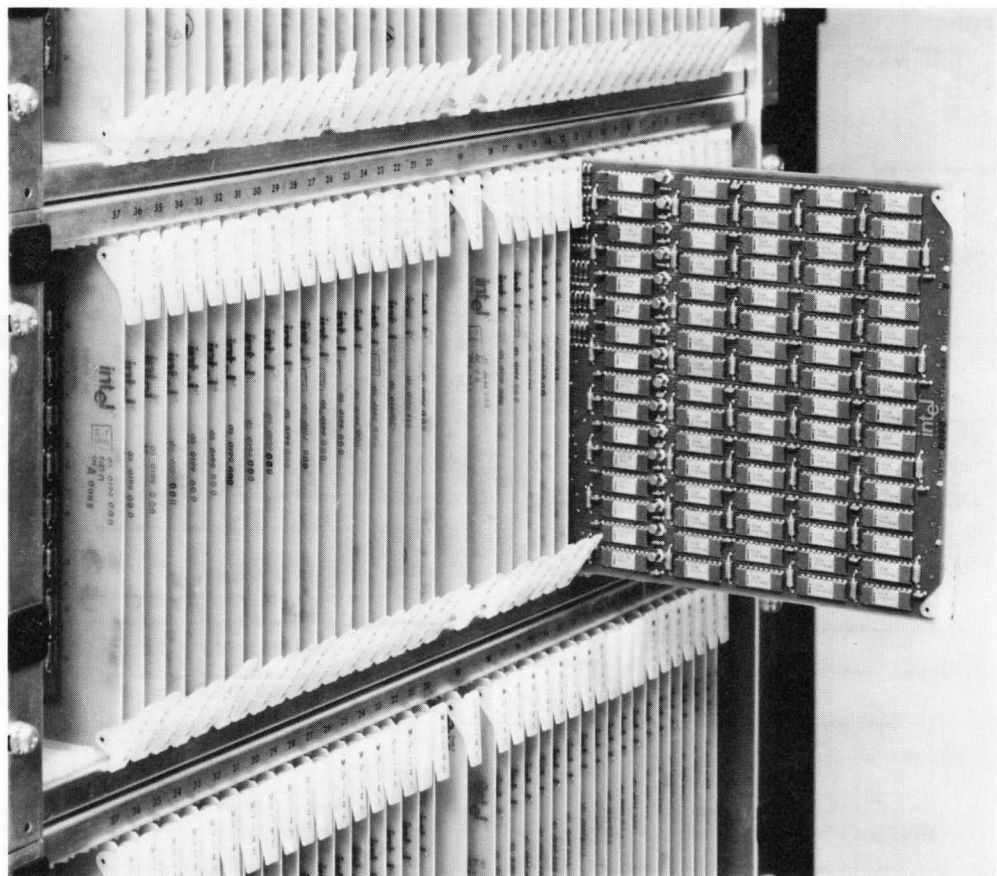
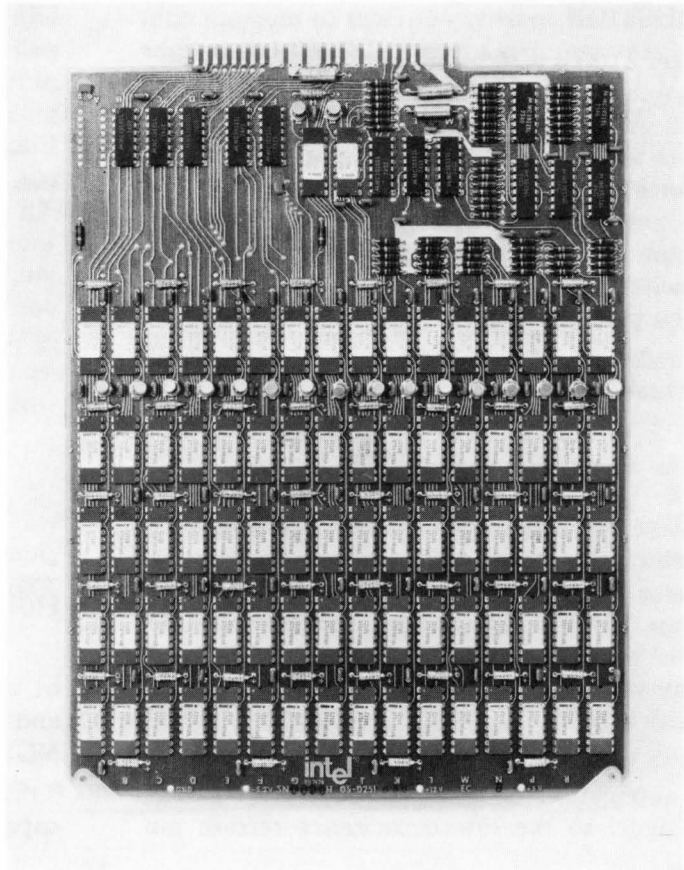


FIGURE 2—2105 block diagram.

Intel
Memory Systems Division
MU-145 memory board,
32K x 2 bit configuration.



256 Byte memory systems module, 32K x 72.

and chip enable require full MOS voltage swings and each represents a fixed capacitive load.

The Intel 2105 output is easily sensed with a number of different devices; additionally, the low capacitance of the data output allows the OR connection of a large number of memory elements.

BASIC OPERATION

Basic Cell Operation

Read or Write Cycle

The basic 2105 storage element, as shown in Figure 3, is comprised of the distributed gate to substarate capacitance of Q_6 and Q_7 . A one or a zero is stored by charging one capacitor and discharging the other. Q_6 and Q_7 are cross coupled and provide a stable flip-flop when Q_1 , Q_2 , Q_4 and Q_5 are turned on. Q_4 and Q_5 are enabled by one of the 32 row select decoders. Enabling Q_4 and Q_5 connects the storage elements to the column I/O bus. A few nano seconds later Q_1 , Q_2 , Q_3 are disabled when Cenable becomes true. When Q_1 and Q_2 are disabled, they form a high resistance load to each of the differential column I/O lines. This allows a differential voltage to be developed across the lines. The differential voltage will either originate from Q_6 and Q_7 (in a read mode) or from the data in line if Write, Enable, Cenable and column decode are all true. In the case of a read cycle, the information in the cell is retained. Enabling the write bus will override the Q_6 and Q_7 levels and charge their distributed capacities to the new data value. If the write bus is not enabled, the data from Q_6 and Q_7 is gated to the read bus by way of Q_8 and Q_9 which are also gated by the column select decode signal. The data on the read bus is amplified by the data out sense amplifier and becomes the data out signal from the device. When chip enable goes false, (logic 0), Q_1 , Q_2 and Q_3 will conduct. The low resistance of these elements insures a zero volt difference across the I/O lines. Incidentally, this provides a refresh condition on the row which is selected and a data hold condition on the other 31 rows.

Refreshing the Cell

During refresh, $Q_1 - Q_3$ are on, connecting both sides of the column I/O bus to V_{DD} through a low resistance path. If Q_4 and Q_5 are turned off (rows not selected), the data on the distributed capacitance of Q_4 and Q_5 will eventually leak off. However, applying a refresh signal to all rows will enable Q_4 and Q_5 on all 1024 cells. Q_4 and Q_6 become a voltage divider to the gate of Q_7 as Q_5 and Q_7 form a voltage divider for the gate of Q_6 . Both dividers form a regenerative feed back network to reinforce the initial charges on the distributed capacity of the storage element. Isolation between

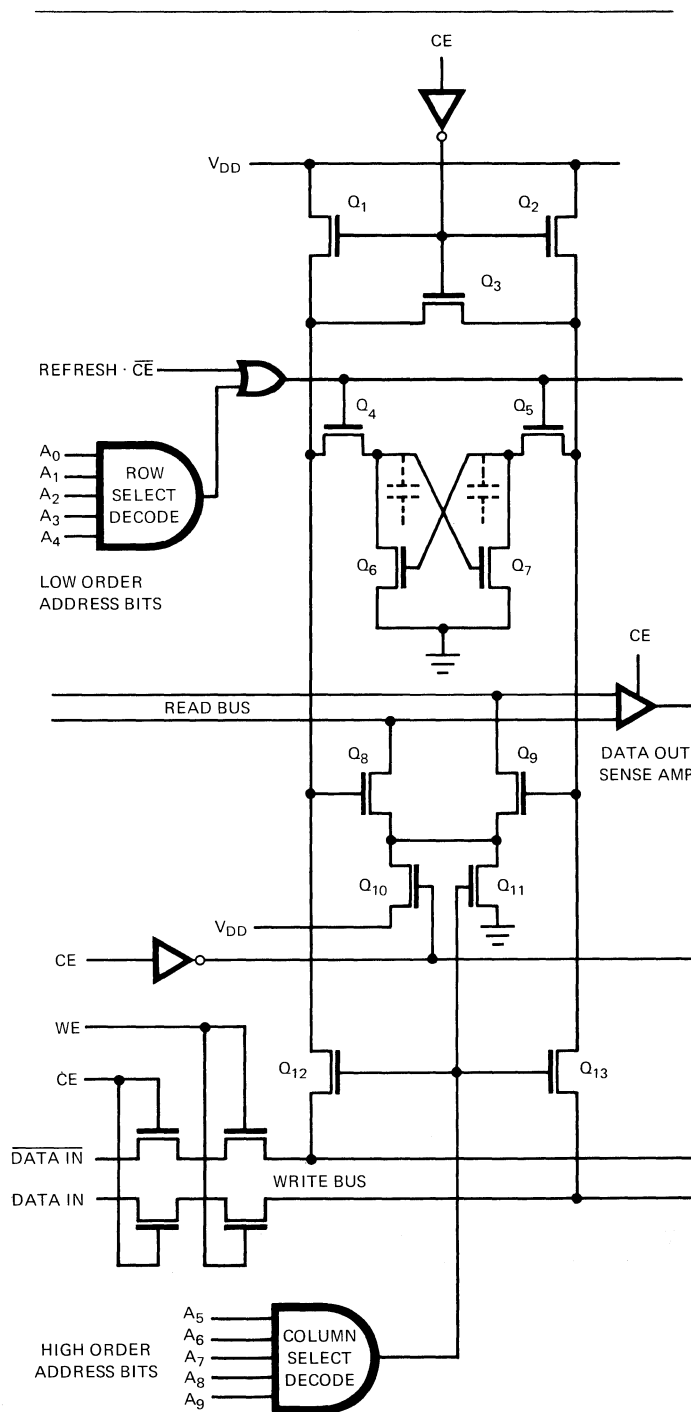


FIGURE 3—Simplified memory cell and associated circuitry.

cells on the same column is provided by the low resistance of Q_1 , Q_2 and Q_3 . Removing the refresh signal restores the circuits to a data hold condition.

Timing

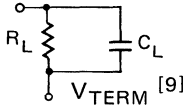
The timing sequence begins, as shown in Figure 4, with the validation of the address prior to a chip enable initiate signal. This time is called the Address Setup Time, (t_{AS+}), and for a 2105-2 is 5nS. As can be seen in the detailed block diagram, (Figure 5), the t_{AS+} time allows the dynamic address latches to settle prior to being clocked with

A. C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 12\text{V} \pm 5\%$, $V_{BB} = -5.2\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$, unless otherwise specified. ^[1]

Read, Write, and Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Planar Refresh Pulses	1	10	μs	
t_{AR}	Address Reset Time	Note 2		ns	
t_{AS+} ^{[3] [5]}	High Address Setup Time	5		ns	
t_{AS-} ^{[4] [5]}	Low Address Setup Time	35		ns	
t_{CE}	Cenable On Time	80	360	ns	
t_{CC}	Cenable Off Time	80		ns	

Read Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY} ^[6]	Read Cycle	190		ns	$t_T = 15\text{ ns}$ $C_{LOAD} = 50\text{ pF}$ $R_{LOAD} = 100\Omega$ Refer to Note 8 
t_{WS}	Write Enable to Cenable Set Up Time	0		ns	
t_{CO}	Cenable Output Delay		65	ns	
t_{ACC} ^[7]	Address to Output Access		85	ns	

Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY} ^[6]	Write Cycle	190		ns	$t_T = 15\text{ ns}$
t_{WP}	Write Enable Pulse Width	70		ns	
t_{WC}	Write Enable to Cenable End	70	120	ns	
t_{DS} ^[10]	Data Set Up Time	70		ns	
t_{DH} ^[11]	Data Hold Time	20		ns	

Read Modify Write Cycle

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC} ^[12]	Read Modify Write Cycle	270		ns	$t_T = 15\text{ ns}$
t_{CEM} ^[13]	Cenable On Time	160	360	ns	

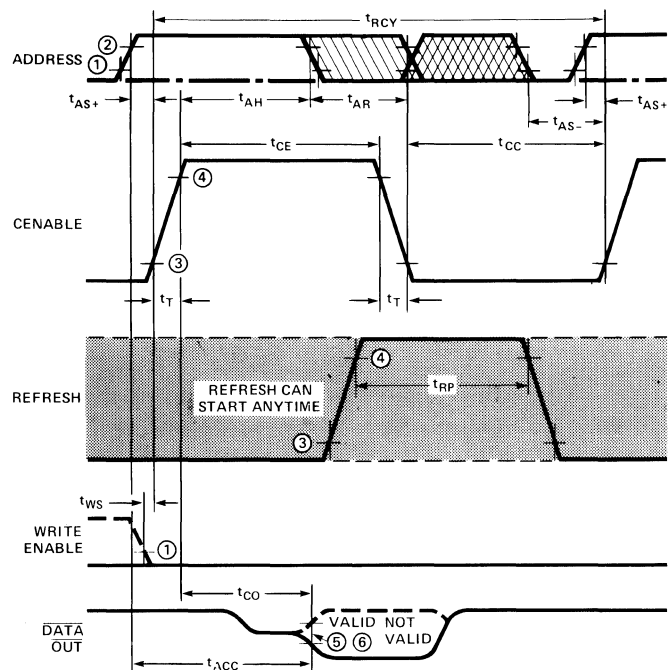
Invisible Planar Refresh Timing (for Asynchronous Operation)

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RP}	Asynchronous Refresh P.W.	$t_{CE} + 140$		ns	The refresh pulse timing is not related to any other signal.
t_{REF}	Time Between Planar Refresh	1	10	μs	

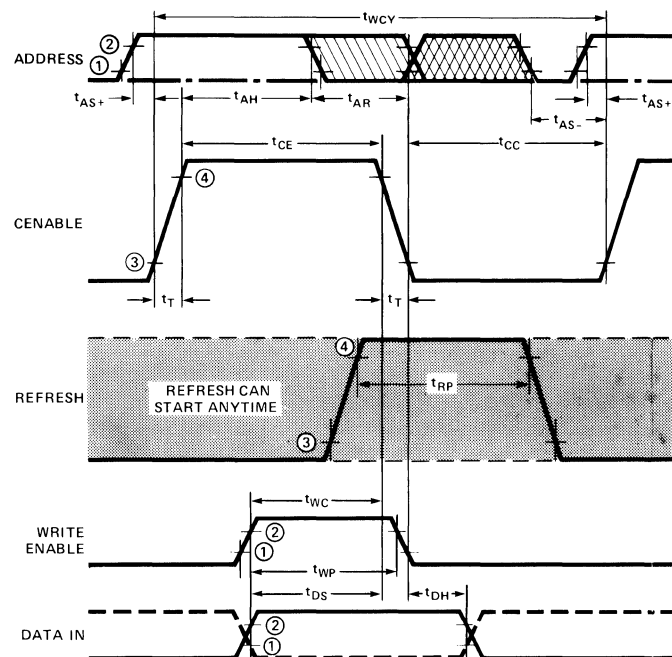
- NOTES: 1. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB} .
2. t_{AR} is defined as $t_{CE} + t_T - t_{AH}$. During t_{AR} addresses may only be reset low or remain stable. Addresses may change after the start of t_{CC} and before the start of t_{AS-} .
3. High addresses must be stable by the start of t_{AS+} time.
4. Low addresses must be stable by the start of t_{AS-} time.
5. To conserve power and reduce sensing noise, it is recommended that all addresses be reset low after t_{CO} time and remain reset until t_{AS+} time.
6. The parameter t_{RCY} and t_{WCY} are defined as $t_T + t_{CE} + t_T + t_{CC}$.
7. The parameter t_{ACC} is defined as $t_{AS+} + t_T + t_{CO}$.
8. The parameter t_{CO} is defined as V_{OL1} or V_{OH1} , whichever occurs last.
9. The load resistor R_L is connected to $V_{termination}$ where $V_{termination} = -1.175\text{V} \pm 60\text{mV}$ at 25°C , $T_C = 1.3\text{mV}/^\circ\text{C}$, $V_{BB}/V_{termination} = 0.226$.
10. The parameter t_{DS} is referenced to the falling edge of Cenable (④) or Write Enable (②), whichever occurs first.
11. The parameter t_{DH} is referenced to the falling edge of Cenable (③) or Write Enable (①), whichever occurs first.
12. The parameter t_{RWC} is defined as $t_{CO} + t_{WC} + 3t_T + t_{CC} + \text{modify time}$ or $t_T + t_{CEM} + t_T + t_{CC} + \text{modify time}$.
13. t_{CEM} applies for Read Modify Write Cycle.

FIGURE 4—2105-2 timing.

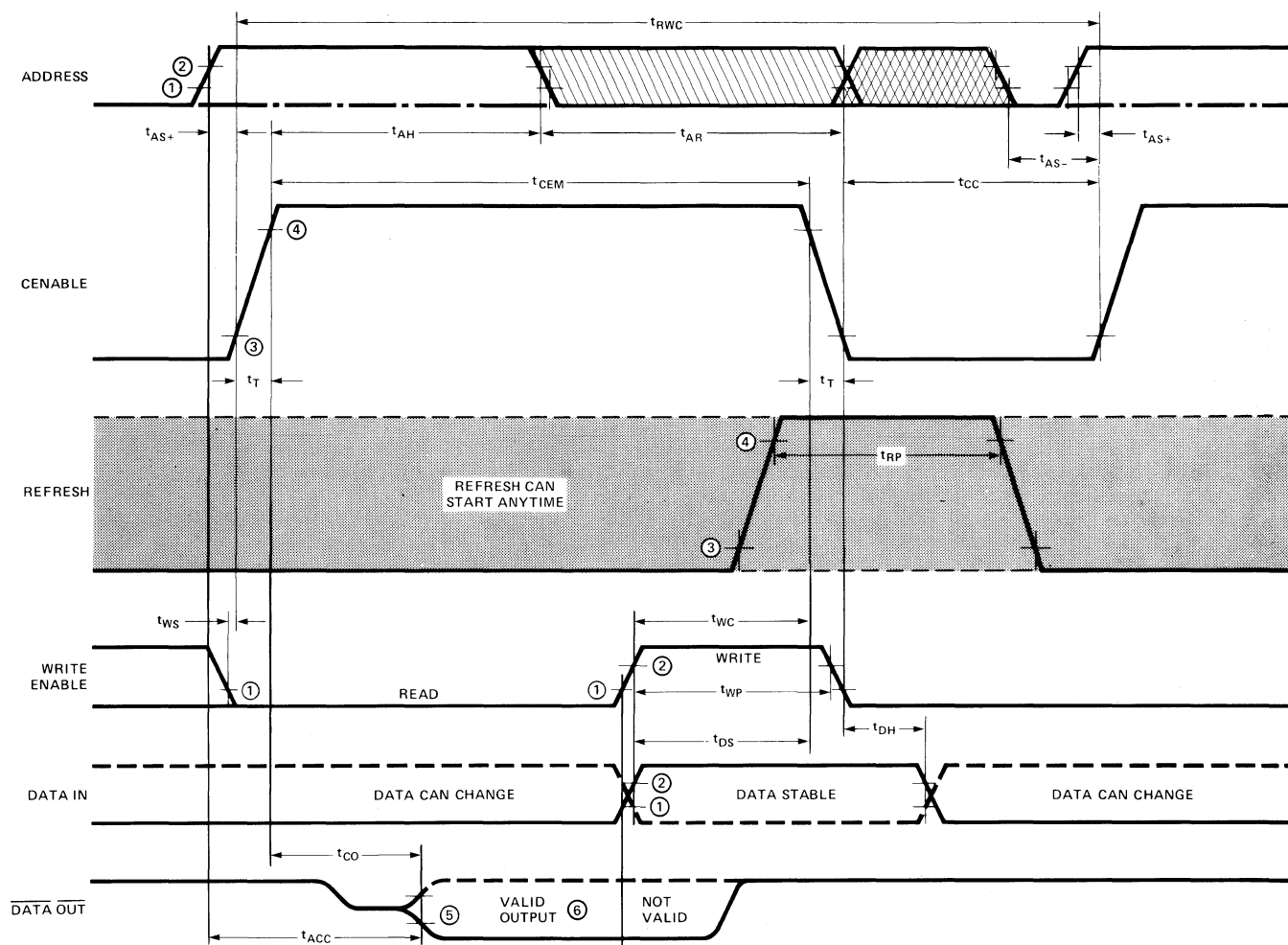
WRITE CYCLE — 2105-2



READ CYCLE — 2105-2



READ MODIFY WRITE CYCLE — 2105-2



- NOTES: ① $V_{SS} = +1.5V$ ③ $V_{SS} = +2.0V$ ⑤ The parameter t_{CO} is defined at V_{OL1} or V_{OH1} , whichever occurs last. $R_L = 100\Omega$, $C_L = 50pF$. ⑥ Data Out is valid during t_{CE} time or until Write Enable goes high.
- ② $V_{SS} = +3.0V$ ④ $V_{DD} = -2.0V$

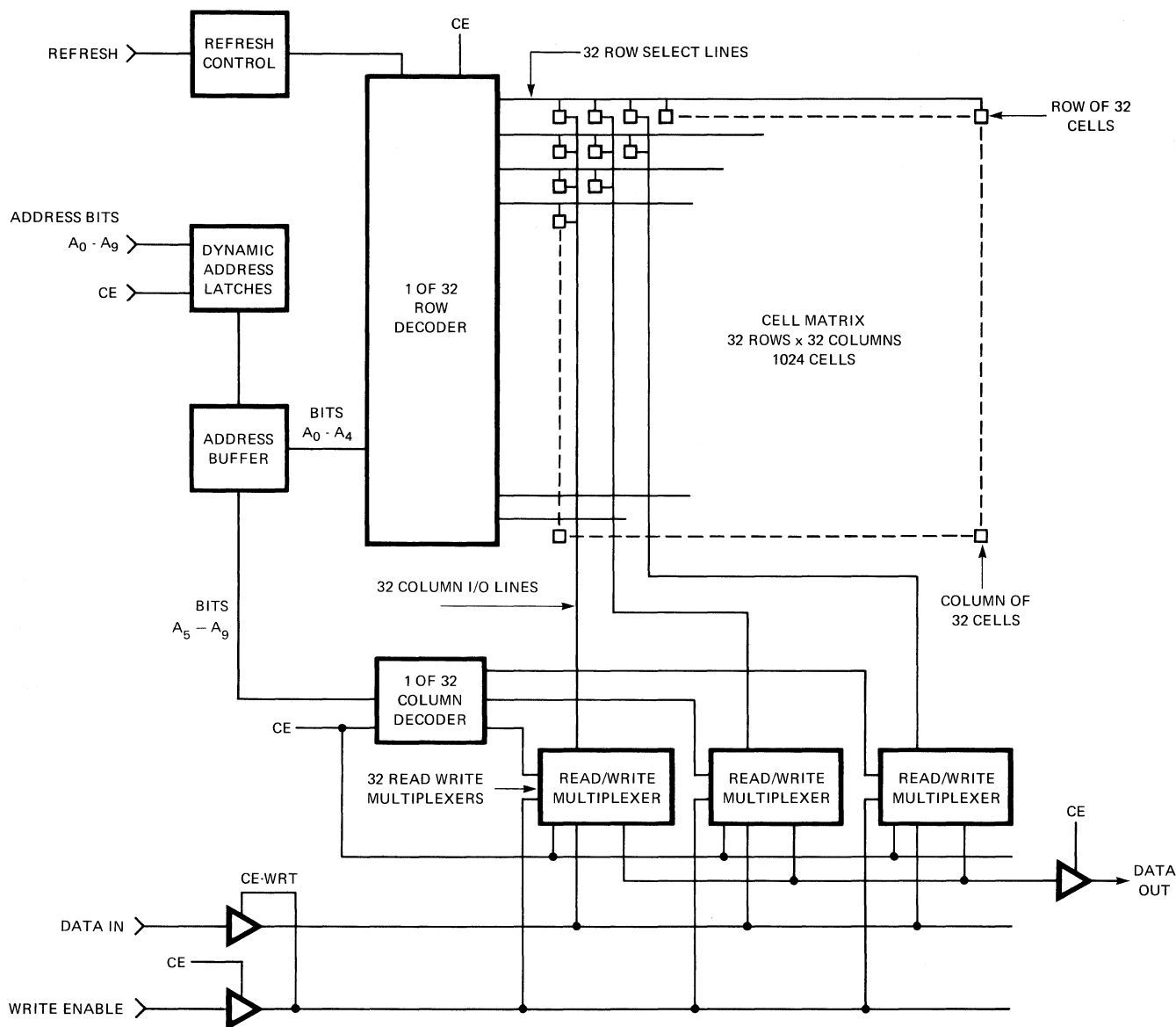


FIGURE 5—Detailed block diagram.

the chip enable signal. The Address Hold Time, (t_{AH}), indicates that the address must remain stable for at least 50nS after the leading edge of Cenable. This time allows the address latches to stabilize and become latched.

After the minimum Address Hold Time, (t_{AH}), the addresses may be reset to a low state or remain unchanged as defined by the Address Reset Time, (t_{AR}).

Low Address Setup Time, (t_{AS-}), requires that addresses be reset low for a minimum of 35nS before the start of the next cycle. This condition pre-charges the address latches which reduces the address setup time. Typically, to reduce data sensing noise and to conserve power, the address lines are reset low after t_{CO} time and left reset until the next setup time requirement. This arrangement provides

an average standby V_{DD} current during Cenable low of 6mA maximum, as opposed to 20mA required if the addresses are left at a high level until t_{AS-} time.

The Cenable signal performs all internal clocking and initiates operation. Cenable clocks the address latches, activates the address decoders, strobes the column selection buses and the data output buffer circuits. It must be in an active high state for at least 80nS (Cenable On Time, t_{CE}) to perform a read or write cycle and be active for at least 160nS (Cenable On Time for Read modify Write, t_{CEM}) for a read modify write cycle. The Cenable signal, (t_{CE}), also has a maximum active high duration of 360nS to insure that all circuits will function in their designated dynamic ranges. The Cenable Off Time, (t_{CC}), indicates that Cenable must be off or

reset low for at least 80nS. Resetting Cenable provides a gating signal for Refresh in addition to providing a pre-charge signal to the circuits and buses in the memory device.

The Write Enable signal is not a latched signal; however, if the cycle is to be a read cycle, Write Enable must be in a low state prior to or at Cenable set up time, as specified by Write Enable to Cenable Set Up Time, (t_{WSE}). Typically, the Write Enable signal is held reset to a low level until a write cycle is commanded and then becomes a Write Enable Pulse, (t_{WEP}), at least 70nS wide and must occur at least 70nS prior to the Cenable trailing edge as indicated by the write enable to Cenable End Time, (t_{WCE}). Both the Data-in and Write Enable signals are buffered and coupled to the read-write interface multiplexer. They have equivalent set up times, but the data in signal must be held at least 20nS after the write enable trailing edge. This is called the Data Hold Time, (t_{DHE}).

Refresh Timing

The Intel planar refresh technique introduces one of the easiest methods for refreshing an MOS device. It requires one, unsynchronized, input at an interval between $1\mu s$ and $10\mu s$. The refresh pulse width, (t_{RP}), needs always be 140ns greater than the Cenable pulse width. If the chip enable pulse width is 155nS then t_{RP} must be at least $155 + 140 = 295nS$. Although there is not a maximum refresh pulse width requirement, overlapping two or more Cenable cycle times with the refresh pulse will consume unnecessary power. Intel has available another 2105 model which provides reductions in cycle times to 180nS and Access Times to 80nS, by requiring a refresh signal synchronous to the system.

DRIVING THE INTEL 2105 MEMORY CHIP

As mentioned in the preceeding section, the Intel 2105 is a very high speed memory device with access times of 80 to 95nS and cycle times of 180 to 230nS.

These high speeds require fast pulse edges and high driving capability from the MOS interface drivers. Because the 2105 is an N-Channel device, a positive leading edge is required for both chip enable and addresses, as N-Channel devices are usually active high and P-Channel devices are usually active low. Consequently, a good driver circuit for P-Channel devices will not be a good driver circuit for N-Channel devices if the positive transition has been excessively compromised. More detail will be found in the next four pages.

The 2105 Inputs

The various voltage input levels for the device are defined in Table I, while Table II defines the capacitance associated with the inputs. As noted in Figure 6, the input characteristics of the 2105 input lines is the capacitance associated with the silicon gate of a MOS device. The leakage is associated with the reverse bias of the NP junction leakage (from diffusion to substrate). However, more than one gate may be internally connected to the input line. This accounts for the additional capacitance associated with the Cenable input in Table II.

Each address input provides a maximum of 6pF of capacitance to the driver output. In a typical card configuration, 16 or 32 address lines are tied together, representing a load of 100 or 200pF. Approximately half of this capacitance is to the substrate, while the other half of the capacitance

TABLE I—DC and operating characteristics

$T_A = 0^\circ C$ to $70^\circ C$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5.2V \pm 5\%$ [3], $V_{SS} = 0V$, unless otherwise specified. [2]

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. [1]	MAX.		
V_{IL}	Input Low Level Voltage (All Inputs)	$V_{SS}-1$		$V_{SS}+1$	V	
V_{IH}	Input High Level Voltage (Address, D_{IN} , WE)	4.0		6.5	V	
V_{IHC}	Input High Level Voltage (CE, Ref)	$V_{DD}-1$		$V_{DD}+0.5$	V	

NOTES: 1. Typical values are for $T_A = 25^\circ C$ and nominal supply voltages. 2. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB} . 3. The V_{BB} supply also may be equal to $-5.2V \pm 5\%$.

TABLE II—Capacitance

$T_A = 25^\circ C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5.2V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.

SYMBOL	PARAMETER	PLASTIC PKG.		UNIT	CONDITIONS
		TYP.	MAX.		
C_{IN}	Input Capacitance (Address, D_{IN} , WE, Ref)	4	6	pF	f = 1MHz. All Unused Pins are at V_{SS} .
C_{OUT}	Data Out Capacitance	4	6	pF	
C_{CE}	Effective Cenable Capacitance	65	85	pF	

NOTE: 1. This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.

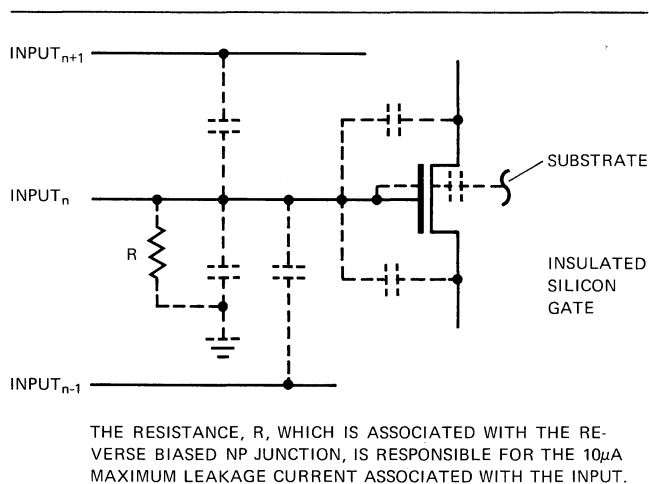


FIGURE 6—Typical input.

is to adjacent address lines. As could be expected with capacitively coupled circuits, if adjacent lines are switched, cross talk can cause adjacent inputs to change state. By driving these lines with a low impedance, this cross talk is minimized.

The chip enable input capacitance is 85pF maximum. Typically 4 of these inputs are tied together, providing a total load of 340pF. The refresh inputs present a load of 6pF each, and typically 16 or 32 lines are tied to a common drive circuit, presenting a load of 100 or 200pF.

Driving MOS Memories

When driving MOS memories, it should be remembered that the inputs to the memory device are primarily capacitive and the printed circuit trace which propagates the input pulses is a section of RF transmission line. Transmission lines have characteristic impedance and propagation delays which will interact with the driver impedance and the terminating impedance, causing reflections and delays which must be considered for optimum system performance.

Because the device inputs are capacitive, the connection of a number of device inputs to the signal input line tends to lower the characteristic impedance and increase the propagation delay by as much as ten to one. If pulses with a rise time less than the final propagation delay of the line are to be propagated, enough energy can be stored in the series inductance to cause severe reflections.

To minimize transmission line problems, the driver elements should be located as close as possible to the memory elements in the array, keeping the connecting printed circuit lines as short as possible.

Series terminations are energy absorbers and will have some effect on the rise time of the pulses being propagated. For maximum effectivity they should be located physically close to the driver element, at the input to the transmission line cir-

cuit. Parallel terminations will also absorb reflections, but will consume power whenever bias is present on the line, while series terminations will only consume power when actual pulses are being propagated. Diode clamps can also be used to solve reflection problems by installing them across the output of the driver element.

With any high speed digital circuitry, attention must be paid to ground returns, as the associated inductance and/or resistance can cause coupling to the other devices as well as modify the characteristic impedance of the line as mentioned earlier. The most efficient ground is a ground plane internal to or on one side of the printed circuit board; another method is to employ a ground grid, where all ground etch is connected vertically on one side of the board and horizontally on the other.

There are many options and trade offs to consider when selecting drivers for the 2105. Package density, printed circuit layout requirements, speed, power and cost must also be considered, with emphasis placed on each variable as dictated by the final overall system requirements.

Maintaining the Input High Level

Presently, there are two acceptable methods for driving the high level input to an MOS device. The traditional method utilizes a TTL type totem pole configuration, with an additional power supply voltage which provides an overdrive to the input of the driver emitter-follower stage, thus insuring complete saturation. This method provides a full output signal swing to V_{DD} with the capability to hold this level. The other, newer method utilizes a complementary collector output configuration. This method provides the required 2105 voltage margins with the ability to hold them, without the requirement of an additional power supply. Unfortunately, the state of the art of integrated circuits does not lend itself to on-chip complementary outputs with sufficient power and speed capabilities. Presented below are several drivers which are suitable for driving the 2105, with results summarized in table IV.

The Intel 3210 and 3211 Drivers

The Intel 3210 and 3211 MOS Memory drivers were developed specifically for N-Channel Memory Devices and have optimized the trade offs mentioned previously. The 3210 accepts standard TTL and DTL logic inputs and converts them to 2105 input levels, while the 3211 accepts standard ECL 10,000 series inputs and converts them to 2105 input levels. Both devices utilize a complimentary collector output configuration by connecting the PNP portion of the circuit external to the integrated package. Logic symbols for each device are presented in Figure 7. Each device contains four

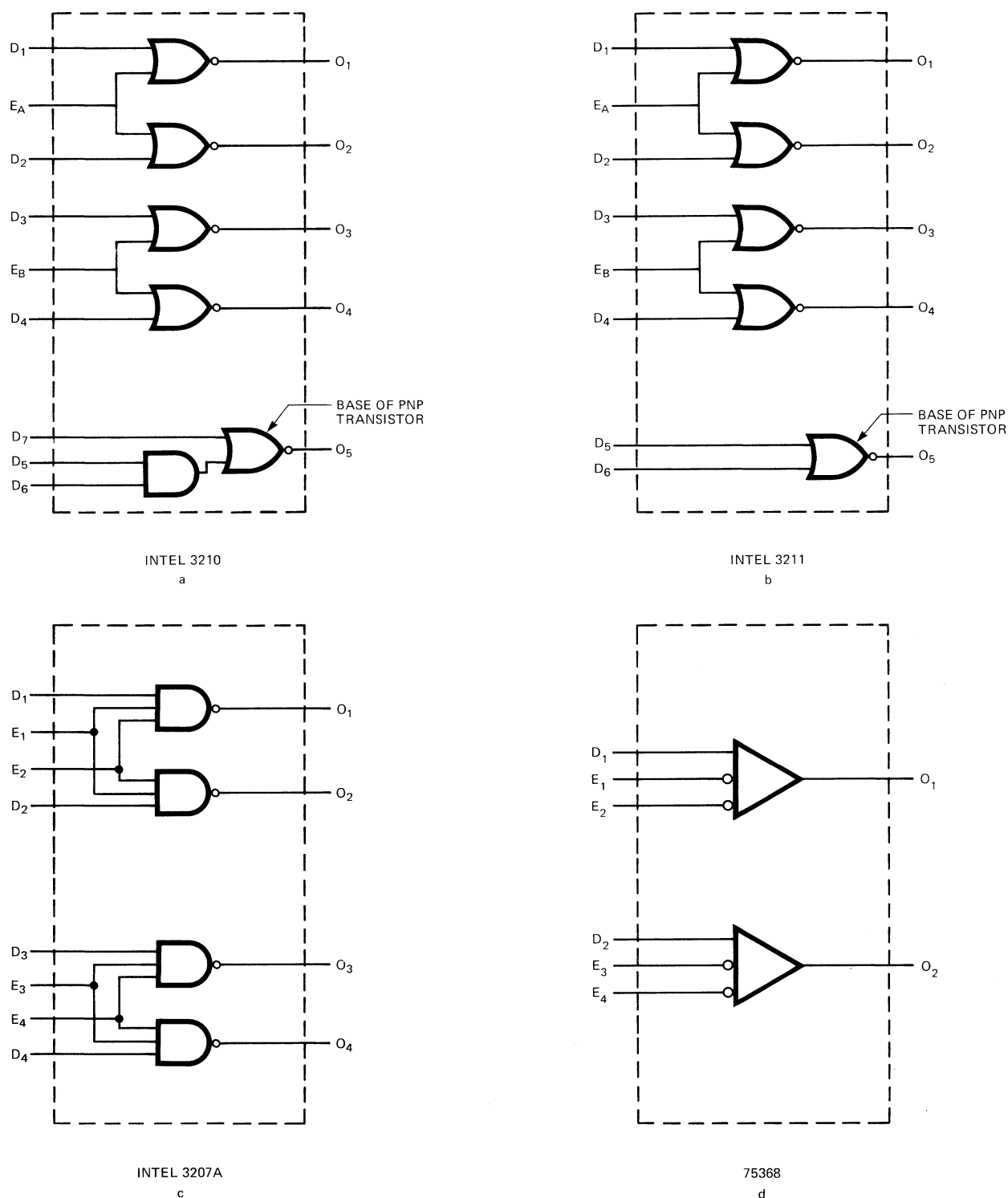


FIGURE 7—Driver logic symbols.

(4) low level converters and one high level converter. The high level circuit drives four 2105 chip enable inputs with typical rise times of 25nS with the required voltage margins. The NOR inputs to the device provide convenient logic elements for gating or strobing addresses, write enable, chip enable and hidden planar refresh to the required active high state. This results in a reduction of chip count, delays and printed circuit board layout com-

plexity. Each chip provides the required output impedance, diode clamps and voltage margins, generally eliminating the need for external series termination resistors and clamping diodes to obtain the expected performance from the memory device. Elimination of the extra power supply also eliminates the extra system and card voltage distribution problems and the decoupling associated with it.

The Intel 3207A

The Intel 3207A will provide the required 2105 margins without the requirement of a discrete PNP transistor. It does, however, require an additional voltage supply of 15 volts connected to the 3207A V_{BB} terminal. The 3207A has 4 circuits per package which can be connected to drive either low voltage or high voltage 2105 inputs, provided all 4 circuits are selected to drive the same level. For the low voltage configuration the 3207A V_{SS} pin must be tied to V_{CC} (+5V). The logic gating (refer to Figure 7) consists of TTL level NAND gates, which may be compatible with the overall system requirements.

As noted in the data sheet, the device has not been characterized for use with the voltages shown in Table III.

TABLE III—3207/2105 voltage conversion

HIGH VOLTAGE			LOW VOLTAGE	
3207	2105	Voltage	2105	Voltage
V_{SS}	V_{DD}	12V	V_{CC}	5V
V_{BB}	Extra ^[1]	15V	V_{DD}	12V
V_{DD}	V_{SS}	0V	V_{SS}	0V

NOTE 1: The 15V supply should be series connected to the 12V supply.

The 75368 Driver

The 75368 is a dual ECL/MOS memory driver packaged in a standard 14 pin Dip. The logic circuit is shown in Figure 7d. Each package contains 2 devices with 3 standard ECL inputs, one non inverting and two inverting.

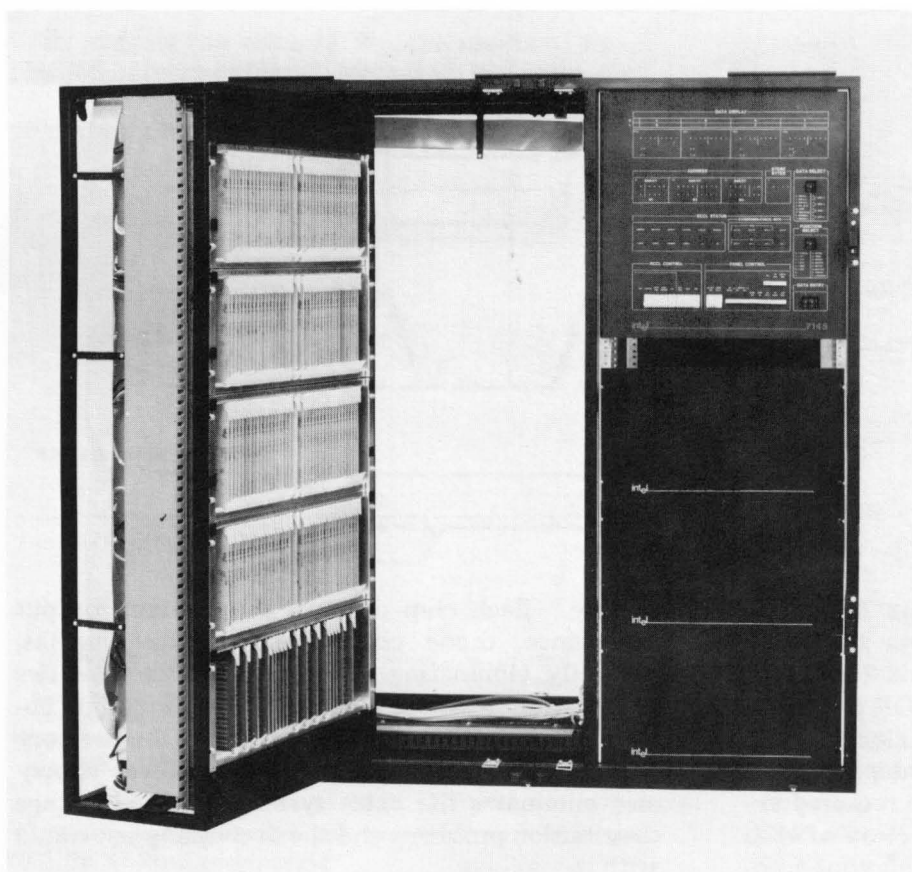
The device does require an additional supply voltage of 15V which can be developed by series connecting a +3V supply to the +12V supply. This supply, V_{CC3} , is expected to provide .6mA for both outputs high, or 3mA for both outputs low.

At the time of this writing complete data is not available on the 75368, but performance curves indicate a typical low level propagation time of 22nS, driving a load of 400pF, and actual lab data indicates a high level propagation time of 25nS driving a load of 200pF.

A possible system approach would be to use the low level portion of the Intel 3211 for driving address lines, and the 75368 for the high level inputs.

TTL as a Low Voltage Driver

Because the 2105 requires a 4.0 volt minimum input high level, a low output impedance from the driver, and an active high transition, using an H or S series TTL logic gate as a low level driver will result in degraded 2105 performance. If a pull-up re-



Intel Memory Systems Division
IN7145 System, 1 megabyte
storage capacity, 128K x 72.

sistor is used to bring the output up from a normal 2.4V, the rise time from the 2.4V level is directly dependent on the R/C time constant of the pull-up resistor and the capacitive load of the memory device pins connected. The minimum pull up resistance which can be used is dependent on the sinking ability of the TTL gate. For example, a standard quad H or S series gate (not a buffer or line driver) will sink 20mA and maintain less than 0.4V at the low output. For $V_{CC} = 5V$, 20mA dictates a minimum pull-up resistor of 250 ohms. Sixteen 2105 low level input lines present a capacitive load of 96pF. Tests and TTL data sheet graphs show that the gate has a total rise time of 35nS to the 4.0 volt level. Extrapolating, the data sheet gives 15nS to the guaranteed 2.4V level and 20nS from the 2.4V level to the 4.0V level. The 20nS figure is close to the calculated value found by transforming the RC exponential equation to:

$$t = RC \ln \frac{V_{CC} - E_i}{V_{CC} - E_c}$$

where E_i is equal to the initial capacitor voltage (2.4V) E_c is equal to the final capacitor voltage (4.0V). This gives a calculated value of an additional 20nS to go from the 2.4V to the required 4.0V level. To provide a margin of an additional 0.8V requires an additional 20nS. The 250 ohms represents a high impedance relative to the other signals and is subject to cross talk from them. Replacing the standard TTL gate with dual buffers or line driver type gates which are capable of sinking the current from a 100 ohm pull-up resistor improves the coupling problem considerably, but is accompanied with an increase in power dissipation and an increase in package count. Using 100 ohm pull-up resistors with the gate output in the normal low state dissipates 250mW in the resistor.

TABLE IV—Driver comparison

	FIGURE	CIRCUITS/DIP		TOTAL POWER [1]		PROPAGATION DELAY + RISE TIME (typical)		SUPPLIES
		High Level	Low Level	mW Typical	mW Maximum	Low Level	High Level	
TTL								
3210	7a	1	4	410/290	550/390	13 nS [2]	30 nS [3]	+5V, +12V
3207A	7c	4	(4) [4]		900/250	19 nS [2]	35 nS [2]	+5V, +12V, +15V [5]
ECL								
3211	7b	1	4	500/400	675/550	18 nS [2]	33 nS [3]	+5V, +12V, -5.2V
75368	7d	2	(2) [6]			22 nS [2]	28 nS [2]	+5V, +12V, +15V, [5] -5.2V, $V_{REF} = -1.3$

NOTES:

1. Power presented for all outputs high/all outputs low.
2. 200pF load.
3. 350pF load.
4. Each DIP may be connected to provide either high level or low level drivers.
5. The +15V should be a 3V supply series connected to the 12V supply.
6. Each circuit may be connected to provide either a high level or a low level driver.

SENSING THE INTEL 2105 MEMORY CHIP

This section will discuss the output waveform and biasing criteria, present several TTL and ECL sensing configurations for the 2105, and summarize them in terms of speed, power and total package size.

Figure 8 presents read cycle waveforms and defines the various states and times pertinent to a read cycle. Figure 9 is taken from an actual double exposed photograph of two read cycles, one reading a Zero and one reading a One. The end of Cenable Output Delay Time (t_{CO}), which is also the end of the Address to Output Access Time (t_{ACC}), is defined as that point in time when, with $V_{TERM} =$ ground and $R_L = 100\Omega$, V_{OL1} is more negative than $-110mV$, or V_{OH1} is less negative than $-40mV$.

Figure 10 shows the equivalent output circuit of the 2105. A differential output is produced which, with CE on, allows about 4mA to flow in the $\overline{DATA\ OUT}$ terminal. Historically, outputs are measured with $R_L = 100\Omega$. C_L is selected to be 50pF, which represents the capacity of 8 $\overline{DATA\ OUT}$ lines OR connected. When the data from the array is Low, the path from V_{BB} through the internal resistor, the CE gate and the left gate in the diagram is completed, presenting a path of approximately $1.2K\Omega$ from $\overline{DATA\ OUT}$ to V_{BB} . Conversely, when data from the array is High, V_{BB} is connected to ground through the same load; about $1.2K\Omega$. As will be shown later, this output gate structure behaves essentially as a constant current source when data out is High.

By varying the value of R_L , the results of figure 11a and 11b are obtained. Note that, as the value of

R_L is increased a larger voltage swing is produced. The maximum voltage produced with $R_L = 100\Omega$ was 400mV, while for $R_L = 500\Omega$ a voltage of 1.4V was produced.

As figure 11a indicates, increasing the resistive part of the R/C load results in stretching the trailing edge of the $\overline{DATA\ OUT}$ (V_{OH1}) signal into the next cycle. This would only be a problem if excessive stretch of the previous cycle was severe enough to change the discrimination level of the next cycle, thus producing a pattern sensitive problem.

The discrimination level, V_{TERM} , (refer to figure 10) can be varied by biasing the load above or below ground. An example of this can be found in the 2105-2 data sheet where $V_{TERM} = -1.175V \pm 60mV$. Experiments have been performed with bias levels between $-2V$ and $+5V$ with results indicating that, within these limits, waveforms similar to figure 11 are produced. For example, if a voltage divider is created between the $\overline{DATA\ OUT}$ pin, $+5V$ and ground as shown in figure 12, a voltage swing compatible with TTL levels is produced, without significantly affecting t_{CO} or the access time. C_L was equal to zero for this experiment.

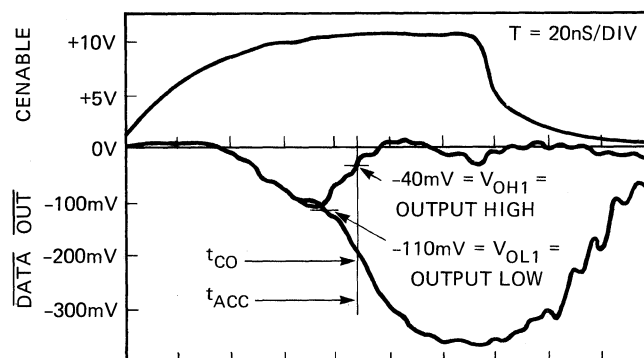


FIGURE 9—2105 output waveform.

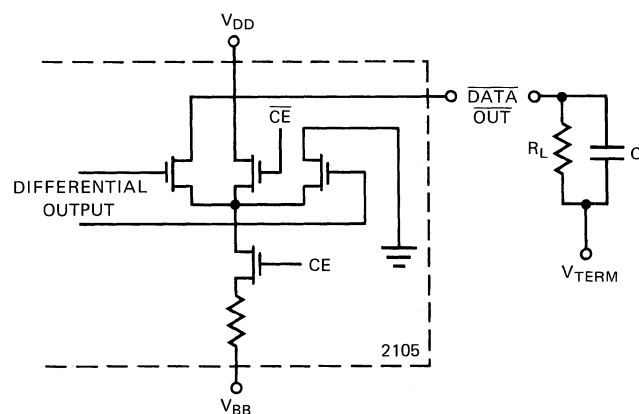
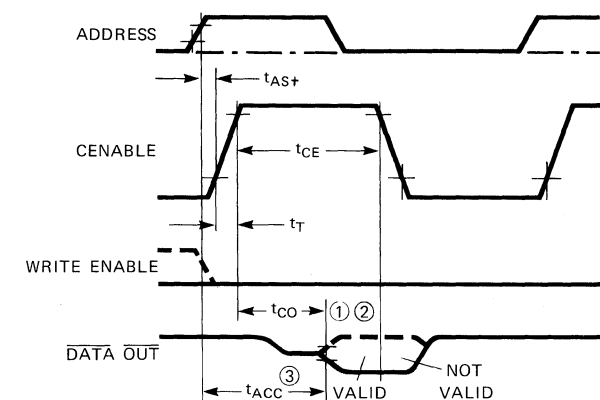


FIGURE 10—Equivalent output circuit of 2105.



NOTES:

1. The parameter t_{CO} (Cenable output delay) is defined at V_{OL1} (output voltage low at point 1) or V_{OH1} (output voltage high at point 1), whichever occurs last, with $R_L = 100\Omega$ and $C_L = 50pF$.
2. Data out is valid during t_{CE} (Cenable on time) or until write enable goes high.
3. t_{ACC} (address to output access time) is defined as t_{AS+} (address setup time) + t_r (Cenable rise time) + t_{CO} .

FIGURE 8—Read cycle timing.

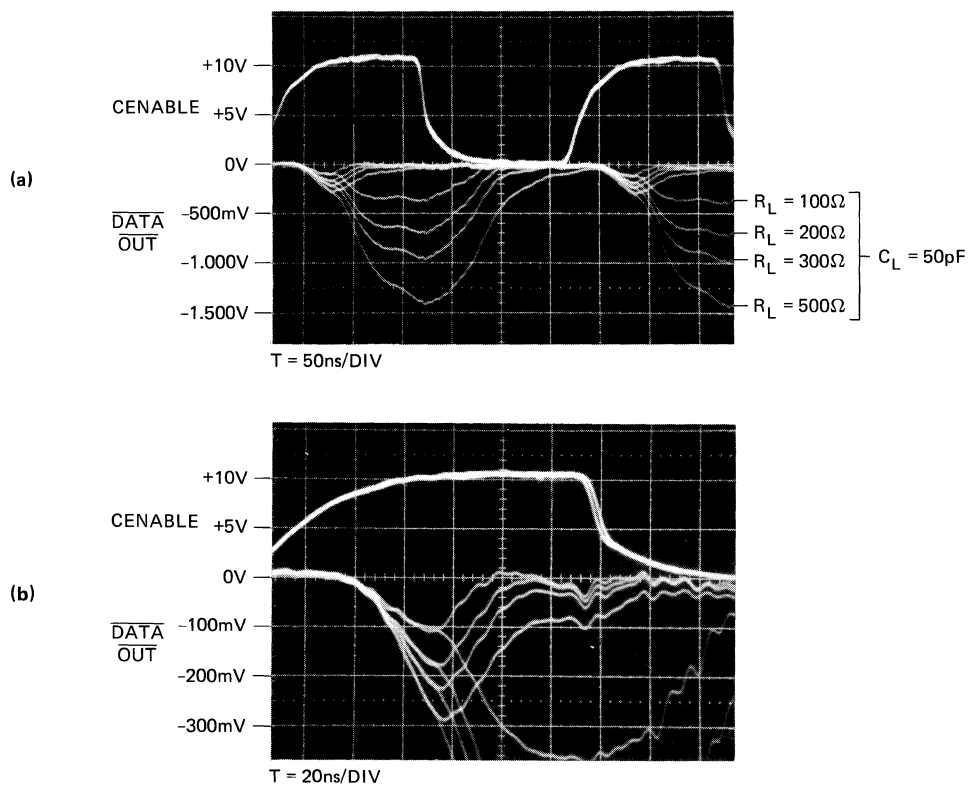


FIGURE 11— $\overline{\text{DATA OUT}}$ waveforms.

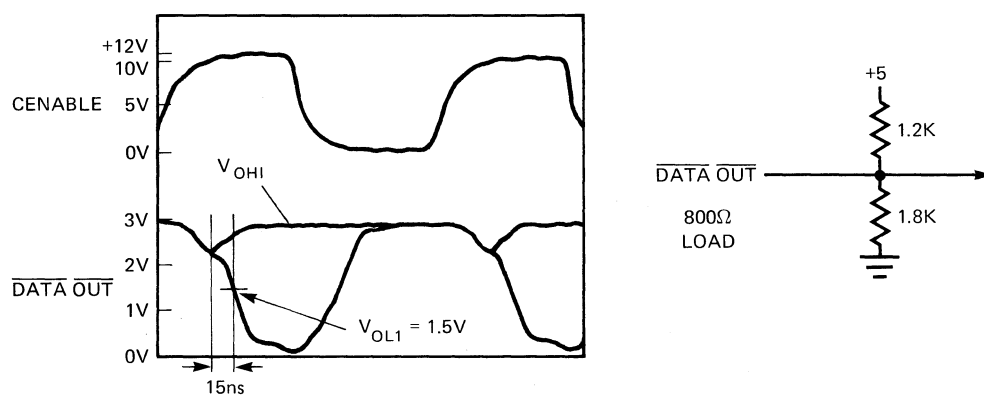


FIGURE 12— $\overline{\text{DATA OUT}}$ signal with bias.

The circuits presented in Figures 13-18 represent six sensing and biasing circuits which provide compatibility with a variety of TTL and ECL data buses. For the purpose of comparing the circuits, Sense Time, (t_s), will be defined as the additional time required beyond the Cenable Output Delay, (t_{CO}), for the sense amplifier to distinguish between a One or a Zero and convert it to a standard logic threshold level. t_s includes worst case propagation time, t_{PROP} .

Figure 13 shows the Intel 3208 hex sense amplifier configuration. The 3208 provides a 60mV level detect, a data output strobe, and TTL open collector outputs. The only supply requirement is a single +5V supply, and, for this configuration both the reference voltage, which is common to all 6 inputs, and the bias voltage are positive with respect to ground.

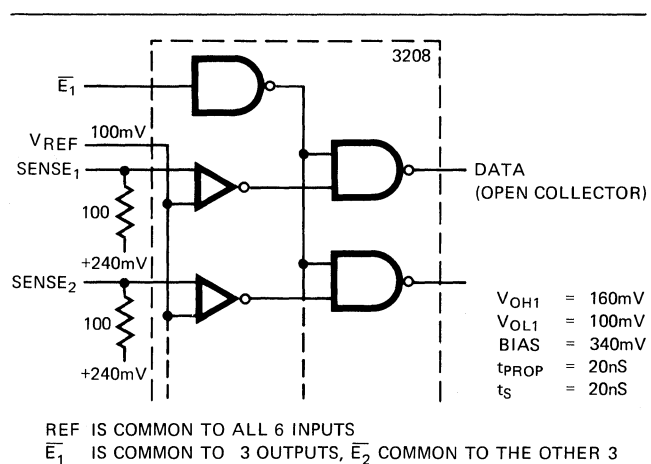


FIGURE 13—Intel 3208.

Figure 14 shows the Intel 3408 hex sense amplifier configuration. The 3408 is essentially identical to the 3208, but has an open window data latch at the output of each amplifier, allowing data to be stored after sensing by applying a 30nS minimum write pulse. The data latch feature can be disabled by grounding the WRITE input.

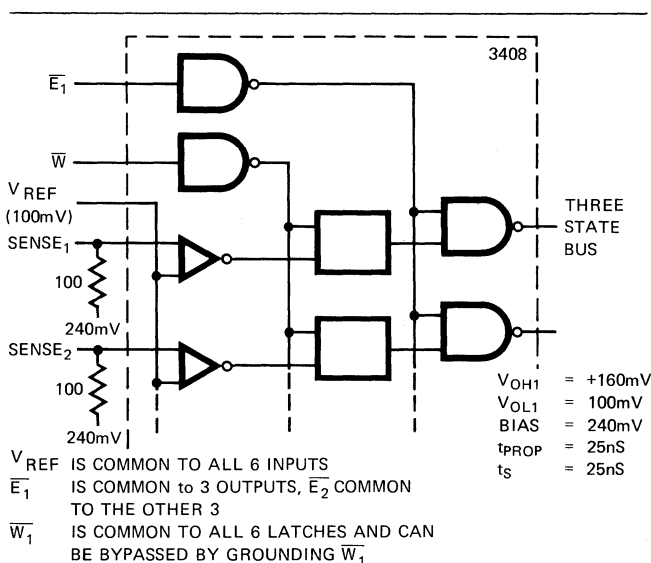


FIGURE 14—Intel 3408.

tical to the 3208, but has an open window data latch at the output of each amplifier, allowing data to be stored after sensing by applying a 30nS minimum write pulse. The data latch feature can be disabled by grounding the WRITE input.

Figure 15 shows a 74S03 TTL gate used as a 2105 sense circuit. 74S03's have four gates as shown per standard 14-pin DIP. To provide TTL compatible levels of +2.0V to +0.8V from the 2105, the input resistance to the TTL gate must effectively be 800Ω at a +2.5V bias level, producing an equivalent V_{OH1} of 2V. Although the maximum 74S03 delay is 7ns, equating the wide TTL threshold margin relative to V_{OH1} results in a sense time of 22ns.

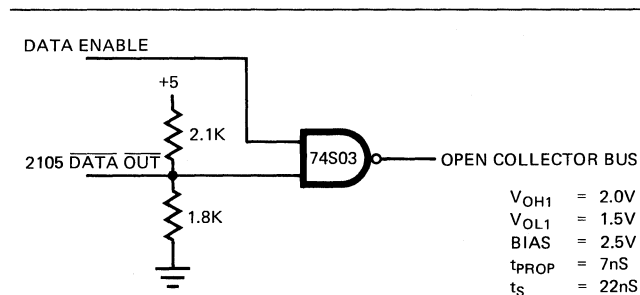


FIGURE 15—TTL 74S03 NAND gate.

Figure 16 shows an ECL 10125 ECL to TTL converter used as a 2105 sense amplifier. The 10125 is available with four circuits per standard 16-pin DIP. Several bias schemes are possible using a differential input; however, the one shown allows an ECL data strobe or enable gate to be OR tied to the 2105 data out line. This circuit will have a t_s of 9ns at the TTL totem pole output.

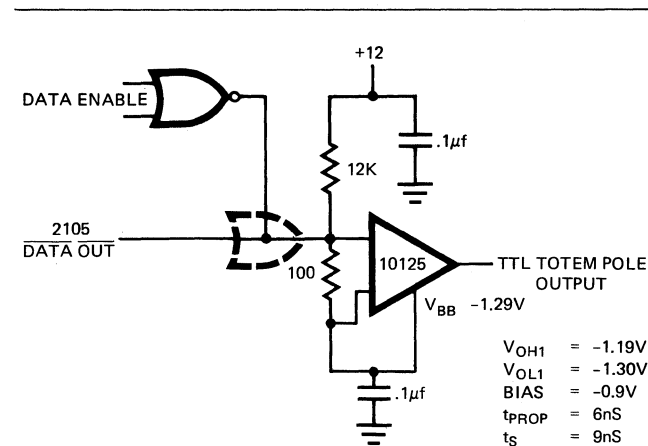


FIGURE 16—ECL 10125 to TTL translator.

Figure 17 shows the 2105 interfacing with an ECL 10101 gate. The 10101 contains four gates per standard 16-pin DIP, and has provided a strobe line common to all four inputs. This configuration provides a form of hysteresis which produces a rel-

atively low circuit gain and input resistance until the sense input and strobe signal reaches the gate's active point. At this point, regeneration, via the 300Ω feedback resistor, occurs, which acts to decrease the switching time through threshold. The sense time, t_s , for this circuit is 5nS. Removing the 300Ω resistor and connecting a 10KΩ resistor between +12V and DATA OUT eliminates the critical strobe requirement, but increases t_s to 7nS.

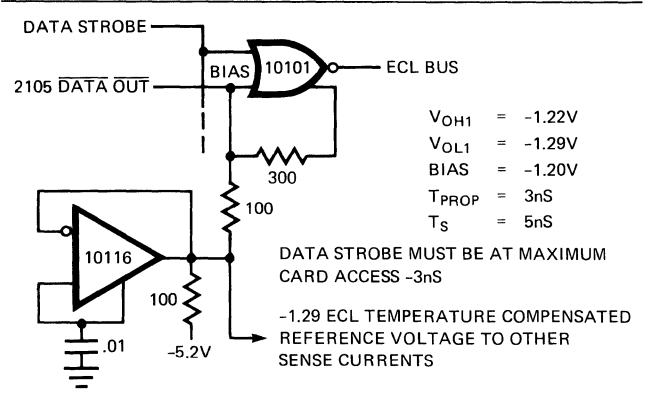


FIGURE 17—ECL 10101 gate.

Figure 18 illustrates an ECL differentially cascaded 2105 sense amplifier configuration. Differentially cascading the ECL 10116 and 10115 will provide a sharper switching level to the data out

bus by way of the double threshold points and the increased gain of the differential input. The 10115 contains four devices per 16-pin DIP, and the 10116 contains three devices per 16-pin DIP. This circuit has a t_s of 6nS.

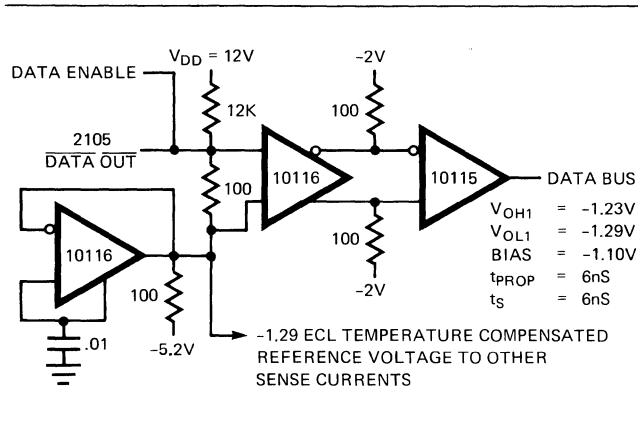


FIGURE 18—Cascaded ECL 10116 and 10115.

Table V presents a summary of the various parameters to aid in the selection of sensing circuits. For TTL applications the 3208/3204 amplifiers provide the highest package density, while the 74S03 provides the lowest power dissipation. For ECL applications, the 10101 provides the lowest mW•ns quotient.

TABLE V—Sense amplifier comparison

	FIGURE	CIRCUITS/DIP	DIPs/AMPLIFIER	t_s	POWER/SENSE BIT		SUPPLIES
TTL							
3208	13	6	1/6	20ns	110mW	2200	+5.0V
3408	14	6	1/6	25ns	104mW	2600	+5.0V
74S03	15	4	1/4	22ns	17mW	374	+5.0V
ECL							
10125	16	4	1/4	9ns	95mW	855	+5V, -5V
10101	17	4	1/4	5ns	25mW	125	-5V
10115	18	4	1/4	6ns	27.5mW	48.8mW	292.8
10116		3	1/3		21.3mW		

2105 VOLTAGE, CURRENT AND DECOUPLING CONSIDERATIONS

Voltage and ground distribution and decoupling are extremely important factors in the design of MOS memory arrays, cards and systems. The 2105 is tested to operate within specified voltage and temperature margins and operation will be severely degraded by inadequate voltage and ground distribution or insufficient decoupling. This section will analyze the nature of the power required for proper operation of the 2105, and present typical printed circuit board layout and voltage decoupling schemes.

Power Supply Requirements

The 2105 N-channel device requires only two voltages for operation. V_{DD} , the most positive voltage, is +12 volts, V_{BB} is either -5 volts or -5.2 volts, and V_{SS} is 0 volts (ground).

V_{BB} is the substrate voltage and is normally equal to the standard ECL -5.2 volt level. V_{BB} is the most negative voltage present and serves to maintain a back bias between the substrate and active elements. Back biasing the substrate increases the MOS threshold levels, and maintains isolation between independent adjacent elements. The current associated with V_{BB} , I_{BB} has three states that are of concern to the designer. The three are presented in Table VI. I_{BB1} is the V_{BB} current with V_{BB} on, but does not include the leading and trailing edge transition currents. I_{BBS} is the standby current and includes the refresh transient currents. $I_{BB AV}$ is the average V_{BB} current over a memory cycle. All three currents vary inversely with temperature as shown in Figure

19. Typical I_{BB} transients are presented in Figure 20.

A positive voltage on the N-channel substrate could occur if the V_{BB} line becomes accidentally connected to a positive voltage line and if the V_{BB} power supply current limit is set lower than the current limit of the positive supply. A positive N-channel substrate to ground (V_{SS}) bias will result in a substrate current through each 2105 device. By use of current limiting power supplies and connecting a diode from V_{BB} to V_{SS} , (anode to V_{BB} and cathode to V_{SS}) the forward substrate currents will be reduced, thus preventing possible catastrophic results from occurring.

V_{DD} is the most positive voltage associated with an N-channel device, and for the 2105 is equal to 12 volts. The V_{DD} current, I_{DD} , varies depending on the mode of operation of the memory. The various levels are presented in Table VII. I_{DD1} is the V_{DD} current with V_{BB} on, but does not include the leading and trailing edge transition currents. I_{DD2} is the current for V_{BB} off and the addresses high which is the maximum current related to addresses cycling on devices that are not selected. I_{DDS} is the standby current with V_{BB} off, and is also related to the refresh frequency. The values presented in Table II are for a refresh period of 10 μ S. $I_{DD AV}$ is the average V_{DD} current over a memory cycle; presented in Table VII for a 230nS cycle time. Typical I_{DD} transient currents are presented in Figure 21, while the I_{DD} current variations with temperature are presented in Figure 22.

TABLE VI— I_{BB} Current

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ^[1]	MAX.		
I_{BB1}	V_{BB} Current During Cenable ON		5.5	10.5	mA	$V_{CE} = 13.1V$, $V_{IN} = 0V$ to 4V, $D_{OUT} = 0V$, $T_A = 25^\circ C$
I_{BBS}	Standby V_{BB} Current During Cenable OFF		2.5	5.0	mA	$V_{CE} = 0V$, $V_{IN} = 0V$ to 4V, $D_{OUT} = 0V$, $t_{REF} = 10\mu s$, $T_A = 25^\circ C$
$I_{BB AV}$	Average V_{BB} Supply Current		4.5	9.0	mA	$t_{cyc} = 230ns$, $t_{REF} = 10\mu s$, $T_A = 25^\circ C$

NOTE: 1. Typical values are for $T_A = 25^\circ C$ and nominal supply voltages.

TABLE VII— I_{DD} Current.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ^[1]	MAX.		
I_{DD1}	V_{DD} Current During Cenable ON		25	40	mA	$V_{CE} = 13.1V$, $V_{IN} = 0V$ to 4V, $T_A = 25^\circ C$
I_{DD2}	V_{DD} Current During Cenable OFF, Address High		13	20	mA	$V_{CE} = 0V$, $V_{IN} = 4V$, $T_A = 25^\circ C$
I_{DDS}	Average Standby V_{DD} Current During Cenable OFF		3.0	6.0	mA	$V_{CE} = 0V$, $V_{IN} = 0V$, $T_A = 25^\circ C$, $t_{REF} = 10\mu s$
$I_{DD AV}$	Average V_{DD} Supply Current		25	39.0	mA	$t_{cyc} = 230ns$, $t_{REF} = 10\mu s$, $T_A = 25^\circ C$

NOTE: 1. Typical values are for $T_A = 25^\circ C$ and nominal supply voltages.

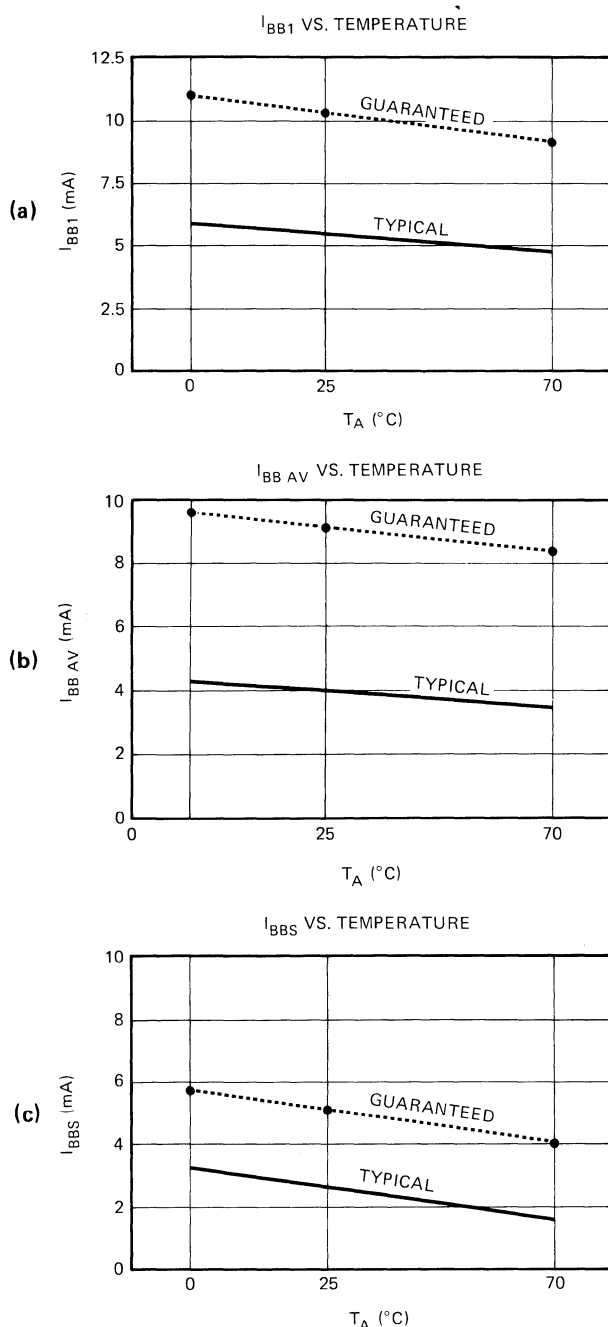


FIGURE 19— I_{BB} VS. Temperature.

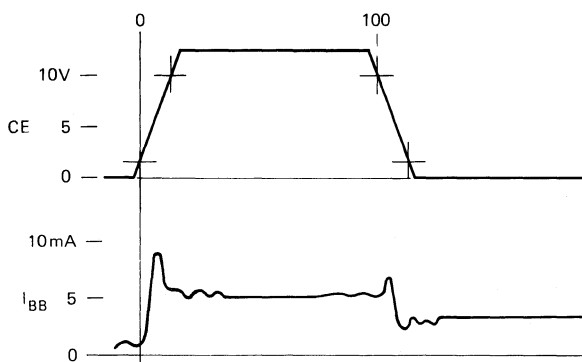


FIGURE 20—Typical I_{BB} transients.

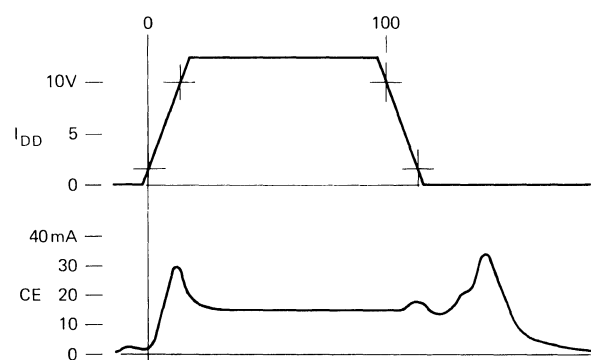


FIGURE 21—Typical I_{DD} transients.

As noted in Table VII, the I_{DDs} standby current includes the average of the planar refresh current. During each refresh pulse, a typical current surge in the order of 100mA and 20nS duration is drawn from the V_{DD} supply. The amount of standby current represented by refresh is calculated by averaging this I_{DD} refresh pulse over the 10 μ S refresh cycle time. Stated in equation form:

$$I_{REF AV} = \frac{\text{ON TIME}}{\text{TOTAL TIME}} \times I_{PREF}$$

OR, numerically

$$I_{REF AV} \pm \frac{20 \times 10^{-9} \text{ SEC}}{10 \times 10^{-6} \text{ SEC}} \times 100\text{mA} = .2\text{mA}$$

The above equation indicates that the average refresh current is proportional to the refresh frequency. Thus, doubling the refresh rate from 100KHz to 200KHz would double $I_{REF AV}$, or, for the I_{DDs} value in Table VII,

$$\begin{aligned} I_{DDs} &= I_{MIN} + I_{REF AV} \\ &= 2.8\text{mA} + .4\text{mA} = 3.2\text{mA} \end{aligned}$$

Memory Card Current Considerations

In this section, the previously described device specifications, tables, waveforms and graphs are used to calculate the current requirements at the card and system levels. Card calculations of both the average and peak currents provides information on the systems power supply, distribution, and decoupling requirements.

Card Calculations (I_{DDs})

The total memory card I_{DDs} current equals the sum of the 2105 and driver standby currents. Calculating the standby current for a typical 16K x 4 or 32K x 2 memory card with 64 Intel 2105 memory devices and 18 Intel 3211 high voltage drivers is shown in Table VIII.

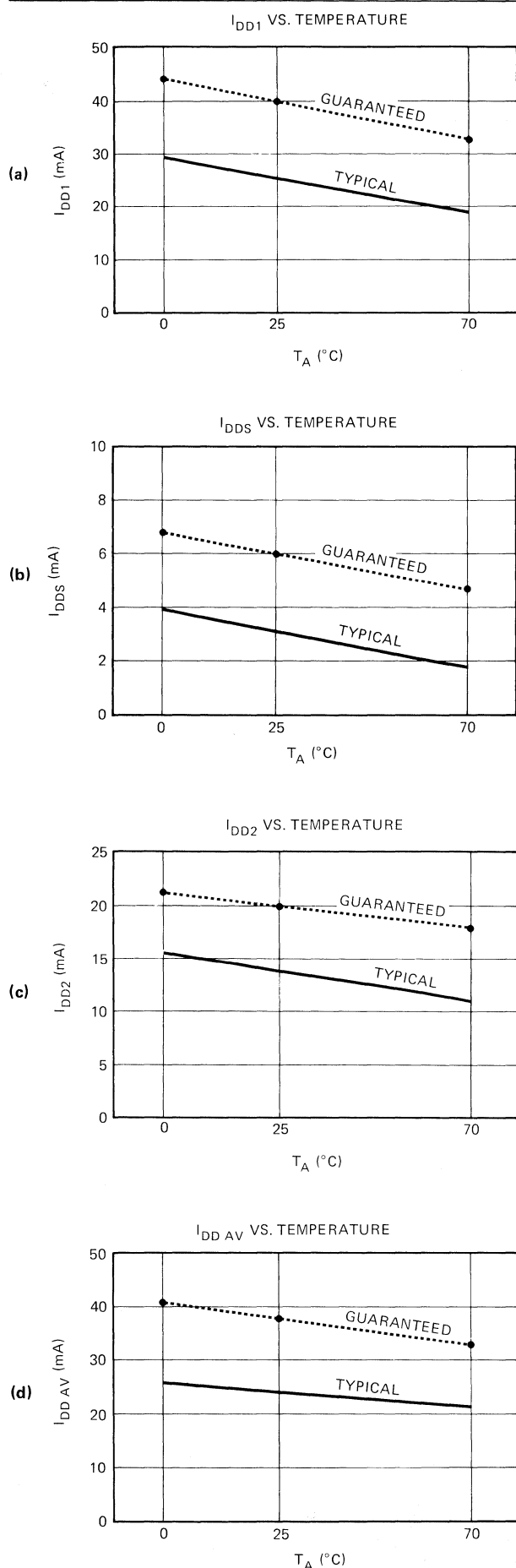


FIGURE 22— I_{DD} Vs. temperature.

TABLE VIII— I_{DD5} Current

DEVICE	NO. OF DEVICES	I_{DD5} /DEVICE ^[1]	TOTAL ^[1]
Intel 2105	64	3mA	192mA
Intel 3211	18	12mA ^[2]	216mA
Total I_{DD5} =			408mA

NOTES:

1. Typical values for nominal voltages and temperature.
2. I_{DD1} from 3210/3211 data sheet.

Card Calculations ($I_{DD CYC}$)

The total I_{DD} cycle current at the card level equals the sum of the currents for both the selected and unselected devices. The number of devices selected on the card is determined by the card and system architecture. The decode format utilized for a particular architecture is dependent on the computer central processor word length, desired storage capacity, and memory modularity. Other factors to consider are the input capacitive load presented to the sense amplifier by OR connecting individual devices, and the number of devices that can be enabled by a single cenable driver and maintain the required cycle and access time.

Figure 23 shows the decoding formats for both 4K x 16 bits and 32K x 2 bit cards, with power calculations presented in Table IX. These calculations are presented as an illustrative example and do not necessarily reflect optimum design for any particular size memory. The 4K x 16 bit card requires that 16 of the 64 2105 memory devices be selected on each cycle, while the 32K by 2 bit card only requires that 8 of the 64 devices be selected.

The number of devices selected per cycle should be minimized while complying with overall system requirements as mentioned above. Each device selected requires the driver to produce enough current to charge the cenable input capacitance. This current can be calculated from

$$P = V^2 C f = IV$$

OR

$$I_{CYC} = V C f$$

where

V is V_{DD}

C is the input capacitance of the cenable input of the 2105

f is the frequency defined by the reciprocal of the cycle time

which is the power required to charge and discharge a capacitor. The actual V_{DD} current is one half I_{CYC} shown above, as the current flows from the driver only during the charging of the input capacitance.

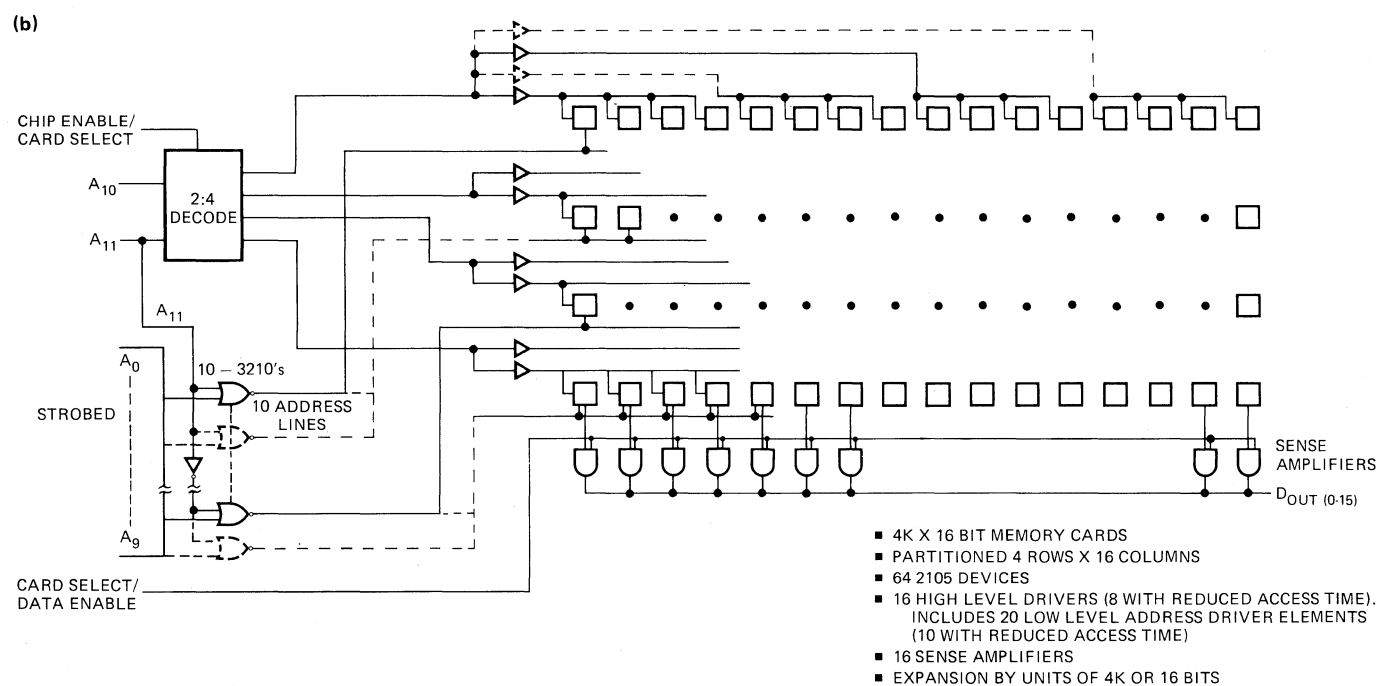
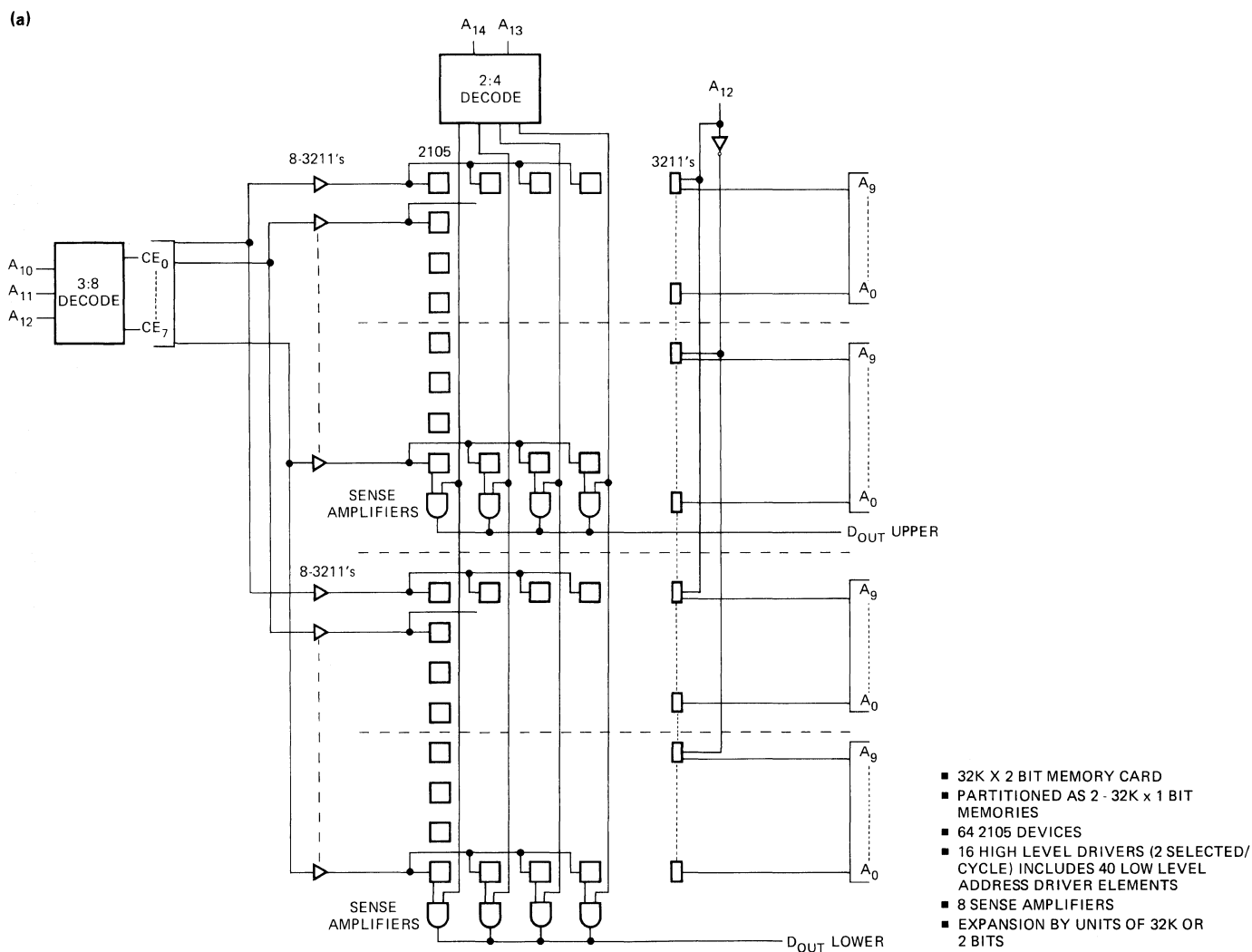


FIGURE 23—Memory card formats.

As shown in Table IX, a large percentage of the total I_{DD} is required for the 56 unselected devices which receive address information. A reduction in the current, which is I_{DD2} , is possible by enabling addresses to only half of the devices on the card during each cycle. This can be done by using the most significant address bit as shown in Figure 23. Enabling addresses to the upper or lower memory blocks would reduce the total I_{DD2} for the 56 unselected devices from 386mA to 166mA, but the 32 devices which have neither a selected enable or selected addresses will still require a standby current of 96mA which provides a net current reduction of $386 - (166 + 96) = 124$ mA.

Card Calculations (I_{BBS})

The total memory card V_{BB} standby current, I_{BBS} , equals the sum of the 2105 I_{BBS} current

plus the sum of the I_{EE1} current for the drivers, in addition to the ECL current requirements. I_{BBS} for 64 2105 devices is 160mA; I_{EE1} for 18 3211 drivers is 360mA. Therefore, the total standby V_{BB} current is 520mA not including the standby current for decoders and other memory control devices.

Card Calculations ($I_{BB CYC}$)

The total V_{BB} cycle current, $I_{BB CYC}$, is equal to the sum of $I_{BB AV}$ for all the selected devices and I_{BBS} for all the unselected devices. As with the V_{DD} calculations, this calculation does not include the memory control devices.

Table X presents the $I_{BB CYC}$ current for a 64 device card, calculated in a similar manner to Table IX.

TABLE IX— I_{DD} cycle current

DEVICE	NO. OF DEVICES SELECTED	NO. OF DEVICES NOT SELECTED	I_{DD}/DEVICE	I_{DD} TOTAL
Intel 2105	8		25 mA ^[1]	200 mA
		56	6.9 mA ^[2]	386.4 mA
Intel 3211	2		19.7 mA ^[3]	39.4 mA
		16	12 mA ^{[1] [4]}	192 mA
Total $I_{DDY CYC}$				= 817.8 mA

NOTES:

1. I_{DD1} from Data Sheet:

$$2. I_{DD2} \times \frac{t_{CE}}{t_{cyc}} + I_{DD1} \times \frac{t_{\overline{CE}}}{t_{cyc}} = 13 \times 10^{-3} \times \frac{90 \times 10^{-9}}{230 \times 10^{-9}} + 3 \times 10^{-3} \times \frac{140 \times 10^{-9}}{230 \times 10^{-9}} = 6.9 \text{mA.}$$

$$3. I_{DD2} \times \frac{t_{CE}}{t_{cyc}} + I_{DD1} \times \frac{t_{\overline{CE}}}{t_{cyc}} + \frac{V_{DD}}{2} \times C \times \frac{1}{t_{cyc}} = 26 \times 10^{-3} \times \frac{90 \times 10^{-9}}{230 \times 10^{-9}} + 12 \times 10^{-3} \times \frac{140 \times 10^{-9}}{230 \times 10^{-9}} + \frac{12}{2} \times 85 \times 10^{-12} \times \frac{1}{230 \times 10^{-9}} = 19.7 \text{mA.}$$

4. Includes 2 Refresh Drivers.

$$C = 85 \text{pF}/2105 \text{ enable input}; V_{DD} = 12 \text{V}; f = \frac{1}{t_{cyc}}; \text{Duty Cycle} = \frac{t_{CE}}{t_{cyc}} \text{ (Cenable ON);}$$

$$\text{Duty Cycle} = \frac{t_{\overline{CE}}}{t_{cyc}} \text{ (Cenable OFF); } t_{cyc} = 230 \text{nS}; t_{CE} = 90 \text{nS}; t_{\overline{CE}} = 140 \text{nS}$$

TABLE X— I_{BB} cycle current

DEVICE	NO. OF DEVICES SELECTED	NO. OF DEVICES NOT SELECTED	I_{BB}/DEVICE	I_{BB} TOTAL
2105	8		4.5 mA ^[1]	36 mA
		56	2.5 mA ^[1]	140 mA
3211		18 ^[2]	20 mA	360 mA
Total $I_{BB CYC}$				= 536 mA

NOTES: 1. Typical Value. 2. From 3211/3212 Data Sheet.

Voltage Distribution

Multilayer Printed Circuit Board Method

Multilayer printed circuit board construction is the preferred method of distributing voltages and ground on any very high-speed memory card. A four layer printed circuit board is usually constructed with the voltage and ground planes located as two inner layers with horizontal or vertical trace runs as the top and bottom planes. A multilayer or ground plane printed circuit board will provide, for a given board size, additional copper for power distribution, more consistent impedance and transmission line characteristics, and more separation between traces. A segment of a typical array is shown in Figure 24.

The factors mentioned above tend to lower the characteristic impedance of the printed circuit traces and increases the mutual impedance between them which results in a considerable reduction in coupling between signals. These factors become increasingly important with fast memory operating times and low threshold voltages encountered when ECL is used as a logic element.

P.C. Board Grid Distribution

An alternative method for voltage and ground distribution on a memory printed circuit board is to grid or mesh the distribution lines. Although the grids may be irregular, they should approach 1 to 3 inch squares. Printed circuit grid distribution is constructed by connecting the horizontal voltage or ground traces on one side of the board to the vertical counter parts on the other side of the board. Grid or mesh construction reduces signal return distances and equalizes current distribution along the buses. Equalizing current flows reduces line voltage drops which reduces voltage and ground variations between devices.

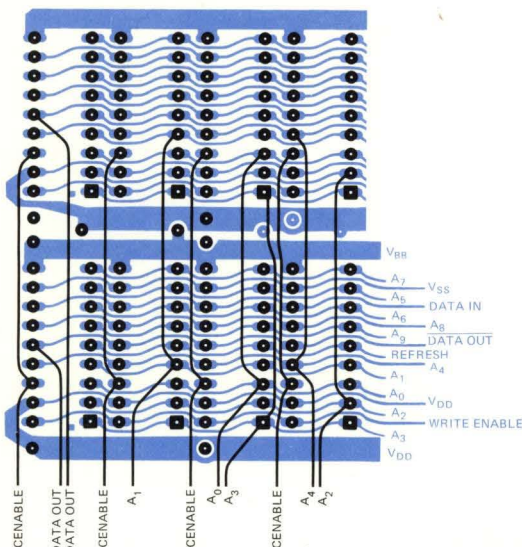


FIGURE 24—Printed circuit board array.

Decoupling Considerations

MOS Memories exhibit small standby currents and relatively large, but short duration transient currents. Decoupling capacitors are used to supply these relatively high transient currents when placed a short distance from the memory device. In effect, the decoupling capacitors average the current pulse over the interval of On Time to Off Time which essentially decreases the frequency of the current components presented to the main power distribution lines and supplies.

Figure 25 shows that two types of capacitors are normally used for decoupling each voltage. The first is usually a disc ceramic type and is located close to the memory device (C_1 and C_2). These capacitors must have sufficient capacity and high enough frequency response to supply the pulse edge currents to the devices without discharging more than an acceptable amount. The leading and trailing edge current spikes shown in Figures 20 and 21 contain many high frequency components which dictate the frequency response characteristics of the capacitor. The capacitance is determined by the voltage drop that can be tolerated at the device and the peak transient current. These high frequency response capacitors should be located adjacent to each memory device, or, if the array is designed with the devices close to each other, they may be located near every other device.

Typical theoretical values for V_{DD} decoupling, (C_1), for the 64 device array described previously indicate .04 μF per 2105, or approximately 32 .1 μF capacitors distributed between alternate devices. Because of the relatively high driver peak currents encountered, decoupling the V_{DD} connection on each driver is recommended.

In a similar manner, the theoretical values for V_{BB} decoupling (C_2) indicates .007 μF per 2105. A more practical value of 0.1 μF for every two to four 2105's is typically used.

The second type of capacitor is usually a tubular tantalum type and is used to integrate the cycle current requirements (C_3 & C_4 in Figure 25). This capacitor will recharge the capacitors mentioned above until the power supply can restore the lost charge. The fall time of the voltage due to the discharge of C_3 or C_4 represents the frequency response requirement of the power supply and distribution lines. The value is related to the difference between the cycle current and the standby current calculated previously, and the frequency response of the power supply.

Typical theoretical values for the 64 device array indicate a total of 100 μF for C_3 , which should be divided into two or three capacitors located near the outer or connector edge of the memory array.

In a similar manner, theoretical values for V_{BB} decoupling indicates $4 \mu F$ for C_4 . However if $.1 \mu F$ per alternate device is used for C_2 as previously

recommended, the total C_3 would equal $3.2 \mu F$, which would supplement or reduce the value of C_4 to less than $1 \mu F$.

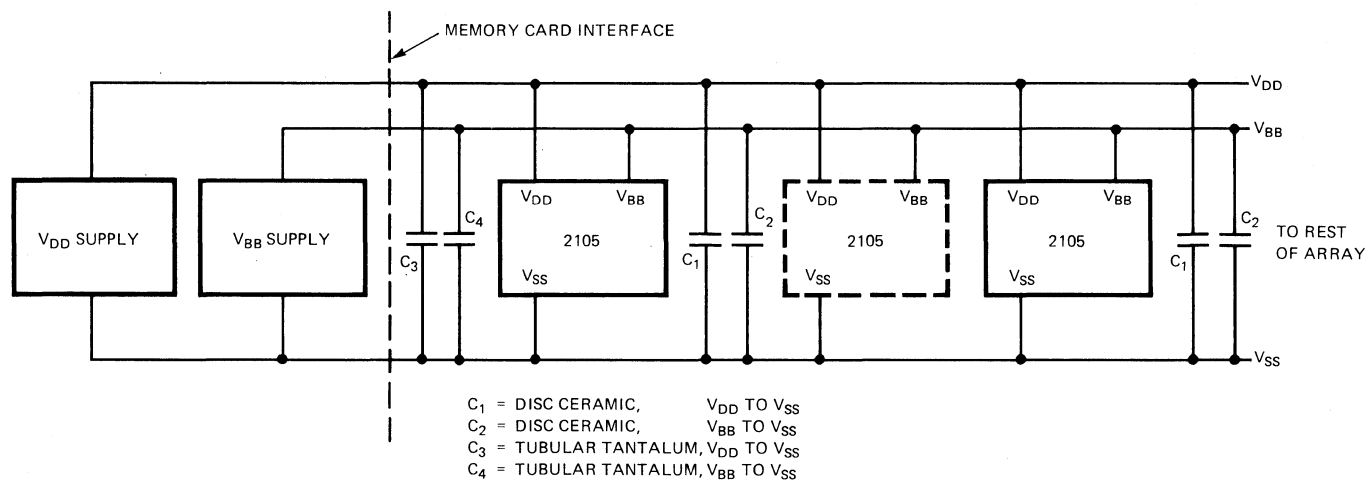


FIGURE 25—Typical decoupling configuration.

Bibliography

1. Charles A Harper, Handbook of Wiring, Cabling and Interconnecting for Electronics, McGraw-Hill, 1972.
2. William R. Blood, MECL System Design Handbook, Motorola, 1972.
3. The Intel Memory Design Handbook, Intel Corporation, August 1973.



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