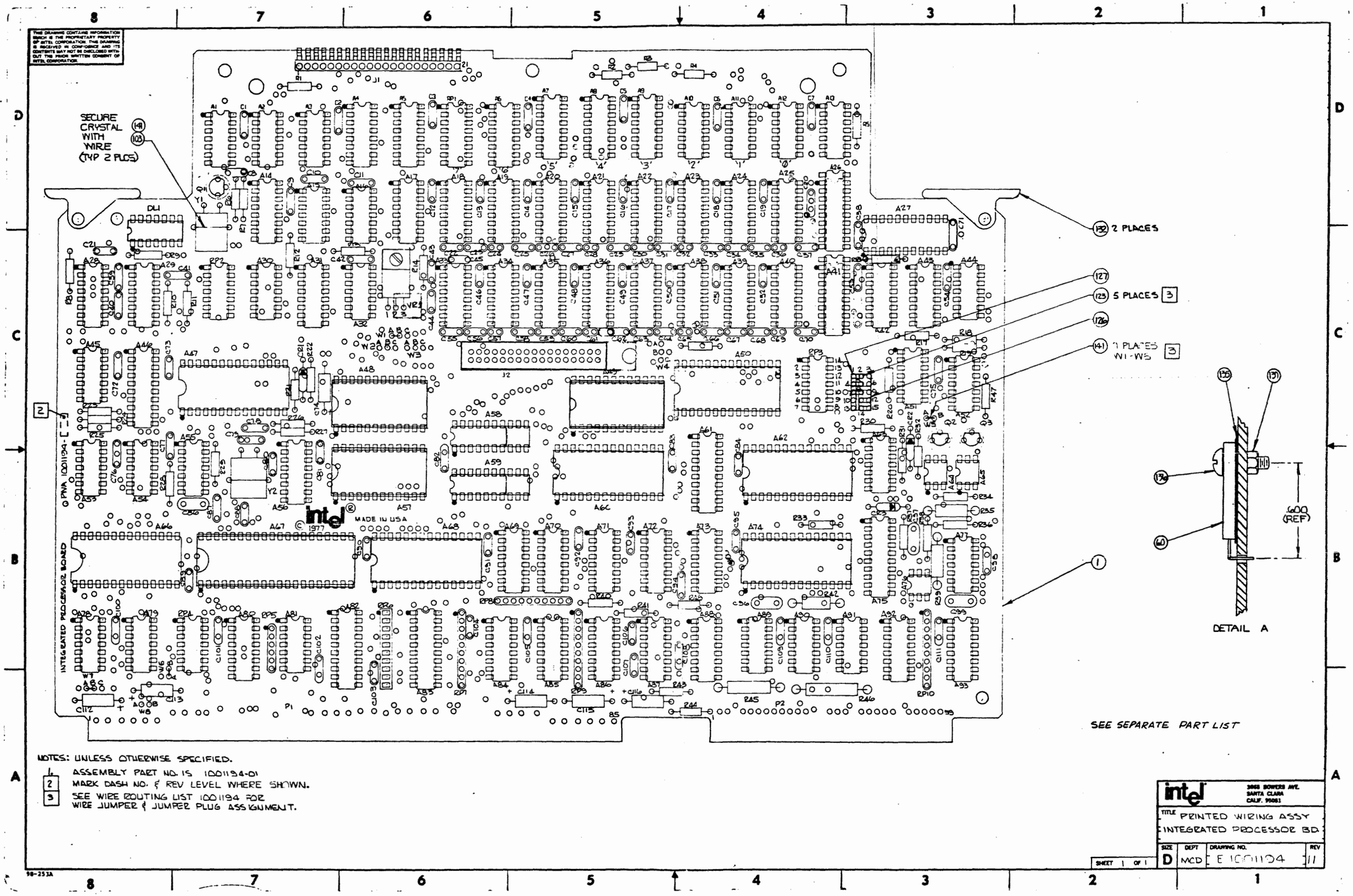
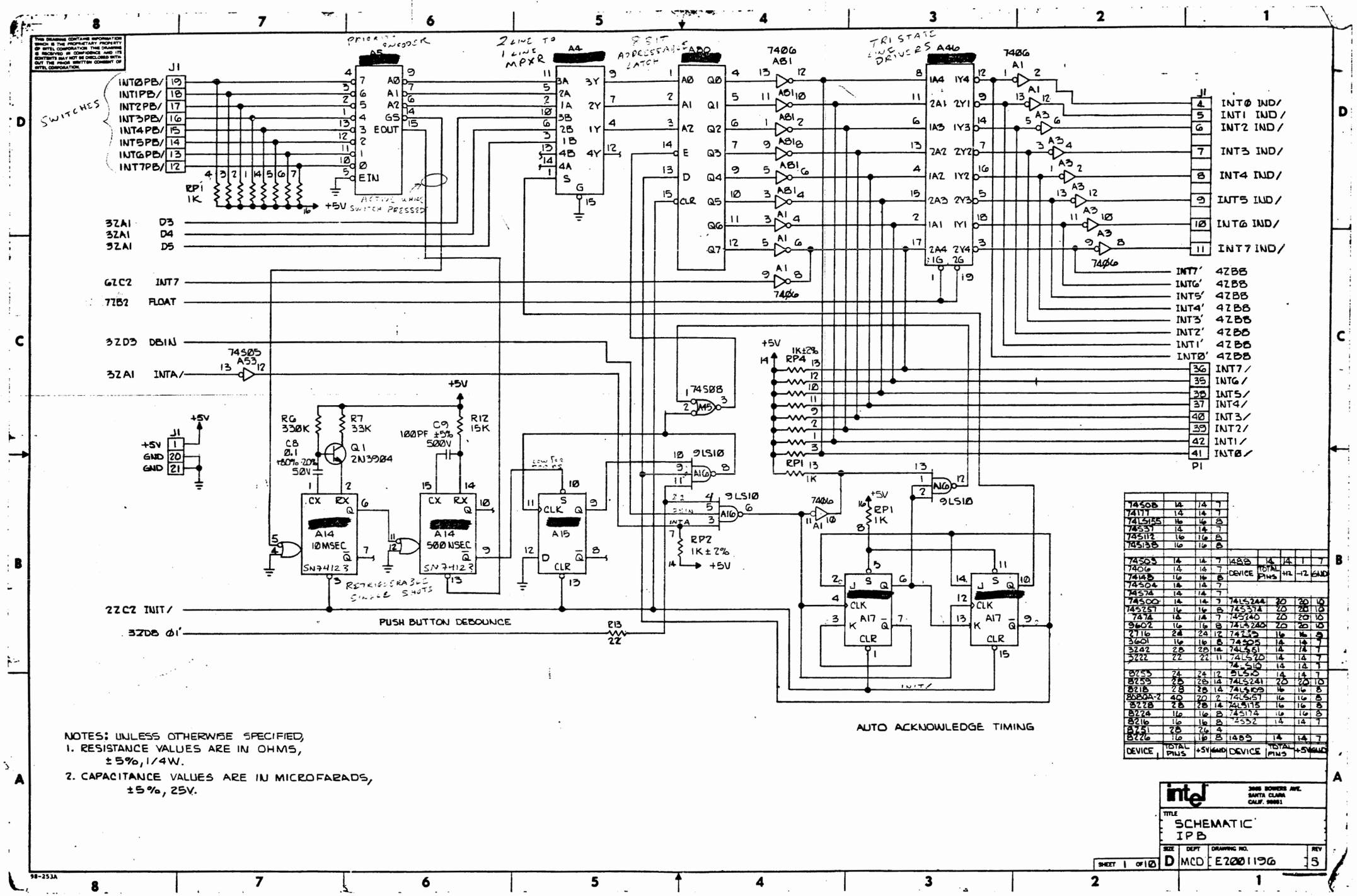


NOTES: UNLESS OTHERWISE SPECIFIED.

1. ASSEMBLY PART NO. IS 1001194-01
2. MARK DASH NO. & REV LEVEL WHERE SHOWN.
3. SEE WIRE ROUTING LIST 1001194 FOR WIRE JUMPER & JUMPER PLUG ASSIGNMENT.

intel	3065 BOWERS AVE. SANTA CLARA CALIF. 95051		
TITLE PRINTED WIRING ASSY INTEGRATED PROCESSOR BD			
SIZE D	DEPT MCD	DRAWING NO. E 1001194	REV 11
SHEET 1 OF 1			

98-253A



DEVICE	TOTAL PINS	+5V	GND
74S08	14	14	7
74177	14	14	7
74LS155	16	16	8
74S37	14	14	7
74S112	16	16	8
74S138	16	16	8
74S03	14	14	7
7406	14	14	7
74148	16	16	8
74S04	14	14	7
7474	14	14	7
74S00	14	14	7
74S257	16	16	8
7474	14	14	7
9602	16	16	8
2716	24	24	12
3601	16	16	8
3242	28	28	14
3222	22	22	11
8255	24	24	12
8255	28	28	14
8218	28	28	14
8080A-2	40	20	2
8228	28	28	14
8224	16	16	8
8216	16	16	8
8251	28	26	4
8226	16	16	8

DEVICE	TOTAL PINS	+5V	GND
1488	14	14	7
1489	14	14	7
74LS244	20	20	10
74S374	20	20	10
74S240	20	20	10
74LS240	20	20	10
74S50	16	16	8
74S05	14	14	7
74LS51	14	14	7
74LS20	14	14	7
74S40	14	14	7
8155	14	14	7
74LS241	20	20	10
74LS109	16	16	8
74LS157	16	16	8
74LS175	16	16	8
74S174	16	16	8
74S32	14	14	7
1485	14	14	7

NOTES: UNLESS OTHERWISE SPECIFIED,
1. RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W.
2. CAPACITANCE VALUES ARE IN MICROFARADS, ±5%, 25V.

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC IPB

SIZE	DEPT	DRAWING NO.	REV
D	MCD	E2001196	5

SHEET 1 OF 10

98-253A

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
-	SEE SHEET 1	—	—	—

BUS PRIORITY RESOLUTION

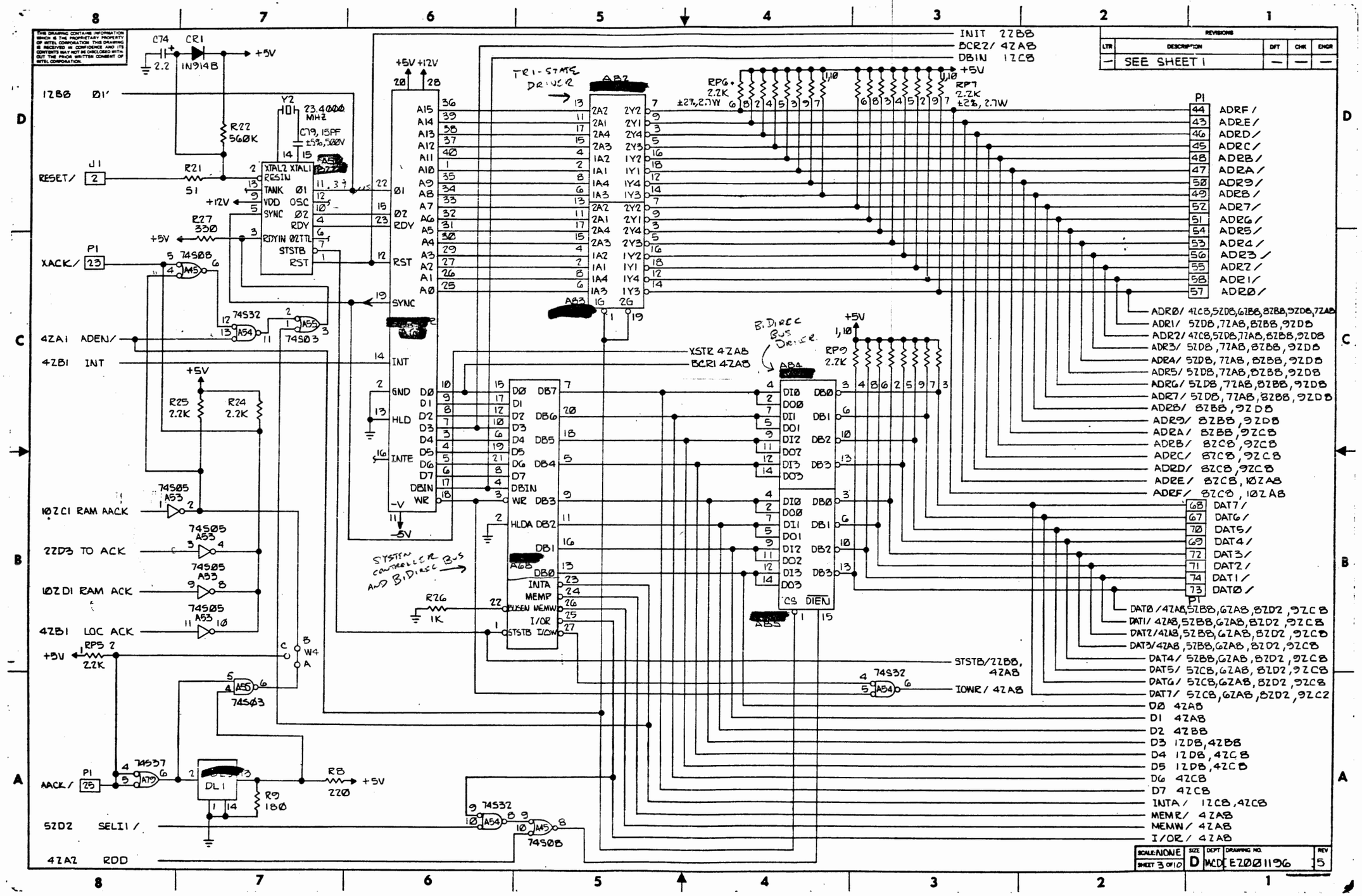
BUS TIME OUT
100µSEC

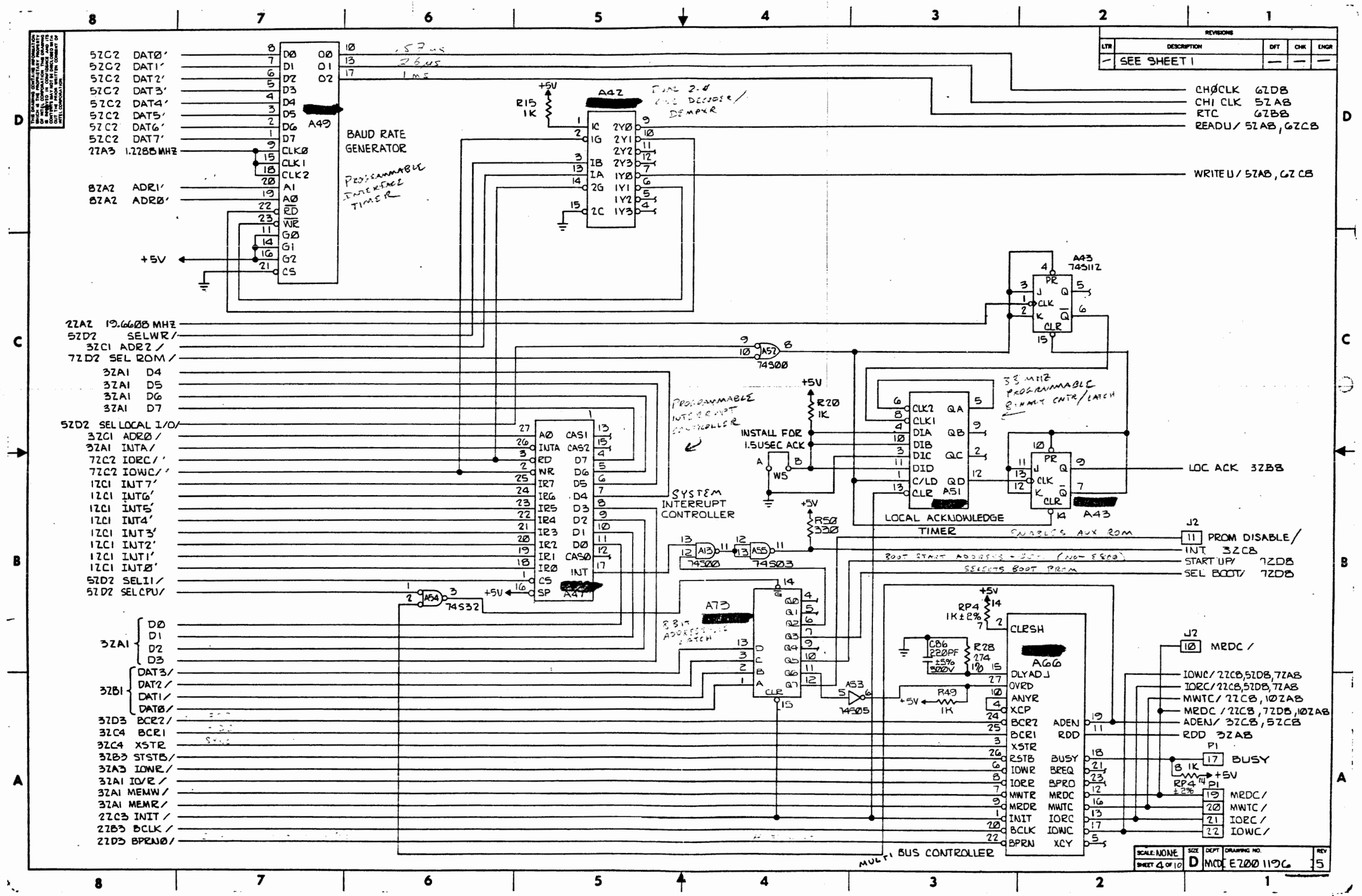
SYSTEM CLOCKS

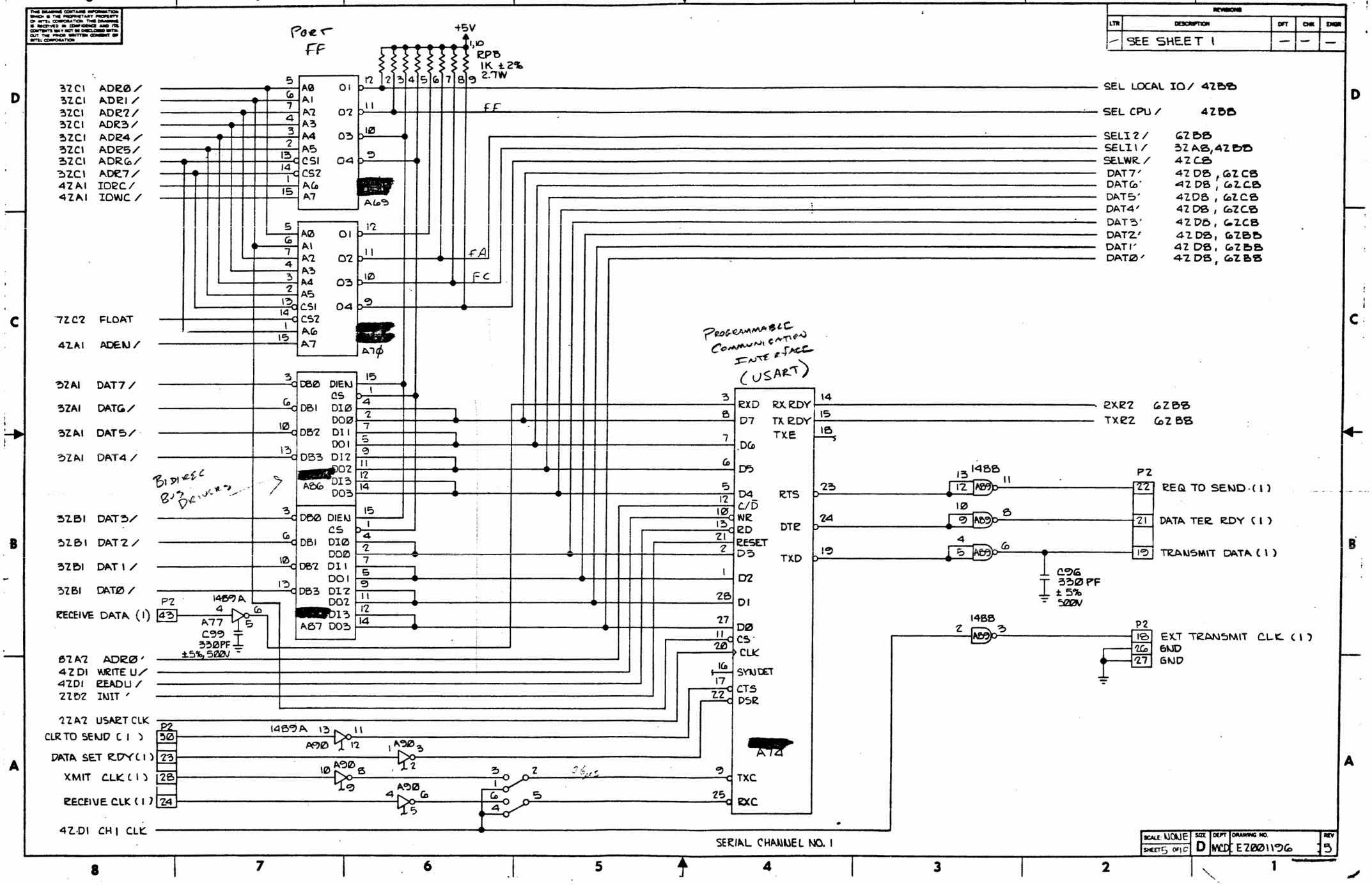
35MHZ PRESETTABLE BINARY COUNTER/LATCH

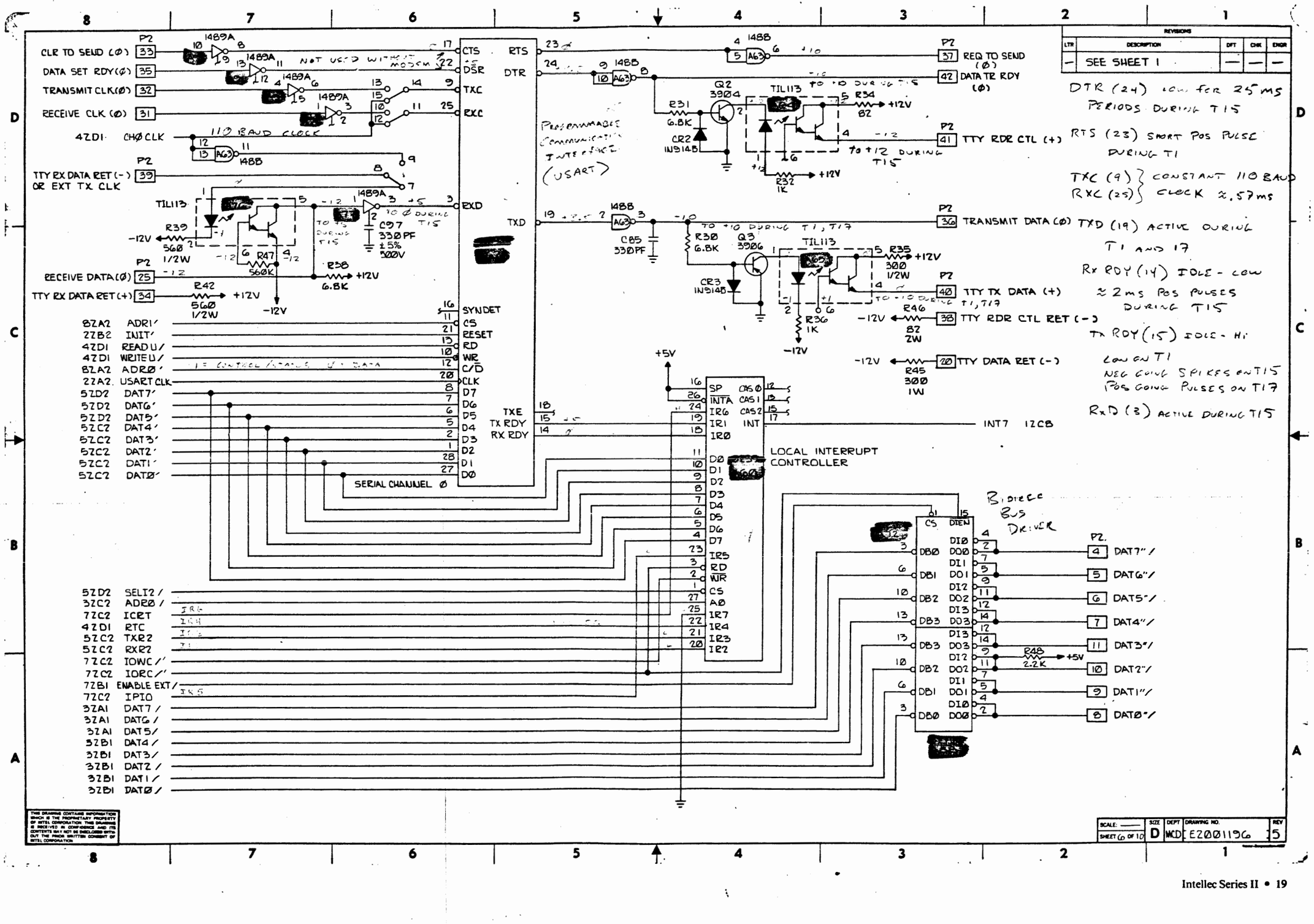
CLOCK GEN/DRIVER

Intellec Series II • 15


THIS DRAWING CONTAINS INFORMATION WHICH IS THE PROPRIETARY PROPERTY OF INTEL CORPORATION. THIS DRAWING IS RECEIVED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.
REVISIONS
LTR DESCRIPTION DFT CHK ENGR
— SEE SHEET 1
C74 2.2
CR1 IN914B
+5V
1ZB8 Ø1'
Y2 23.4000 MHz
C79, 15PF ±5%, 500V
R22 560K
J1
RESET/ 2
R21 51
XTAL2 XTAL1 RESIN TANK VDD SYNC OSC ØZ RDY RDYIN ØZTTL STSTB RST
+12V
R27 330
P1
XACK/ 23
74S08 A45
74S32 A54 A55
74S03
4ZA1 ADEN/
4ZB1 INT
R25 2.2K
R24 2.2K
74S05 A53
1ØZC1 RAM AACK
2ZD3 TO ACK
1ØZD1 RAM ACK
4ZB1 LOC ACK
RP5 2 2.2K
W4
74S37 A49
AACK/ 25
DL1
R8 220
R9 180
+5V
5ZD2 SELI1/
4ZA2 RDD
SYSTEM CONTROLLER AND BIDIREC BUS
R26 1K
TRI-STATE DRIVER
A62
A63
A64
A65
A66
A67
A68
B. DIREC BUS DRIVER
RP6 2.2K ±2%, 2.7W
RP7 2.2K ±2%, 2.7W
RP9 2.2K
INIT 2ZB8
BCR2/ 4ZA8
DBIN 1ZC8
XSTR 4ZA8
BCR1 4ZA8
STSTB/2ZB8, 4ZA8
IOWR/ 4ZA8
P1
ADRØ/ 41C8,5ZD8,6ZB8,8ZB8,9ZD8,7ZA8
ADR1/ 5ZD8,7ZA8,8ZB8,9ZD8
ADR2/ 41C8,5ZD8,7ZA8,8ZB8,9ZD8
ADR3/ 5ZD8,7ZA8,8ZB8,9ZD8
ADR4/ 5ZD8,7ZA8,8ZB8,9ZD8
ADR5/ 5ZD8,7ZA8,8ZB8,9ZD8
ADR6/ 5ZD8,7ZA8,8ZB8,9ZD8
ADR7/ 5ZD8,7ZA8,8ZB8,9ZD8
ADR8/ 8ZB8,9ZD8
ADR9/ 8ZB8,9ZD8
ADRA/ 8ZB8,9ZC8
ADRB/ 8ZC8,9ZC8
ADRC/ 8ZC8,9ZC8
ADRD/ 8ZC8,9ZC8
ADRE/ 8ZC8,1ØZA8
ADRF/ 8ZC8,1ØZA8
DAT7/
DAT6/
DAT5/
DAT4/
DAT3/
DAT2/
DAT1/
DAT0/
DAT0/47A8,5ZB8,6ZA8,8ZD2,9ZC8
DAT1/ 4ZA8,5ZB8,6ZA8,8ZD2,9ZC8
DAT2/4ZA8,5ZB8,6ZA8,8ZD2,9ZC8
DAT3/4ZA8,5ZB8,6ZA8,8ZD2,9ZC8
DAT4/ 5ZB8,6ZA8,8ZD2,9ZC8
DAT5/ 5ZC8,6ZA8,8ZD2,9ZC8
DAT6/ 5ZC8,6ZA8,8ZD2,9ZC8
DAT7/ 5ZC8,6ZA8,8ZD2,9ZC2
DØ 4ZA8
D1 4ZA8
D2 4ZB8
D3 1ZD8,4ZB8
D4 1ZD8,4ZC8
D5 1ZD8,4ZC8
D6 4ZC8
D7 4ZC8
INTA/ 1ZC8,4ZC8
MEMR/ 4ZA8
MEMW/ 4ZA8
I/OR/ 4ZA8
SCALE:NONE SIZE D DEPT MCD DRAWING NO. EZØØ11796 REV 5
SHEET 3 OF 10


REVISIONS
LTR DESCRIPTION DFT CHK ENGR
— SEE SHEET 1
5ZC2 DAT0'
5ZC2 DAT1'
5ZC2 DAT2'
5ZC2 DAT3'
5ZC2 DAT4'
5ZC2 DAT5'
5ZC2 DAT6'
5ZC2 DAT7'
7ZA3 1.2288 MHZ
8ZA2 ADR1'
8ZA2 ADR0'
+5V
A49
BAUD RATE GENERATOR
PROGRAMMABLE INTERVAL TIMER
D0 D1 D2 D3 D4 D5 D6 D7
CLK0 CLK1 CLK2
A1 A0 RD WR G0 G1 G2 CS
.52 uS
2.6 uS
1 mS
R15 1K
A42
DUAL 2-4 LINE DECODER/ DEMUXR
1G 1C 2G 2C 1A 1B 2Y0 2Y1 2Y2 2Y3 1Y0 1Y1 1Y2 1Y3
CH0CLK 6ZD8
CH1 CLK 5ZA8
RTC 6ZB8
READU/ 5ZA8, 6ZC8
WRITEU/ 5ZA8, 6ZC8
2ZA2 19.6608 MHZ
5ZD2 SELWR/
3ZC1 ADR2/
7ZD2 SEL ROM/
3ZA1 D4
3ZA1 D5
3ZA1 D6
3ZA1 D7
5ZD2 SEL LOCAL I/O/
3ZC1 ADR0/
3ZA1 INTA/
7ZC2 IORC/
7ZC2 IOWC/
1ZC1 INT7'
1ZC1 INT6'
1ZC1 INT5'
1ZC1 INT4'
1ZC1 INT3'
1ZC1 INT2'
1ZC1 INT1'
1ZC1 INT0'
5ZD2 SEL11/
5ZD2 SELCPU/
A47
AD CAS1 INTA CAS2 RD D7 WR D6 IR7 D5 IR6 D4 IR5 D3 IR4 D2 IR3 D1 IR2 D0 IR1 CAS0 IR0 INT CS SP
PROGRAMMABLE INTERRUPT CONTROLLER
SYSTEM INTERRUPT CONTROLLER
A54 74S32
A13 74S00
A55 74S03
A57 74S00
A73
8 BIT ADDRESSABLE LATCH
D0 D1 D2 D3
DAT3/ DAT2/ DAT1/ DAT0/
3ZB1
3ZA1
3ZD3 BCR2/
3ZC4 BCR1
3ZC4 XSTR
3ZB3 STSTB/
3ZA3 IOWR/
3ZA1 IO/R/
3ZA1 MEMW/
3ZA1 MEMR/
2ZC3 INIT/
2ZB3 BCLK/
2ZD3 BPRN0/
A43 74S112
PR J CLK K Q CLR
R20 1K
INSTALL FOR 1.5USEC ACK
WS
+5V
R50 330
LOCAL ACKNOWLEDGE TIMER
33 MHZ PROGRAMMABLE BINARY CNTR/LATCH
CLK2 CLK1 DIA DIB DIC DID C/LD CLR QA QB QC QD A51
LOC ACK 3ZB8
A43
ENABLES AUX ROM
BOOT START ADDRESS = FC00 (NOT E800)
SELECTS BOOT PROM
J2 11 PROM DISABLE/
INT 3ZC8
START UP/ 7ZD8
SEL BOOT/ 7ZD8
RP4 1K±2%
CLRSH
A66
CB6 220PF ±5% 500V
R28 274 1%
R49 1K
DLYADJ OVRD ANYR XCP BCR2 BCR1 XSTR RSTB IOWR IORR MWTR MRDR INIT BCLK BPRN ADEN RDD BUSY BREQ BPRO MRDC MWTC IORC IOWC XCY
J2 10 MRDC/
IOWC/ 2ZC8,5ZD8,7ZA8
IORC/ 2ZC8,5ZD8,7ZA8
MWTC/ 2ZC8, 10ZA8
MRDC / 2ZC8, 7ZD8, 10ZA8
ADEN/ 3ZC8, 5ZC8
RDD 3ZA8
P1 17 BUSY
8 1K
RP4 ±2%
P1 19 MRDC/
20 MWTC/
21 IORC/
22 IOWC/
MULTI BUS CONTROLLER
SCALE: NONE SIZE D DEPT MCD DRAWING NO. E7001196 REV 5
SHEET 4 OF 10


Port FF
+5V
RPB 1K ±2% 2.7W
SEL LOCAL IO/ 42BB
SEL CPU/ 42BB
SELI2/ 62BB
SELI1/ 32A8, 42BB
SELWR/ 42C8
DAT7' 42D8, 62C8
DAT6' 42D8, 62C8
DAT5' 42D8, 62C8
DAT4' 42D8, 62C8
DAT3' 42D8, 62C8
DAT2' 42D8, 62B8
DAT1' 42D8, 62B8
DAT0' 42D8, 62B8
FF
FA
FC
A69
A70
A74
PROGRAMMABLE COMMUNICATION INTERFACE (USART)
BIDIREC BUS DRIVERS
RXR2 62BB
TXR2 62BB
REQ TO SEND (1)
DATA TER RDY (1)
TRANSMIT DATA (1)
EXT TRANSMIT CLK (1)
GND
GND
C96 330 PF ±5% 500V
C99 330PF ±5%, 500V
SERIAL CHANNEL NO. 1
SCALE: NONE
SHEET 5 OF 10
SIZE D
DEPT WCD
DRAWING NO. E2001196
REV 5


REVISIONS
LTR DESCRIPTION DFT CHK ENGR
— SEE SHEET 1
P2
CLR TO SEND (Ø) 33
DATA SET RDY (Ø) 35
TRANSMIT CLK (Ø) 32
RECEIVE CLK (Ø) 31
TTY RX DATA RET (-) OR EXT TX CLK 39
RECEIVE DATA (Ø) 25
TTY RX DATA RET (+) 34
1489A
NOT USED WITH MODEM
4ZD1 CHØ CLK
110 BAUD CLOCK
1488
TIL113
R39 560Ω 1/2W
R47 560K
R38 6.8K
R42 560Ω 1/2W
+12V
-12V
C97 330PF ±5% 500V
TO Ø DURING T15
CTS
DSR
TXC
RXC
RTS
DTR
TXD
RXD
SYNDET
CS
RESET
RD
WR
C/D
CLK
D7
D6
D5
D4
D3
D2
D1
D0
TXE
TX RDY
RX RDY
SERIAL CHANNEL Ø
8ZA2 ADR1'
2ZB2 INIT'
4ZD1 READU/
4ZD1 WRITEU/
8ZA2 ADRØ'
2ZA2 USART CLK
5ZD2 DAT7'
5ZD2 DAT6'
5ZD2 DAT5'
5ZC2 DAT4'
5ZC2 DAT3'
5ZC2 DAT2'
5ZC2 DAT1'
5ZC2 DATØ'
5ZD2 SELI2/
3ZC2 ADRØ/
7ZC2 ICRT
4ZD1 RTC
5ZC2 TXR2
5ZC2 RXR2
7ZC2 IOWC/'
7ZC2 IORC/'
7ZB1 ENABLE EXT/
7ZC2 IPIO
3ZA1 DAT7/
3ZA1 DAT6/
3ZA1 DAT5/
3ZB1 DAT4/
3ZB1 DAT3/
3ZB1 DAT2/
3ZB1 DAT1/
3ZB1 DATØ/
IR6
IR4
IR5
PROGRAMMABLE COMMUNICATION INTERFACE (USART)
REQ TO SEND (Ø) 37
DATA TR RDY (Ø) 42
TTY RDR CTL (+) 41
TRANSMIT DATA (Ø) 36
TTY TX DATA (+) 40
TTY RDR CTL RET (-) 38
TTY DATA RET (-) 20
Q2 3904
Q3 3906
R34 8Ω 2W
R35 300Ω 1/2W
R46 8Ω 2W
R45 300Ω 1W
R30 6.8K
R31 6.8K
R32 1K
R36 1K
C85 330PF
CR2 IN5148
CR3 IN5148
+5V
SP
INTA
IR6
IR1
IRØ
CAS Ø
CAS 1
CAS 2
INT
INT7 12CB
LOCAL INTERRUPT CONTROLLER
CS
A0
RD
WR
IR7
IR4
IR3
IR2
D7
D6
D5
D4
D3
D2
D1
D0
BIDIREC BUS DRIVER
DIEN
DB0
DB1
DB2
DB3
DI0
DO0
DI1
DO1
DI2
DO2
DI3
DO3
R48 2.2K
PZ.
4 DAT7"/
5 DAT6"/
6 DAT5"/
7 DAT4"/
11 DAT3"/
10 DAT2"/
9 DAT1"/
8 DATØ"/
DTR (24) LOW FOR 25MS PERIODS DURING T15
RTS (23) SHORT POS PULSE DURING T1
TXC (9) } CONSTANT 110 BAUD
RXC (25) } CLOCK ≈.57MS
TXD (19) ACTIVE DURING T1 AND 17
RX RDY (14) IDLE - LOW
≈2MS POS PULSES DURING T15
TX RDY (15) IDLE - HI
LOW ON T1
NEG GOING SPIKES ON T15
POS GOING PULSES ON T17
RXD (8) ACTIVE DURING T15
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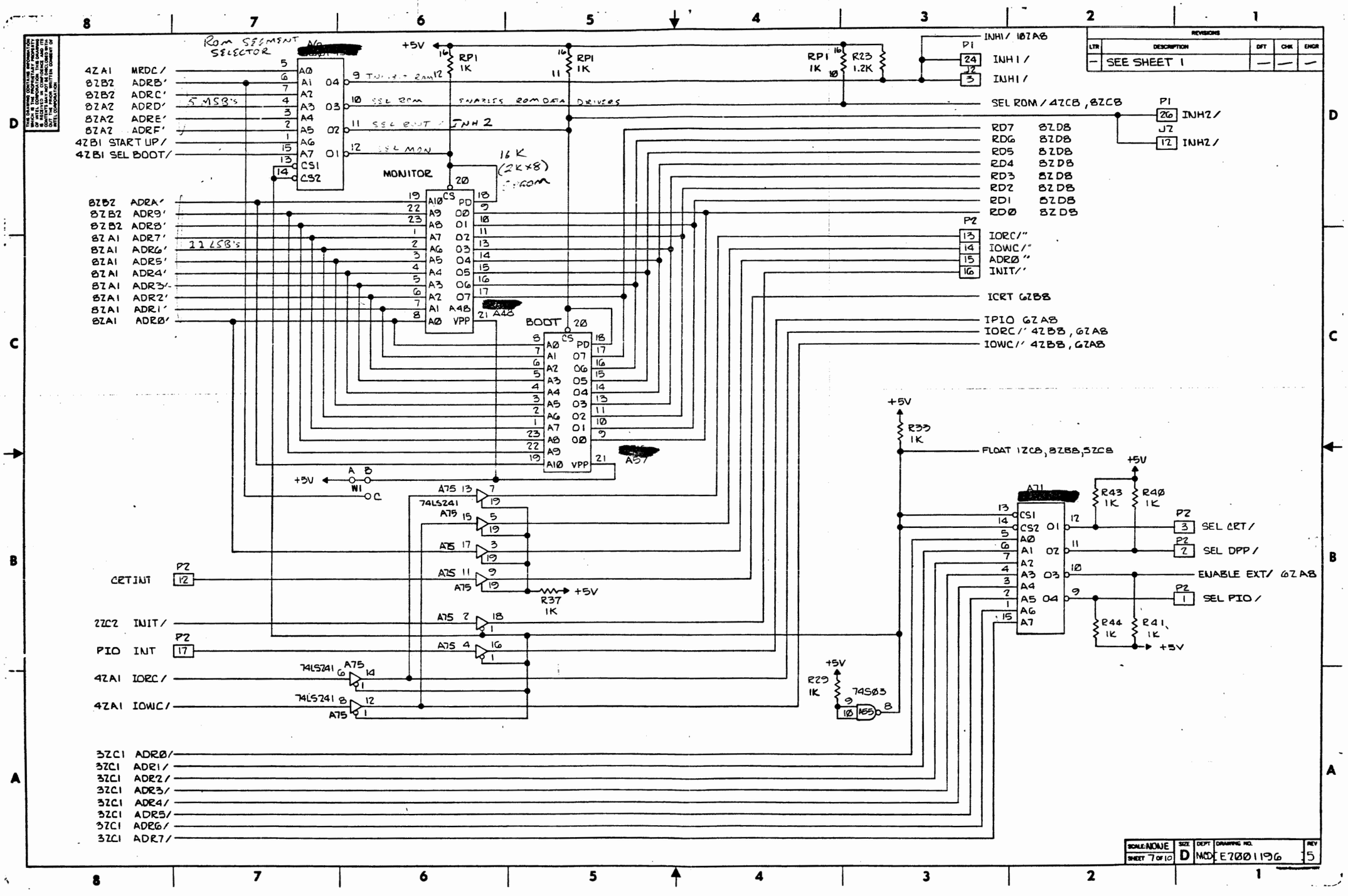
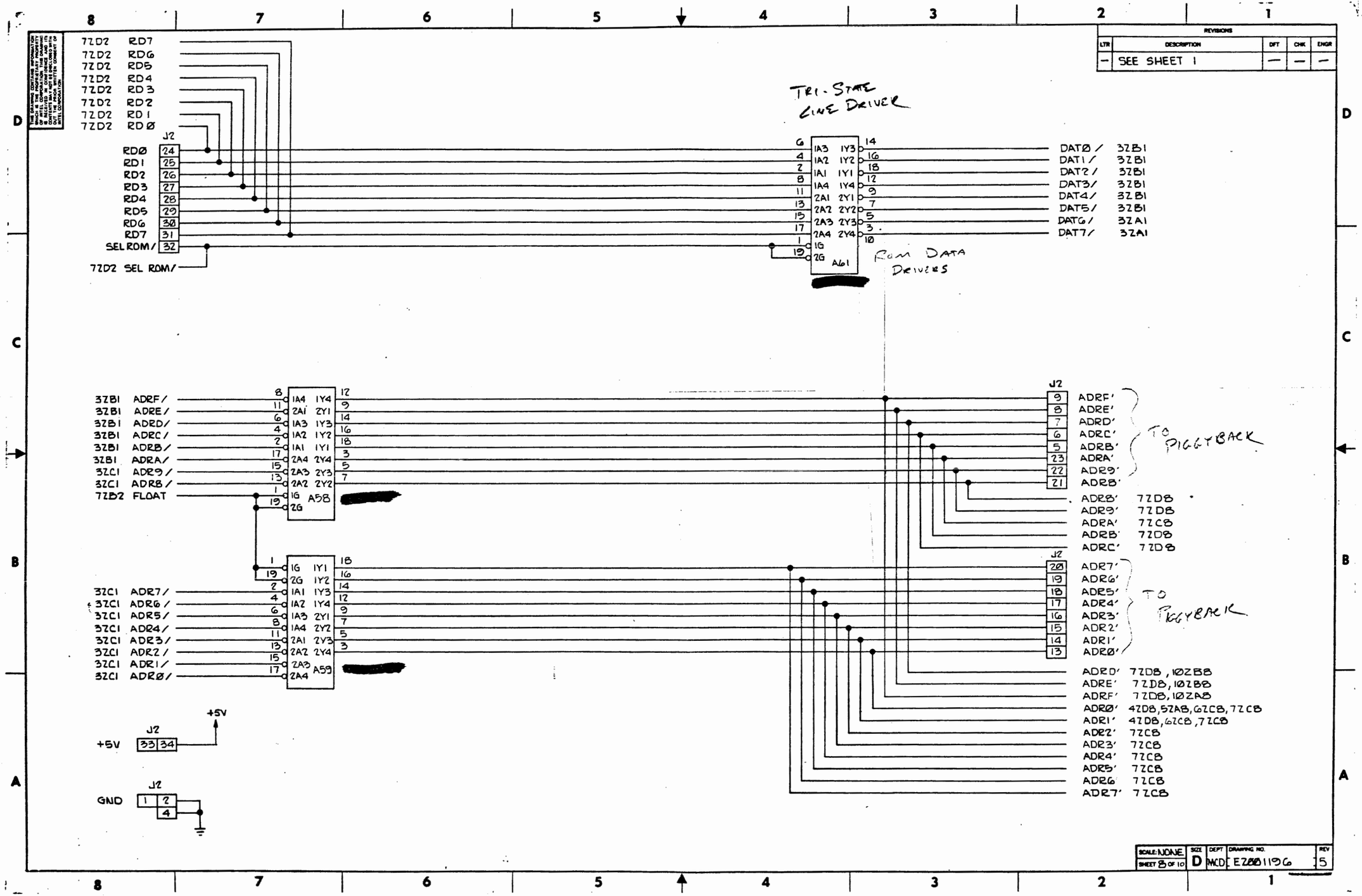
SCALE: —
SHEET 6 OF 10
SIZE D
DEPT WCD
DRAWING NO. E2001196
REV 5


ROM SEGMENT NO SELECTOR
5 MSB's
11 LSB's
MONITOR
16K (2K×8) EPROM
BOOT
MRDC/
ADRB'
ADRC'
ADRD'
ADRE'
ADRF'
START UP/
SEL BOOT/
ADRA'
ADR9'
ADR8'
ADR7'
ADR6'
ADR5'
ADR4'
ADR3'
ADR2'
ADR1'
ADR0'
+5V
RP1 1K
R23 1.2K
R37 1K
R29 1K
R33 1K
R43 1K
R40 1K
R44 1K
R41 1K
INH1/ 10ZA8
INH1/
SEL ROM/ 47C8, 8ZC8
INH2/
RD7 8ZD8
RD6 8ZD8
RD5 8ZD8
RD4 8ZD8
RD3 8ZD8
RD2 8ZD8
RD1 8ZD8
RD0 8ZD8
IORC/"
IOWC/"
ADR0"
INIT/'
ICRT GZB8
IPIO GZA8
IORC/' 47B8, GZA8
IOWC/' 47B8, GZA8
FLOAT 1ZC8, 8ZB8, 5ZC8
SEL CRT/
SEL DPP/
ENABLE EXT/ GZA8
SEL PIO/
GETINT
2ZC2 INIT/
PIO INT
47A1 IORC/
47A1 IOWC/
74LS241
74S03
3ZC1 ADR0/
3ZC1 ADR1/
3ZC1 ADR2/
3ZC1 ADR3/
3ZC1 ADR4/
3ZC1 ADR5/
3ZC1 ADR6/
3ZC1 ADR7/
REVISIONS
LTR DESCRIPTION DFT CHK ENGR
— SEE SHEET 1
SCALE: NONE
SHEET 7 OF 10
SIZE D
DEPT MCD
DRAWING NO. E7001196
REV 15


REVISIONS
LTR DESCRIPTION DFT CHK ENGR
— SEE SHEET 1 — — —
TRI-STATE LINE DRIVER
RAM DATA DRIVERS
TO PIGGYBACK
TO PIGGYBACK
SCALE: NONE
SHEET 8 OF 10
SIZE D
DEPT MCD
DRAWING NO. E2801196
REV 5

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
–	SEE SHEET 1	–	–	–

ADDRESS MAPPER/REFRESH COUNTER

16K x 1 DYNAMIC RAM

10ZA1 REFON
10ZA1 ROW
3ZC1 ADR0/
ADR1/
ADR2
ADR3
ADR4/
ADR5/
ADR6/
ADR7/
ADR8/
ADR9/
ADRA/
3ZC1 ADRB/
3ZB1 ADRC/
3ZB1 ADRD/
10ZB1 RAS1/
10ZB1 RAS2/
10ZC1 CAS/
10ZA1 W/

CNT, REFRE, ROWE, A0–A13, ZERO DET., A5Ø, N.C., RP3 47, RP5 2.2K, W4, R16 1K

A0–A8, WE, CAS, RAS, DO7 DI7 … DO0 DI0, A18, A19, A20, A21, A22, A23, A24, A25, A33–A39, A40, VDD, VCC, VSS, VBB, +12V, +5V, -5V, -10V

W8, P1, YZ1, R14 82Ω, C43 1.0 +80%-20% 50V, C44 1.0

A41 2Y4 … 1Y1, DAT0/ … DAT7/, MEMW/, 3ZB1, 10ZA1

A26 1D … 8D, CONTROL, CLK, EDGE-TRIGGERED LATCH

DATA STROBE 10ZC1
MEMR/ 10ZA1

C17–C19, C46–C52, 78, 88 .1 +80%-20% 50V

P1
-12V 79 80
-10V 77 78
+5V 3 4, 5 6, 81 82, 83 84
GND 1 2, 11 12, 75 76, 85 86
+12V 7 8

C20, 23, 25, 27, 29, 31, 33, C35, 37, 47, 56, 58, 60, 62, C64, 66, 68, 78, 80–84, 89–95, C98, 100–111. .1 +80% -20% 50V
C1–7, 10, 11, 38, 39, C53, 54, 72, 73, 75–77 .01
C112, C116 22 +10%, 15V
C114 22 +10%, 15V
C115 22 +10%, 15V
C22, 26, 30, 34, 45, C55, 59, 63, 67 1.0 +80% -20% 50V
C24, 28, 32, 36, C57, 61, 65, 69 .01 +80% -20% 50V
C113 22 +10% 15V
C45, 87 .1 +80% -20% 50V

SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 9 OF 10	D	MCD	E2001196	5

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
—	SEE SHEET 1	—	—	—

2ZA2 19.6608 MHZ

RAM ACK 3ZBB

DATA STROBE 9ZB1

CAS/ 9ZBB

RAM AACK 3ZBB

RAS1/ 9ZC8

RAS2/ 9ZB8

REFON/ 9ZD8

MEMW/ 9ZC1

MEMR/ 9ZB2

ROW 9ZD8

W/ 9ZBB

REFRESH CONTROLLER

2 LINE TO 1 LINE DATA SELECTOR MPXR

8ZA2 ADRD'

8ZA2 ADRE'

3ZB1 ADRE/

3ZB1 ADRF/

8ZA2 ADRF'

4ZA1 MRDC/

7ZD2 INH1/

4ZA1 MWTC/

R17 4.75K 1/4W ±1% 15PPM

C71 .0047 50V

RP2 1K

R1 33

R2 1.2K

R3 1.2K

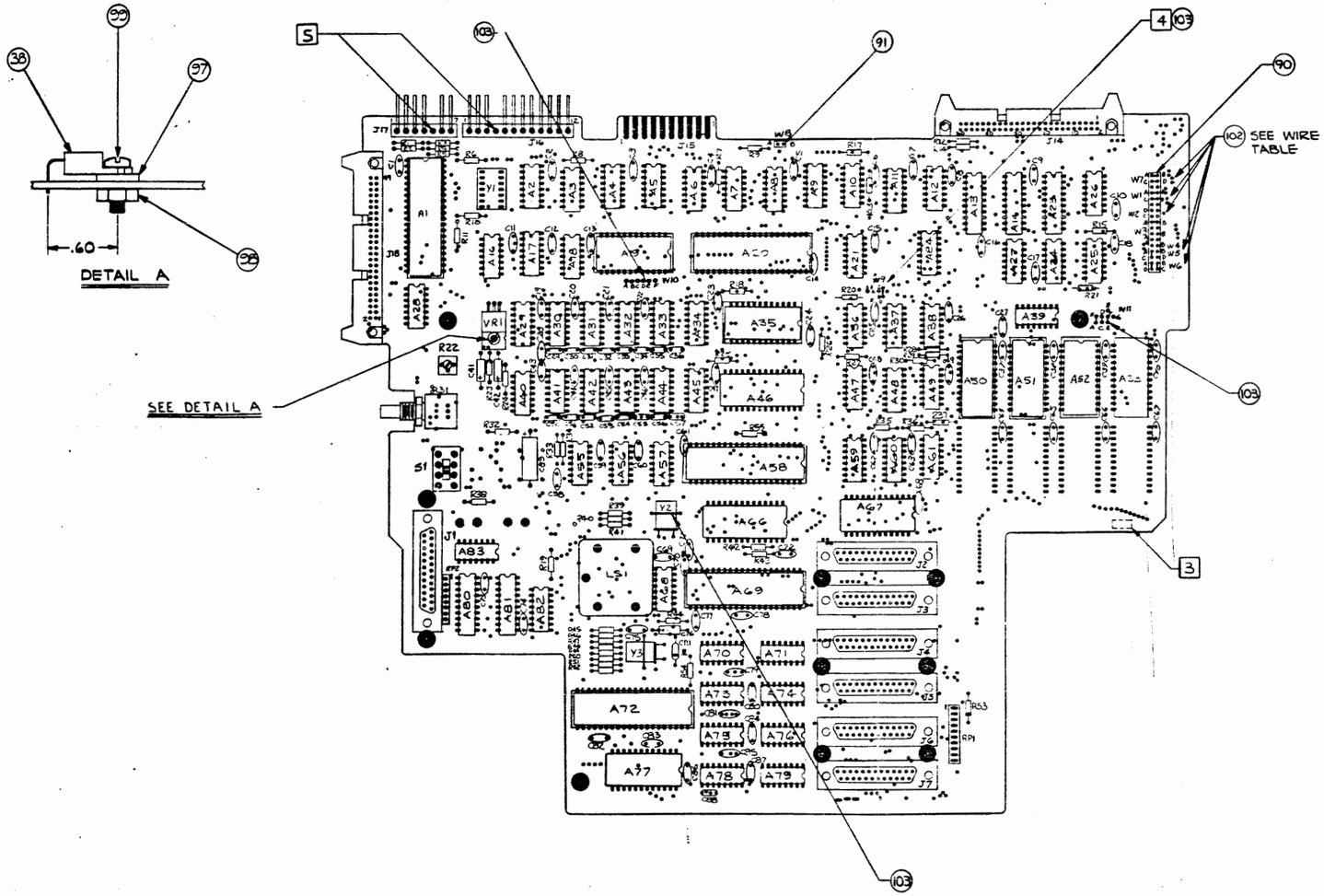
R4 1.2K

R5 1K

74S00 74S04 74LS51 74LS10

RAM TIMING AND REFRESH CONTROL

SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 10 OF 10	D	MCD	E2001196	15



5 CONNECTOR PINS, J17-5 AND J16-4, ARE TO BE CUT OFF FOR KEYING.

4 JUMPER W9--2108 DEVICE TYPE A6H (S1627) CAN BE SUBSTITUTED FOR P/L ITEM NO. 16 IF JUMPER W38-W3E IS DELETED, AND W3B W3A IS ADDED.

3 MARK DASH NO. AND REV LEVEL WITH CONTRASTING PERM COLOR, .12 HIGH, WHERE SHOWN.

2. WORKMANSHIP PER MCD QAW 007.

1. ASSY PART NO. IS 1001241-04.

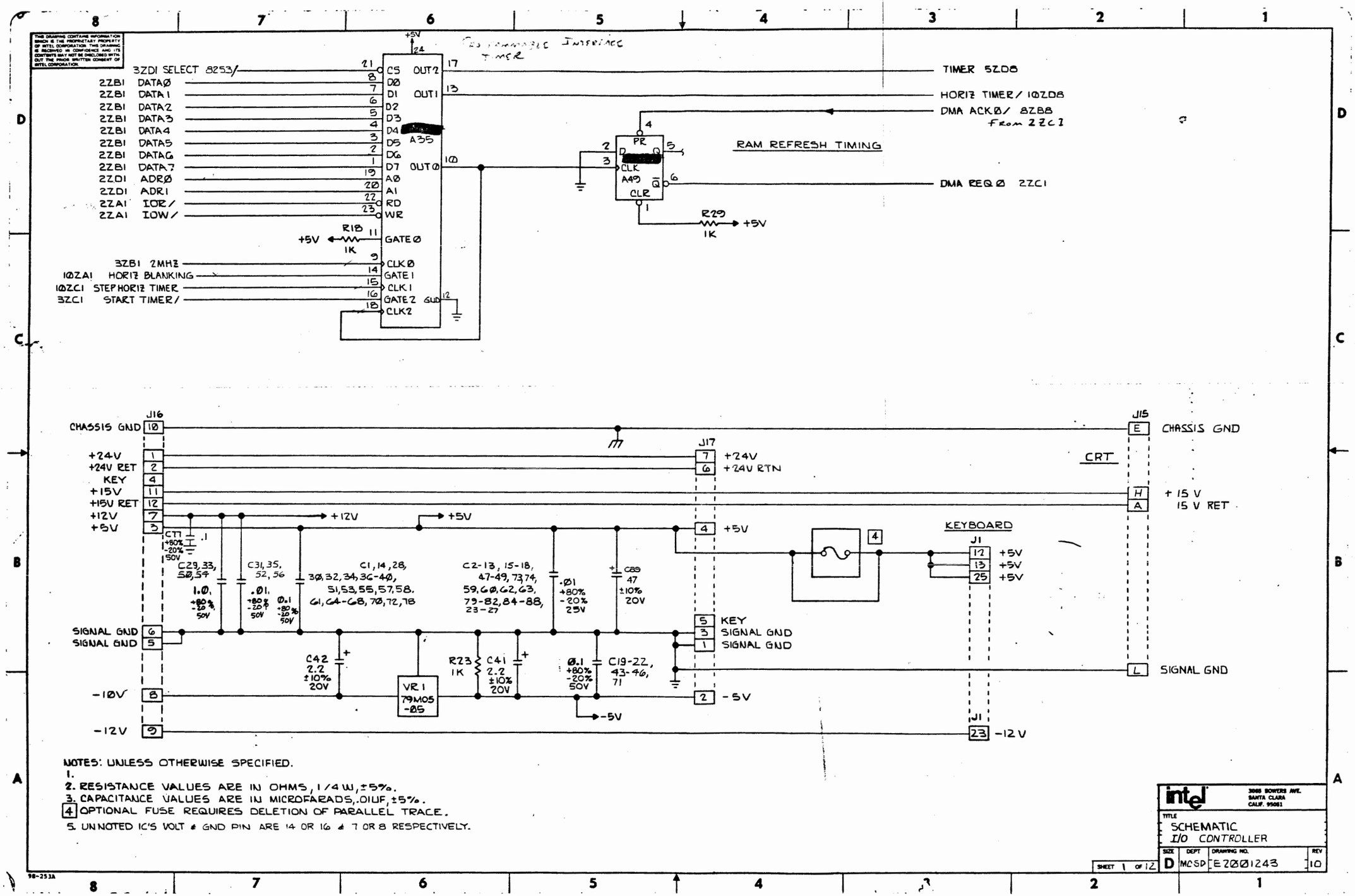
NOTE: UNLESS OTHERWISE SPECIFIED,

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: PRINTED WIRING ASSEMBLY I/O CONTROLLER

SIZE	DEPT	DRAWING NO	REV
D	MCSD	E 1001241	18

SHEET 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED.
1.
2. RESISTANCE VALUES ARE IN OHMS, 1/4 W, ±5%.
3. CAPACITANCE VALUES ARE IN MICROFARADS, .01UF, ±5%.
4. OPTIONAL FUSE REQUIRES DELETION OF PARALLEL TRACE.
5. UNNOTED IC'S VOLT & GND PIN ARE 14 OR 16 & 7 OR 8 RESPECTIVELY.

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC I/O CONTROLLER

SIZE	DEPT	DRAWING NO.	REV
D	MCSD	E2001243	10

SHEET 1 OF 12

98-253A

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
—	SEE SHEET 1	—	—	—

μP AND DMA

Programmable DMA controller

Clock gen/driver for 8080

88:F I/O Port

DMA used only for: Ram Refresh, Ram → CRT, Ram → Disk

System Controller/Bus Driver

22.032 MHz 8ZD8, 3ZA8

RESET 3ZB8

+5V, +12V, -5V

R34 1K, R33 1K, R40 1K, R39 1K, R59 470, R44 560K, R36 330, R35 470, R43 1K, R42 1K

CR1 1N9148

C69 ±10% 20PF 500V, Y2 22.032 MHz, C76 2.2μF ±10% 20V

2.79 MHz

MASTER RESET/ J14-29

5ZD1 DMA ENABLE

10ZA1 END OF RASTER INTR

A58, A69, A66, A67

8ZA8, 11ZD8, 12ZD8, ADR1 1ZD8, 3ZB8, 5ZB8

ADR0 1ZD8, 3ZB8, 4ZD8, 8ZA8, 10ZA8, 11ZD8, 12ZD8

ADR2 8ZA8, 11ZD8, 12ZD8

ADR3 8ZA8, 11ZD8, 12ZD8

ADR4, ADR5, ADR6 } 3ZD8, 8ZA8, 11ZD8, 12ZD8

ADR7

SELECT 8757/ 3ZD1

DMA REQ 0 1ZD2 RAM

DMA REQ1 3ZC1 DISK

DMA REQ2 10ZA1 CRT

DMA ACK 0/ 8ZB8, 1ZD3

DMA ACK 1/ 3ZB8

DMA ACK 2/ 10ZA8

DMA ON 3ZD8

DMA ON' 3ZD8

DATA7, DATA6 } 1ZD8, 3ZC8, 4ZA8, 5ZB8, 9ZB8, 10ZB8

DATA5, DATA4 } 1ZD8, 3ZC8, 4ZA8, 5ZD8, 9ZB8, 10ZB8

DATA3, DATA2, DATA1, DATA0 } 1ZD8, 3ZC8, 4ZA8, 5ZD8, 9ZD8, 10ZB8

MEMW/ 8ZD8

MEMR/ 9ZC8, 8ZD8, 11ZC8

IOW/, IOR/ } 1ZD8, 3ZD8, 10ZA8

ADR8, ADR9 } 8ZB8, 11ZB8, 12ZD8

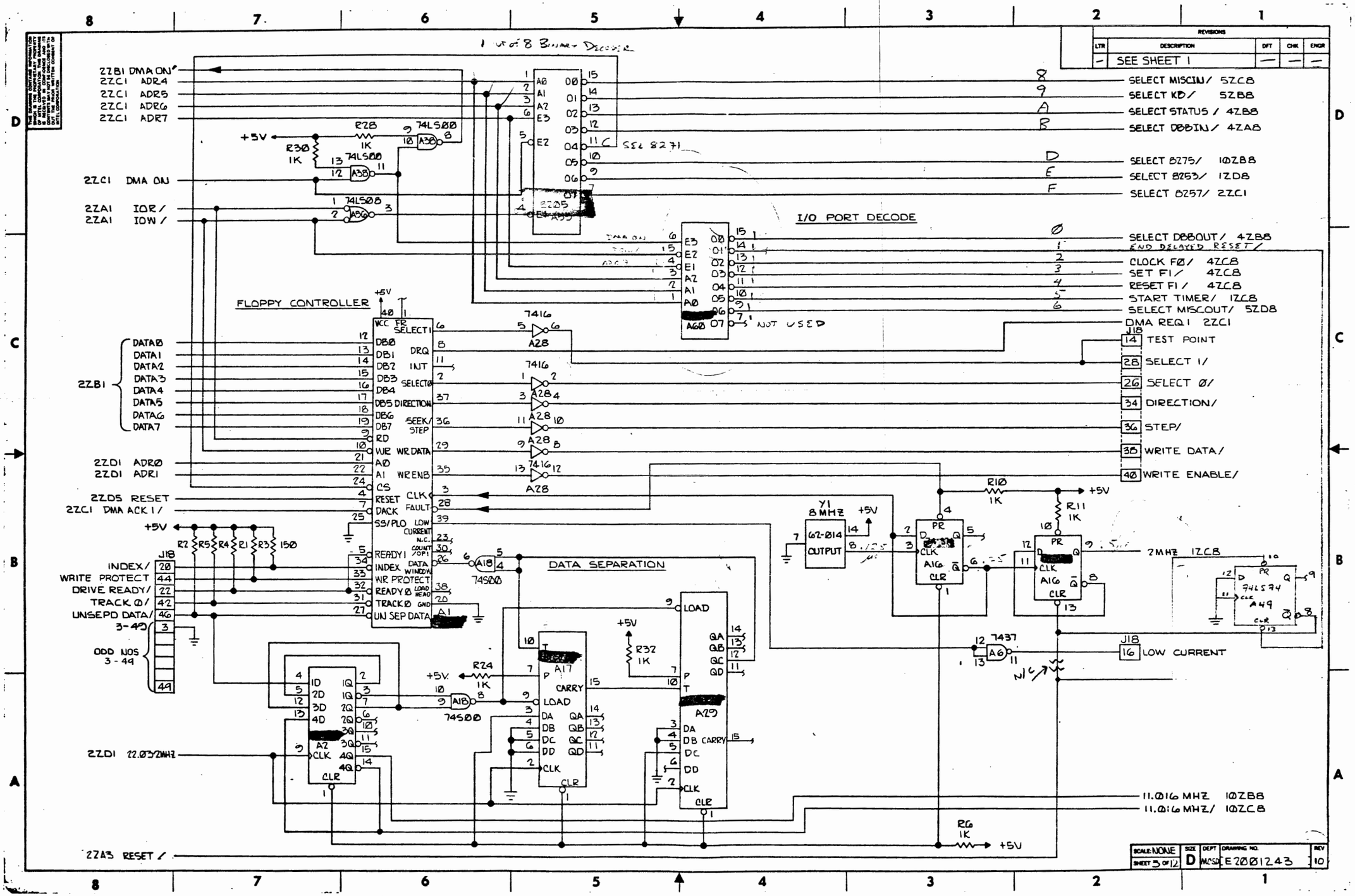
ADRA, ADRB, ADRC, ADRD } 8ZB8, 11ZB8

ADRE, ADRF } 8ZD8, 11ZB8

INITL2/ 5ZB8, 6ZA8, 8ZC8, 4ZD8

RESET/ 3ZA8, 10ZA8

SCALE: NONE	SIZE D	DEPT WSD	DRAWING NO. E 2001243	REV 10
SHEET 2 OF 4				


1 of 8 Binary Decode
2ZB1 DMA ON/
2ZC1 ADR4
2ZC1 ADR5
2ZC1 ADR6
2ZC1 ADR7
+5V
R28 1K
R30 1K
74LS00
2ZC1 DMA ON
2ZA1 IOR/
2ZA1 IOW/
8205
8271
8 SELECT MISCIN/ 5ZC8
9 SELECT KB/ 5ZB8
A SELECT STATUS / 4ZB8
B SELECT DBBIN/ 4ZA8
D SELECT 8275/ 10ZB8
E SELECT 8253/ 1ZD8
F SELECT 8257/ 2ZC1
I/O PORT DECODE
Ø SELECT DBBOUT/ 4ZB8
1 END DELAYED RESET/
2 CLOCK FØ/ 4ZC8
3 SET F1/ 4ZC8
4 RESET F1/ 4ZC8
5 START TIMER/ 1ZC8
6 SELECT MISCOUT/ 5ZD8
7 NOT USED
DMA REQ1 2ZC1
FLOPPY CONTROLLER
2ZB1 DATAØ DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7
2ZD1 ADRØ
2ZD1 ADR1
2ZD5 RESET
2ZC1 DMA ACK1/
DRQ
INT
SELECTØ
DIRECTION
SEEK/ STEP
WR DATA
WR ENB
CLK
FAULT
LOW CURRENT
READY1
INDEX
WR PROTECT
READYØ
TRACKØ
UN SEP DATA
INDEX/
WRITE PROTECT
DRIVE READY/
TRACK Ø/
UNSEPD DATA/
ODD NOS 3-49
DATA SEPARATION
2ZD1 22.032MHZ
2ZA3 RESET/
TEST POINT
SELECT 1/
SELECT Ø/
DIRECTION/
STEP/
WRITE DATA/
WRITE ENABLE/
LOW CURRENT
Y1 8 MHZ
62-014 OUTPUT
2MHZ 1ZC8
11.Ø16 MHZ 10ZB8
11.Ø16 MHZ/ 10ZC8
SCALE: NONE
SHEET 5 OF 12
SIZE D
DEPT MCSD
DRAWING NO. E2001243
REV 10

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
—	SEE SHEET 1	—	—	—

MASTER INTERFACE

DATA BYTE BUFFER (DBB)

INDICATES PRESENCE OF BYTE TO BE SENT TO IPB

OUTPUT BUFFER FULL FLAG/

INPUT BUFFER FULL FLAG/

INDICATES PRESENCE OF NEW BYTE FROM IPB

2ZD1 ADR0 — PORT 00 => OBF; PORT 01 => CLEARS OBF

2ZA3 / INITLZ

3ZC1 RESET FI/ — PORT 40

3ZC1 CLOCK FB/ — PORT 20

3ZC1 SET FI/ — PORT 30

F0 FLAG (BUSY)

SET WHEN IOC 8080 BUSY. UNABLE TO ACCEPT NEW BYTE FROM IPB

R15 1K +5V

COMMAND/DATA FLAG

IO C1 => READS STATUS
IO C0 => READS OUT BUFF
} IPB

3ZD1 SELECT STATUS / — PORT A0

3ZC1 SEL DBBOUT/ — PORT 00

3ZD1 SEL DBBIN/ — PORT 20

2ZB1, 11ZB1, 12ZC1: DATA 0, DATA 1, DATA 2, DATA 3, DATA 4, DATA 5, DATA 6, DATA 7

D3 DATA/COMMAND
D2 BUSY/
D1 IBF/
D0 OBF/

74LS00, 74LS04, 74LS32, 74LS241

OUTPUT BUFFER

INPUT BUFFER

TRI-STATE OUTPUT COMMON HIGH

0 / OBF
1 / IBF
2 / BUSY
3 / DAT/CMD

IOWC/
SEL IOC/ (SELECT/)
IORC/
COMMAND/DATA (ADDR#)

J14

35	IOWC/
44	SEL IOC/ (SELECT/)
37	IORC/
33	COMMAND/DATA (ADDR#)
42	MASTER D0/
45	MASTER D1/
47	MASTER D2/
43	MASTER D3/
49	MASTER D4/
46	MASTER D5/
48	MASTER D6/
50	MASTER D7/

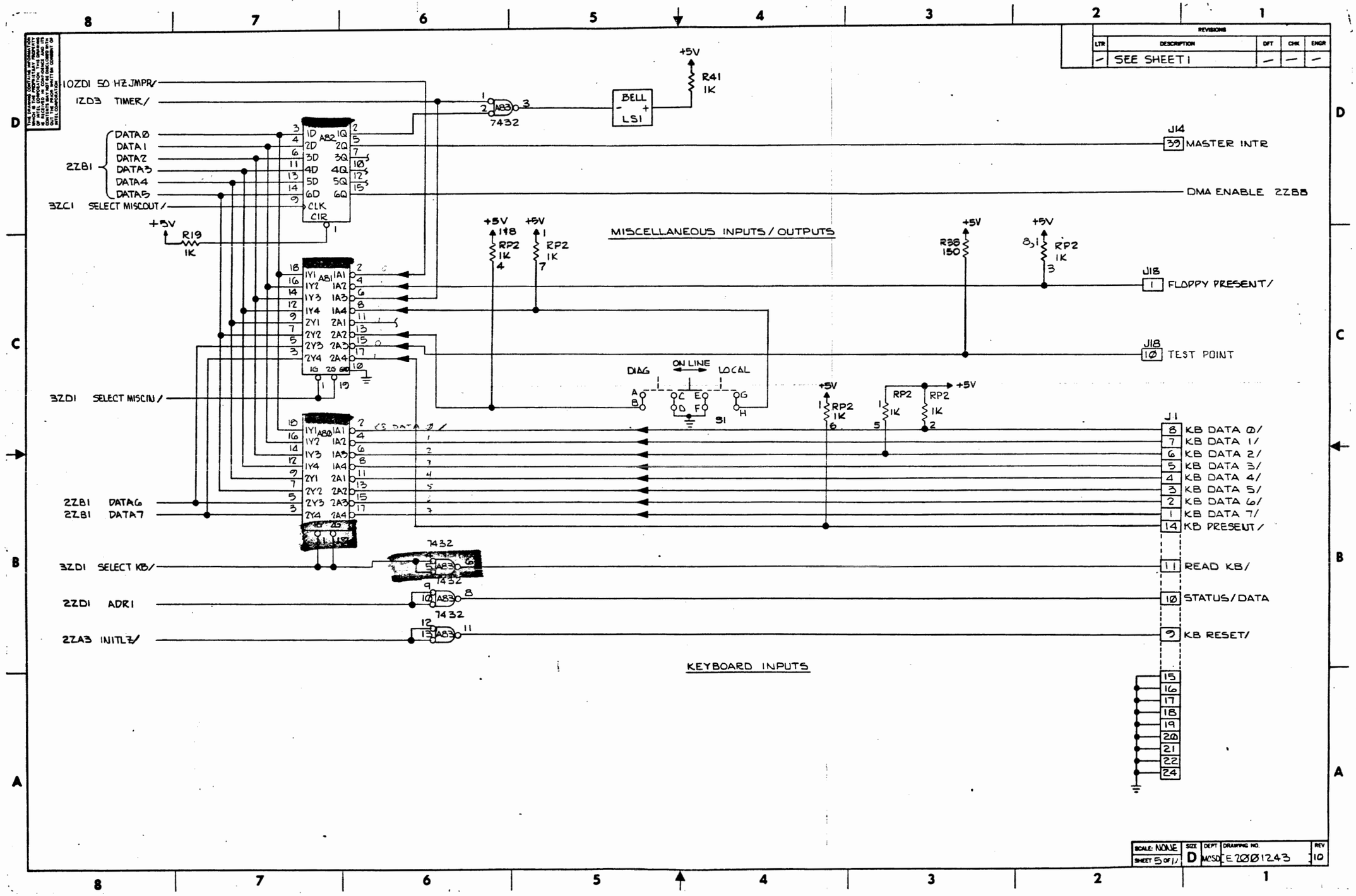
To IPB

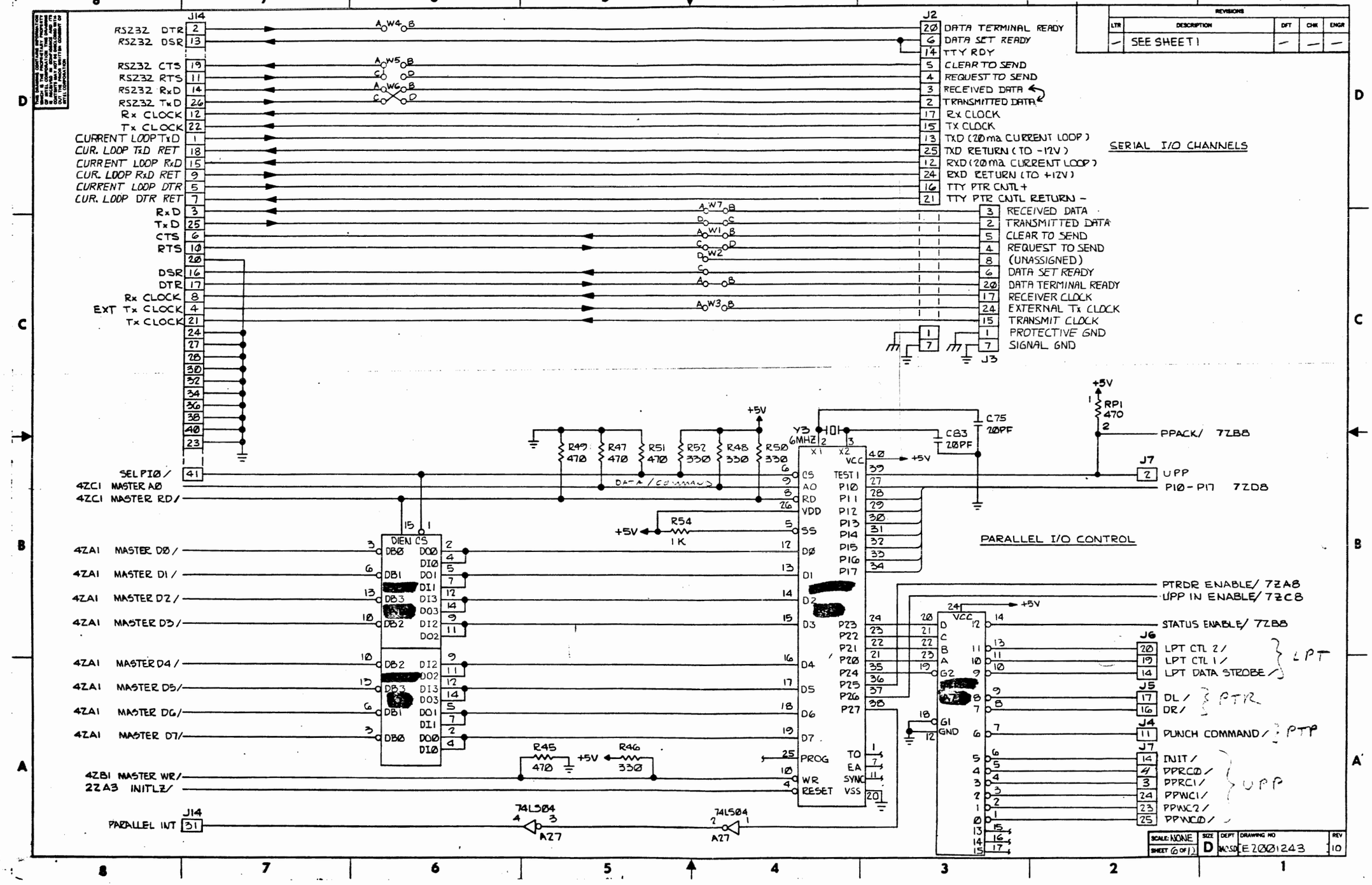
To P10

MASTER A0 6ZB8
MASTER RD/ 6ZB8
MASTER WR/ 6ZA8

MASTER D0/ 6ZB8
MASTER D1/ 6ZB8
MASTER D2/ 6ZB8
MASTER D3/ 6ZB8
MASTER D4/ 6ZA8
MASTER D5/ 6ZA8
MASTER D6/ 6ZA8
MASTER D7/ 6ZA8

SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 4 OF 12	D	MCSD	E 2001243	10


REVISIONS
LTR DESCRIPTION DFT CHK ENGR
– SEE SHEET 1 – – –
10ZD1 50 HZ JMPR/
1ZD3 TIMER/
2ZB1 DATA0 DATA1 DATA2 DATA3 DATA4 DATA5
3ZC1 SELECT MISCOUT/
3ZD1 SELECT MISCIN/
2ZB1 DATA6
2ZB1 DATA7
3ZD1 SELECT KB/
2ZD1 ADR1
2ZA3 INITLZ/
7432
R41 1K
BELL LS1
R19 1K
R38 150
RP2 1K
MISCELLANEOUS INPUTS / OUTPUTS
DIAG ON LINE LOCAL
J14 39 MASTER INTR
DMA ENABLE 2ZB8
J18 1 FLOPPY PRESENT/
J18 10 TEST POINT
J1 8 KB DATA 0/
7 KB DATA 1/
6 KB DATA 2/
5 KB DATA 3/
4 KB DATA 4/
3 KB DATA 5/
2 KB DATA 6/
1 KB DATA 7/
14 KB PRESENT/
11 READ KB/
10 STATUS/DATA
9 KB RESET/
15 16 17 18 19 20 21 22 24
KEYBOARD INPUTS
SCALE: NONE SIZE D DEPT MCSD DRAWING NO. E 2001243 REV 10
SHEET 5 OF 11


REVISIONS
LTR DESCRIPTION DFT CHK ENGR
– SEE SHEET 1 – – –
J14
RS232 DTR 2
RS232 DSR 13
RS232 CTS 19
RS232 RTS 11
RS232 RxD 14
RS232 TxD 26
Rx CLOCK 12
Tx CLOCK 22
CURRENT LOOP TxD 1
CUR. LOOP TxD RET 18
CURRENT LOOP RxD 15
CUR. LOOP RxD RET 9
CURRENT LOOP DTR 5
CUR. LOOP DTR RET 7
RxD 3
TxD 25
CTS 6
RTS 10
DSR 16
DTR 17
Rx CLOCK 8
EXT Tx CLOCK 4
Tx CLOCK 21
J2
20 DATA TERMINAL READY
6 DATA SET READY
14 TTY RDY
5 CLEAR TO SEND
4 REQUEST TO SEND
3 RECEIVED DATA
2 TRANSMITTED DATA
17 Rx CLOCK
15 TX CLOCK
13 TXD (20ma CURRENT LOOP)
25 TXD RETURN (TO -12V)
12 RXD (20ma CURRENT LOOP)
24 RXD RETURN (TO +12V)
16 TTY PTR CNTL+
21 TTY PTR CNTL RETURN –
SERIAL I/O CHANNELS
3 RECEIVED DATA
2 TRANSMITTED DATA
5 CLEAR TO SEND
4 REQUEST TO SEND
8 (UNASSIGNED)
6 DATA SET READY
20 DATA TERMINAL READY
17 RECEIVER CLOCK
24 EXTERNAL Tx CLOCK
15 TRANSMIT CLOCK
1 PROTECTIVE GND
7 SIGNAL GND
J3
W4
W5
W6
W7
W1
W2
W3
SEL P1Ø/ 41
4ZC1 MASTER AØ
4ZC1 MASTER RD/
4ZA1 MASTER DØ/
4ZA1 MASTER D1/
4ZA1 MASTER D2/
4ZA1 MASTER D3/
4ZA1 MASTER D4/
4ZA1 MASTER D5/
4ZA1 MASTER D6/
4ZA1 MASTER D7/
4ZB1 MASTER WR/
2ZA3 INITLZ/
PARALLEL INT J14 31
DIEN CS
DBØ DBI DB3 DB2
DØØ DØ1 DØ3 DØ2 DIØ DI1 DI3 DI2
74LS04 A27
74LS04 A27
R49 470
R47 470
R51 470
R52 330
R48 330
R50 330
DATA/COMMAND
+5V
R54 1K
R45 470
R46 330
Y3 6MHZ
C75 20PF
C83 20PF
X1 X2 VCC TEST 1 P1Ø P11 P12 P13 P14 P15 P16 P17
CS AO RD VDD VSS DØ D1 D2 D3 D4 D5 D6 D7 PROG WR RESET
P23 P22 P21 P20 P24 P25 P26 P27
TO EA SYNC VSS
RP1 470
PPACK/ 7ZB8
J7 2 UPP
P1Ø–P17 7ZD8
PARALLEL I/O CONTROL
PTRDR ENABLE/ 7ZA8
UPP IN ENABLE/ 7ZC8
STATUS ENABLE/ 7ZB8
J6
20 LPT CTL 2/
19 LPT CTL 1/
14 LPT DATA STROBE/
LPT
J5
17 DL/
16 DR/
PTR
J4
11 PUNCH COMMAND/
PTP
J7
14 INIT/
4 PPRCØ/
3 PPRC1/
24 PPWC1/
23 PPWC2/
25 PPWCØ/
UPP
VCC GND
SCALE: NONE
SHEET 6 OF 10
SIZE D
DEPT MCSD
DRAWING NO E2001243
REV 10

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
-	SEE SHEET 1	—	—	—

PARALLEL I/O

6ZB1 P1Ø–P17

6ZB1 UPP IN ENABLE/

6ZB1 STATUS ENABLE/

6ZB1 PTRDR ENABLE/

6ZC1 PPACK/

A78 A79 A75 A76 A73 A74

J6: 9 GND, 10 GND, 11 GND, 12 GND, 15 GND, 25 CHASSIS GND

J7: 22 PWDØ/, 12 PRDØ/, 21 PWD1/, 1 GND, 13 GND

PAPER TAPE READER

J5: 1 DATA TRACK 1/, 2 DATA TRACK 2/, 3 DATA TRACK 3/, 4 DATA TRACK 4/, 5 DATA TRACK 5/, 6 DATA TRACK 6/, 7 DATA TRACK 7/, 8 DATA TRACK 8/, 11 GND, 12 GND, 13 GND, 24 GND, 25 CHASSIS GND

PAPER TAPE PUNCH

J4: 1 DATA TRACK 1/, 2 DATA TRACK 2/, 3 DATA TRACK 3/, 4 DATA TRACK 4/, 5 DATA TRACK 5/, 6 DATA TRACK 6/, 7 DATA TRACK 7/, 8 DATA TRACK 8/, R53 +5V 1K, 10 DIRECTION, 14 INPUT MOVE SELECT, 15 OUTPUT MOVE SELECT, 18 GND, 23 GND, 25 GND, 16 CHASSIS GND, 17 CHASSIS GND

PROGRAMME

J7: 11 PRD1/, 20 PWD2/, 10 PRD2/, 19 PWD3/, 9 PRD3/, 18 PWD4/, 8 PRD4/, 17 PWD5/, 7 PRD5/, 16 PWD6/, 6 PRD6/, 15 PWD7/, 5 PRD7/

J6: 1 DATA 1, 2 DATA 2, 3 DATA 3, 4 DATA 4, 5 DATA 5, 6 DATA 6, 7 DATA 7, 8 DATA 8

RP1 470Ø ×4, +5V

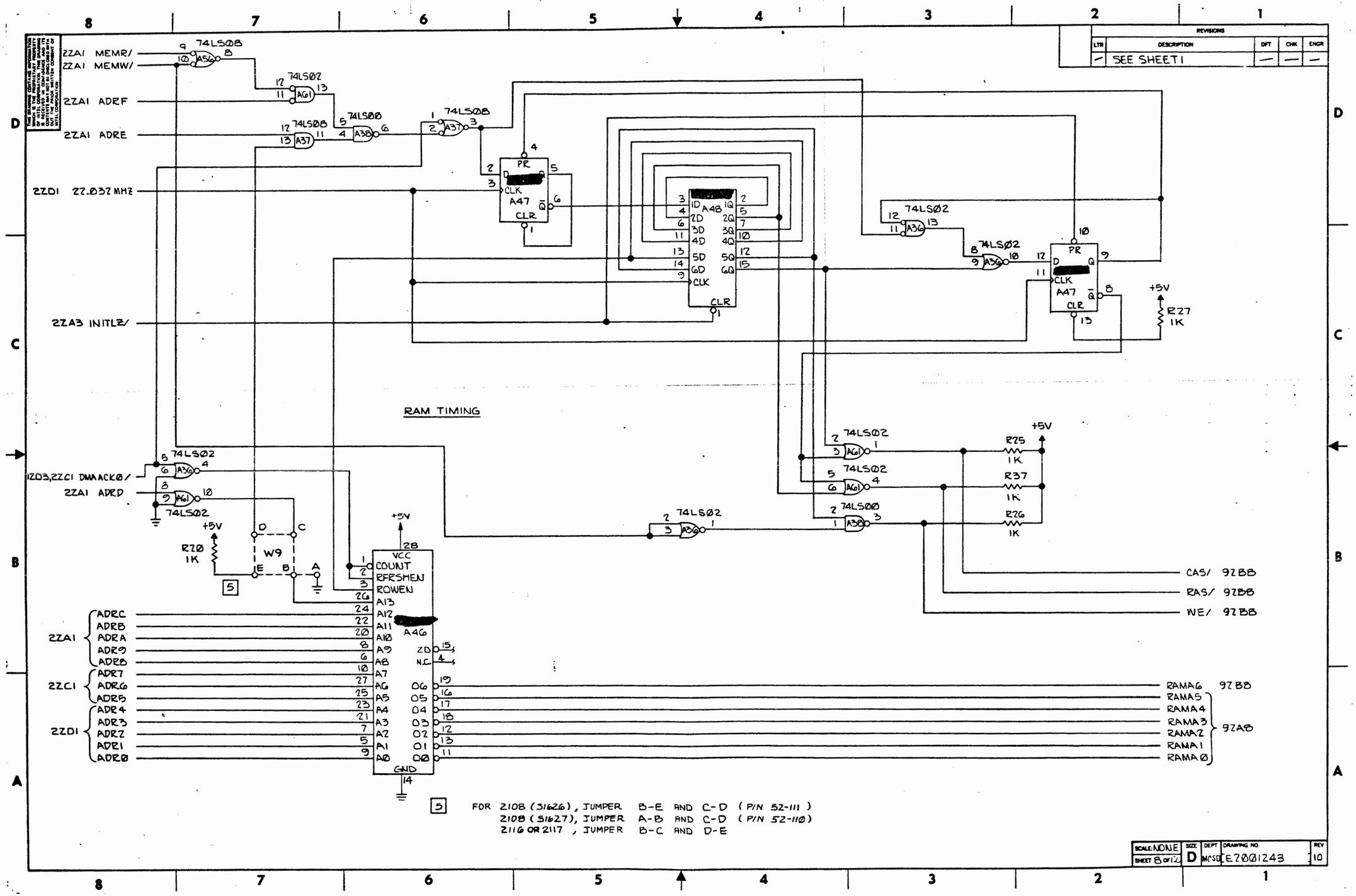
J4: 12 PUNCH READY/, 13 SYSTEMS READY/

J5: 9 DATA READY/, J5 14 SYSTEMS READY

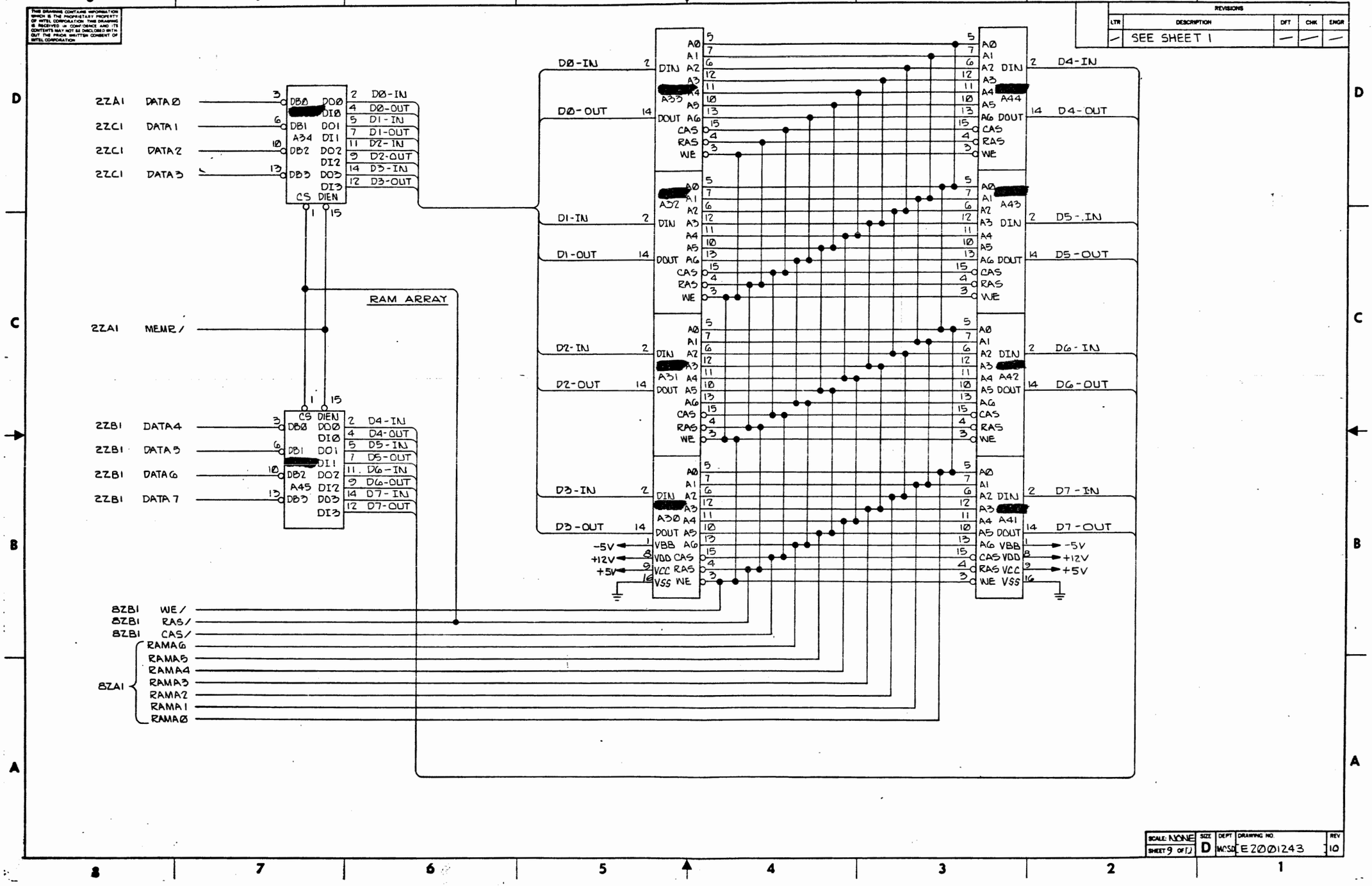
J6: 17 BUSY/, 16 ACKNOWLEDGE/, 22 SELECT/

PRINTER

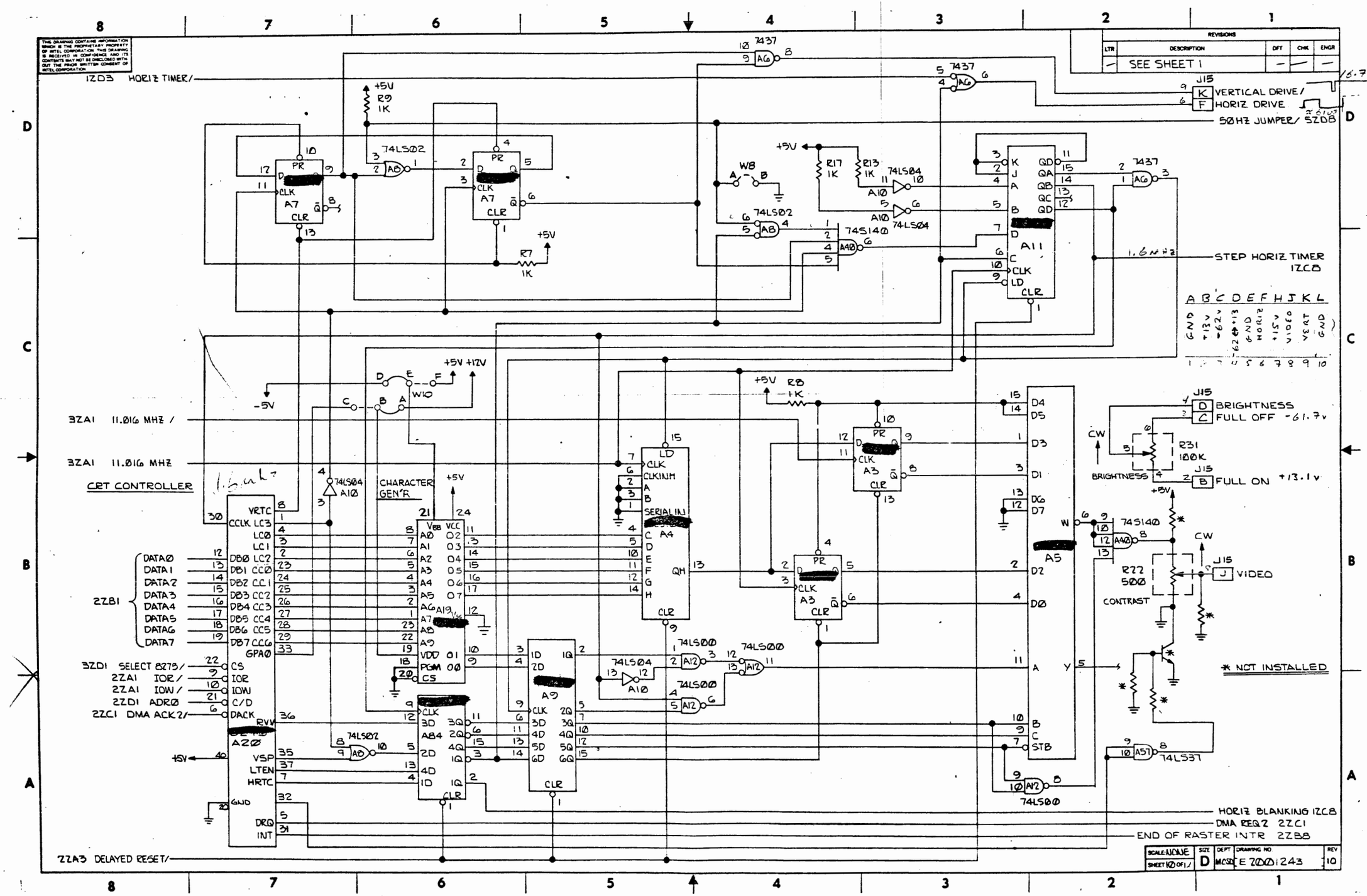
SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 7 OF 7	D	MCS	E 2ØØ1243	10


REVISIONS
LTR DESCRIPTION DFT CHK ENGR
— SEE SHEET1
2ZA1 MEMR/
2ZA1 MEMW/
2ZA1 ADRF
2ZA1 ADRE
2ZD1 22.032 MHz
2ZA3 INITLZ/
74LS08
74LS02
74LS00
A56
A61
A37
A38
A36
PR
CLR
CLK
A47
A48
R27 1K
+5V
RAM TIMING
2ZD3,2ZC1 DMAACK0/
2ZA1 ADRD
R28 1K
W9
D
C
E
B
A
5
VCC
COUNT
RFRSHEN
ROWEN
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
ZD
NC
O6
O5
O4
O3
O2
O1
O0
GND
A46
2ZA1 ADEC ADRB ADRA ADR9 ADR8
2ZC1 ADR7 ADR6 ADR5
2ZD1 ADR4 ADR3 ADR2 ADR1 ADR0
R25 1K
R37 1K
R26 1K
CAS/ 9ZBB
RAS/ 9ZBB
WE/ 9ZBB
RAMA6 9ZB8
RAMA5
RAMA4
RAMA3
RAMA2
RAMA1
RAMA0
9ZA8
5 FOR 2108 (51626), JUMPER B-E AND C-D (P/N 52-111)
2108 (51627), JUMPER A-B AND C-D (P/N 52-110)
2116 OR 2117, JUMPER B-C AND D-E
SCALE:NONE
SHEET 8 OF 12
SIZE D
DEPT MCSD
DRAWING NO. E2001243
REV 10

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
—	SEE SHEET 1	—	—	—



SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 9 OF 10	D	MCSD	E2001243	10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REVISIONS
LTR DESCRIPTION DFT CHK ENGR
— SEE SHEET 1
1ZD3 HORIZ TIMER/
+5V R9 1K
74LS02
74LS04
74LS14Ø
74LS00
74LS37
R17 1K
R13 1K
R7 1K
W8
W10
R31 100K
R22 500
CONTRAST
BRIGHTNESS
CW
J15
VERTICAL DRIVE/
HORIZ DRIVE
5ØHZ JUMPER/ 5ZD8
16.7ms
2.61ms
STEP HORIZ TIMER 1ZC8
1.6MHz
BRIGHTNESS
FULL OFF -61.7v
FULL ON +13.1v
VIDEO
* NOT INSTALLED
3ZA1 11.Ø16 MHZ /
3ZA1 11.Ø16 MHZ
CRT CONTROLLER
CHARACTER GEN'R
2ZB1
DATAØ
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
3ZD1 SELECT 8279/
2ZA1 IOR/
2ZA1 IOW/
2ZD1 ADRØ
2ZC1 DMA ACK 2/
VRTC
CCLK
DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
GPAØ
CS
IOR
IOW
C/D
DACK
RVV
VSP
LTEN
HRTC
DRQ
INT
HORIZ BLANKING 1ZC8
DMA REQ 2 2ZC1
END OF RASTER INTR 2ZB8
2ZA3 DELAYED RESET/
SCALE: NONE
SIZE D
DEPT MCSD
DRAWING NO E 7001243
REV 10
SHEET 10 OF 11

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
/	SEE SHEET 1	/	/	/

ROM CONTROL

0000-07FF

1000-17FF

0800-0FFF

1800-1FFF

A50 A51 A52 A53

DATA0- DATA7

DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7

ADR0 ADR1 ADR2 ADR3 ADR4 ADR5 ADR6 ADR7 ADR8 ADR9

2ZD1 2ZC1 2ZA1 2ZA1

+5V

A27 74LS04

2ZA1 MEMR/

2ZA1 ADRE 2ZA1 ADRB 2ZA1 ADRC

E3 E1 E2 A0 A1 A2 A39

W11

2ZA1 ADRF 2ZA1 ADRD 2ZA1 ADRA

R21 1K

DATA0- DATA7 4ZA8

SELECT 2000-27FF/ 12ZD8

SELECT 2800-2FFF/ 12ZC8

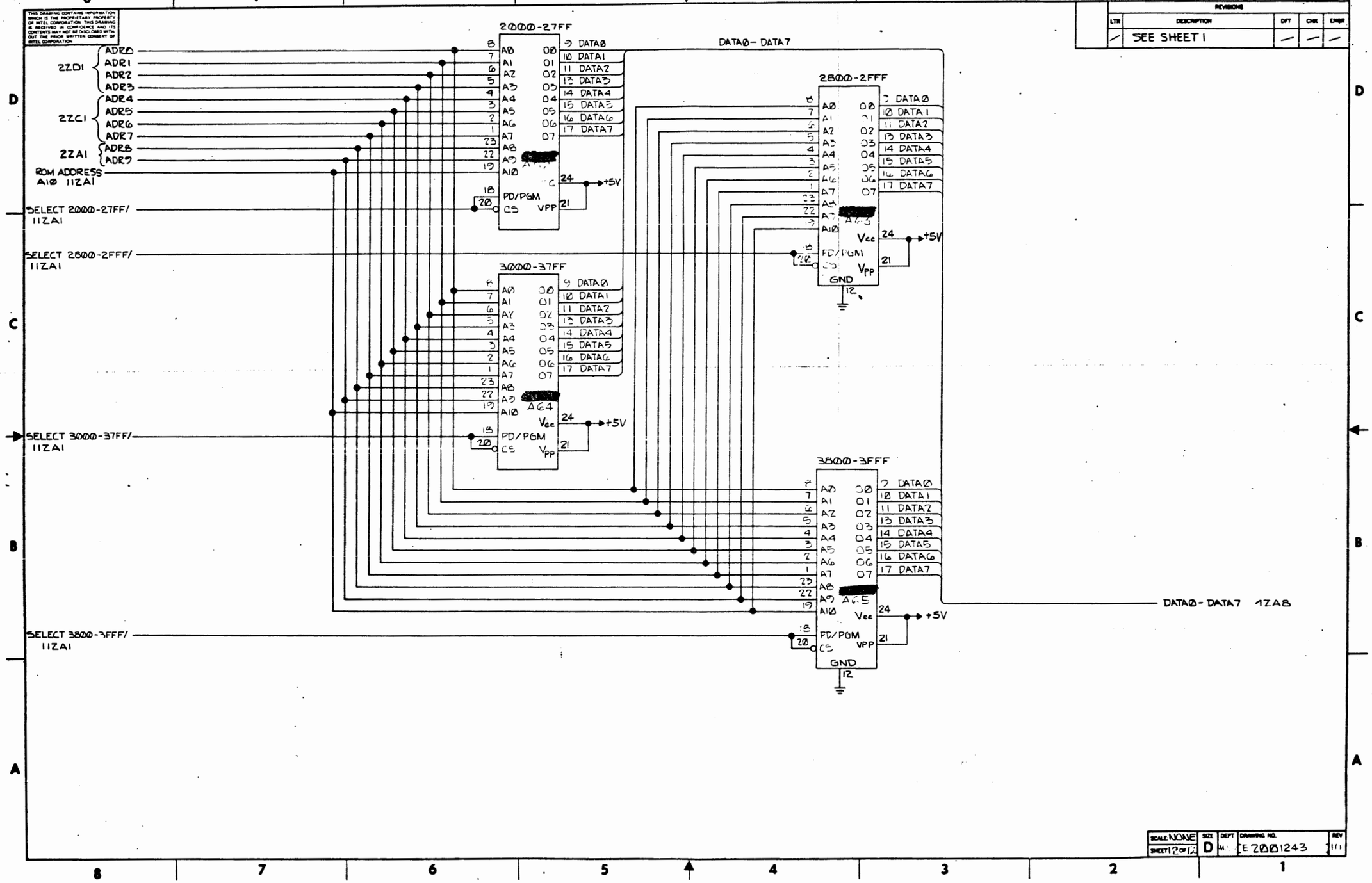
SELECT 3000-37FF/ 12ZC8

SELECT 3800-3FFF/ 12ZB8

ROM ADDRESS A10 12ZD8

SCALE: NONE	SIZE	DEPT	DRAWING NO.	REV
SHEET 1 OF 2	D	MCS	E 2001243	10

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
/	SEE SHEET 1	—	—	—



SCALE: NONE	SIZE D	DEPT	DRAWING NO. CE2001243	REV
SHEET 12 OF 12				