Chapter 7
PROM MODULE

The PROM Module has been designed to provide up to 6,144 (6K) X 8-bit words of PROM storage for 8-bit computer systems or 2,048 (2K) X 16-bit words of storage for 16-bit computer systems. Up to twenty-four 8702A erasable and electrically programmable read only memory (PROM) devices can be included on the module. Each 8702A PROM provides 256 X 8 bits of storage. Any one of the four currently available versions of the popular 8702A memory can be used with the PROM Module:

- 8702A access time = 1.0 μs
- 8702A-S614 access time = 1.5 μs
- 8702A-S314 access time = 1.7 μs
- 8702A-S714 access time = 2.5 μs

Intel's 1702A PROM's or 1302 ROM's (both pin-compatible with the 8702A) can also be used on the PROM Module, in place of the 8702A's.

The 24 PROM elements are organized into a 4K memory bank and a 2K memory bank. The user independently selects the address range for the 4K and 2K memory banks on 4K or 2K boundaries, respectively. Any address blocks within the maximum 64K range can be selected. The addresses assigned to the 2K memory bank can even coincide with those assigned to 2048 X 8-bit words in the 4K bank to implement a 2048 X 16-bit PROM storage capacity.

The PROM Module is available as an optional component within the INTELLEC MDS System, or can be obtained independently on an OEM basis. The module is implemented on a single 12-in. X 6.75-in. printed circuit board. The module requires only DC power at levels of +5 VDC and −10 VDC.

7.1 FUNCTIONAL ORGANIZATION OF THE PROM MODULE

For descriptive purposes, the PROM Module can be viewed as consisting of four functional blocks:

- Memory storage block
- Address control block
- Timing control block
- Byte selection block

These functional units are illustrated in Figure 7-1.

The *memory storage block* consists of up to twenty-four 1702A (8702A) erasable and electrically programmable-read-only-memory (PROM) elements. Each 1702A element stores 256 X 8-bit words of data (2048 bits). The 24 elements are organized into two switch-selectable banks. One bank includes 16 elements and provides 4096 (4K) X 8 bits of PROM storage. The other bank includes eight elements and provides 2048 (2K) X 8 bits of storage.

The *address control block* determines whether the 4K or 2K memory bank is to be accessed (or both for 16-bit words), as well as determining the particular location within the selected bank(s). The address control block includes three jumper pads, and two nine-position rotary switches. The combination of jumper connection and switch settings determine how the 16-bit address from the CPU is to be decoded.

The *timing control block* is responsible for generating the acknowledge signals (AACK/ and XACK/), the inhibit RAM signal (INH1/) and the DATA ENABLE/ signal. The AACK/ and XACK/ signals are returned to the CPU; INH1/ prevents RAM devices from responding to memory addresses intended for the PROM Module; and the DATA ENABLE/ signal strobes the data words (8 or 16-bit) through the byte selection logic and onto the bus. Because several versions of the 8702A PROM are available (each version having a different access time), the timing control block includes an access time select switch which defines delay times for the AACK/ and XACK/ acknowledge signals.

The *byte selection block* controls the flow of data to the data bus via an eight-pair jumper pad (J4).

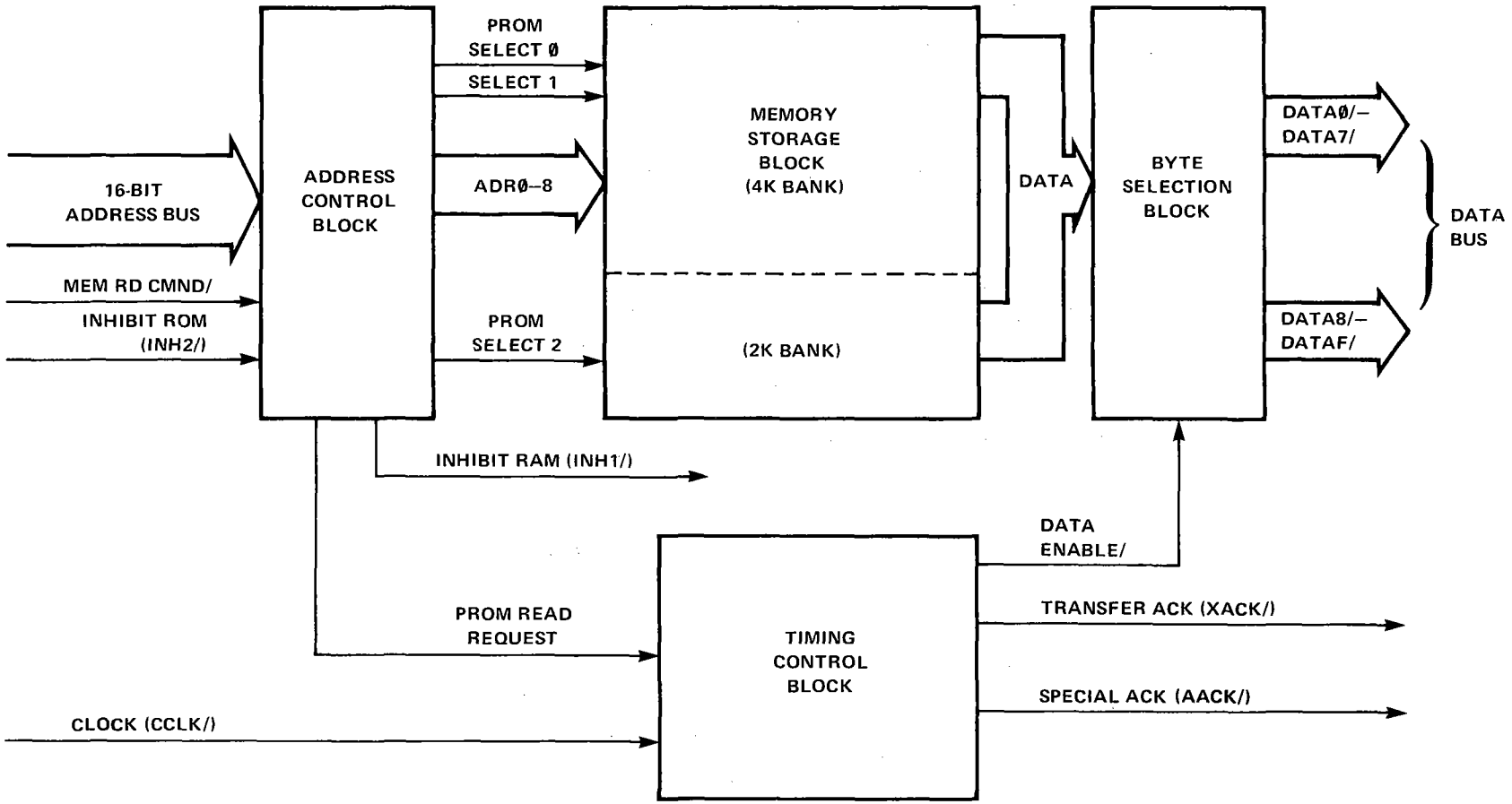


Figure 7-1. PROM Module Functional Block Diagram

The byte selection block can be configured to allow 16-bit data words; jumper pad J4 is removed. In such a case, both the 4K and 2K memory banks are enabled in the address control block, though only 2048 bytes of the 4K bank will be used. The byte selection logic, in the absence of J4, would route the data byte from the 4K bank to the low-order data bus lines (DATAØ/–DAT7/) and would route the data byte from the 2K bank to the high-order data bus lines (DATA8/–DATAF/). In 8-bit systems, the J4 jumper pad must be present to provide a data path from the 2K memory bank to the low-order data bus lines (DATAØ/–DATA7).

7.2 PROM MODULE: THEORY OF OPERATION

In this section, we provide a detailed theory of operation description for the PROM Module. The schematic (4 sheets) for the PROM Module is provided in Figure 7-6, located in Section 7.2.4.

7.2.1 PHYSICAL MEMORY IMPLEMENTATION

The actual memory on the PROM Module consists of up to twenty-four 8702A programmable-read-only-memory (PROM) elements. Each 8702A element has a 256 X 8-bit capacity. The 24 PROM elements are partitioned into two memory banks. One bank includes 4096 (4K) X 8 bits of storage (16 PROM elements), while the other bank includes 2048 (2K) X 8 bits (8 PROM elements). The address ranges for the two banks are switch-selectable as described in Section 7.2.2. In addition, the 2K bank can be used with 2048 words in the 4K bank to implement 2K X 16-bit word storage; as previously described.

The 8702A PROM's are shown on sheets 2, 3 and 4 of the module schematic, Figure 7-6.

7.2.2 MEMORY ADDRESS DECODING

The address control block is responsible for decoding the 16-bit address output by the CPU during all PROM read operations. The address control logic includes three jumper pads and two rotary switches that determine the specific address space to be occupied by the PROM elements. The majority of the address control logic is shown on sheet 1 of the module schematic, Figure 7-6.

The 16 address bits are received by the PROM Module at pins P1-43 through P1-58 and buffered by 3404 inverting buffer circuits. The eight least significant address lines (ADRØ/–ADR7/) are applied to the address inputs of the 8702A PROM elements (AØ–A7). These address lines uniquely identify one of 256 X 8-bit words in each PROM.

Address lines ADR8/, ADR9/, and ADRA/, each feed the address inputs of three 3205 decoders (shown on sheets 2, 3 and 4 of the module schematic). Each decoder is associated with eight PROM elements. The decoders are enabled by one of the three PROM SELECT signals (derived from the five most significant address bits as described below). Each of the eight decoder outputs is applied to the chip select input on one of the eight associated PROMs. During a PROM read operation, only one of the outputs (specified by ADR8/, ADR9/, and ADRA/) on one of the decoders (specified by ADRB/–ADRF/) will be active. Thus, only that PROM element which is specified by the eight high-order address bits is enabled.

The five most significant address lines (ADRB/–ADRF/) are directed to the address selection network, where the PROM SELECT signals are generated. Address line ADRB/ is applied (in either an active-low or active-high form) to one of two inputs on the three 7402 negative-AND gates that actually generate the PROM SELECT signals. The other input to each of these gates is supplied by one of the two rotary switches (S3 and S4). The nine-position rotary switches are tied back to the outputs of two 3205 decoders. Address lines ADRC/, ADRD/, and ADRE/ feed the address inputs of these two decoders. The two decoders are enabled by address line ADRF/. The particular level (high or low) on ADRF/ that enables the decoders is dependent on the setting of the X2 and Y2 jumper pads (pads 7-8-9 and 10-11-12, respectively). A rotary switch output, then, will be active (low) only if its associated decoder is enabled by ADRF/ (as specified by X2 of Y2) and the value on address lines ADRC/–ADRE/ matches the setting of the switch (position 9 means the switch is off).

To generate the PROM SELECT Ø signal, the output of switch S4 must be low (active) but ADRB/ must be high (inactive). To generate PROM SELECT 1, the output of switch S4 must be low (active), and ADRB/ must be low (inactive). To generate PROM SELECT 2, the output of switch S3 must be active and the 2K address select jumper (pad 1-2-3) must be connected such that the input to A41-8 is low.

PROM SELECT Ø enables the least significant 2048 X 8-bit words of the 4K memory bank (sheet 2 of the schematic). PROM SELECT 1 enables the most significant 2048 X 8-bit words of the 4K memory bank (sheet 3 of the schematic). PROM SELECT 2 enables the 2K memory bank.

To summarize: The five most significant address bits (ADRB/–ADRF/) specify one of three 2048 word sections (eight PROM elements per section) within the PROM Module. The particular 2048 word section which is enabled is indicated by one of the three PROM SELECT signals. Address bits ADR8/, ADR9/, and ADRA/, in turn, enable one of the eight PROMs in the selected 2048 word section. Finally, the eight least significant address bits (ADRØ/–ADR7/) specify one of 256 X 8-bit words within the selected PROM element.

As we mentioned above, the actual 2048 word section which is selected by decoding the five high-order address bits is dependent on a number of variables. That is, various jumper connections and switch settings determine the actual addresses that a particular PROM element will respond to. In essence, the user assigns a particular set of addresses to each of the three 2048 word sections (8 PROM elements per section) on the module.

The addresses for the 2K memory bank are determined by the following connections and switch settings:

- 2K address select jumper pad (1-2-3)
- Y2 decoder enable jumper pad (10-11-12)
- Rotary switch (S3) referred to as Y1

The addresses for the 4K memory bank are determined by these connections and switch settings:

- X2 decoder enable jumper pad (7-8-9)
- Rotary switch (S4), referred to as X1

The following technique can be used for address selection:

1. If the module is being used in an 8-bit configuration, the address range of the *4K bank* is-

   XØØØ to XFFF (base 16)

   where $X = X_1 + X_2$ (hexadecimal addition),

   X_1 is determined by switch X_1
   (values 0 to 7 as detailed on the PCB), and

   X_2 is determined by jumper X_2
   (values 0 or 8 as detailed on the PCB).

   The address range of the *2K bank* is:

   YØØØ to Y7FF
   or Y8ØØ to YFFF (base 16)

   where $Y = Y_1 + Y_2$

   Y_1 and Y_2 are selected in a manner similar to X_1 and X_2, described above.

   The second most significant hexadecimal digit in the 2K bank address range is determined by jumper 1-2-3. One position yields YØØØ, the other Y8ØØ.

2. If the module is being used in a 16-bit configuration, connector J4 must be removed. Half of the 4K bank is used for the upper byte of the 16-bit words, while the 2K bank is used for the lower byte. X and Y are selected as described above. In 16-bit configurations, however, X and Y must be set equal.

Table 7-1 lists the addresses that result from the various combinations of jumper connections and switch settings.

Note in Table 7-1 that the address range for the 2K memory bank can be different than that for the 4K memory bank or it can respond to the same addresses as one of the two 2048 word sections within the 4K memory bank. When the 2K and 4K memory banks have mutually exclusive address ranges, the PROM Module provides 6,144 (6K) X 8-bit words of storage. When the address range for the 2K module is the same as the address range for

Table 7-1

ADDRESS SWITCH POSITIONS

ADDRESS RANGE (HEX)	4K BANK			2K BANK			
	X1* [SWITCH S4]	X2 [JUMPER 7-8-9]	PROM** CHIP LOCATIONS	Y1* [SWITCH S3]	Y2 [JUMPER 10-11-12]	2K ADDRESS SELECT [JUMPER 1-2-3]	PROM** CHIP LOCATIONS
0000–07FF	1	8–9	A1–A8	1	11–12	2–1	A23–A30
0800–0FFF	1		A12–A19	1		2–3	
1000–17FF	2		A1–A8	2		2–1	
1800–1FFF	2		A12–A19	2		2–3	
2000–27FF	3		A1–A8	3		2–1	
2800–2FFF	3		A12–A19	3		2–3	
3000–37FF	4		A1–A8	4		2–1	
3800–3FFF	4		A12–A19	4		2–3	
4000–47FF	5		A1–A8	5		2–1	
4800–4FFF	5		A12–A19	5		2–3	
5000–57FF	6		A1–A8	6		2–1	
5800–5FFF	6		A12–A19	6		2–3	
6000–67FF	7		A1–A8	7		2–1	
6800–6FFF	7		A12–A19	7		2–3	
7000–77FF	8		A1–A8	8		2–1	
7800–7FFF	8	8–9	A12–A19	8	11–12	2–3	
8000–87FF	1	8–7	A1–A8	1	11–10	2–1	
8800–8FFF	1		A12–A19	1		2–3	
9000–97FF	2		A1–A8	2		2–1	
9800–9FFF	2		A12–A19	2		2–3	
A000–A7FF	3		A1–A8	3		2–1	
A800–AFFF	3		A12–A19	3		2–3	
B000–B7FF	4		A1–A8	4		2–1	
B800–BFFF	4		A12–A19	4		2–3	
C000–C7FF	5		A1–A8	5		2–1	
C800–CFFF	5		A12–A19	5		2–3	
D000–D7FF	6		A1–A8	6		2–1	
D800–DFFF	6		A12–A19	6		2–3	
E000–E7FF	7		A1–A8	7		2–1	
E800–EFFF	7		A12–A19	7		2–3	
F000–F7FF	8		A1–A8	8		2–1	
F800–FFFF	8	8–7	A12–A19	8	11–10	2–3	A23–A30

*Position 9 is OFF.

**NOTE: PROM chip locations A1–A8 are enabled by PROM SELECTØ, locations A12–A19 by PROM SELECT1 and locations A23–30 by PROM SELECT2.

2048 words within the 4K bank, the module will provide 2048 (2K) X *16-bit* words of storage. In this configuration, only 16 PROM elements would be resident on the module.

The address control block also includes a PROM resident select switch which prevents an attempted access to a non-existent portion of PROM storage from being executed (e.g., if all 24 PROM positions on the module are not being used). One of the three PROM SELECT signals is generated whenever the PROM Module is being accessed. In addition to enabling the selected PROM, the PROM SELECT signals are each applied to one of three 7403 NAND gates. The other input on each of these 7403 sections is tied to +5 VDC (through a resistor) and to one of three poles on the PROM resident select switch (S1). If a particular PROM SELECT signal is true and the associated pole on the S1 switch is open (indicating that the addressed 2048 word section is present and operational), the 7403 gate is activated. Table 7-2 lists the settings on the PROM resident switch (S1) that enable the three 2048 word blocks on the module.

The outputs of the three 7403 gates are wire-ORed together, then inverted. This inverted result is inverted again and asserted at connector pin P1-24 as the inhibit RAM signal (INH1/). INH1/ prevents a RAM device from responding to a memory address intended for the PROM Module.

The inverted, ORed output of the three 7403 gates is also applied to one input of a 7408 AND gate. The other 7408 input is furnished by the result of ANDing the memory read command (MRDC) and the active-low inhibit ROM signal (INH1/). The output of the 7408 gate constitutes the PROM READ REQUEST signal. PROM READ REQUEST is made available to the timing control block (see Section 7.2.3).

7.2.3 PROM TIMING CONTROL

The timing control logic is responsible for acknowledging the PROM read operation and enabling the byte selection logic, at the proper times. Because various 8702A PROMs with different access times are currently available, the timing control logic has been designed to selectively coordinate overall PROM Module timing with the speed of the PROM devices actually being used. The timing control block includes an eight-pole access timer select switch which allows the user to specify module timing as a function of the PROM type.

PROM READ REQUEST, which is normally held low, goes high when a PROM is to be accessed (see Section 7.2.2). It is inverted and applied to the byte selection logic under the mnemonic DATA ENABLE/. DATA ENABLE/ enables the eight (or 16) 8098 hex inverters that drive the data bus (see sheet 4 of the module schematic). The active-high level on PROM READ REQUEST is also applied to the D-input of a 7474 flip-flop (shown at A22-12). This high level also enables two other 7474 sections, the XACK/ and AACK/ latches, which had been held in the pre-reset state by the low level on PROM READ REQUEST. The command clock signal, CCLK/ (received at pin P1-31), clocks all three 7474 flip-flops, though only the first 7474 latch (output at A22-9) will toggle to the set state at this time. The Q output of this set latch (A22-9) presents a high level to the active-low load (LD) inputs of two 74161 synchronous, 4-bit counters. The two counters are wired together as a single 8-bit counter (i.e., the carry output of the first counter enables the second counter). This 8-bit counter scheme now increments its output value once for each CCLK/ pulse received, beginning with the pre-loaded value. The pre-loaded value is determined by the setting of the access timer select switch (S2). As we mentioned above, the S2 switch setting is dependent on the type and speed of 8702A PROM device actually being used. Table 7-3 provides the proper swtich settings for each of the four 8702A PROM types.

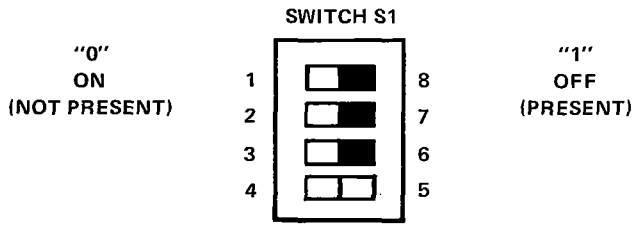
The QC output of the top 74161 counter is applied to one input of a 7408 AND gate. The QB output of the bottom 74161 counter feeds the D-input of the AACK/ latch. On the next positive-going edge of CCLK/ after QB goes high, the AACK/ latch is clocked to the set state. The low $\overline{Q}$ output of this latch is then applied to its pre-set input, thus maintaining its set condition through subsequent occurrences of CCLK/. The high Q output is inverted and driven through connector pin P1-25 as the special acknowledge signal, AACK/. The Q output is also applied to the 7408 AND gate with QC from the first counter. The output of this 7408 gate, in turn, feeds the D-input of the XACK/ latch. The next positive-going edge of CCLK/ after the 7408

Table 7-2

PROM RESIDENT SELECT SWITCH (S1) SETTINGS

MEMORY BANK	PROM CHIP LOCATIONS	S1 SWITCH POLES	SWITCH SETTINGS FOR 8702 INSTALLATION*	
			NOT PRESENT	PRESENT
2K	A23–A30 (PROM SELECT2)	1,8	0	1
4K	A1–A8 (PROM SELECT0)	2,7	0	1
	A12–A19 (PROM SELECT1)	3,6	0	1

*0=OFF, closed circuit between +5V and ground
1=ON, open circuit between +5V and ground



NOTE: POLES 4, 5 NOT USED.

SETTING SHOWN INDICATES ALL THREE 2048 WORD BLOCKS ARE PRESENT AND OPERATIONAL.

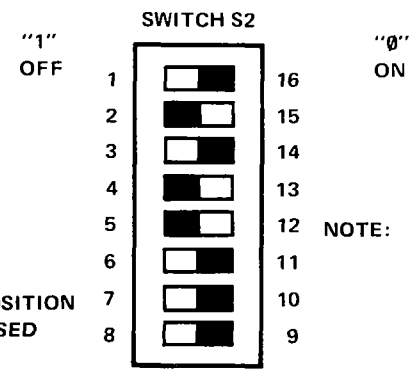
NOTE: NUMBERING REFERS TO DIP PIN DESIGNATIONS RUNNING COUNTERCLOCKWISE FROM THE UPPER LEFT CORNER OF THE SWITCH MODULE. IGNORE VENDOR DESIGNATIONS.

Table 7-3

ACCESS TIMER SELECT SWITCH (S2) SETTINGS

DEVICE TYPE	ACCESS TIME	SWITCH SETTINGS (S2)*							
		1,16	2,15	3,14	4,13	5,12	6,11	7,10	8,9
8702A	1.0 μs	0	1	0	1	1	0	0	0
8702A–S614	1.5 μs	1	0	1	0	1	0	0	0
8702A–S314	1.7 μs	0	0	1	0	1	0	0	0
8702A–S714	2.5 μs	1	1	0	1	0	0	0	0

*0=ON, closed circuit between +5V and ground
1=OFF, open circuit between +5V and ground



NOTE: DARK SIDE REPRESENTS POSITION OF SLIDER OR THE DEPRESSED SIDE OF A ROCKER SWITCH.

NOTE: NUMBERING REFERS TO DIP PIN DESIGNATIONS RUNNING COUNTERCLOCKWISE IN ASCENDING ORDER FROM THE UPPER LEFT-HAND CORNER OF THE SWITCH MODULE. VENDOR LABELING ON THE SWITCH SHOULD BE IGNORED.

SETTING SHOWN IS FOR 8702A DEVICE (ACCESS TIME = 1.0 μs

goes active clocks this latch set. The $\overline{Q}$ output is applied to the pre-set input locking the latch in the set state. The Q output is inverted and driven through connector pin P1-23 as the transfer acknowledge signal, XACK/. When DATA ENABLE/ (described above) goes false at the end of the memory read cycle, the two 8098 circuits which drive XACK/ and AACK/ are disabled.

Timing for XACK/ and AACK/ for each of the four 8702A PROM types is provided in Figures 7-2 through 7-5.

7.2.4 PROM MODULE SCHEMATIC

Figure 7-6 provides a complete schematic drawing (4 sheets) of all circuitry on the PROM Module.

7.3 UTILIZATION: PROM MODULE

This section provides information on utilization of the PROM Module.

7.3.1 INSTALLATION

In installing the PROM Module, the user must take account of:

(a) environmental extremes
(b) mounting considerations
(c) electrical connections
(d) power requirements
(e) signal requirements
(f) address assignments
(g) access timer selection
(h) byte selection

Environment

Temperature extremes can cause instability, or result in permanent damage to the circuits on the module. Ambient temperature must therefore be maintained within the limits of 0° and 70° Centigrade. Exercise caution in locating the module, giving particular attention to radiant and conducive sources of heat. Remember that the module itself, when installed, will contribute some heat to the environment. Maintain an adequate clearance, to permit the convective dissipation of heat from the elements on the card.

Relative humidity should not exceed 90%, noncondensing.

Mounting

Avoid locating the module near vibrating machinery. Exposure to prolonged or violent vibration may cause fatigue or impact failure of connections on the board, resulting in abnormally high noise levels or outright failure of the assembly.

Dimensions of the module are 12-in. X 6.75-in. Be sure to allow enough additional clearance to ensure adequate cooling.

The module is designed to plug directly into two standard, double-sided PC edge connectors; an 86-pin connector and a 60-pin auxiliary connector. The connectors can serve as a mounting, as well as an electrical junction, if the environment is not too severe. Card guide slots are desirable, for the additional protection they afford. Should vibration be a problem, however, or should the assembly be used in a portable equipment application, an additional retaining bracket will have to be provided. When mounting the board, remember that it is desirable to orient the assembly vertically whenever possible. This optimizes convective cooling of the components on the module.

Electrical Connections

The PROM Module communicates with the motherboard and, consequently, the rest of the system, through a standard 86-pin, double-sided PC edge connector (P1), 0.156-in. contact centers, as shown in Figure 7-7. Control Data VPB01E43A00A1 is one suitable type of connector. Pin allocations on this connector are given in Table 7-4 of Section 7.3.2. The module can also communicate with other modules in the system, through the auxiliary 60-pin, double-sided PC edge connector (P2), 0.1-in. contact centers (see Figure 7-7). Pin allocations for this connector (primarily used for test points) are listed in Table 7-5.

The PROM Module requires DC power at levels of +5 VDC and −10 VDC.

Refer to the pin lists in Tables 7-4 and 7-5 of Section 7.3.2 for power connections.

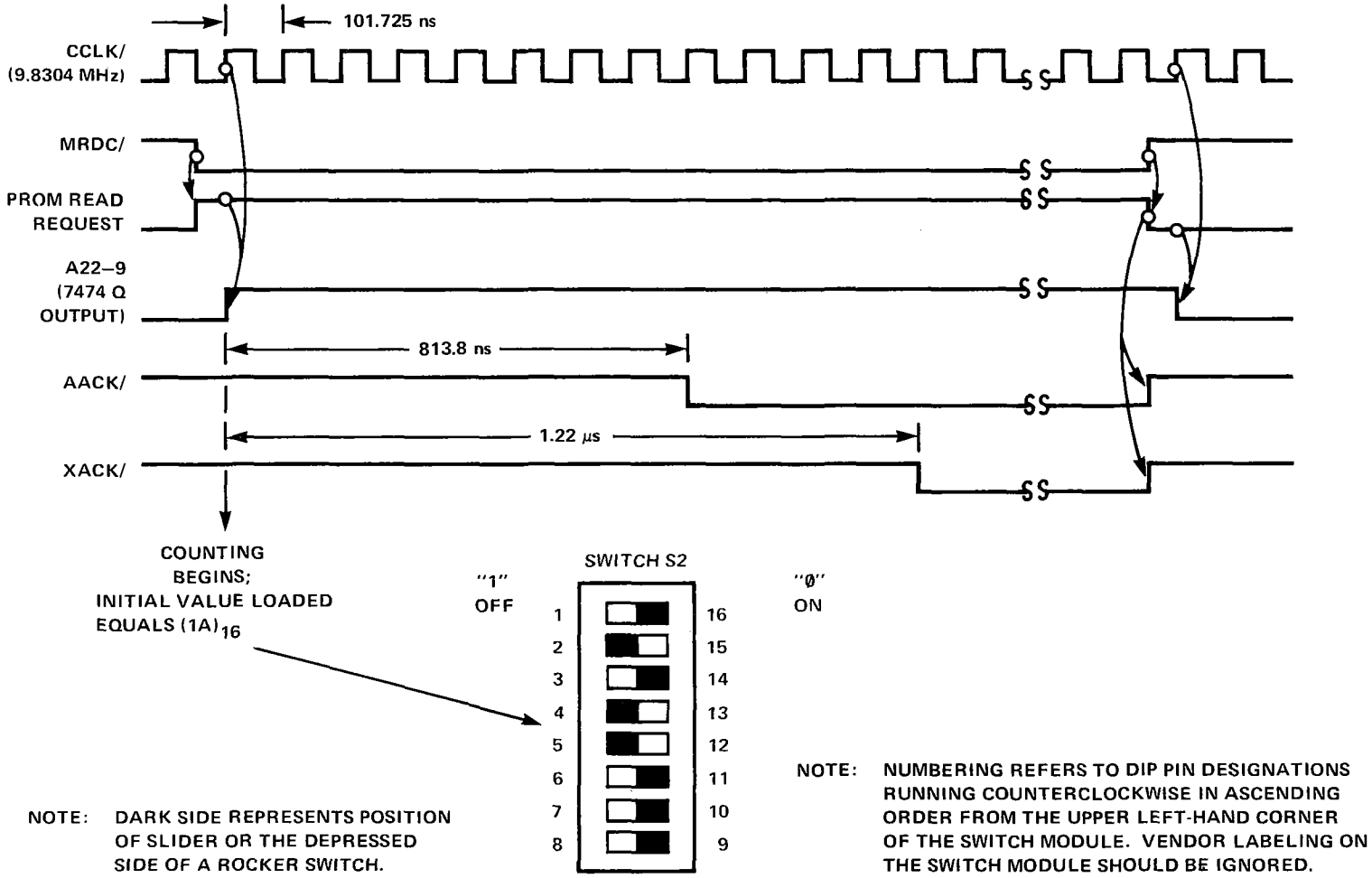


Figure 7-2. PROM Module Timing for 8702A PROMs (Access Time = 1.0 μs)

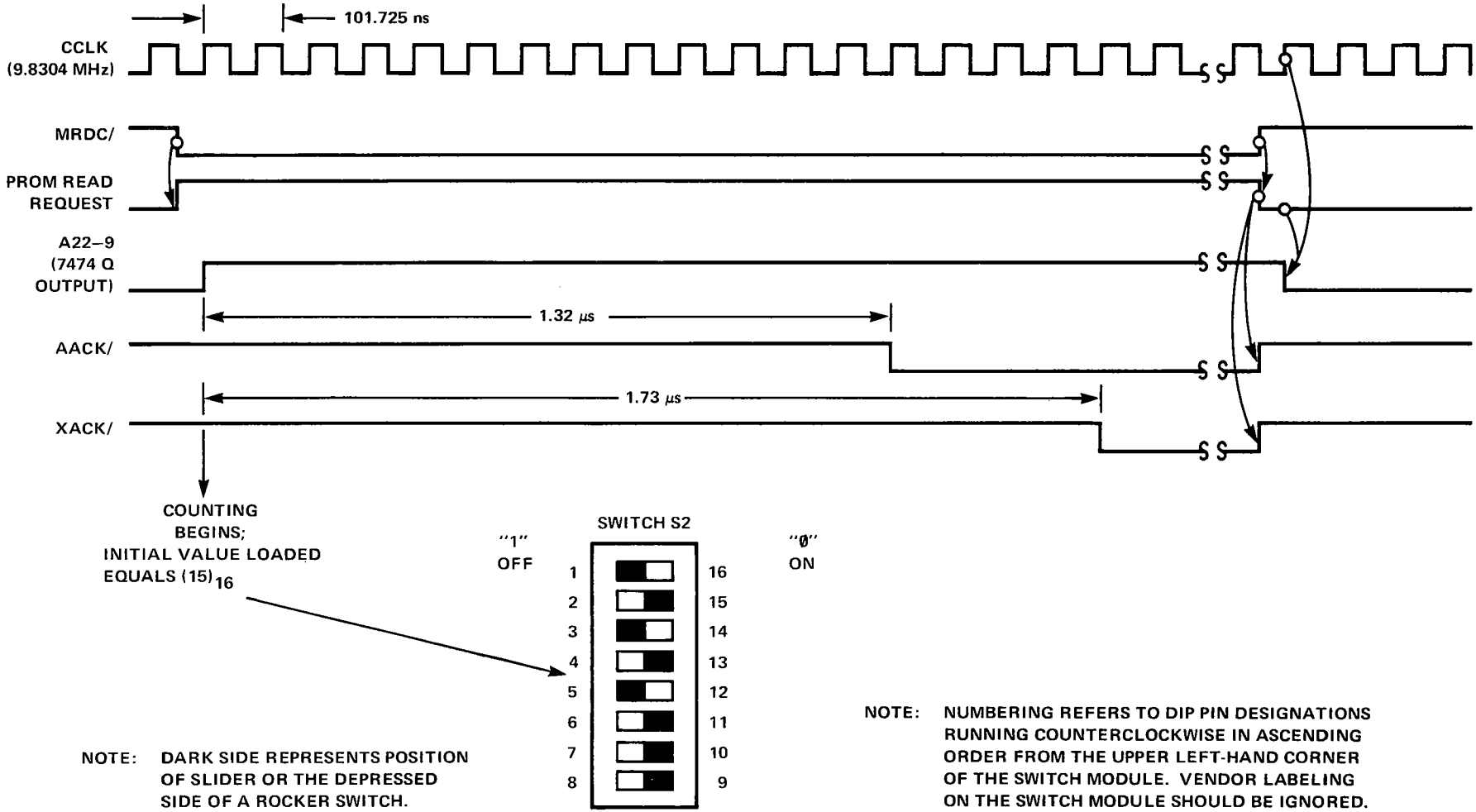


Figure 7-3. PROM Module Timing for 8702A-S614 PROMs (Access Time = 1.5 μs)

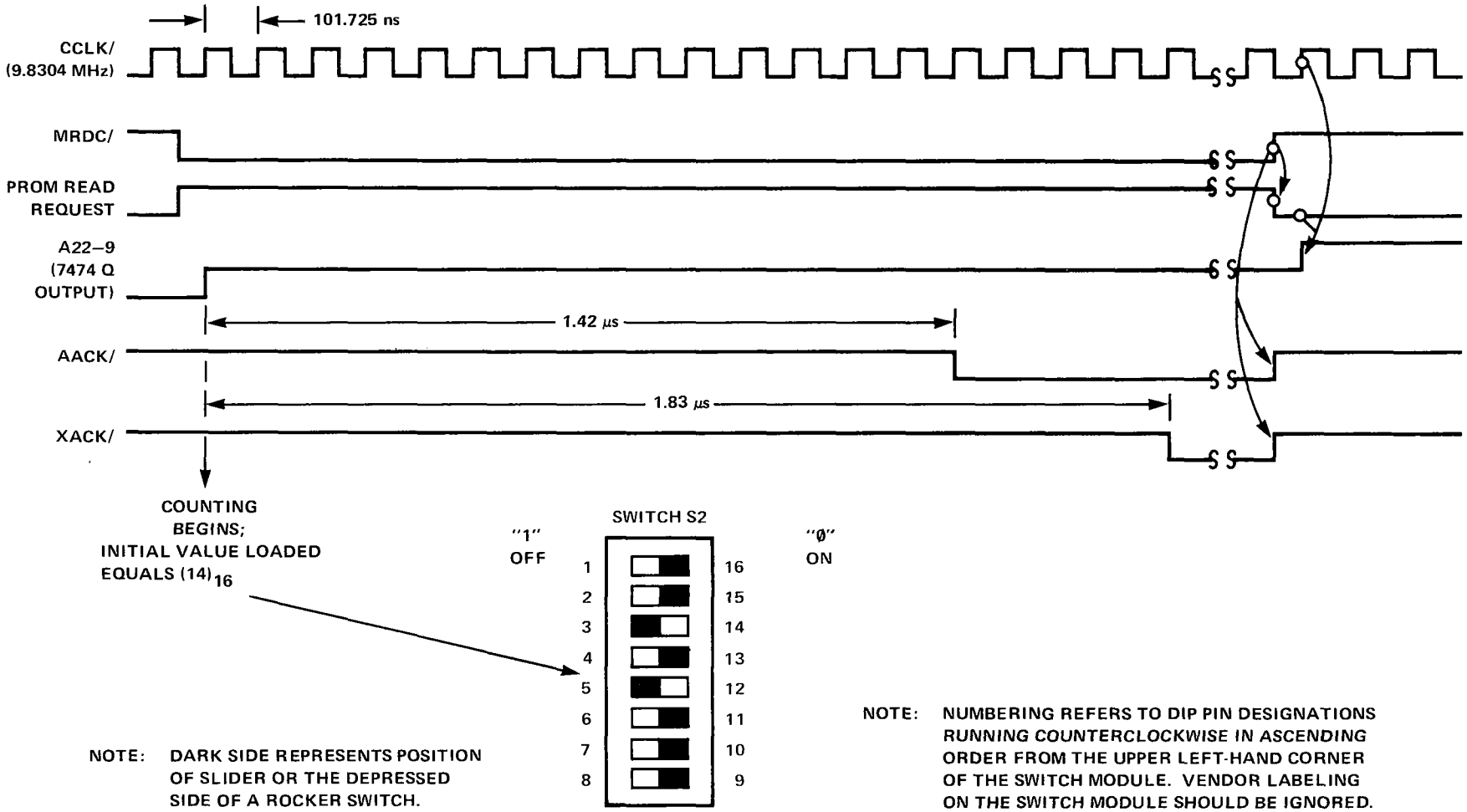


Figure 7-4. PROM Module Timing for 8702A-S314 PROMs (Access Time = 1.7 μs)

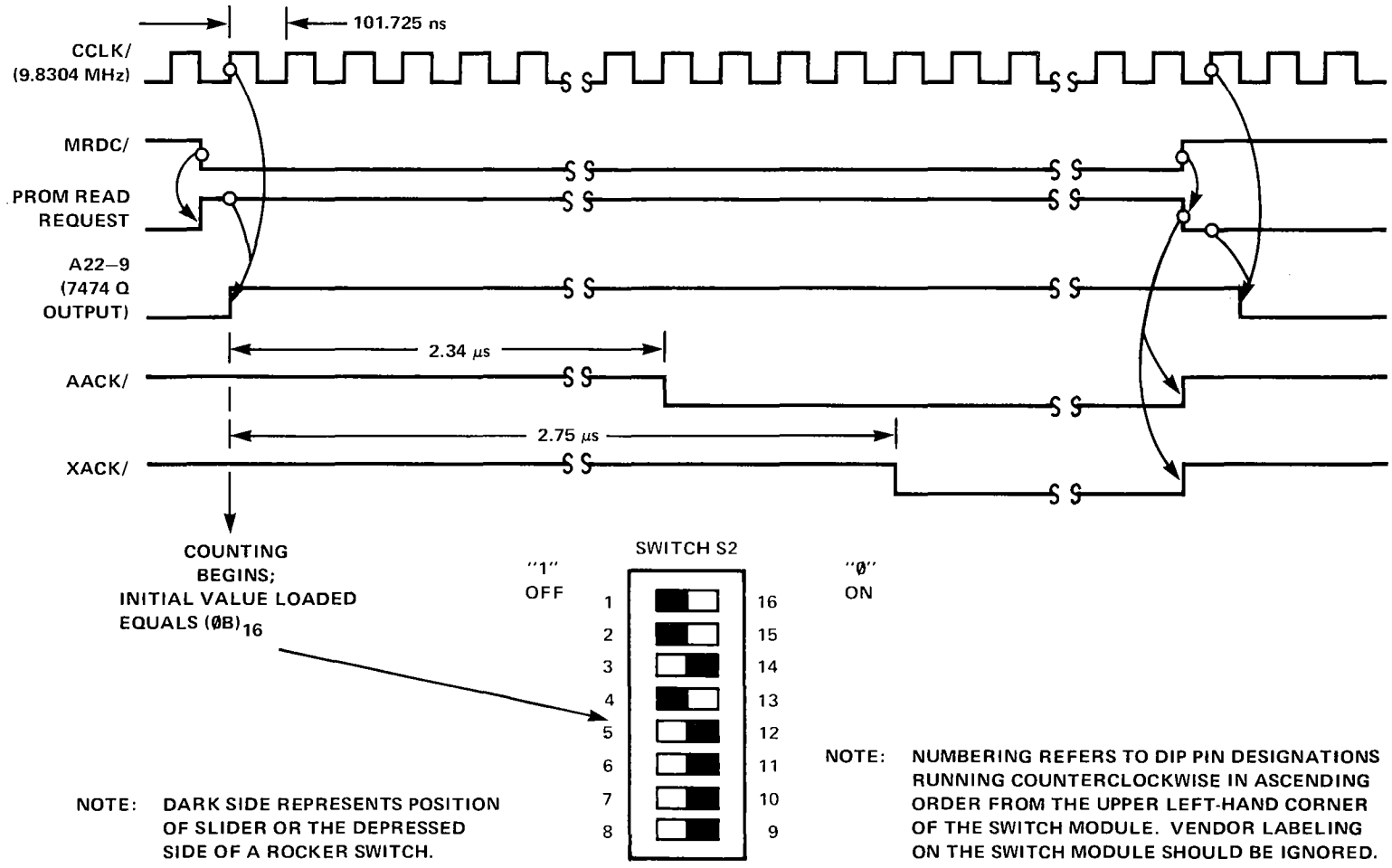
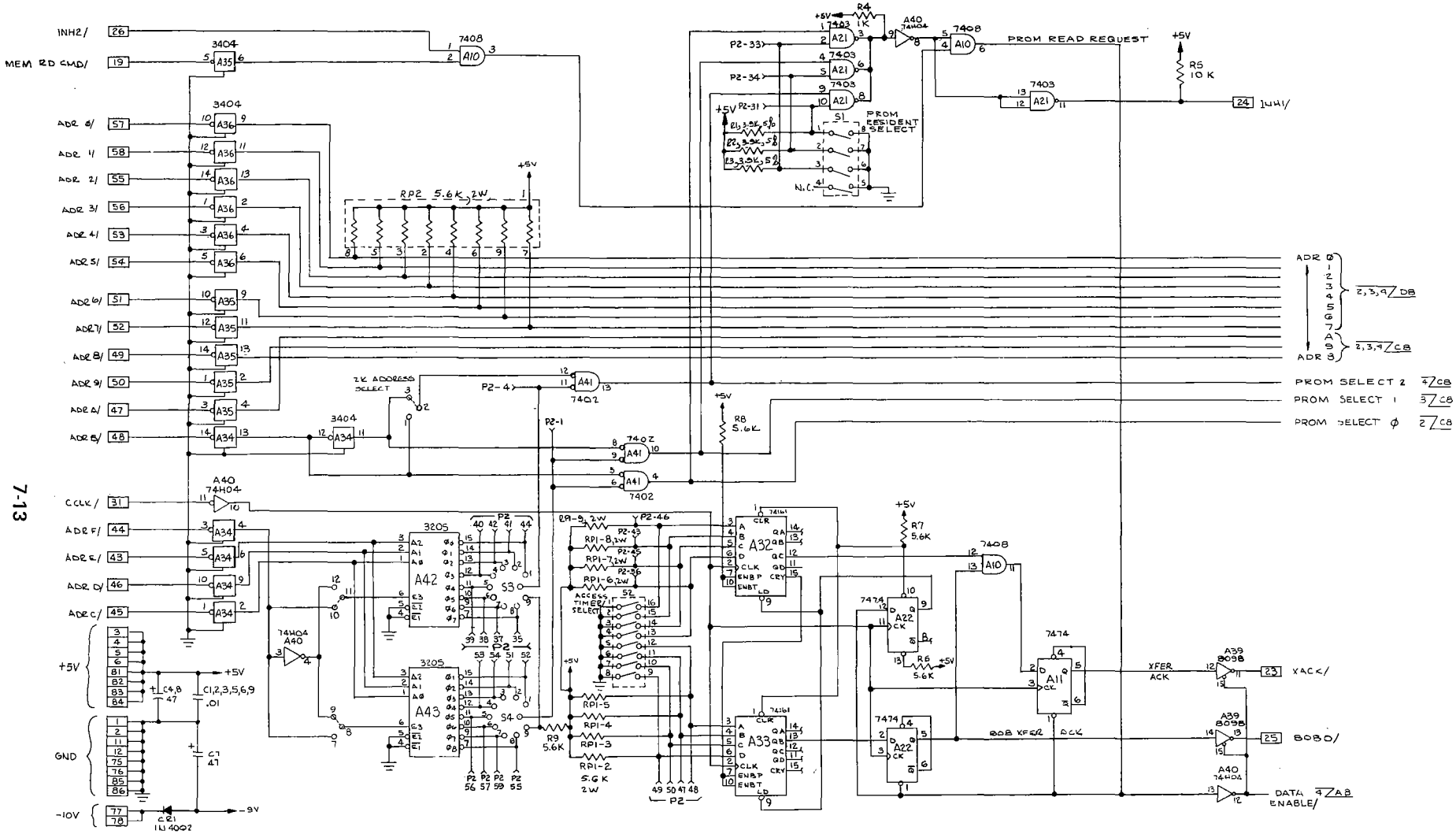


Figure 7-5. PROM Module Timing for 8702A-S714 PROMs (Access Time = 2.5 μs)



NOTE : UNLESS OTHERWISE SPECIFIED

1. ARTWORK REVISION LEVEL IS REV A
2. RESISTOR VALUES ARE IN OHMS, ± 10%, 1/4W.
3. CAPACITOR VALUES ARE IN MICROFARADS.
4. J4 JUMPERS INSTALLED WHEN MODULE USED AS -01, J1,2,3 AND 5 USED FOR TEST PURPOSES ONLY.
5. ALL 1702A PROMS ARE OPTIONAL ITEMS AND ARE SHOWN ON SCHEMATIC FOR CIRCUIT CONTINUITY ONLY. (REF 6K X 8 A1-A8, A12-A19, A23-A30) (REF 2K X 16 A12-A19, A23-A30)

Figure 7-6. PROM Module Schematic (Sheet 1 of 5)

intel © 1978	3065 BOWERS AVE. SANTA CLARA CALIF. 95051		
TITLE SCHEMATIC, PROM MEMORY MODULE			
SIZE D	DEPT 410	DRAWING NO. 2000315	REV B

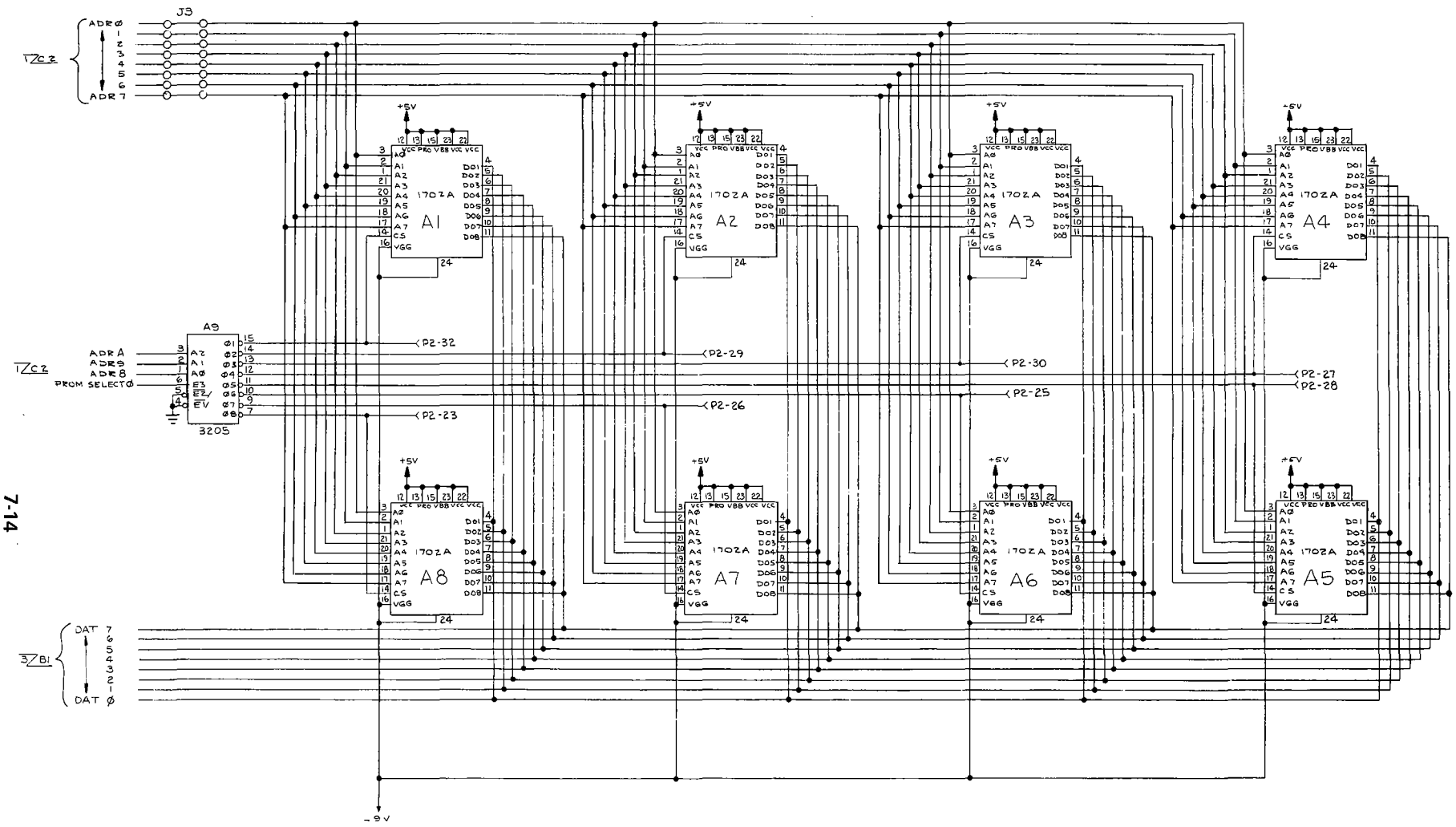


Figure 7-6. PROM Module Schematic (Sheet 2 of 5)

SCALE:	SIZE	DEPT	DRAWING NO.	REV
SHEET 2 OF 5	D	410	2000315	B

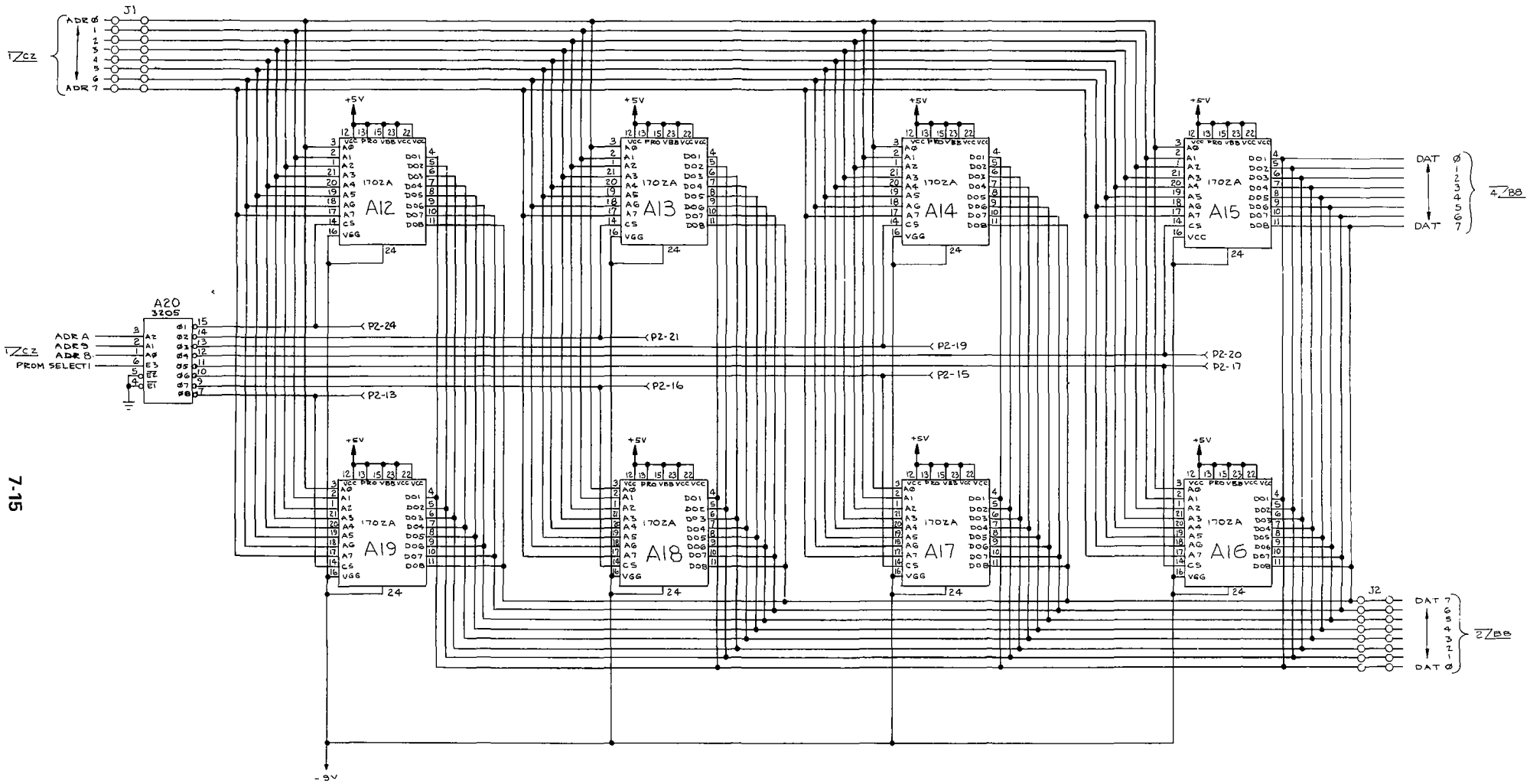


Figure 7-6. PROM Module Schematic (Sheet 3 of 5)

SCALE:	SIZE	DEPT	DRAWING NO.	REV
SHEET 3 OF 5	D	410	2000315	B

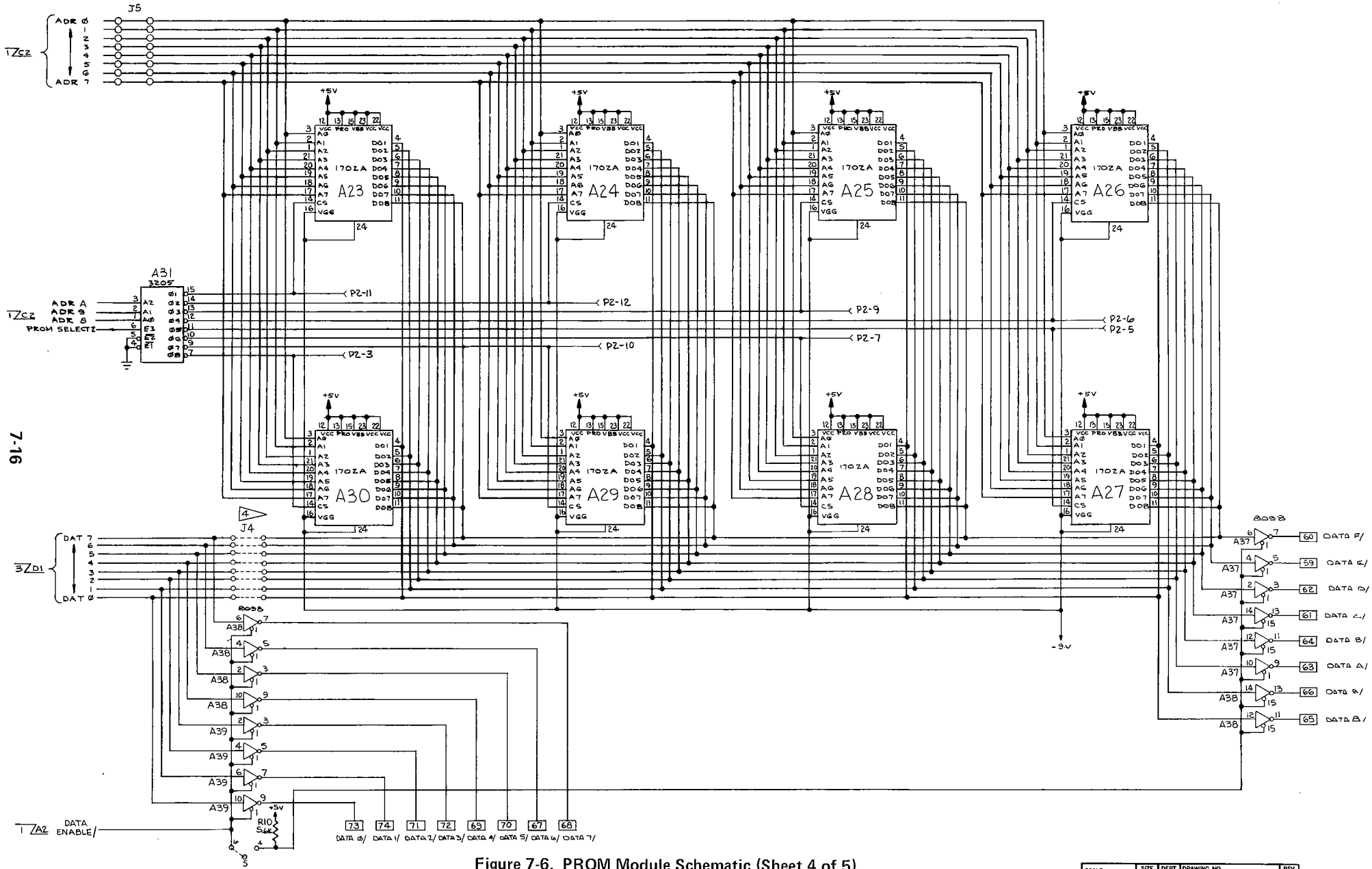


Figure 7-6. PROM Module Schematic (Sheet 4 of 5)

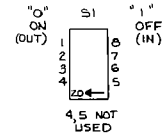
SCALE:	SIZE	DEPT	DRAWING NO.	REV
SHEET 4 OF 5	D	410	2000315	B

ADDRESS SWITCH POSITION TABLE

		4K BANK $X_1 + X_2$			2K BANK $Y_1 + Y_2$			
ADDRESS		X_1 (S4)	X_2	LOCATION	Y_1 (S3)	Y_2	2K BANK MOD	LOCATION
ØØØ	7FF	0	8-9	A1 - A8	0	11-12	2-1	A23 - A30
8ØØ	FFF	0	↑	A12 - A19	0	↑	2-3	↑
1ØØØ	17FF	1		A1 - A8	1		2-1	
18ØØ	1FFF	1		A12 - A19	1		2-3	
2ØØØ	27FF	2		A1 - A8	2		2-1	
28ØØ	2FFF	2		A12 - A19	2		2-3	
3ØØØ	37FF	3		A1 - A8	3		2-1	
38ØØ	3FFF	3		A12 - A19	3		2-3	
4ØØØ	47FF	4		A1 - A8	4		2-1	
48ØØ	4FFF	4		A12 - A19	4		2-3	
5ØØØ	57FF	5		A1 - A8	5		2-1	
58ØØ	5FFF	5		A12 - A19	5		2-3	
6ØØØ	67FF	6		A1 - A8	6		2-1	
68ØØ	6FFF	6		A12 - A19	6		2-3	
7ØØØ	77FF	7	↓	A1 - A8	7	↓	2-1	
78ØØ	7FFF	7	8-9	A12 - A19	7	11-12	2-3	
8ØØØ	87FF	0	8-7	A1 - A8	0	11-10	2-1	
88ØØ	8FFF	0	↑	A12 - A19	0	↑	2-3	
9ØØØ	97FF	1		A1 - A8	1		2-1	
98ØØ	9FFF	1		A12 - A19	1		2-3	
AØØØ	A7FF	2		A1 - A8	2		2-1	
A8ØØ	AFFF	2		A12 - A19	2		2-3	
BØØØ	B7FF	3		A1 - A8	3		2-1	
B8ØØ	BFFF	3		A12 - A19	3		2-3	
CØØØ	C7FF	4		A1 - A8	4		2-1	
C8ØØ	CFFF	4		A12 - A19	4		2-3	
DØØØ	D7FF	5		A1 - A8	5		2-1	
D8ØØ	DFFF	5		A12 - A19	5		2-3	
EØØØ	E7FF	6		A1 - A8	6		2-1	
E8ØØ	EFFF	6		A12 - A19	6		2-3	
FØØØ	F7FF	7		A1 - A8	7		2-1	
F8ØØ	FFFF	7	8-7	A12 - A19	7	11-10	2-3	A23 - A30

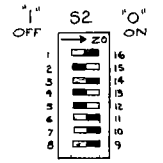
PROM RESIDENCY (S1)

BANK	LOCATION	SWITCH PIN NO.	1702A INSTALLATION	
			OUT	IN
2K	A23 - A30	1, 8	0	1
4K	A1 - A8	2, 7	0	1
	A12 - A19	3, 6	0	1



(S2) TIMING SWITCH SETTING TABLE

DEVICE	ACCESS TIME	1/16	2/15	3/14	4/13	5/12	6/11	7/10	8/9
1702A	1.0 US	0	1	0	1	1	0	0	0
1702A-S6I4	1.5 US	1	0	1	0	1	0	0	0
1702A-S3I4	1.7 US	0	0	1	0	1	0	0	0
1702A-S7I4	2.5 US	1	1	0	1	0	0	0	0



SETTING SHOWN IS FOR 1702A DEVICE

Figure 7-6. PROM Module Schematic (Sheet 5 of 5)

SCALE: —	SIZE	DEPT	DRAWING NO.	REV
SHEET 5 OF 5	D	410	2000315	B

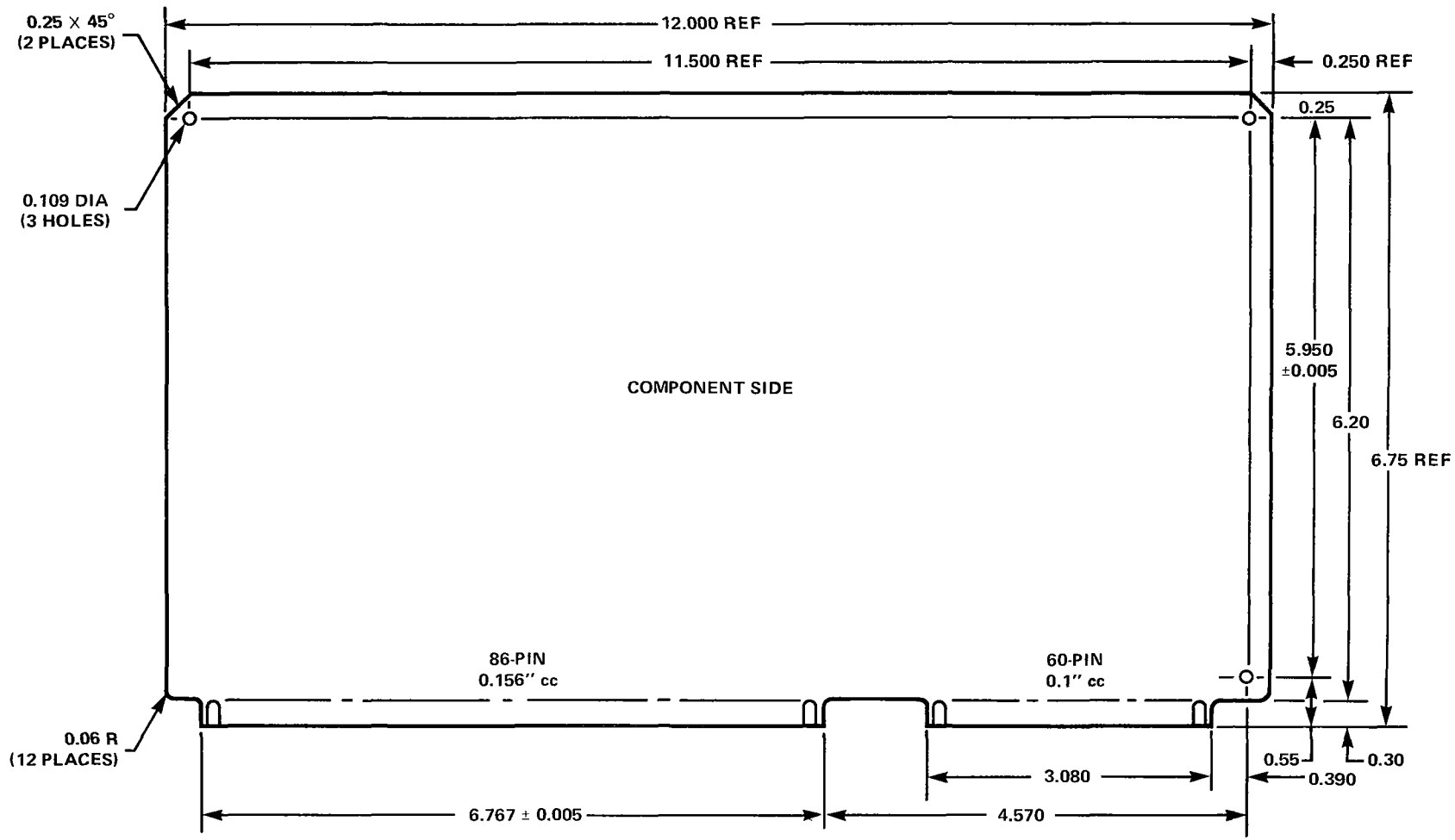


Figure 7-7. PROM Module Connectors

Signal Requirements

All data and control functions appearing at the module edge connectors are at TTL levels. Electrical characteristics of the signal inputs and outputs, as well as power inputs, are given in Section 7.4.

Signal descriptions and connector pin allocations are given in Section 7.3.2.

Address Assignments

The storage elements on the PROM Module are organized into a 4096 (4K) X 8-bit memory bank (16 PROM devices) and a 2048 (2K) X 8-bit memory bank (8 PROM devices).

The user must assign memory addresses to the 4K bank (if it is present) by:

- Setting the X1 switch (S4) to the appropriate position; and
- Joining the appropriate connections on the X2 jumper pad (7-8-9),

as defined in Table 7-1 (Section 7.2.2).

In addition, the PROM RESIDENT SELECT switch (S1) must be such that it reflects the PROM chip locations which are actually occupied, as described in Table 7-2 (Section 7.2.3).

Figure 7-8 illustrates the locations of the various switches and jumper pads on the PROM Module.

Access Timer Selection

There are several versions of the 8702A PROM device, with each version having a different access time. The PROM Module has been designed to operate with any one version. The user must, however, set the ACCESS TIMER SELECT switch (S2) on the PROM Module (see Figure 7-8) as defined in Table 7-3 (Section 7.2.3). The ACCESS TIMER SELECT switch dictates timing of the acknowledge signals, XACK/ and 8080/.

Byte Selection

The PROM Module can be used to store 8 or 16-bit words. The module can provide a maximum capability of 6,144 (6K) X 8-bit words (using 24 PROM's) or 2048 (2K) X 16-bit words (using 16 PROM's).

If 16-bit storage is required, the user must assign the same addresses to the 2048 locations in the 4K memory bank (8 PROMs) as are assigned to the 2K memory bank (also 8 PROMs) as explained in Section 7.2.2 (Table 7-1). In addition, jumper points 4-6 should be connected to provide a pathway via which the DATA ENABLE/ signal can enable the eight 8098 TRI STATE hex inverters that drive the high-order byte of the 16-bit word (from the 2K memory bank) on the data bus (DAT8/–DATF/). Because the high-order byte from the 2K memory bank is being driven on data lines DAT8/–DATF/, there is no need for maintaining a data path between the 2K memory bank and the low-order data lines DATØ/–DAT7/. The low-order byte from the 4K memory bank is driven on these low-order data lines. Consequently, the eight-pair jumper pad, J4, should be removed in 16-bit configurations. The DATA ENABLE/ and the J4 jumper connections are shown on sheet 4 of the module schematic, Figure 7-6.

7.3.2 PIN LISTS: PROM MODULE

The following section provides connector pin allocations for the PROM Module. The pins and their designated signal functions for the 86-pin connector (P1) are listed in Table 7-4. The same information for the 60-pin auxiliary connector (P2) is listed in Table 7-5.

7.4 OPERATING CHARACTERISTICS: PROM MODULE

This section provides detailed information concerning the AC and DC characteristics of the PROM Module.

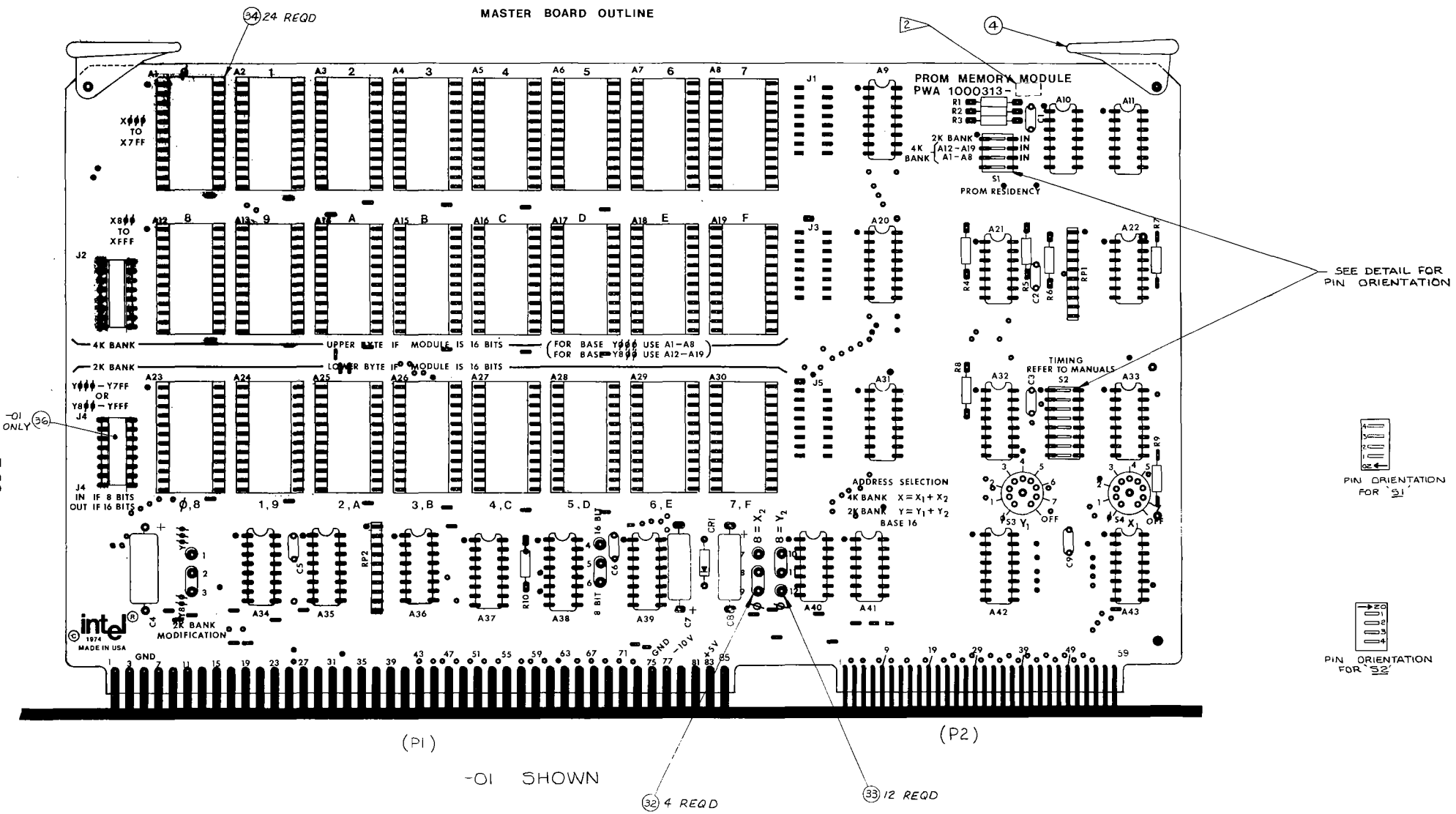
7.4.1 AC CHARACTERISTICS

The AC characteristics of the PROM Module are summarized in Figure 7-9.

7.4.2 DC CHARACTERISTICS

The DC characteristics of the PROM Module are summarized in Table 7-6. Power requirements are cited below:

	TYP	MAX
V_{CC} +5 VDC ±5%	1.54A	2.54A
V_{BB} -10 VDC ±5%	0.84A	1.45A



NOTE: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY NO. IS 1000313-XX

2 MARK DASH NO. IN POSITION SHOWN.

Figure 7-8. PROM Module Assembly Drawing

intel	3065 BOWERS AVE SANTA CLARA CALIF 95051	
TITLE: PRINTED WIRING ASSEMBLY PROM MEMORY MODULE		
SIZE D	PART NO. 410	DRAWING NO. 1000313
REV C		

Table 7-4

P1 CONNECTOR PIN LIST

PIN	SIGNAL	FUNCTION
1	GND	Ground
2	GND	
3	+5 VDC	Power inputs
4	+5 VDC	
5	+5 VDC	
6	+5 VDC	
7		
8		
9		
10		
11	GND	Ground
12	GND	
13		
14		
15		
16		
17		
18		
19	MRDC/	Memory read command
20		
21		
22		
23	XACK/	Acknowledge transfer
24	INH1/	Inhibit RAM
25	AACK/	Advance acknowledge
26	INH2/	Inhibit ROM
27		
28		
29		
30		
31	CCLK/	Common clock (9,8304 MHz)
32		
33		
34		
35		
36		
37		
38		
39		
40		
41		
42		
43	ADRE/	Address bus

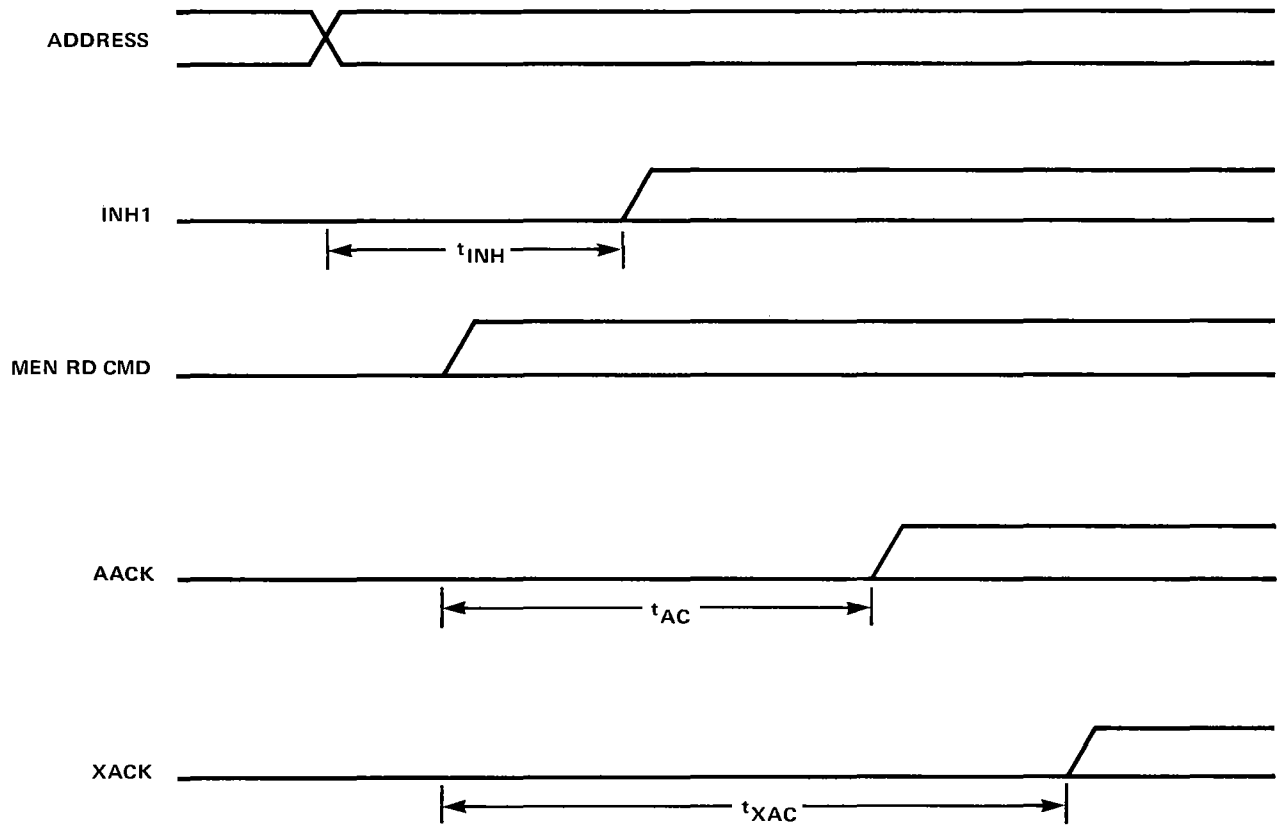
PIN	SIGNAL	FUNCTION
44	ADRF/	Address bus
45	ADRC/	
46	ADRD/	
47	ADRA/	
48	ADRB/	
49	ADR8/	
50	ADR9/	
51	ADR6/	
52	ADR7/	
53	ADR4/	
54	ADR5/	
55	ADR2/	
56	ADR3/	
57	ADRØ/	
58	ADR1/	
59	DATE/	Data bus
60	DARF/	
61	DATC/	
62	DATD/	
63	DATA/	
64	DATB/	
65	DAT8/	
66	DAT9/	
67	DAT6/	
68	DAT7/	
69	DAT4/	
70	DAT5/	
71	DAT2/	
72	DAT3/	
73	DATØ/	
74	DAT1/	
75	GND	Ground
76	GND	
77	-10 VDC	Power inputs
78	-10 VDC	
79		
80		
81	+5 VDC	Power inputs
82	+5 VDC	
83	+5 VDC	
84	+5 VDC	
85	GND	Ground
86	GND	

Table 7-5

P2 CONNECTOR PIN LIST (TEST POINTS)

PIN	SIGNAL*	FUNCTION	PIN	SIGNAL	FUNCTION
1	S4-10		31	S1-1	
2			32	CSA1	
3	CSA30		33	S1-3	
4	S3-10		34	S1-2	
5	CSA27		35	S3-8	
6	CSA26		36	S2-13	
7	CSA28		37	S3-7	
8			38	S3-6	
9	CSA25		39	S3-5	
10	CSA29		40	S3-4	
11	CSA23		41	S3-2	
12	CSA24		42	S3-4	
13	CSA19		43	S2-15	
14			44	S3-1	
15	CSA17		45	S2-14	
16	CSA18		46	S2-16	
17	CSA16		47	S2-11	
18			48	S2-12	
19	CSA14		49	S2-9	
20	CSA15	TEST POINTS	50	S2-10	
21	CSA13		51	S4-2	TEST POINTS
22			52	S4-1	
23	CSA23		53	S4-4	
24	CSA12		54	S4-3	
25	CSA6		55	S4-8	
26	CSA7		56	S4-3	
27	CSA4		57	S4-6	
28	CSA5		58		
29	CSA2		59	S4-7	
30	CSA3		60		

*Designations refer to devices shown on the schematic. For example, pin 40 lists S3-4 which refers to position 4 on switch S3, shown on sheet 1 of the module schematic.



		8702A	8702A-S614	8702A-S314	8702A-S714
INH1	t_{INH}	102 ns	102 ns	102 ns	102 ns
AACK	t_{AC}	700 ns	1.2 µs	1.3 µs	2.3 µs
XACK	t_{XAL}	1.1 µs	1.6 µs	1.7 µs	2.8 µs

Figure 7-9. AC Characteristics of the PROM Module

Table 7-6

DC CHARACTERISTICS OF THE PROM MODULE

SIGNALS (DEVICE)	PARAMETERS	MIN.	MAX.	UNIT	TEST CONDITIONS
ADR0/–ADRF/	V_{IL}-Input low voltage		0.85	V	V_{CC} = 5.0V
RD CMD/	V_{IH}-Input high voltage	2.0		V	V_{CC} = 5.0V
(3404)	I_R-Input leakage current		10	μA	$V_{CC} = V_R$ = 5.25V
	I_F-Input load current		–0.25	mA	V_{CC} = 5.25, V_R = 0.45V
INH2/	V_{IL}-Input low voltage		0.8	V	
(7408)	V_{IH}-Input high voltage	2.0		V	
	I_R-Input leakage current		1	mA	V_{CC} = 5.25V, V_R = 5.5V
	I_F-Input load current		–1.6	mA	V_{CC} = 5.25V
INH1/	V_{OL}-Low level output voltage		0.4	V	V_{CC} = 4.75V, V_{IH} = 2V,
(7403)	V_{OH}-High level output voltage		*		I_{OL} = 16 mA
XACK/	V_{OL}-Low level output voltage		0.4	V	V_{CC}= 4.5V, I_{OL} = 32 mA
AACK/	V_{OH}-High level output voltage	2.4		μA	V_{CC} = 4.5V, I_{OH} = –5.2 mA
DATØ/–DATF/	I_{LH}- Input current at high voltage		–40	μA	V_{CC} = 5.25V, High Z, V_R = 0.5, DIS = 2.0V
(8093)	I_{LL}-Input current at low voltage		40	μA	V_{CC} = 5.25V, High Z, V_0 = 2.4V
CCLK/	V_{IL}-Input low voltage	2		V	V_{CC} = 5.25V
(74H04)	V_{IH}-Input high voltage		0.8	V	V_{CC} = 5.0V
	I_R-Input leakage current		1	mA	V_{CC} = 5.25V, V_I = 5.5V
	I_F-Input load current		–2.0	mA	V_{CC} = 5.25V, V_{IL} = 0.4V

*Open connector 10K P.U.