Chapter 5
MONITOR MODULE

The Monitor Module has been designed specifically to provide the INTELLEC MDS System with firmware-storage for the Monitor program (2K words), and I/O interfaces to the following peripheral devices:

- Teletype (TTY) including paper tape reader
- Cathode Ray Tube (CRT) terminal or other compatible device (TTL or RS232 interfaces are jumper selectable)
- High-Speed Paper Tape Reader and Punch
- Line Printer
- PROM Programmer

The Monitor Module is not, however, confined to use as a component only within the INTELLEC MDS System. The general-purpose design of the interface logic for the read-only-memory, and the fact that the read-only-memory can store 2048 8-bit or 16-bit words (by including an additional 8316 ROM on the module), allow it to store the monitor program for almost any 8-bit or 16-bit computer system. In addition, the powerful, general-purpose design of the I/O interfaces makes the Monitor Module an ideal, low-cost component for most computer systems that rely on TTY, CRT, paper tape, and/or line printer devices for input/output.

Most control and status information, as well as all data flow, that is transferred to/from the I/O interfaces on the Monitor Module proceeds via the system data bus. The different devices and types of transfer (i.e., control output, status input or data I/O) are uniquely identified by dedicated I/O addresses (carried on the separate address bus) and two I/O commands (I/O read or I/O write); thus making the Monitor Module extremely easy to incorporate into almost any computer system. Consequently, Intel has made the Monitor Module, like all other INTELLEC modules, available independently on an OEM basis.

As a stand-alone product, the Monitor Module is almost entirely self-contained. It requires only DC power, at levels of +5, +12, and −10 VDC.

All circuitry is mounted on a single, 12-in. × 6.75-in. printed circuit board. Power and most signal connections enter the module through an 86-pin, double-sided edge connector (0.156-in. center). An auxiliary 60-pin, double-sided edge connectors (0.1-in. centers) is also present for use at the designer's discretion. All communication with the peripheral I/O devices proceeds through a 100-pin, double-sided edge connector (0.1-in. centers) on top of the Monitor Module.

5.1 FUNCTIONAL ORGANIZATION OF THE MONITOR MODULE

To facilitate describing the operation of the Monitor Module, we have divided the module's logic into 11 functional units, as shown in Figure 5-1:

(1) Monitor ROM
(2) I/O Command Decode Logic
(3) Command Strobe/Transfer Acknowledge Logic
(4) USART Clock Generator Logic
(5) CRT Interface
(6) Teletype (TTY) Interface
(7) High-Speed Paper Tape Reader/Punch Interface
(8) PROM Programmer Interface
(9) Line Printer Interface
(10) Monitor Interrupt Logic
(11) Bidirectional Data Bus Driver

The Monitor Module can include 2048 × 8-bit words of read-only-memory (ROM) for storage of the system monitor program in minimum 8-bit system configurations. The *Monitor ROM* responds to addresses $F8ØØ_{16}$ to $FFFF_{16}$ when enabled by a switch on the module.

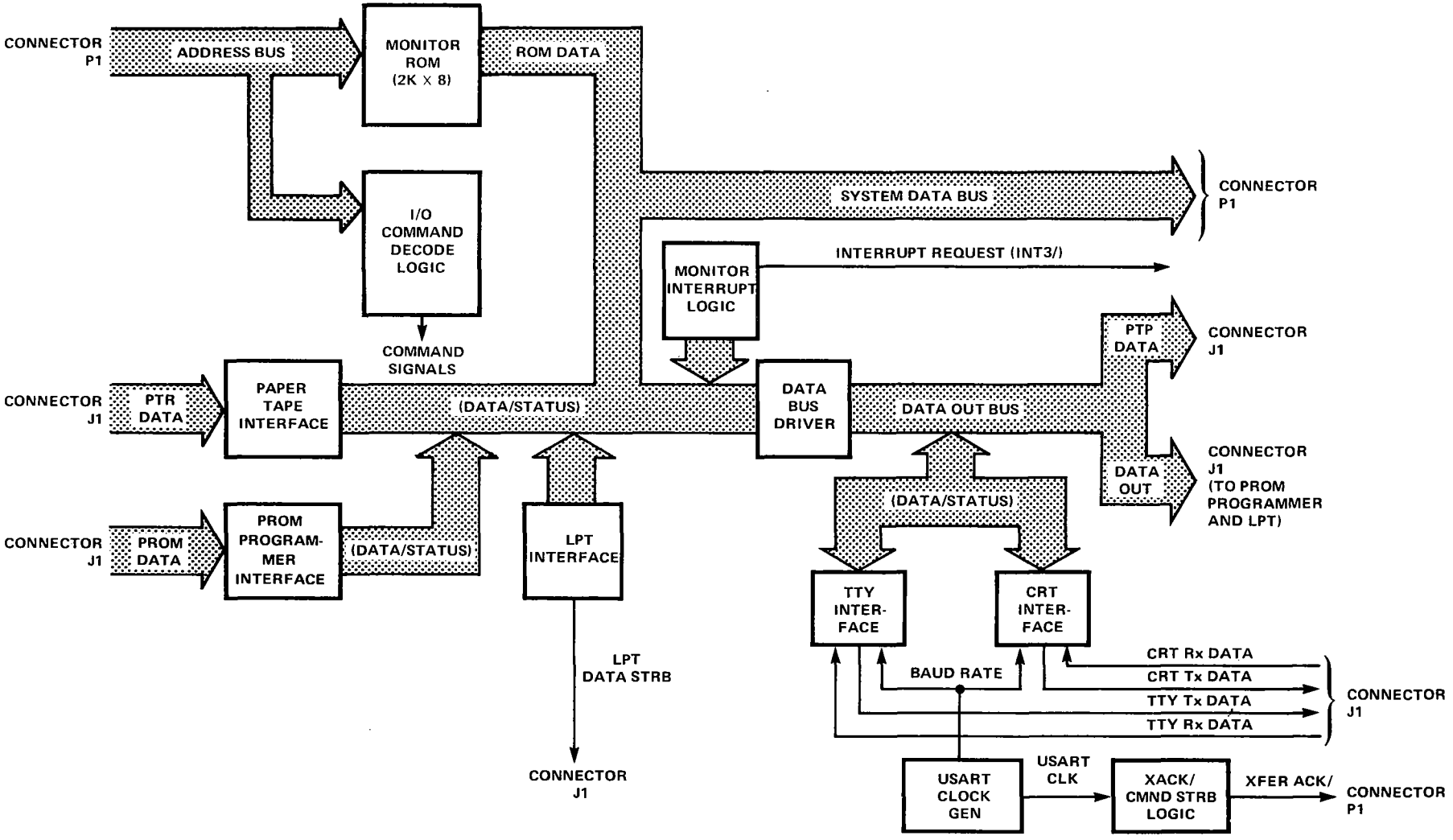


Figure 5-1. Monitor Module Functional Organization and Data Flow

The various peripheral interfaces on the Monitor Module control the transfer of data, control, and status information between their associated I/O devices and a Central Processor (CPU) Module. The CPU module specifies the I/O device to be accessed and the type of transfer to be performed (i.e., data, control, or status) by executing an I/O instruction to a particular I/O port. The *I/O command decode logic* accepts the I/O read or write command and eight address bits, and generates the appropriate signal, specifying the device and the type of transfer.

The *command strobe/transfer acknowledge logic*, as its name implies, is responsible for generating the CMND STRB and XFER ACK/ signals. CMND STRB is used to gate various control signals to a line printer or a PROM Programmer peripheral. XFER ACK/ informs the CPU that output data has been accepted or that input data has been placed on the data lines.

The CRT and TTY interfaces are implemented with 8251 USART chips. The *USART clock generator logic* includes a soldered jumper pad scheme for selecting a variety of USART baud rates. The USART clock generator logic also provides a timing reference pulse (USART CLK) to the command strobe/transfer acknowledge logic, as well as to the CRT and TTY interfaces.

The *CRT interface* provides a variable-speed, parallel-serial, asynchronous communications interface for use with compatible keyboard and cathode ray tube (CRT) display peripherals. The functional specifications are:

- Direction – input and output
- Baud rate – 110/300/600/1200/400/4800/ 9600 baud (selectable)
- Code format – 7 through 12 level code (programmable)
- Parity – odd/even (programmable)
- Interface – TTL/RS232 (selectable)

The *TTY interface* provides an incremental, asynchronous parallel-serial interface to a teletype and its associated paper tape reader. The functional specifications are:

- Baud rate – 110 baud
- Code format – standard output: 11 level code; standard input: 10 level (7 through 12 level code, programmable)
- Parity – odd
- Drive – output: 20 mA current loop; input: 12 VDC

The *high-speed paper tape reader/punch interface* provides an 8-bit data input path, two command bit outputs and a single ready status input for a 200 CPS paper tape reader, and an 8-bit data output path, two command bit outputs and a single ready status input for a 75 CPS paper tape punch. Either device can be advanced or reversed one character, using the two command bit outputs.

The *PROM Programmer interface* provides an 8-bit path to a PROM Programmer peripheral for the transfer of data, address, control and status information. The PROM interface also presents the necessary commands to the PROM Programming peripheral, specifying the direction and the type of transfer that is to occur.

The *line printer interface* has been designed to operate with printers which are capable of receiving input commands as coded ASCII characters in the same manner as data. A ready status input must be provided by the printer electronics and sensed by the Monitor Module on one of the two status inputs. The line printer interface also includes a data strobe (LPT DAT STRB/) line to the printer.

The *Monitor interrupt logic* provides a hardware scheme that can be utilized by a user-generated operating system or specialized application routine to service TTY, CRT, paper tape reader, paper tape punch, or line printer devices on an interrupt basis. Each time that a device indicates that it is ready, the appropriate service request signal is generated. The service request lines form a 7-bit interrupt status word which can be read by the CPU. In addition, if Monitor Module interrupts are enabled, an active service request results in an interrupt request to the CPU on level 3.

Monitor Module interrupts can be enabled or disabled, and device service requests can be reset individually or as a group by executing a single output instruction.

The *bidirectional data bus driver* directs data flow to/from the system bus on the motherboard (via connector P1), and directs data outputs to the paper tape punch bus and the data out bus (both via connector J1).

5.2 MONITOR MODULE: THEORY OF OPERATION

The following sub-sections provide a complete description of the theory of operation for each of the functional units on the Monitor Module.

The Monitor Module accepts/transmits signals, data and power through three different PC edge connectors:

- J1 Peripheral connector (to/from I/O peripherals)
- P1 Bus connector (to/from the system bus)
- P2 Auxiliary connector (to/from the auxiliary bus)

To avoid any ambiguity when referring to connector pins in subsequent paragraphs, we will always list the connector as well as the pin whenever such references are required; for example, P1-14 refers to pin 14 on connector P1. Pin lists for the three connectors are provided in Section 5.3.2.

The schematic (3 sheets) for the Monitor Module is provided in Figure 5-18, located in Section 5.2.12.

5.2.1 MONITOR ROM

The Monitor ROM and associated logic consists of a 3205 three-to-eight decoder, two 2048 X 8-bit read-only-memory (ROM) chips (only one ROM is present in 8-bit systems, like an INTELLEC MDS using an 8080 CPU module), and various drivers and gating circuits, as shown on sheet 1 of the module schematic, Figure 5-18.

The three most significant address lines (ADRD/–ADRF/) are applied to the three A inputs of the decoder. The three decoder enable inputs are provided by the two next most significant address lines (ADRB/ and ADRC/) and the inhibit ROM signal (INH2/). When active, INH2/ prevents the Monitor ROM from being addressed. In the standard system, the Oϕ decoder output is applied to one of the two inputs of a 7426 NAND gate. Oϕ is true when INH2/ is false and the address lines specify a value of F8ØØ$_{16}$ or greater. The other input to the 7426 NAND gate is supplied by the EN ROM switch on the printed circuit board. When active, the 7426 section's open collector output asserts the inhibit RAM signal (INH1/) on the system bus (pin P1-24). INH1/ prevents RAM locations from responding to addresses meant for the Monitor ROM.

The EN ROM switch input, the decoder output (Oϕ) and the memory read command (MRDC) are gated together in a 7410 NAND section. The output of the 7410 feeds the command strobe/transfer acknowledge logic (see Section 5.2.3), and enables the 8316 ROM(s) that store the Monitor program and the eight (or 16) 8098 inverting driver circuits that enable data onto the system data bus.

The 11 least significant address lines (ADRØ/–ADRA/) are applied to the address inputs of the 2048 X 8-bit ROM(s). The data outputs are applied to the 8098 circuits which, when enabled, drive the data bus (DATØ/–DAT7/ or DATF/).

5.2.2 I/O COMMAND DECODE LOGIC

The CPU will specify the type of I/O transfer to be performed (i.e., data, control or status transfer), as well as the particular device to be accessed by executing an I/O read or I/O write instruction directed to an I/O port with an address between FØ$_{16}$ and FB$_{16}$ (inclusive). The I/O command decode logic generates the appropriate command signal after examining the I/O command from the CPU (IORC/ or IOWC/) and the port address.

The I/O command decode logic consists of three 3205 three-to-eight decoders and assorted gating circuits, as shown on sheet 1 of the module schematic, Figure 5-18.

During the execution of I/O instructions, the 8080 CPU duplicates the 8-bit port address on the high-order eight address lines and on the low-order eight address lines. The I/O command decode logic interrogates the eight low-order address bits (ADRØ/–ADR7/). Address lines ADR5/, ADR6/, and ADR7/

are applied to the inputs of one of the 3205 decoders; ADR4/ is applied to one of the negative chip enable inputs. Consequently, the decoder output of Oϕ is true only when a port address of F$\emptyset_{16}$ or greater is present on the address lines. This Oϕ output is fed to chip enable inputs on the other two 3205 decoders; as well as to various gates in the I/O command decode logic. These gates and decoders interrogate address lines ADR$\emptyset$/–ADR3/ in conjunction with the two I/O commands, I/O read (IORC/) and I/O write (IOWC/).

Because the logic in this section is relatively easy to decipher by merely examining the schematic drawing, we will not verbally step through each gate and decoder. Instead, we have summarized in Table 5-1 the command signals which are generated as a result of each possible combination of port address and I/O command. The I/O command decode logic is not referred to a clock pulse; the appropriate command signal is generated whenever the corresponding port address and I/O command are received by the I/O command decode logic. Conversely, the command signal goes false whenever the CPU removes the address or the I/O command.

5.2.3 COMMAND STROBE/TRANSFER ACKNOWLEDGE LOGIC

The command strobe/transfer acknowledge (CMND STRB/XFER ACK) logic consists of a 74193 up/down counter, two 7474 D-type flip-flops, and assorted gating circuits as shown on sheet 1 of the module schematic, Figure 5-18.

Timing for the CMND STRB/XFER ACK logic is provided by the USART CLK signal generated in the USART clock generation logic (see Section 5.2.4). USART CLK is applied to the clock input of a 7474 flip-flop. The Q output of this 7474 section enables the up-count-pulse that sequences the 74193 up/down counter during Monitor Module operations. When the Monitor Module is inactive (i.e., when the system is not accessing the resident monitor or one of resident I/O interfaces), the 7474 section remains pre-set and the load input to the 74193 counter remains true, forcing the following output from the counter: QA=1, QB=0, QC=0, QD=1.

This load input, however, goes false and the 7474 flip-flop that provides sequencing pulses is enabled, whenever one of the following events occur:

- The Monitor ROM is being accessed *or*
- An I/O read or write instruction to an I/O port with an address between F$\emptyset_{16}$ and FB$_{16}$ (inclusive) is being executed, but data is *not* being read from the PROM Programmer (see the next to last paragraph of this section).

  NOTE: I/O ports with addresses between F$\emptyset_{16}$ and FB$_{16}$ are dedicated to peripherals which are controlled by logic on the Monitor Module (see the description of the I/O command decode logic in Section 5.2.2).

When one of the aforementioned conditions is indicated, the 74193 counter begins sequencing. With each up-count-pulse (i.e., every 406.9 ns), the binary value represented by the four counter outputs is incremented by one. The count is initially set to 9_{10} (1001), essentially disabling the CMND STRB/XFER ACK logic. The sequencing which follows as a result of each up-count-pulse, however, is different for cycles in which the PROM Programmer is accessed or data is output to a line printer, than it is for Monitor ROM read operations and all other I/O operations. The CMND STRB signal is only used in the former case (see Sections 5.2.8 and 5.2.9). Consequently we will deal with the two cases separately.

Output to Line Printer or PROM Programmer

The third up-count-pulse to the counter (output= 1100) activates the QC output which removes the reset input to a second 7474 flip-flop. The combinations of QC=1 from the counter and $\overline{Q}$=1 from the 7474 flip-flop, enables a 7400 NAND gate which generates CMND STRB. CMND STRB is used to gate out command signals to the PROM Programmer peripheral or a line printer. During data output operations to the PROM or line printer peripherals, the fifth up-count-pulse (output= 1110) causes the QB output to go high again. Because QC is also high, the leading edge of QB clocks the 7474 flip-flop (A15-3) set. The $\overline{Q}$ output of this flip-flop disables the 7400 gate at which CMND STRB originates. The seventh up-count-

Table 5-1

I/O COMMAND LOGIC

PORT ADDRESS (HEXADECIMAL)	I/O COMMAND	COMMAND SIGNAL (SOURCE)	FUNCTION
FØ	IOWC/	PROM WRT DATA (A19-2)	Enable data output pulse to PROM Programmer
F1	IOWC/	PROM ADR HIGH-CTL (A19-4)	Enable control pulse to PROM Programmer
F2	IOWC/	PROM ADR LOW (A19-6)	Enable address pulse to PROM Programmer
F3	IOWC/	INT CTL/ (A32-12)	Clock data bit 7 into Monitor interrupt enable/ disable flip-flop and reset interrupts for those devices specified by data bits 0–6.
F8	IOWC/	PTP DAT/ (A32-11)	Enable and latch data output (8 bits) to paper tape punch
F9	IOWC/	PT CTL/ (A32-10)	Enable control bits (data bits 2, 3, 4, or 5) to paper tape reader/punch or data bit 1 to TTY
FA	IOWC/	LPT DAT/ (A32-9)	Enable data strobe to line printer
FB	IOWC/	LPT CTL/ (A32-7)	Enable control bits (data bits 0 or 1) to line printer (not used with standard line printer)
FØ, F1, F2 or FA	IOWC/	DELAY XFER ACK (A18-6)	Indicates output to PROM Programmer or line printer (which require a longer I/O write cycle)
FØ or F1	IORC/	EN PROM RD DATA/ (A58-8)	Indicates data or status input from PROM Programmer
FØ	IORC/	PROM RD DATA (A19-12)	Read data command to PROM Programmer
F1	IORC/	PROM RD STATUS (A19-10)	Read status command to PROM Programmer
F8	IORC/	PTR DATA/ (A33-11)	Enable data from paper tape reader
F9	IORC/	PR STAT/ (A33-10)	Enable status word from paper reader/punch
FA	IORC/	INT STAT/ (A33-9)	Enables interrupt status word onto data bus
FB	IORC/	LTP STAT/ (A33-7)	Enables status bits (data bits 0 and 1) from line printer onto data bus (bit 1 is not used with standard line printer)
F7, F6, F5 or F4	———	CRT OR TTY/ (A50-12)	Indicates that CRT or TTY is to be accessed.
F5 or F4	———	TTY EN/Q (A20-6)	Enables USART for TTY
F6 or F7	———	CRT EN/ (A20-11)	Enables USART for CRT

pulse (output=0111) causes the QD output to go low, enabling a 7408 negative-input NOR gate. The output of this 7408 section is gated through to an 8093 non-inverting driver which asserts XFER ACK/ on the system bus (pin P1-23). The high-to-low transition on the counter's QD output disables the up-count-pulse, thus "freezing" the CMND STRB/XFER ACK logic until the I/O write command (IOWC/) is withdrawn by the CPU. When IOWC/ goes false, the counter's internal state is again pre-set to 9_{10} (1001), thus resetting the CMND STRB/XFER ACK logic.

Monitor ROM Read and All Other I/O Operations

The operation of the CMND STRB/XFER ACK logic proceeds somewhat differently when the specified I/O operation is not a data transfer to a line printer or the PROM Programmer. The third up-count-pulse to the counter causes the QC output to go high, as previously described. In this case, however, the high level on the QC line activates the 7400 gate at A28-5. The other input to this gate (A28-4) will be high if data is not being output to the PROM Programmer or a line printer. The output of this active 7400 section is gated through to pin P1-23 and constitutes an active level on the XFER ACK/ line. Thus, XFER ACK/ occurs 1.628 μs earlier than in the line printer-PROM Programmer case. XFER ACK/ informs the CPU that the Monitor Module has responded to the I/O command. The active output of the 7400 gate also disables the up-count-pulse to the counter, thus freezing the CMND STRB/XFER ACK logic, 1.628 μs sooner than previously described. The XFER ACK/ line will remain active until the I/O read (IORC/) or I/O write (IOWC/) command signal is removed by the CPU.

Actually one other special case exists. The XFER ACK/ signal for cycles in which data is read from the PROM Programmer is not generated on the Monitor Module. The PROM RD ACK/ signal is received at pin J1-10 and gated through to the XFER ACK/ output at pin P1-23.

Timing for the CMND STRB/XFER ACK logic is shown in Figures 5-2 and 5-3.

5.2.4 USART CLOCK GENERATOR LOGIC

Using the 9.8304 MHz CCLK/ clock input, the USART clock generator logic develops the timing reference for its selectable CRT/TTY baud rate network, as well as the USART CLK pulse used by the command strobe/transfer acknowledge logic (see Section 5.2.3). The USART clock generator logic consists of two 7493A binary counters, two 74109 J-$\overline{K}$ flip-flops, two 74161 synchronous counters, a jumper pad for baud rate selection and various gating circuits, as shown on sheet 2 of the module schematic, Figure 5-18.

The CCLK/ pulse (period=101.725 ns) is received at pin P1-31, inverted and applied to the B input of the first 7493A counter. The QD output is tied to the A input. Consequently, the QC output looks like the output from a divide-by-four counter. The resultant signal, USART CLK, has a period that is four times that of the CCLK/ input (i.e., USART CLK period=406.9 ns), as shown in Figure 5-4. USART CLK provides a timing reference for the command strobe/transfer acknowledge logic (Section 5.2.3), as well as for the CRT interface (USART pin 20 – see Section 5.2.5) and TTY interface (USART pin 20 – see Section 5.2.6).

The QA counter output divides the CCLK/ input by 16 (i.e., QA output period=1.627 μs). This 1.627-μs square-wave signal is applied to baud rate jumper connection 26 (allowing a selectable baud rate of 38,200 baud). The 1.6-μs clock is also fed into the A input of the second 7493A counter. The QA output is tied to the B input. Consequently, QA provides a divide-by-two output, QB a divide-by-four output, QC a divide-by-eight output, and QD a divide-by-sixteen output. QA, QB, QC, and QD are applied to baud rate jumper connections 24, 20, 18 and 22, respectively (allowing selectable baud rates of 19,200, 9600, 4800 and 2400). The QD output also clocks a 74109 J-$\overline{K}$ flip-flop, causing it to toggle and further divide the QD output by two. The Q output from this J-$\overline{K}$ section is applied to baud rate jumper connection 14, allowing a selectable baud rate of 1200 baud. This Q output is also available at pin P2-38 on the auxiliary connector. Table 5-2 lists all of the selectable baud rates with the corresponding jumper connections that enable a particular rate. Notice that the

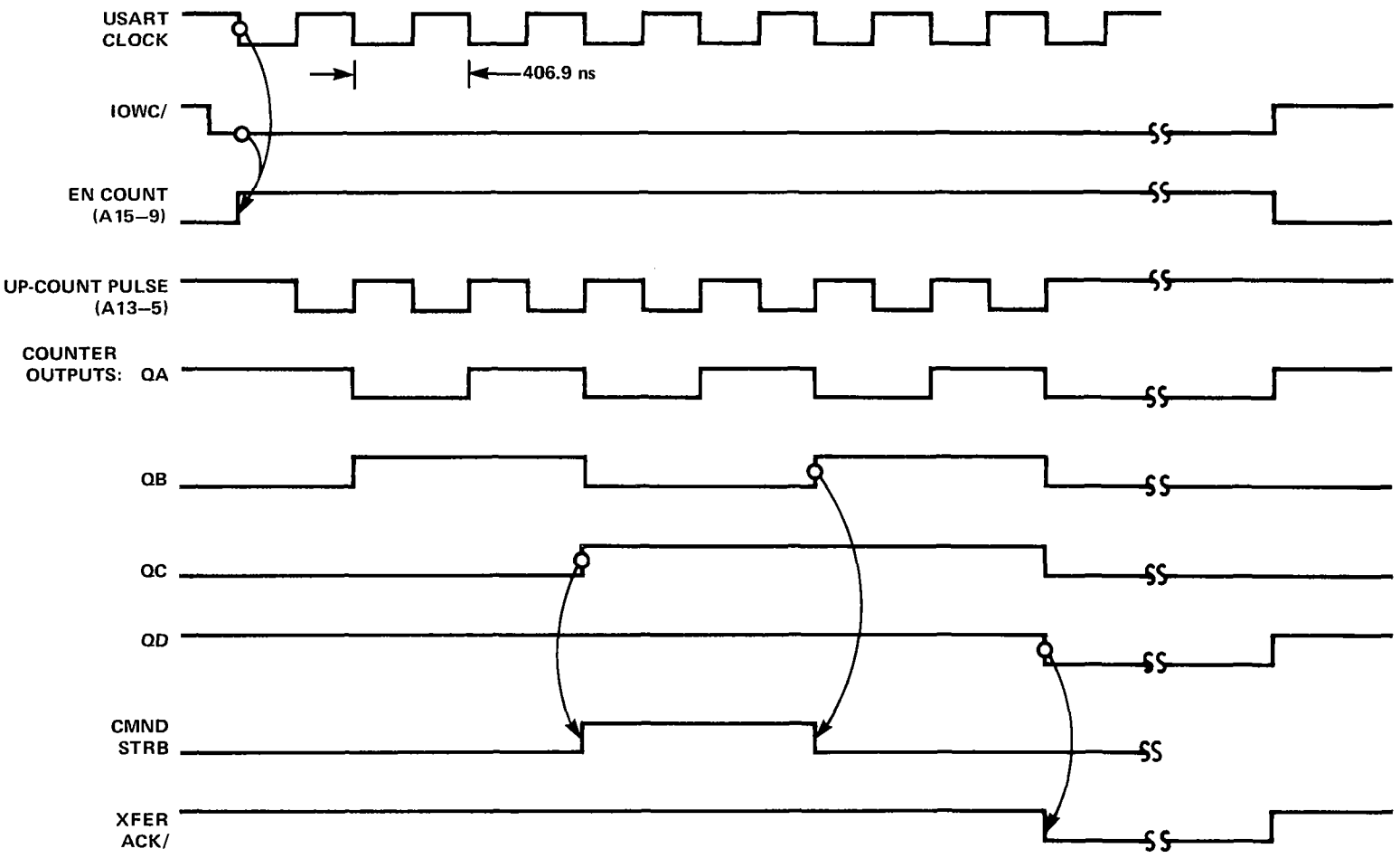
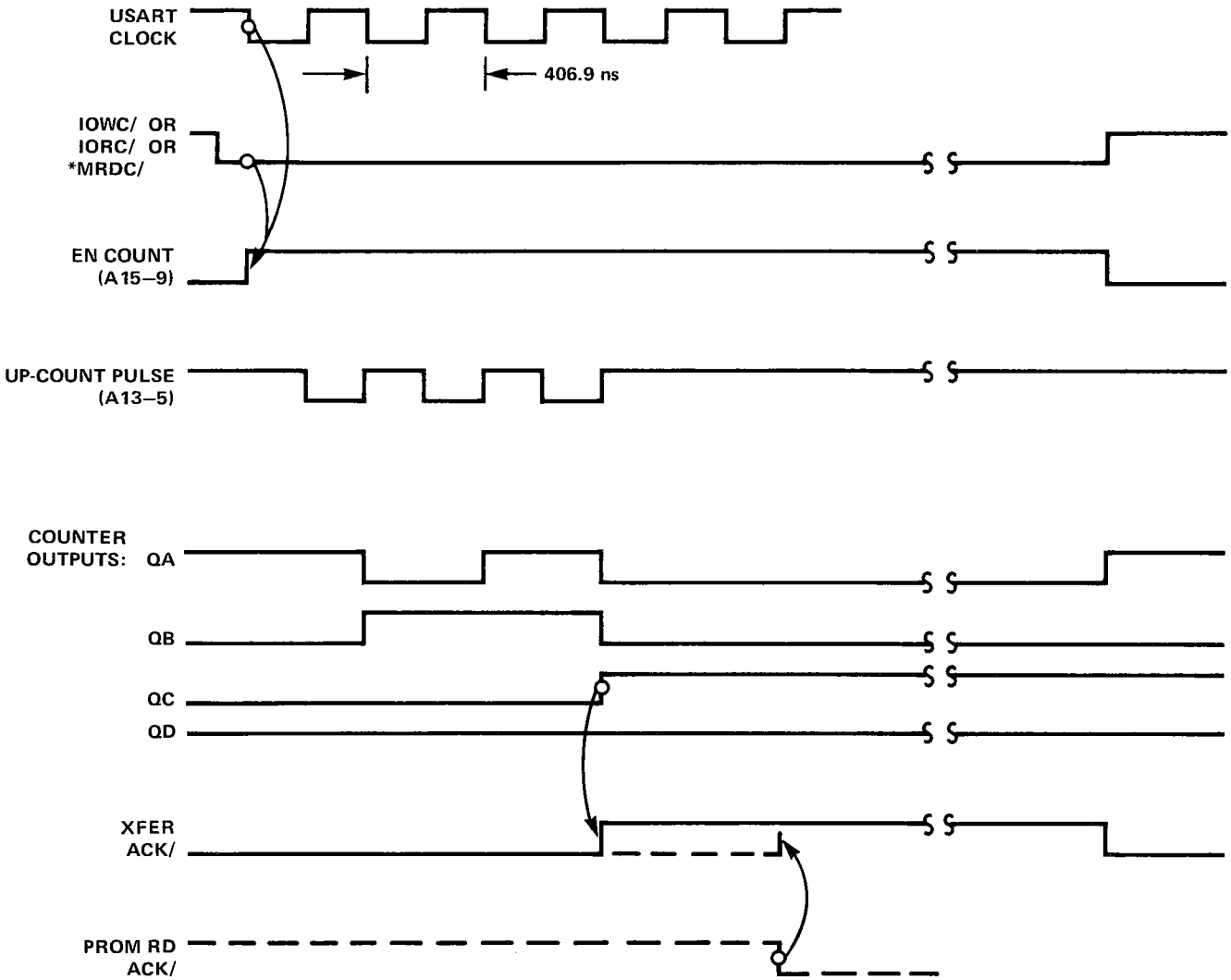


Figure 5-2. Timing for CMND STRB/XFER ACK During Output Operations to Line Printer or PROM Programmer



*THIS ASSUMES THAT MRDC/ IS ISSUED IN CONJUNCTION WITH A ROM ADDRESS AND THAT THE EN ROM SWITCH IS ENABLED.

Figure 5-3. Timing for XFER ACK During Monitor ROM Read, PROM Programmer Read and General I/O Operations

USART can divide the frequency of the timing pulse by either 16 or 64 (programmable).

Finally, the 1.627-μs clock is applied to the clock inputs of the two 74161 synchronous counters. The two 74161 counters and the accompanying 74109 J-$\overline{K}$ flip-flop can be viewed as a 9-bit divide-by-512 cascaded counter network with the 74109 flip-flop storing the least significant bit (the 74109 toggles with each clock pulse). This counter network is loaded to a value of 163_{10} then sequenced up to 512_{10}, with each count occurring on the leading edge of the 1.627-μs clock. The QD output of the second 74161 counter (i.e., the most significant bit of the counter network) essentially divides the driving 1.627-μs clock by 349_{10} (512–163= 349). After 349 counts, the network is loaded to 163_{10}, and counting begins again. The QD output provides a high signal of 416.7 μs duration that re-occurs every 568 μs (see Figure 5-5). This signal defines a 110 baud rate (1÷568 μs=1760 Hz; 1760 Hz÷16=110 baud) that is made available to the TTY USART and also applied to baud rate jumper connection 16, for selectable use by other peripheral interfaces such as the CRT USART.

There are seven jumper connection-pairs in the baud rate jumper pad network. The selected rate is

Table 5-2

BAUD RATE SELECTION

PROGRAMMABLE BAUD RATES		JUMPER CONNECTIONS
(BAUD = FREQUENCY ÷ 16)	(BAUD = FREQUENCY ÷ 64)	
19,200 baud	4,800 baud	23–24
9,600 baud	2,400 baud	19–20
4,800 baud	1,200 baud	17–18
2,400 baud	600 baud	21–22
1,200 baud	300 baud	13–14
110 baud	Not used	15–16

NOTE: MDS monitor software utilizes the following divisions of the USART's input clock:

CRT channel ÷ 64
TTY channel ÷ 16

Refer to the appropriate column above when altering the monitor modules output baud rate through hardware jumpers.

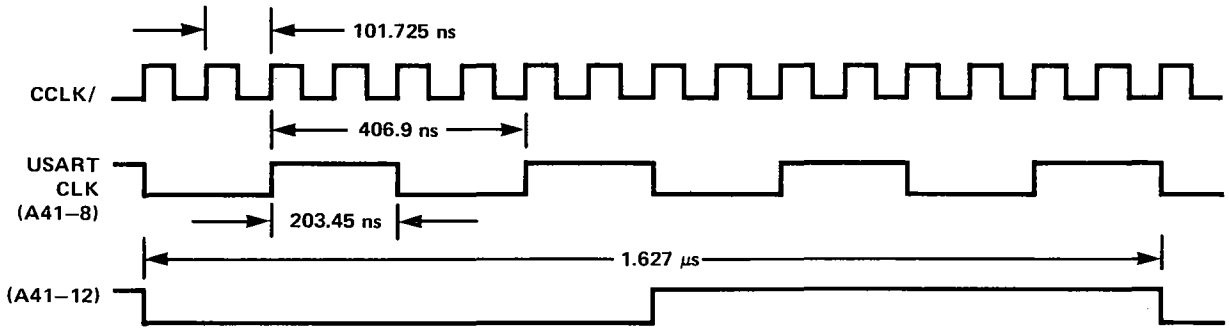
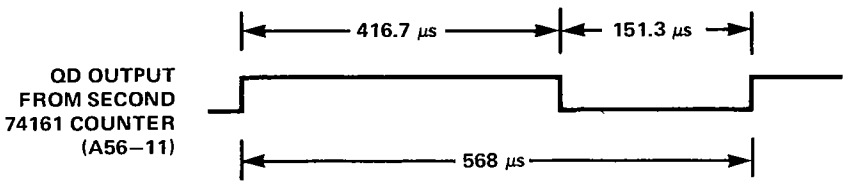


Figure 5-4. USART Clock Timing



PERIOD = 568 µs = 349 X 1.627 µs DRIVING CLOCK PULSE FROM FIGURE 5-4.

1 ÷ 568 µs = 1750 Hz; 1760 Hz ÷ 16 = 110 BAUD

Figure 5-5. Timing for 110 Baud Rate

applied to one input of a 7408 AND gate. The other input is normally tied, through a resistor, to +5 VDC; however, the other input can be supplied by pin P2-32 on the auxiliary connector. The output of this 7408 gate is applied to the CRT USART, and is available on the auxiliary connector at pin P2-28.

5.2.5 CRT INTERFACE

The CRT interface has been implemented with an 8251 USART chip (A16), as shown on sheet 2 of the module schematic, Figure 5-18.

The CRT USART presents a parallel, 8-bit interface to the system data bus and a serial interface to the CRT or other compatible device. We will describe each portion of the total interface separately.

Parallel Interface

The CRT parallel interface is enabled by the CRT EN/ signal which, you will recall, is generated in the I/O command decode logic (Section 5.2.2) whenever the CPU executes an I/O instruction directed to port $F6_{16}$ or $F7_{16}$. The accompanying I/O command, I/O read (IORC/) or I/O write (IOWC/), dictates the direction of data flow. The least significant address bit, ADRØ/, differentiates between port addresses $F6_{16}$ (ADRØ=0) and $F7_{16}$ (ARDØ=1).

Control Output

An output instruction (IOWC/ is true) to port $F7_{16}$ (CRT EN/ and ADRØ/ are true) causes the CRT USART to accept a control byte through its data bus pins (DBØ–DB7).

The control byte can be either the mode control word or the command control word, depending on the sequence in which it is sent. Every control byte is a command control word unless it is sent immediately after the USART is reset. The USART can be reset from the front panel's RESET switch or can be reset under program control by outputting the appropriate command control word. Following a reset (manually or programmatically initiated), the first control byte received by the USART is interpreted as a mode control word; thereafter (until a reset), all control bytes will be interpreted as command control words. Figure 5-6 illustrates the USART algorithm for determining whether a control byte is a mode control or command control word.

The various bits in the mode control word specify the baud rate, character length, parity and the number of stop bits. Table 5-3 lists the specific function of each mode control bit. Note that the actual baud rate selected is dependent on the configuration of the baud rate jumper network in the USART clock generator logic (see Section 5.2.4).

The various bits in the command control word instruct the USART to enable/disable the receiver and transmitter, to reset errors, to reset internal control and return to the mode control cycle, and to set/clear the Data Terminal Ready output. Figure 5-7 defines the function of each command control bit.

Data Output

An output instruction to port $F6_{16}$ (CRT EN/ is true and ADRØ/ is false) causes the CRT USART to accept a data byte through its data bus pins. Bit 0 is the least significant bit and bit 7 is the most significant bit. The CRT interface will subsequently transmit the data byte (if the transmitter is enabled), in serial fashion, to the CRT device as described in a later paragraph.

Status Input

An input instruction (IORC/ is true) to port $F7_{16}$ (CRT EN/ and ADRØ/ are true) causes the CRT USART to output a status byte from its data bus pins. The status byte is enabled through the bidirectional data bus driver logic (see Section 5.2.11) and out onto the system bus (pins P1-67 through 74). The status bits are the result of status and error checking functions performed within the USART.

Bit definitions for the status byte are given in Figure 5-8.

Data Input

An input instruction (IORC/ is true) to port $F6_{16}$ (CRT EN/ is true and ADRØ/ is false) causes the CRT USART to output a data byte (previously

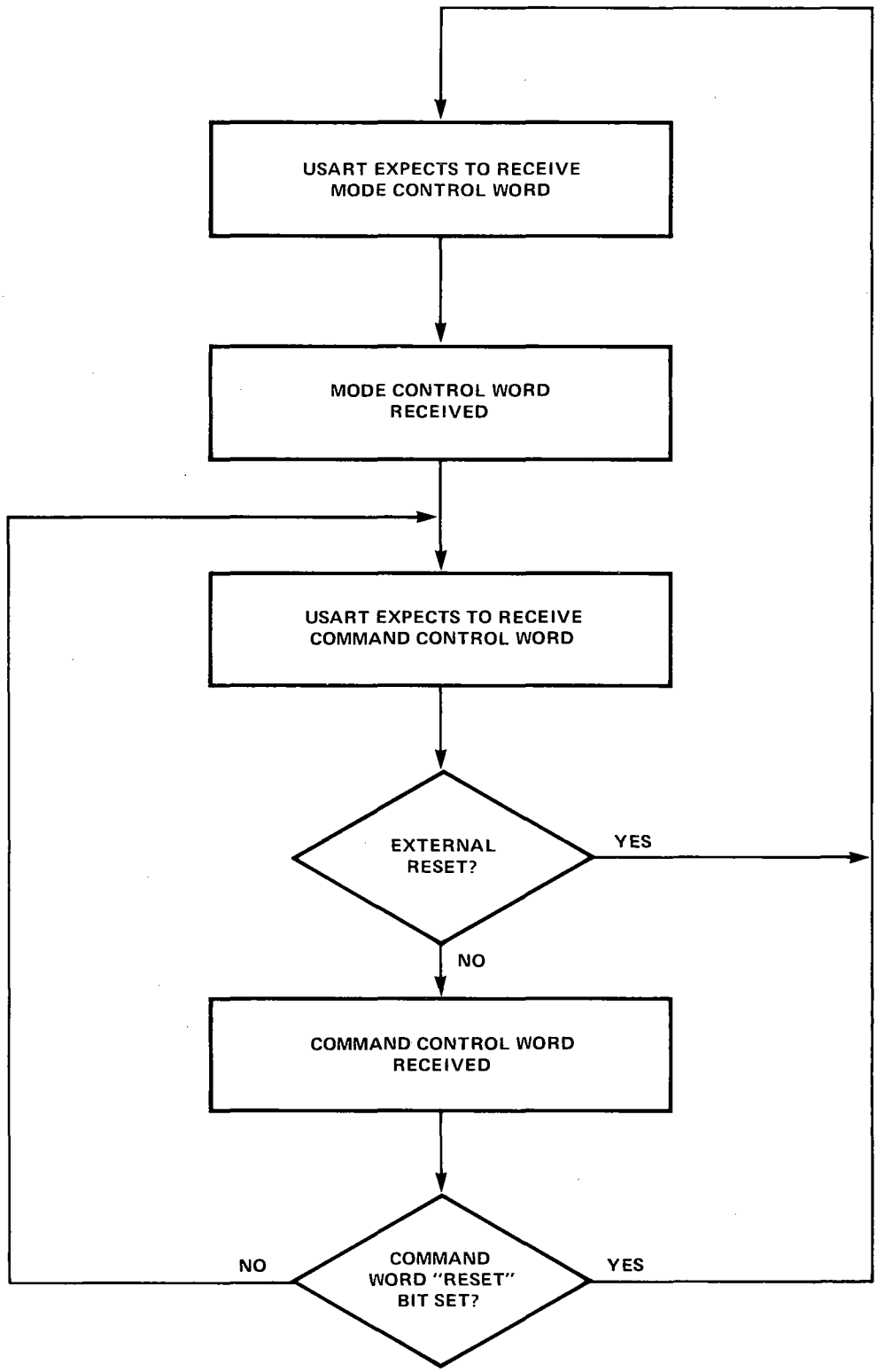
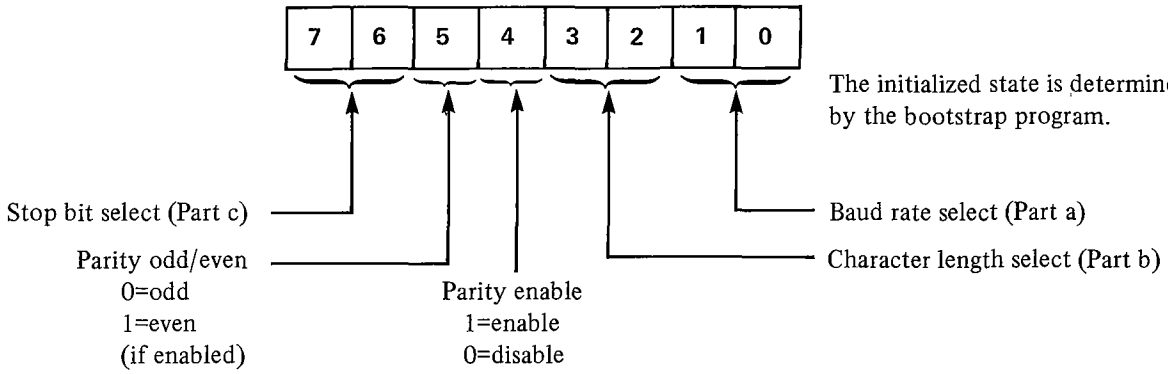


Figure 5-6. USART Algorithm for Control Byte Interpretation

Table 5-3

BIT DEFINITIONS FOR USART MODE CONTROL WORD
(FIRST CONTROL BYTE AFTER RESET)



BIT 1	BIT 0	JUMPER CONFIGURATIONS 19–20 (9600X16)	17–18 (4800X16)	21–22 (2400X16)	13–14 (1200X16)	15–16 (110X16)	
0	0	*	*	*	*	*	BAUD RATE
0	1	*	*	*	*	*	
1	0	9600	4800	2400	1200	110	
1	1	2400	1200	600	300	*	

*Illegal mode-jumper configuration
(For TTY; baud rate=110 only; Bit 1=1, Bit 0=0)

Part a: Baud Rate Select (Bits 0 and 1)

BIT 3	BIT 2	CHARACTER LENGTH
0	0	5
0	1	6
1	0	7
1	1	8

Part b: Character Length Select (Bits 2 and 3)

BIT 7	BIT 6	STOP BITS
0	0	Illegal
0	1	1
1	0	1.5
1	1	2

Part c: Stop Bit Select (Bits 6 and 7)

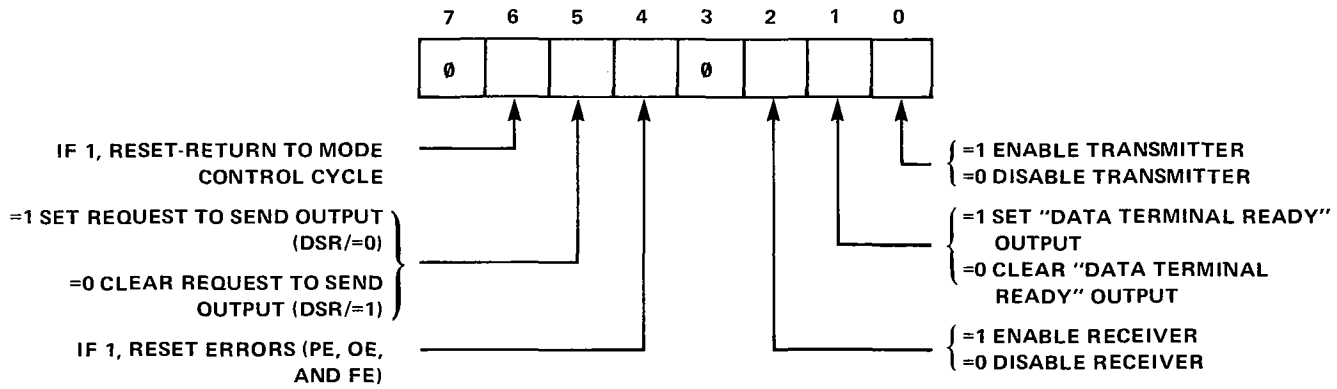


Figure 5-7. Bit Definitions for USART Command Control Word

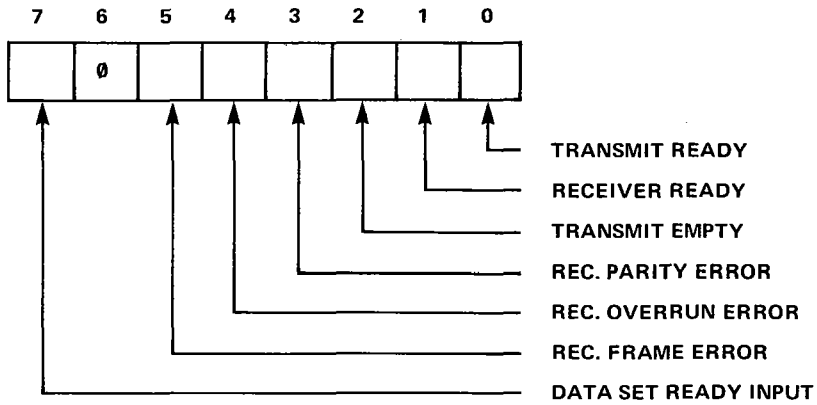


Figure 5-8. Bit Definitions for CRT Status Word

received from the CRT device as described below) from its data bus pins. The data byte is enabled through the bidirectional data bus driver logic (Section 5.2.11) and out onto the system data bus. Bit 0 is the least significant bit and bit 7 is the most significant or parity bit.

Timing for the USART's internal functions are provided by the USART CLK signal (see Section 5.2.4). The USART is reset by the occurrence of a high level on the SYS RST line.

Serial Interface

The CRT USART presents a serial, asynchronous variable-speed interface to the CRT (or other compatible) device. The transmission/reception speed (i.e., baud rate) is referred to timing pulses received through the USART's TxC and RxC inputs. Based on the RxC and TxC inputs and the contents of bits 0 and 1 in the last control byte received (see Table 5-3), the USART exhibits a particular baud rate.

When the CRT USART has a data bit for the device (previously received in parallel from the data bus), it generates a request to send data signal (CRT USART RTS/). If the device is ready to accept the data bit, it returns a clear to send data signal (CRT USART CTS/). The data bit is serially transmitted over the CRT Tx DATA/ line (pin J1-30). This line can be modified to exhibit the drive characteristics of a TTL interface (disconnect jumpers 2-3 and connect 1-2) or an RS232 interface (jumpers 2-3 are connected). If the TTL interface is used, the data from the CRT USART is driven by an 8093 driver circuit. If the RS232 interface is used, the data is inverted, gated through a 7426 negative-OR gate with open collector output and applied to the base of transistor Q1. When the data output from the USART is low (data=logical 0), the +12V source shown on the schematic is grounded through the open collector. As a result, transistor Q1 is activated and a positive voltage potential exists at the transistor's collector output. This positive potential drives current on the CRT Tx DATA/ line. When the USART output is high (data=logical 1), Q1 is turned off and a −10V source sinks current on the transmission line.

The CRT device sends data serially to the CRT interface via the CRT Rx DATA/ line (pin J1-28). Like the transmit line, the receive line can be modified to exhibit TTL or RS232 characteristics. If the TTL interface is used (jumpers 4-5 are disconnected and 5-6 are connected), the input is applied directly to pin 3 on the USART. If the RS232 interface is used (jumpers 4-5 are connected while 5-6 are disconnected), the CRT device will sink current on the CRT Rx DATA/ line when it is sending a logical 1. Transistor Q2 turns off; consequently, a +5V source (tied to the collector of Q2) presents a high voltage level to USART pin 3. When the CRT device sends a logical 0 bit, the receive line is driven to a positive potential between +3 and +25 VDC. The +5V source that feeds the base of Q2 activates the transistor, opening a path between the other +5V source (tied to the collector) and ground; thus presenting a low voltage level to USART pin 3.

The CRT USART accepts one input from the CRT device, data set ready (CRT DSR/). The CRT USART outputs one line to the CRT device, data terminal ready (CRT DTR/).

Interrupts

Like most of the other I/O interfaces on the Monitor Module, the CRT interface includes provisions that allow it to be interrupt driven. When the USART has a data byte for the CPU, the Rx RDY output (pin 14 on the USART) goes true. Rx RDY clocks a 7474 flip-flop set. The Q output (CRT INP INT/) goes low. CRT INP INT/ constitutes bit 5 in the interrupt status word (see Section 5.2.10). CRT INP INT/ indicates that the CRT interface requires service to input a data byte to the CPU. When the CRT USART is ready to receive a data byte from the CPU, the Tx RDY output (pin 15) goes true, clocking another 7474 flip-flop set. The $\overline{Q}$ output of this flip-flop (CRT OUT INT/) constitutes bit 0 of the interrupt status word. CRT OUT INT/ indicates that the CRT USART requires service to receive the next data byte from the CPU. If jumper 7-8 is disconnected and jumper 8-9 is connected, CRT OUT INT/ will be generated as a result of the Tx EMPTY output (pin 18), instead of Tx RDY.

Both the CRT INP INT/ and CRT OUT INT/ flip-flops can be reset as the result of an interrupt control output sequence (see Section 5.2.10).

5.2.6 TELETYPE (TTY) INTERFACE

The TTY interface has been implemented with an 8251 USART chip (A17), as shown on sheet 2 of the module schematic, Figure 5-18.

Like the CRT USART, the TTY presents a parallel, 8-bit interface to the system data bus and a serial interface to the TTY device. The two "sides" of the TTY interface are described separately.

Parallel Interface

The TTY parallel interface is enabled by the TTY EN/ signal, which, you recall, is generated in the I/O command decode logic (Section 5.2.2) whenever the CPU executes an I/O instruction directed to port $F5_{16}$ or $F4_{16}$. The accompanying I/O command, I/O read (IORC/) or I/O write (IOWC/), dictates the direction of data flow. The least significant address bit, ADRØ/, differentiates between port addresses $F5_{16}$ (ADRØ=1) and $F4_{16}$ (ADRØ=0).

Control Output

An output instruction (IOWC/ is true) to port $F5_{16}$ (TTY EN/ and ADRØ/ are true) causes the TTY USART to accept a control byte through its data bus pins (DBØ–DB7). The control byte can be either a Mode Control Word or a Command Control Word. The TTY USART distinguishes between the two according to the same algorithm that we defined for the CRT USART (see Figure 5-6). Table 5-3 also describes bit definitions for the TTY Mode Control Word, with the single exception being that the TTY USART can only operate at 110 baud. Normally, the TTY Mode Control Word is equal to CD_{16}, specifying an 11 level code (eight data bits, disabled parity and two stop bits). The TTY Command Control Word is exactly as defined for the CRT in Figure 5-7.

Data Output

An output instruction to port $F4_{16}$ (TTY EN/ is true and ADRØ/ is false) causes the TTY USART to accept a data byte through its data bus pins. Bit 0 is the least significant bit and bit 7 is the most significant bit. The TTY interface will subsequently transmit the data byte, in serial fashion, to the TTY device as described in a later paragraph.

Status Input

An input instruction (IORC/) to port $F5_{16}$ (TTY EN/ and ADRØ/ are true) causes the TTY USART to output a status byte from its data bus pins. The status byte is enabled through the bidirectional data bus driver logic (see Section 5.2.11) and out onto the system data bus (pins P1-67 through 74). The status bits are the result of status and error checking functions performed within the USART. Bit definitions for the status byte are given in Figure 5-9.

Data Input

An input instruction to port $F4_{16}$ (TTY EN/ is true and ADRØ/ is false) causes the TTY USART to output a data byte (previously received from the

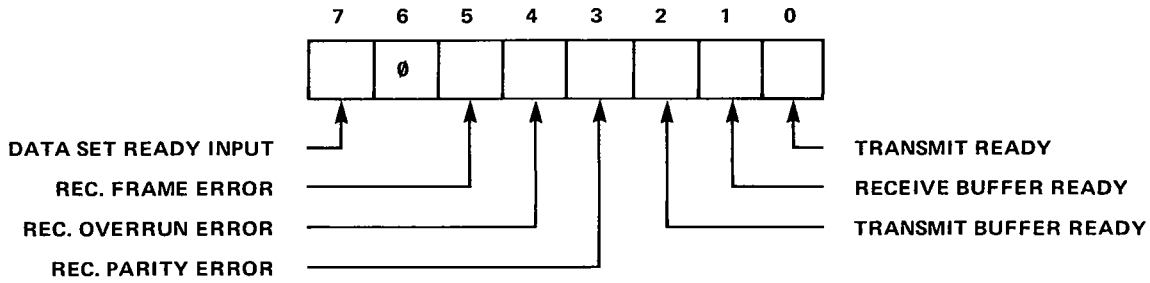


Figure 5-9. Bit Definitions for TTY Status Word

TTY device, as described below) from its data bus pins. The data byte is enabled through the bidirectional data bus. Bit 0 is the least significant bit and bit 7 is the most significant or parity bit from the TTY.

Timing for the USART's parallel interface to the system data bus is provided by the USART CLK signal (see Section 5.2.4). The USART can be reset by a high pulse on the SYS RST line.

Serial Interface

The TTY USART presents a serial, asynchronous, current loop interface to the TTY device. The USART baud rate (110 baud) is derived from a 1760-Hz timing signal received through the USART's TxC and RxC inputs (1760 Hz÷16 cycles/bit=110 baud). The timing signal is supplied by the USART clock generator logic (see Section 5.2.4).

When the TTY USART has a data bit for the device (previously received in parallel from the data bus), it serially transmits the data bit over the TTY Tx DATA line (pin J1-4). Notice that the USART's clear to send data (CTS/) output is tied to the USART's request to send data (RTS/) input. The data bit from the USART's TxD output (pin 19) is inverted and applied to the base of transistor Q5. Q5 turns on, allowing the +5V source (shown on the schematic) to drive current through the transistor and the TTY Tx DATA line.

The TTY device sends data serially to the TTY interface via the TTY Rx DAT line (pin J1-16). The device will cause an open circuit on the TTY Rx DAT line when it is sending a logical 0. Transistor Q3 turns off; consequently, a +5V source (tied to the collector of Q3) is applied to a 7404 inverter and a low voltage level appears at pin 3 on the USART. Notice that the first logical 0 bit received, the start bit, resets the latch that stores advance tape commands to the TTY paper tape reader (TTY ADV RDR/). TTY ADV RDR/ is described later in this sub-section.

When the TTY device sends a logical 1 bit, the receive line is essentially shorted to TTY Rx DAT RET (47Ω to +12 VDC). This activates transistor Q3, opening a path between the +5V source (tied to the collector) and ground. The resultant low voltage level is inverted by the 7404 section and a high voltage level appears at pin 3 on the USART.

The TTY USART accepts one input from the TTY device, data set ready (TTY DSR/). The TTY interface outputs one control command, the TTY reader control signal (TTY RDR CTL), as we mentioned above. TTY RDR CTL is generated when the CPU executes an output instruction to port $F9_{16}$ and the data byte that is output has a logical 1 in bit position one. Recall from Section 5.2.2, that the occurrence of IOWC/ while a value of $F9_{16}$ is present on the address lines results in the generation of the paper tape control signal (PT CTL/). PT CTL/ is inverted and NANDed (gate A38-11,12,13 on sheet 2 of the module schematic) together with data bit 1 (DAT1) to produce TTY ADV RDR/. TTY ADV RDR/ is applied to a S-R latch (consisting of two 7400 negative-OR gates). This latch stores the signal. On the trailing edge of TTY ADV RDR/, the contents of the latch are gated through to the base of transistor Q4. The transistor turns on and drives current through the TTY RDR CTL line (pin J1-12) to the TTY paper tape reader. After the tape is advanced one character and the start bit (logical 0) appears on the receive data line

(TTY Rx DAT), the low voltage level that is applied to pin 3 of the USART also is applied to one of the inputs of the top 7400 section in the latch, causing the latch to reset. Transistor Q4 turns off and TTY RDR CTL goes false. Figure 5-10 illustrates timing for TTY RDR CTL.

Interrupts

Like the CRT interface, the TTY interface includes provisions that allow it to be interrupt driven. When the USART has a data byte for the CPU, the Rx RDY output (pin 14 on the USART) goes true. Rx RDY clocks a 7474 flip-flop set. The $\overline{Q}$ output (TTY INP INT/) goes low. TTY INP INT/ constitutes bit 1 in the interrupt status word (see Section 5.2.10). TTY INP INT/ indicates that the TTY interface requires service to input a data byte to the CPU. When the TTY USART is ready to receive a data byte from the CPU, the Tx RDY output (pin 15) goes true, clocking another 7474 flip-flop set. The Q output of this flip-flop (TTY OUT INT/) constitutes bit 0 of the interrupt status word. TTY OUT INT/ indicates that the TTY USART requires service to receive the next data byte from the CPU. If jumper 11-12 is disconnected and jumper 10-11 is connected, TTY OUT INT/ will be generated as a result of the Tx EMPTY output (pin 18), instead of Tx RDY.

Both the TTY INP INT/ and TTY OUT INT/ flip-flops can be reset as the result of an interrupt control output sequence (see Section 5.2.10).

5.2.7 HIGH-SPEED PAPER TAPE READER/ PUNCH INTERFACE

The high-speed paper tape reader/punch (HSPTR/P) interface consists of three 7474 D-type flip-flops, twenty-two 8097 bus rivers, two 3404 6-bit latches (actually only 8 of the 12 bits are used), and various gating circuits, as shown on sheets 2 and 3 of the module schematic, Figure 5-18.

Recall from Section 5.2.2, that the I/O command decode logic generates the following paper tape-related signals when the appropriate port address

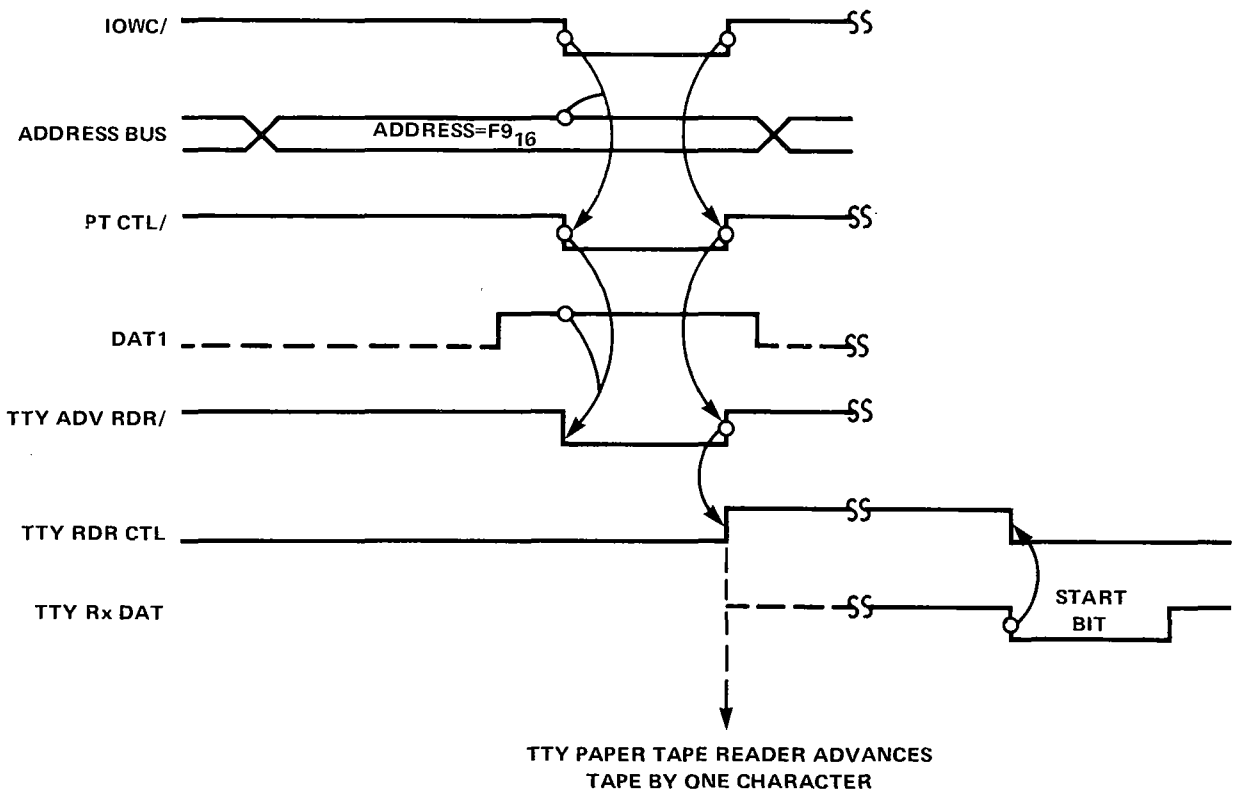


Figure 5-10. Timing for TTY Reader Control

and I/O read or write signal is received by the Monitor Module:

COMMAND SIGNAL		PORT ADDRESS (HEX)		I/O COMMAND
PTP DAT/	=	F8	AND	IOWC/ (output)
PT CTL/	=	F9	AND	IOWC/ (output)
PTR DATA/	=	F8	AND	IORC/ (input)
PT STAT/	=	F9	AND	IORC/ (input)

Data Output

When an output instruction to port $F8_{16}$ is executed (PTP DAT/ is true), the data byte, that is placed on the system data bus by the CPU, is received by the Monitor Module (at pins P1-67 through 74) and fed to the module's bidirectional data bus driver logic (see Section 5.2.11). The driver logic inverts the data bits and applies them to the eight inputs of the 3404 latches. The eight data bits are inverted by the 3404 section and output to 8097 non-inverting driver circuits which make the data byte available to the paper tape punch device (via connector J1).

Control Output

When an output instruction to port $F9_{16}$ is executed (PT CTL/ is true), the control byte that is placed on the system data bus by the CPU is received by the Monitor Module and gated together with PT CTL/ to produce the appropriate command signal(s) for the high-speed paper tape reader/punch or the TTY paper tape reader (see Section 5.2.6). Figure 5-11 gives bit definitions for the paper tape control byte.

If data bit 3 (DAT3) is true, the resultant output of NANDing DAT3 and PT CTL pre-sets a 7474 flip-flop. The Q output of this flip-flop enables a forward or reverse advance of tape on the high-speed reader as determined by bit 2 (DAT2) of the control byte. If DAT2 is true (logical 1), PTR DRV LFT/ (pin J1-17) causes the high-speed paper tape reader to advance the tape one character in the reverse (left) direction. PTR DRV RT/ (pin J1-22) causes the reader to advance the tape one character in the forward (right) direction. When the reader completes the tape advance (in either direction), the paper tape reader ready signal (PTR RDY/) goes true and pre-resets the enabling 7474 flip-flop.

If data bit 5 (DAT5) of the control byte is true (logical 1), the resultant output of NANDing DAT5 and PT CTL produces the paper tape advance signal (PTP ADV). If data bit 4 (DAT4) is false (logical 0), PT CTL/ enables DAT4 through a 3404 inverter; the inverted output (PTP FOR) is driven to the punch by an 8097 circuit. The occurrence of a true level on PTP FOR (pin J1-63) will cause the punch to advance one character in the forward direction on the positive-going edge of PTP ADV (pin J1-60).

If data bit 1 (DAT1) of the control byte is true (logical 1), the resultant output of NANDing DAT1 and PT CTL will generate TTY ADV RDR/. TTY ADV RDR/ causes the TTY paper tape reader to advance one character as described in Section 5.2.6.

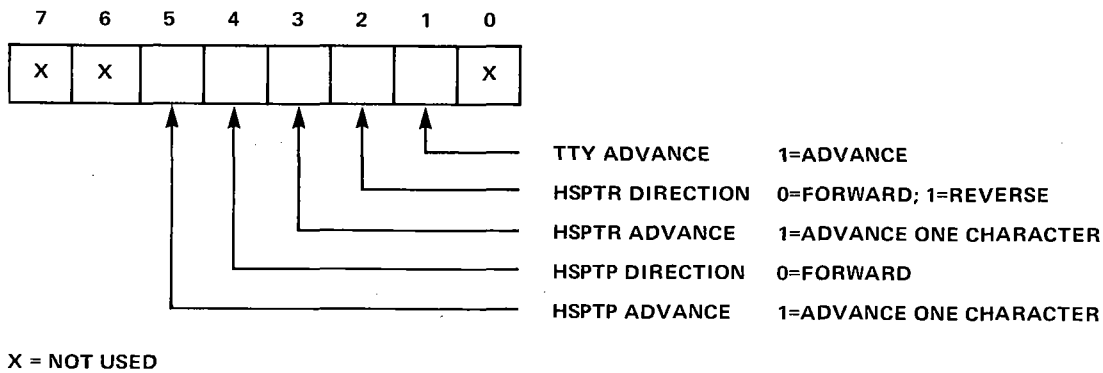


Figure 5-11. Bit Definitions for Paper Tape Control Byte

Data Input

When an input instruction to port $F8_{16}$ is executed (PTR DATA/ is true), the data byte from the high-speed paper tape reader (received at pins J1-64 to 71) is enabled through eight 8097 circuits by PTR DAT/ and placed on the system data bus (DATØ/–DAT7/) at pins P1-67 through 74.

Status Input

When an input instruction to port $F9_{16}$ is executed (PT STAT/ is true), the six status bits from the high-speed paper tape reader and punch (received at pins J1-21, 72, 74, 78, 80, 82) are enabled through six 8097 circuits by PT STAT/ and placed on the system data bus (DATØ–DAT5) at pins P1-69 through 74. Figure 5-12 gives bit definitions for the status byte.

Interrupts

The paper tape reader/punch interface includes provisions that allow it to be interrupt driven. A high-to-low transition on the PTP RDY/ or PTR RDY/ status line clocks the 7474 flip-flop associated with that status line to the set state. The $\overline{Q}$ outputs of these two 7474 sections constitute the punch (PTP OUT INT/) and reader (PTR INP INT/) interrupt status lines to the Monitor interrupt logic (see Section 5.2.10). PTP OUT INT/ is bit 2 and PTR INP INT/ is bit 3 of the interrupt status word. Both the PTP OUT INT/ and PTR INP INT/ flip-flops can be reset as the result of an interrupt control output sequence, as described in Section 5.2.10).

5.2.8 PROM PROGRAMMER INTERFACE

The PROM Programmer interface consists of eight 8097 bus receiver/driver circuits and various gating circuits, as shown on sheets 2 and 3 of the module schematic, Figure 5-18.

Recall from Section 5.2.2, that the I/O command decode logic generates the following PROM-related signals when the appropriate port address and I/O read or write signal is received by the Monitor Module:

COMMAND SIGNAL		PORT ADDRESS (HEX)		I/O COMMAND
PROM ADR HIGH-CTL	=	F1	AND	IOWC/
PROM ADR LOW	=	F2	AND	IOWC/
PROM WRT DATA	=	FØ	AND	IOWC/
EN PROM RD DATA	=	FØ or F1	AND	IORC/
PROM RD DATA	=	FØ	AND	IORC/
PROM RD STATUS	=	F1	AND	IORC/

High Address – Control Output

When an output instruction to port $F1_{16}$ is executed (PROM ADR HIGH-CTL is true), the PROM address-control byte, that has been output to the system data bus by the CPU, is received by the Monitor Module (at pins P1-67 through 74) and fed to the module's bidirectional data bus driver logic (see Section 5.2.11) which asserts the byte on the peripheral data out bus (via connector J1). The resultant output of NANDing command strobe

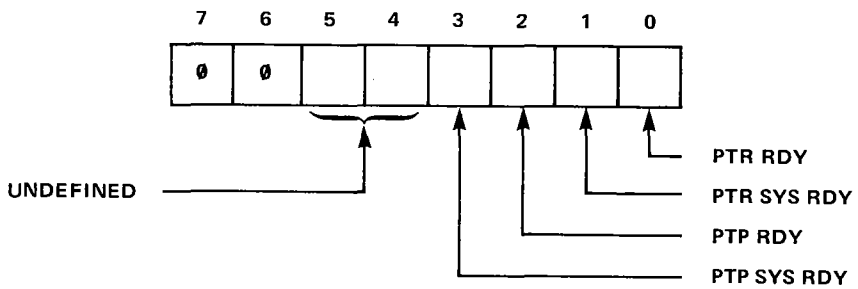


Figure 5-12. Bit Definitions for Paper Tape Status Word

(CMND STRB – see Section 5.2.3) and PROM ADR HIGH-CTL provides a PROM control pulse (PROM CTL PLS//) to the PROM Programmer peripheral (via pin J1-98). The address-control byte consists of the four most significant address bits (on data lines 0, 1, 2, and 3) and four control bits (on data lines 4, 5, 6, and 7).

Low-Address Output

When an input instruction to port $F2_{16}$ is executed (PROM ADR LOW is true), the PROM low-address byte (not to be confused with the I/O port address bytes on the address bus), that has been output to the system data bus by the CPU, is received by the Monitor Module (at pins P1-67 through 74) and fed to the module's bidirectional data bus driver logic which asserts the byte on the peripheral data out bus (via connector J1). The resultant output of NANDing command strobe (CMND STRB) and PROM ADR LOW provides a PROM address pulse (PROM ADR PLS/) to the PROM Programmer (via pin J1-100). The PROM low-address byte constitutes the eight least significant address bits (bit 0 is the LSB) of the 12-bit PROM address that is formed by concatenating bits 0–3 of the address-control byte described in the previous paragraph with the PROM low-address byte.

Data Output

When an output instruction to port $F\emptyset_{16}$ is executed (PROM WRT DATA is true), the data byte, that has been output to the system data bus by the CPU, is received by the Monitor Module and fed to the module's bidirectional data bus driver logic, which asserts the byte on the peripheral data out bus (via connector J1). The resultant output of NANDing command strobe (CMND STRB) with PROM WRT DATA provides a data pulse (PROM WRT DAT PLS/) to the PROM Programmer (via pin J1-96). The data byte is written into the PROM location specified by the 12-bit PROM address described above.

Data or Status Input

An input instruction addressed to port $F\emptyset_{16}$ or $F1_{16}$ (EN PROM RD DATA/ is true) specifies that a data or status byte is to be input from the PROM Programmer to the CPU. If port $F\emptyset_{16}$ is addressed, the PROM RD DATA signal is applied to an 8098 inverting driver and output to the PROM Programmer from pin J1-89 as PROM RD DAT/.

If port $F1_{16}$ is addressed, the PROM RD STATUS signal is driven by an 8098 circuit through pin J1-90 to the PROM Programmer under the mnemonic PROM RD STAT/. The data or status byte that is input (at pins J1-85 through 88 and 91 through 94) to the Monitor Module is enabled through eight 8097 receiver/driver circuits by EN PROM RD DATA/. The 8097 circuits, in turn, drive the data or status byte onto the system data bus (through pins P1-67 to 74).

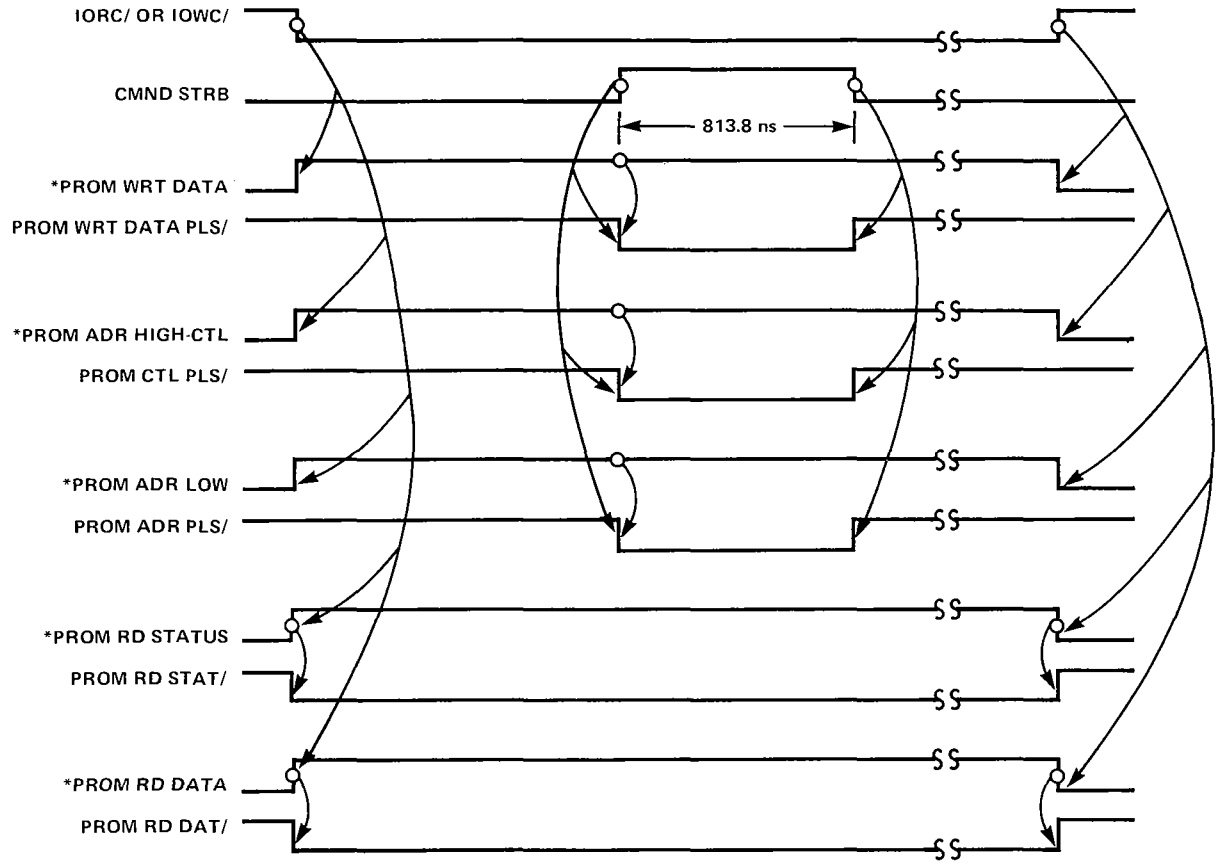
Timing for the PROM Programmer interface is illustrated in Figure 5-13.

5.2.9 LINE PRINTER INTERFACE

The line printer interface has been designed to operate with printers which are capable of receiving input commands as coded ASCII characters in the same manner as data. Timing inputs must be provided by the printer electronics and sensed by the Monitor Module on the two status inputs. The line printer interface consists of a 7474 flip-flop (which latches LPT ACK/) and various gating circuits which are used to generate two control outputs and a data strobe, as well as the circuits that receive the two status inputs and place them onto the system data bus. All of the line printer interface logic is shown on sheet 2 of the module schematic, Figure 5-18.

Recall from Section 5.2.2, that the I/O command decode logic generates the following line printer-related signals when the appropriate port address and I/O read or write signal is received by the Monitor Module:

COMMAND SIGNAL		PORT ADDRESS (HEX)		I/O COMMAND
LPT DAT/	=	FA	AND	IOWC/
LPT CTL/	=	FB	AND	IOWC/
LPT STAT/	=	FB	AND	IORC/



*NOTE: ONLY ONE OF THESE SIGNALS WILL BE TRUE IN ANY GIVEN CYCLE.

Figure 5-13. PROM Programmer Interface Timing

Data Output

When an output instruction to port FA_{16} is executed, LPT DAT is NANDed with CMND STRB (see Section 5.2.3) to generate the line printer data strobe (LPT DAT STRB/) which is available to the line printer at pin J1-95. Data output to the system data bus by the CPU is received by the Monitor Module (at pins P1-67 through 74), gated through the bidirectional data bus driver logic (Section 5.2.11) and made available on the peripheral data out bus (via connector J1).

Control Output

When an output instruction to port FB_{16} is executed, LPT CTL is NANDed separately with bits 0 (DAT$\emptyset$) and 1 (DAT1) of the control byte (that was output by the CPU) to form two control outputs to the line printer device, LPT CTL$\emptyset$/ (pin J1-24) and LPT CTL1/ (pin J1-23).

Status Input

When an input instruction to port FB_{16} is executed, LPT STAT/ enables two 8097 non-inverting drivers which pass the two status bits from the line printer, LPT BUSY (pin J1-56) and LPT STAT1/ (pin J1-54), to data lines 0 and 1 of the system data bus (DAT$\emptyset$/ and DAT1/).

Interrupts

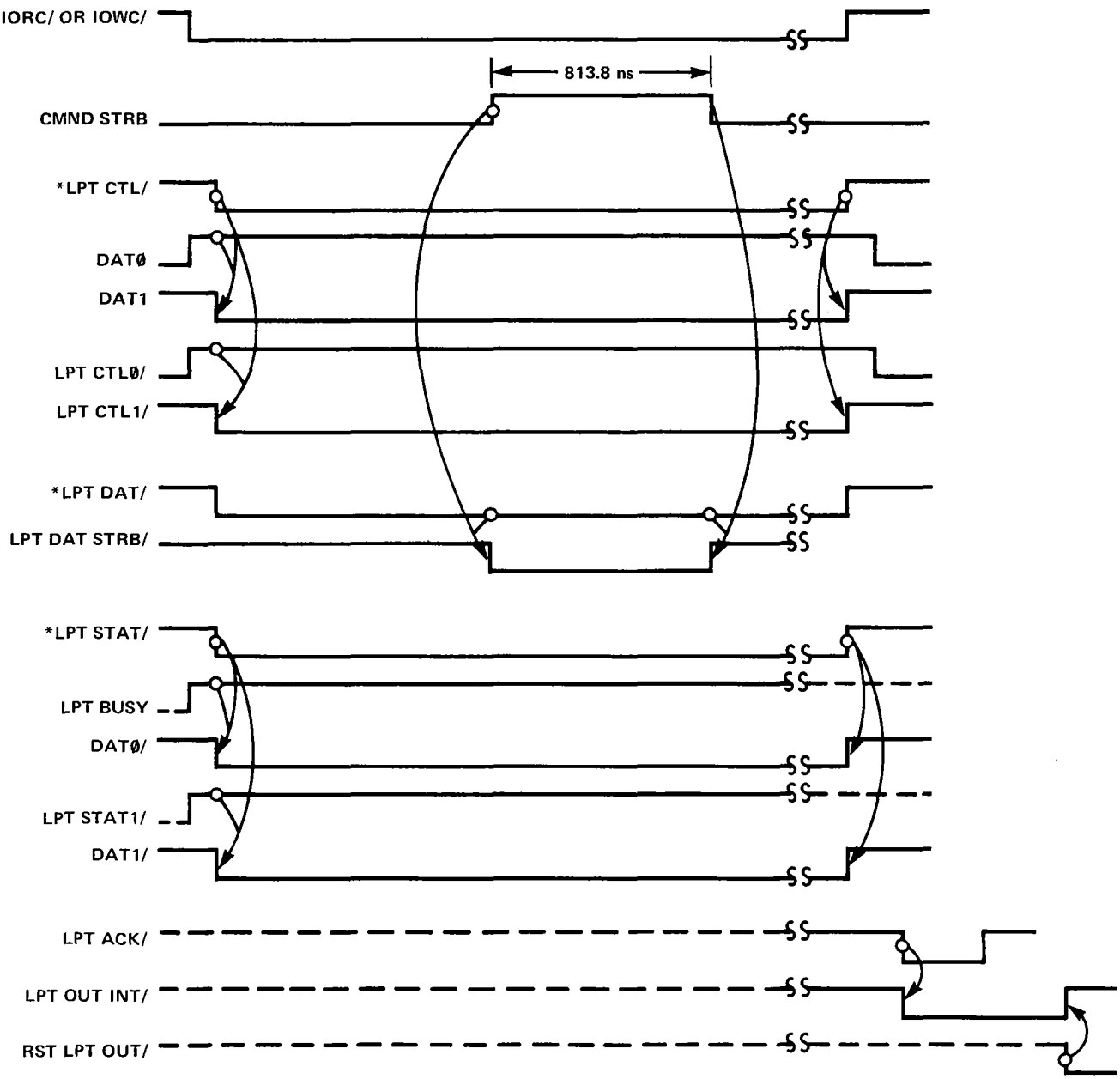
When the line printer device accepts a data byte from the system data bus, it returns an acknowledge signal (LPT ACK/) to the interface (at pin J1-25). On its positive-going edge, LPT ACK/ clocks a 7474 latch set. The $\overline{Q}$ output of the 7474 section (LPT OUT INT/) constitutes bit 6 of the interrupt status word. The LPT OUT INT/ flip-flop can be reset as the result of an interrupt control output sequence, as described in Section 5.2.10.

Timing for the line printer interface is illustrated in Figure 5-14.

5.2.10 MONITOR INTERRUPT LOGIC

The Monitor interrupt logic groups the seven interrupt lines from the TTY, CRT, paper tape reader/punch, and line printer interfaces into a status word that can be read, under program control, by the CPU. In addition, the interrupt logic will, if enabled, issue an interrupt request on level 3 when one of the interface interrupt lines goes true. The monitor interrupt logic consists of six 8097 bus drivers, one 8093 bus driver, one 7474 D-type flip-flop, and assorted gating circuits, as shown on sheet 3 of the module schematic, Figure 5-18.

Recall from Section 5.2.2, that the I/O command decode logic generates the following interrupt-related signals when the appropriate port and I/O



*NOTE: ONLY ONE OF THESE SIGNALS WILL BE TRUE IN A GIVEN CYCLE.

Figure 5-14. Line Printer Interface Timing

read or write signal is received by the Monitor Module:

COMMAND SIGNAL		PORT ADDRESS (HEX)		I/O COMMAND
INT CTL/	=	F3	AND	IOWC/
INT STAT/	=	FA	AND	IORC/

Control Output

When an output instruction to port $F3_{16}$ is executed (INT CTL/ is true), the control byte that is output to the system data bus by the CPU is received by the Monitor (at pins P1-67 through 74), passed through the bidirectional data bus driver logic (see Section 5.2.11), and supplied to the interrupt logic. Bits 0–6 of the control byte specify whether a particular interface interrupt flip-flop is to be reset (e.g., if data bit 0=logical 1, the TTY OUT INT flip-flop is reset). Bit 7 enables or disables the interrupt logic's ability to assert an interrupt request on level 3. Specific bit definitions for the interrupt control byte are given in Figure 5-15.

Bits 0–6 of the control byte are each applied to one of two inputs on seven 7400 NAND gates. The other input to these 7400 gates is supplied by the ORed result of INT CTL and SYS RST (the system reset pulse). Consequently, during an interrupt control output sequence, those 7400 gates that are associated with a data line that represents a logical 1 bit are activated. The output of each active 7400 gate constitutes one of seven reset interrupt signals, as defined below:

DATA BIT	RESET INTERRUPT SIGNAL
0	RST TTY OUT/
1	RST TTY INP/
2	RST PTP OUT/
3	RST PTR INP/
4	RST CRT OUT/
5	RST CRT INP/
6	RST LPT OUT/

These clear signals reset the appropriate interrupt flip-flop in their associated interface.

Bit 7 of the control byte is applied to the D input of a 7474 flip-flop in the interrupt logic. The positive-going edge of INT CTL/ clocks the level on the D-input into the latch. The Q output of this enable-interrupt flip-flop feeds one input of a 7426 NAND gate. The other input is supplied by a 7430 eight-input OR gate. When any one of the interrupt lines from the I/O interfaces (e.g., TTY OUT INT/) is true, this 7430 provides a high level to the 7426 input. If the enable-interrupt latch is set, the open collector output from the 7426 gate drives an active-low interrupt request on the interrupt priority level 3 line (INT3/; pin P1-40).

A true level on the system reset line (SYS RST/) resets the enable interrupt flip-flop and causes all seven reset interrupt signals to the interfaces to be generated.

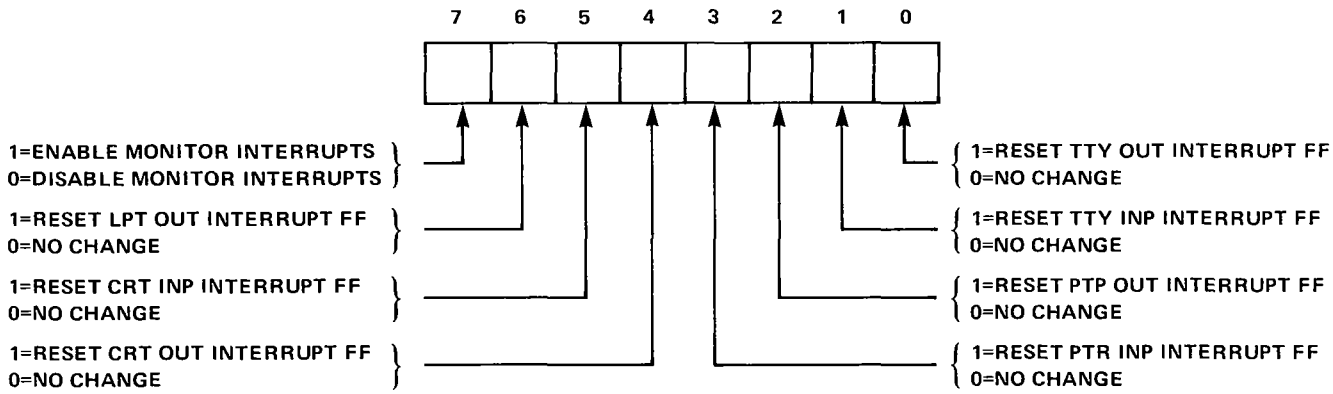


Figure 5-15. Bit Definition for Interrupt Control Word

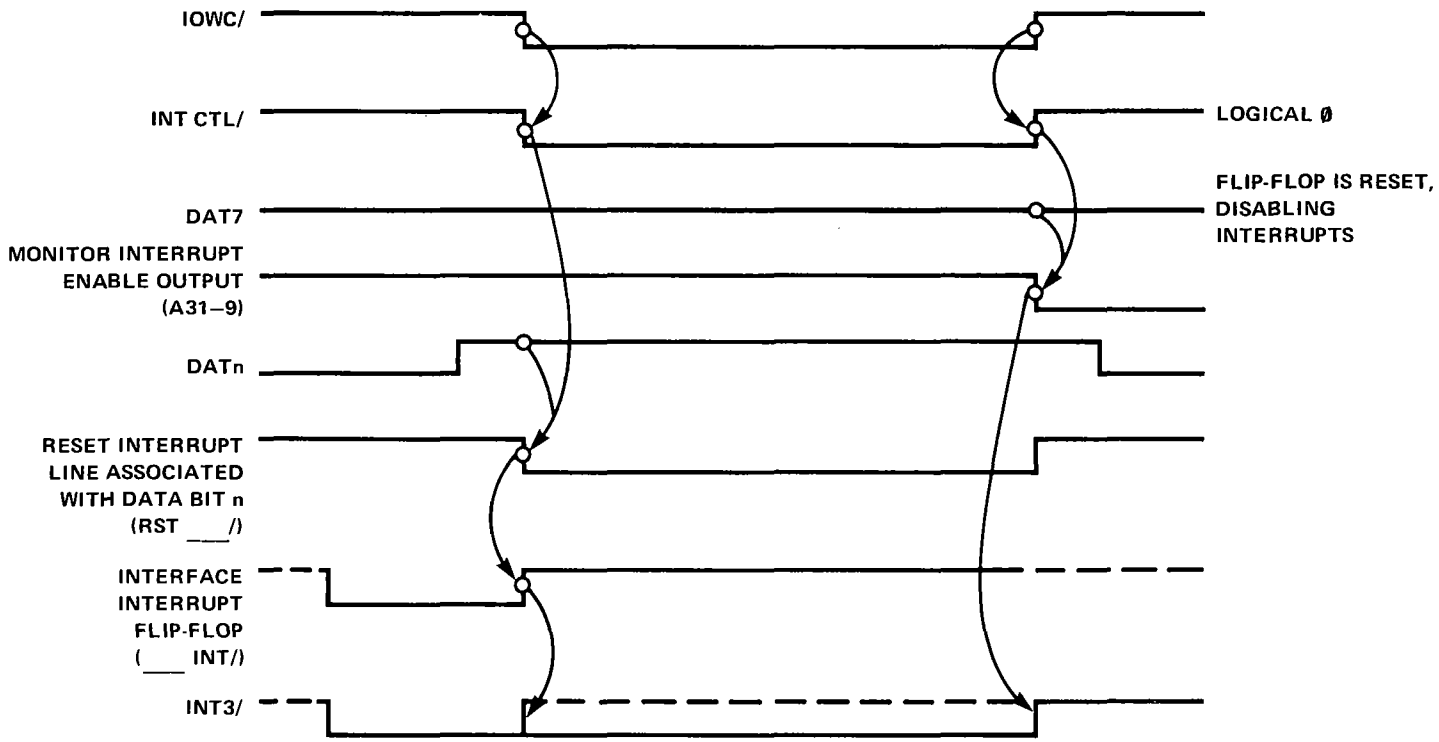


Figure 5-16. Interrupt Control Logic Timing

Timing for the interrupt control logic is illustrated in Figure 5-16.

Status Input

When an input instruction to port FA_{16} is executed, INT STAT/ enables the seven I/O interface interrupt lines through 8097 bus driver circuits (LPT OUT INT/ is actually driven by an 8093 circuit) and out onto the system data bus (DATØ/–DAT6/). The levels on these interrupt lines constitute the interrupt status word, shown in Figure 5-17. This status word could be interrogated by a user-generated operating system or application routine to determine the exact source(s) of interrupt request(s), resolve priority among concurrent requests, and call the proper I/O service routine.

5.2.11 BIDIRECTIONAL DATA BUS DRIVER LOGIC

The bidirectional data bus driver logic routes status or data input bytes from the TTY or CRT USART's onto the system data bus. In the other direction, the driver logic routes data output or control bytes from the system data bus to the TTY or CRT data bus pins, the paper tape punch output bus, the peripheral data out bus, or the Monitor interrupt logic. The driver logic consists of two 8226 4-bit bidirectional bus drivers and other assorted gates, inverters and drivers, as shown on sheet 3 of the module schematic, Figure 5-18.

When an input instruction specifying that a data or status byte is to be input from the TTY or CRT USART, the I/O command decode logic (section 5.2.2) generates the CRT OR TTY/ signal. CRT OR TTY/ is NANDed with IORC/ (the I/O read signal from the CPU) at a 7432 section. The active-low output from this gate is applied to the direction control enable (DCE) inputs on the 8226 bus drivers. A low level at the DCE inputs directs the 8226 devices to gate data or status from the USART data bus lines to the system data bus, DATØ/–DAT7/ (pins P1-67 to 74).

Except during TTY or CRT input cycles, the level on the 8226's DCE inputs is high, reversing the direction of data flow through the 8226 devices. Output data, placed on the system data bus by the CPU (or another bus master module), enters the monitor module at pins P1-67 to 74 and flows through the two 8226 drivers to the TTY or CRT USART data bus pins, the paper tape punch output bus logic, the peripheral data out bus or the Monitor interrupt logic.

If the data or control byte is intended for the TTY or CRT USART's, the TTY EN/ or CRT EN/ and the IOWC/ signals enable the byte into the appropriate USART, as described in Sections 5.2.5 and 5.2.6.

If the data byte is intended for the paper tape punch, the PTP DAT/ signal enables the byte through the 3404 latches in the PTP output bus logic and out to punch device (via the J1 connector).

If the data, control or address byte is intended for the PROM Programmer or line printer peripherals, the byte is driven onto the peripheral data bus by various 8098 and 8097 circuits (through connector J1). If the line printer is the specified destination, the LPT DAT STRB/ signal (see Section 5.2.9)

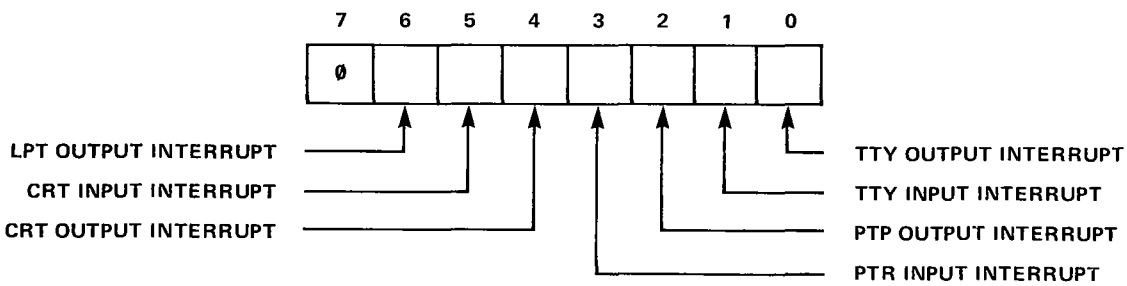


Figure 5-17. Bit Definitions for Interrupt Status Word

directs the line printer to accept the data byte. If the PROM Programmer peripheral is the specified destination, the PROM WRT DAT PLS/, PROM CTL PLS/ or PROM ADR PLS/ signal will direct the PROM Programmer to accept the data, address/control or address byte (see Section 5.2.8).

If the control byte is intended for the Monitor interrupt logic, the INT CTL/ signal will enable the control bits to reset the specified interrupt flip-flops, as described in Section 5.2.10.

5.2.12 MONITOR MODULE SCHEMATIC

Figure 5-18 provides a complete schematic drawing (3 sheets) of all logic on the Monitor Module

5.3 UTILIZATION: MONITOR MODULE

This section provides information on utilization of the Monitor Module.

5.3.1 INSTALLATION

In installing the Monitor Module, the user must take account of:

(a) environmental extremes
(b) mounting considerations
(c) electrical connections
(d) power requirements
(e) signal requirements
(f) jumper connections

Environment

Temperature extremes can cause instability, or result in permanent damage to the circuits on the module. Ambient temperature must therefore be maintained within the limits of 0° to 70° Centigrade. Exercise caution in locating the module, giving particular attention to radiant and conducive sources of heat. Remember that the module itself, when installed, will contribute some heat to the environment. Maintain an adequate clearance, to permit the convective dissipation of heat from the elements on the card.

Relative humidity should not exceed 90%, non-condensing.

Mounting

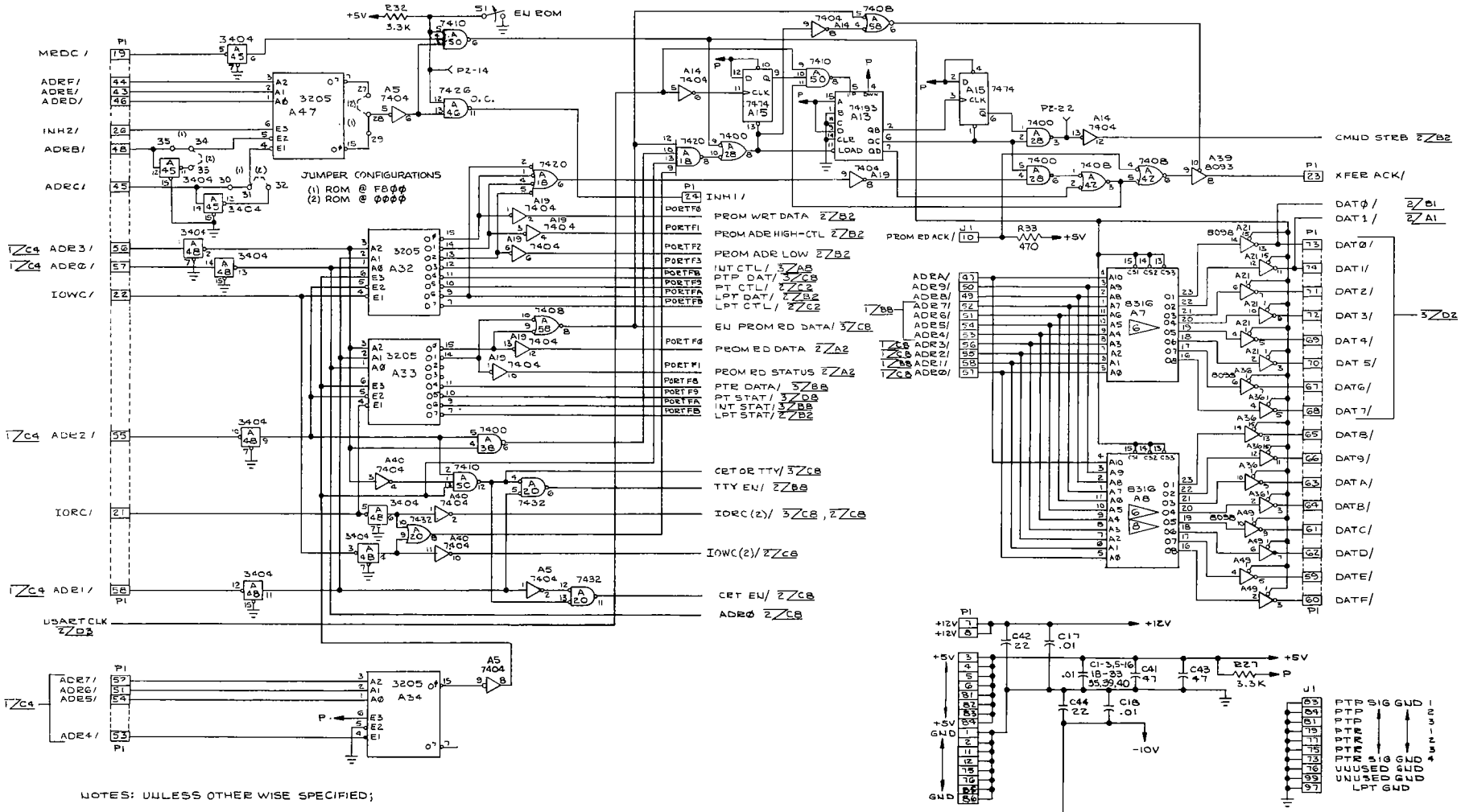
Avoid locating the module near vibrating machinery. Exposure to prolonged or violent vibration may cause fatigue or impact failure of connections on the board, resulting in abnormally high noise levels or outright failure of the assembly.

Dimensions of the module are 12-in. X 6.75-in. Be sure to allow enough additional clearance to ensure adequate cooling.

The module is designed to plug directly into three standard, double-sided PC edge connectors. An 86-pin connector and a 60-pin auxiliary connector are on one edge of the board; a 100-pin connector is on the opposite edge. The connectors can serve as a mounting, as well as an electrical junction, if the environment is not too severe. Card guide slots are desirable, for the additional protection they afford. Should vibration be a problem, however, or should the assembly be used in a portable equipment application, an additional retaining bracket will have to be provided. When mounting the board, remember that it is desirable to orient the assembly vertically whenever possible. This optimizes convective cooling of the components on the module.

Electrical Connections

The Monitor Module communicates with the motherboard and, consequently, the rest of the system, through a standard 86-pin, double-sided PC edge connector (P1), 0.156-in. contact centers, as shown in Figure 5-19. Control Data VPB01E43A-00A1 is one suitable type of connector. Pin allocations on this connector are given in Table 5-6 of Section 5.3.2. The module can also communicate with other modules in the system (or with test equipment), through the auxiliary 60-pin, double-sided PC edge connector (P2), 0.1-in. contact centers (see Figure 5-19). Pin allocations for this connector are listed in Table 5-7. The module transfers information to/from the peripheral devices via a 100-pin, double-sided PC edge connector (J1) which attaches to the edge opposite that of the other two connectors. This connector has 0.1-in. contact centers. Viking 3VH50/1JN5 is one suitable type of connector for communicating with the peripheral devices. Pin allocations for this connector are given in Table 5-8.



NOTES: UNLESS OTHER WISE SPECIFIED;

1. THIS SCHEMATIC REFLECTS PWA 1000351-01 REV B.
2. RESISTANCE IS IN OHMS.
3. CAPACITANCE IS IN MICRO-FARADS.
4. ALL DIODES ARE IN914.
5. USED ONLY WITH USART EMULATOR (C34,C36,C37, C38)
6. ROMS MUST BE ORDERED WITH INVERTED ADDRESS, POSITIVE DATA. (A7, A8)
7. A16, A17 (8251's) NOT USED WITH USART EMULATOR.
8. A8 IS USED FOR 16 BIT APPLICATION ONLY.
9. THESE PINS ARE NOT USED; J1-5,7,9,11,13,15,40

Figure 5-18. Monitor Module Schematic (Sheet 1 of 3)

intel © INTEL 1978	3065 BOWERS AVE. SANTA CLARA CALIF. 95051		
TITLE: SCHEMATIC MONITOR			
SIZE: D	DEPT: 410	DRAWING NO.: 1000353	REV: C

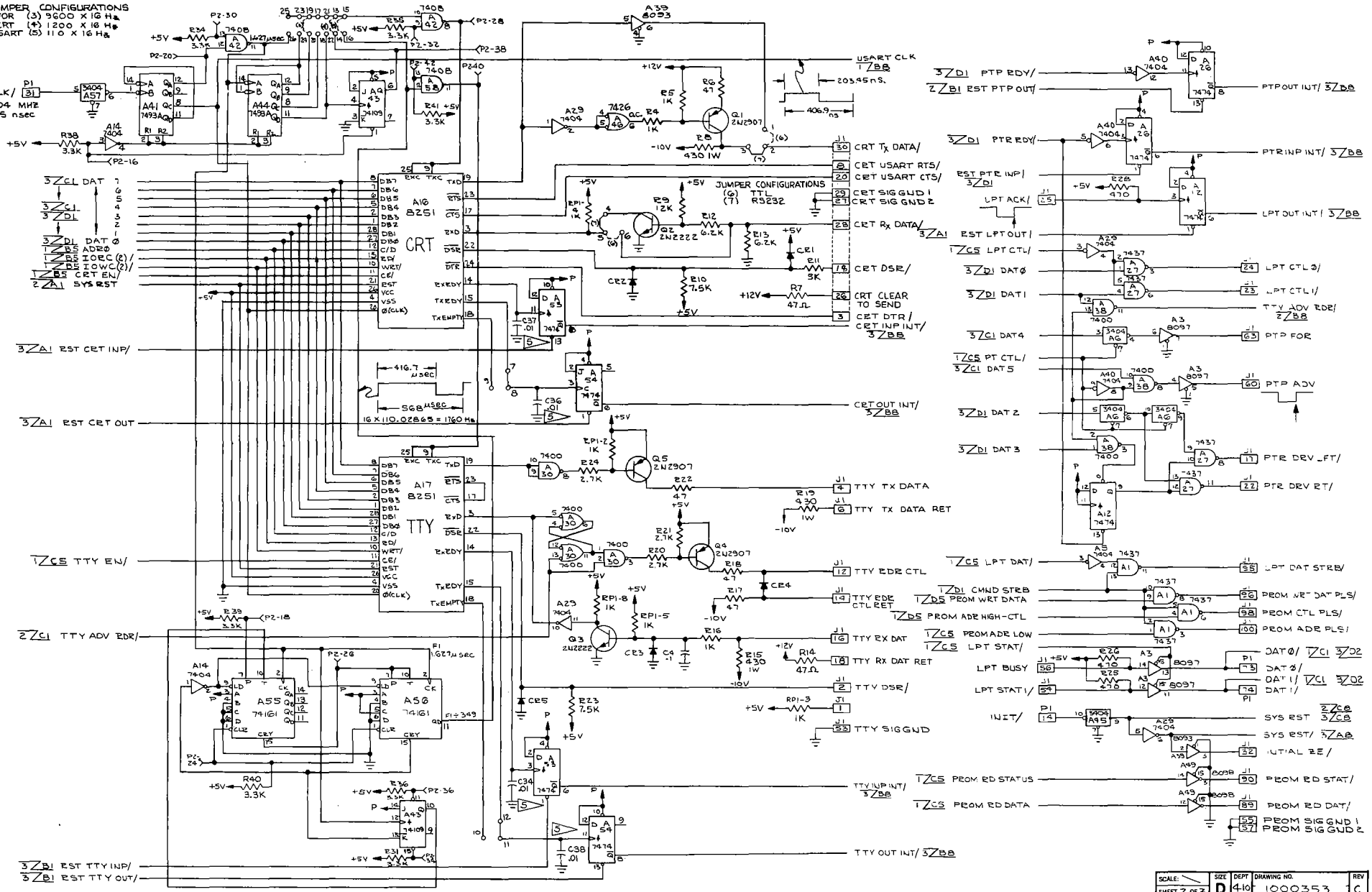


Figure 5-18. Monitor Module Schematic (Sheet 2 of 3)

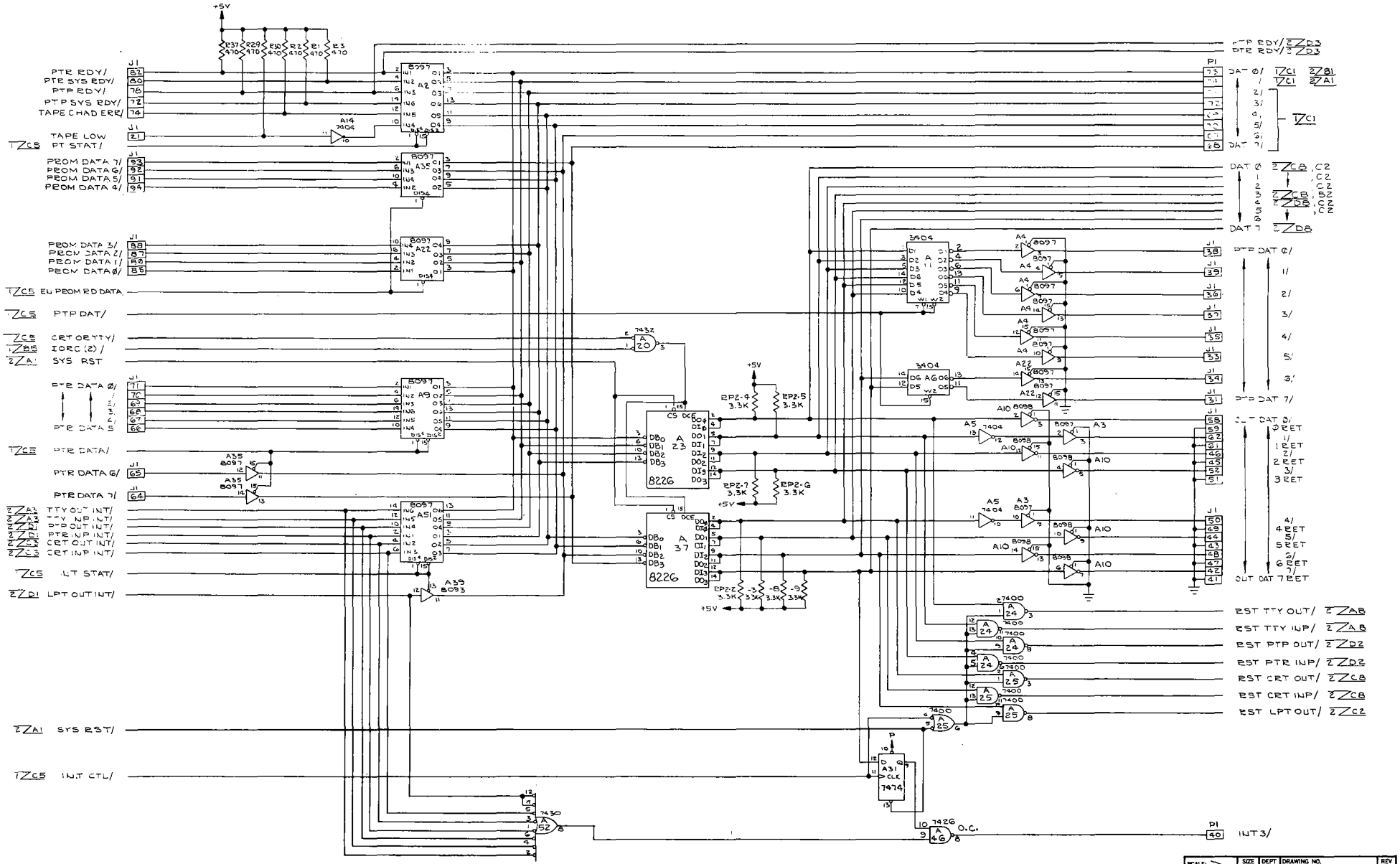


Figure 5-18. Monitor Module Schematic (Sheet 3 of 3)

SCALE:	SIZE	DEPT	DRAWING NO.	REV
SHEET 3 OF 3	D	4-10	1000353	C

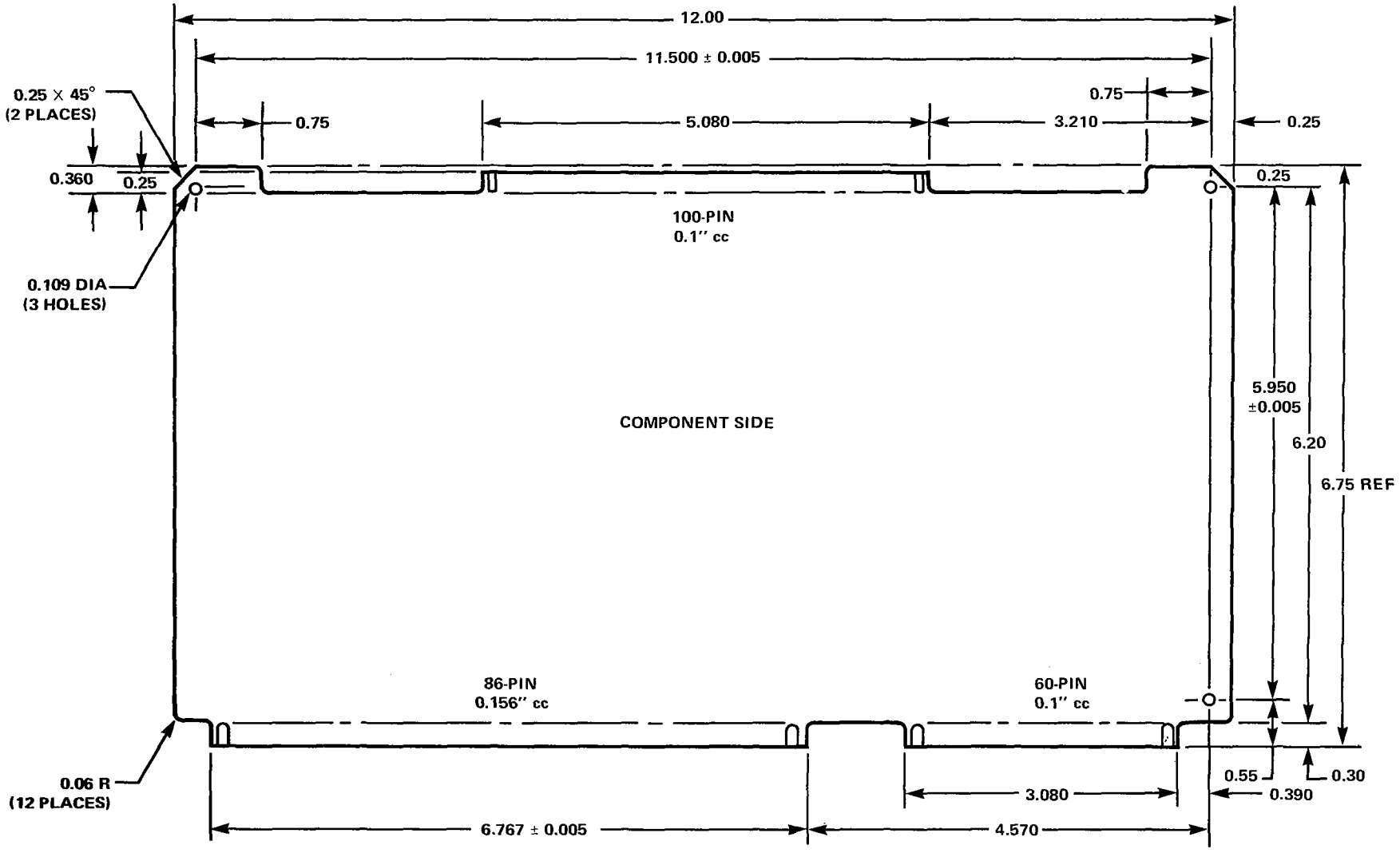


Figure 5-19. Monitor Module Connectors

The Monitor Module requires DC power at levels of +5 VDC, −10 VDC, and +12 VDC.

Refer to the pin lists in Tables 5-6 and 5-8 of Section 5.3.2 for power connectors.

Signal Requirements

All data and control functions appearing at the module edge connectors are at TTL levels (except those connected to TTY and CRT devices having RS232, current loop interfaces). Electrical characteristics of the signal inputs and outputs as well as power inputs are given in Section 5.4

Signal descriptions and connector pin allocations are given in Section 5.3.2

Jumper Connections

There are three groups of jumper pads on the Monitor Module.

The first group, consisting of jumper pads 1-2-3 and 4-5-6, is shown on sheet 2 of the module schematic, Figure 5-18. These two jumper pads determine the interface drive characteristics for the CRT interface. If jumper pads 2-3 and 4-5 are connected, the transmit (CRT Tx DATA/) and receive (CRT Rx DATA/) lines, respectively, will exhibit RS232 interface characteristics. If, however, jumper points 1-2 and 5-6 are connected instead, the transmit and receive lines, respectively, will exhibit TTL drive characteristics.

The second set of jumpers are also shown on sheet 2 of the module schematic. These seven jumper pairs provide different frequency timing signals for use in selecting a particular baud rate for data communication devices. Table 5-4 lists the seven jumper pairs with the frequency of the signals which they provide to the input of the 7408 gate (A42-10) shown on the schematic drawing. When enabled, the output of this 7408 gate is available at pin P2-28 (on the auxiliary connector).

The third group of jumper pads allows the Monitor ROM to respond to addresses other than those in the range $F8ØØ_{16}$–$FFFF_{16}$, as defined in Table 5-5. These jumper pads, 27-28-29, 33-34-35, and 30-31-32, are shown on sheet 1 of the module schematic.

Table 5-4

BAUD RATE JUMPER NETWORK CONNECTIONS

JUMPER PAIR	FREQUENCY (kHz)	BAUD RATE (baud)*
25-26	614.6	38,412
23-24	307.3	19,206
19-20	153.6	9,600
17-18	76.8	4,800
21-22	38.4	2,400
13-14	19.2	1,200
15-16	1.76	110

*Where baud rate = frequency ÷ 16 cycles/bit

NOTE: The MDS monitor utilizes a ÷ 16 for its TTY channel and a ÷ 64 for its CRT channel.

Table 5-5

ROM ADDRESS JUMPER NETWORK CONNECTIONS

JUMPER CONFIGURATIONS	ROM STARTING ADDRESS (HEX)
28-29, 30-31, 34-35 (standard)	F8ØØ
27-28, 30-31, 34-35	18ØØ
28-29, 31-32, 34-35	E8ØØ
27-28, 31-32, 34-35	Ø8ØØ
28-29, 30-31, 33-34	FØØØ
27-28, 30-31, 33-34	1ØØØ
28-29, 31-32, 33-34	EØØØ
27-28, 31-32, 33-34	ØØØØ

5.3.2 PIN LISTS: MONITOR MODULE

The following section provides connector pin allocations on the Monitor Module. The pins and their designated signal functions for the 86-pin connector (P1) are listed in Table 5-6. The same information for the 60-pin auxiliary connector (P2) is listed in Table 5-7. Pin and signal information for the 100-pin peripheral connector (J1) is given in Table 5-8.

Table 5-6

P1 CONNECTOR PIN LIST

PIN	SIGNAL	FUNCTION
1	GND	Ground
2	GND	
3	+5 VDC	Power inputs
4	+5 VDC	
5	+5 VDC	
6	+5 VDC	
7	+12 VDC	Power inputs
8	+12 VDC	
9		
10		
11	GND	Ground
12	GND	
13		
14	INIT/	System reset
15		
16		
17		
18		
19	MRDC/	Memory read command
20		
21	IORC/	I/O read command
22	IOWC/	I/O write command
23	XACK/	Acknowledge transfer
24	INH1/	Inhibit RAM
25		
26	INH2/	Inhibit ROM
27		
28		
29		
30		
31	CCLK/	Bus clock (9.8304 MHz)
32		
33		
34		
35		
36		
37		
38		
39		
40	INT3/	Interrupt request on level 3
41		
42		
43	ADRE/	Address bus

PIN	SIGNAL	FUNCTION
44	ADRF/	Address bus
45	ADRC/	
46	ADRD/	
47	ADRA/	
48	ADRB/	
49	ADR8/	
50	ADR9/	
51	ADR6/	
52	ADR7/	
53	ADR4/	
54	ADR5/	
55	ADR2/	
56	ADR3/	
57	ADRØ/	
58	ADR1/	
59	DATE/	Data bus
60	DATF/	
61	DATC/	
62	DATD/	
63	DATA/	
64	DATB/	
65	DAT8/	
66	DAT9/	
67	DAT6/	
68	DAT7/	
69	DAT4/	
70	DAT5/	
71	DAT2/	
72	DAT3/	
73	DATØ/	
74	DAT1/	
75	GND	Ground
76	GND	
77	-10 VDC	Power inputs
78	-10 VDC	
79		
80		
81	+5 VDC	Power inputs
82	+5 VDC	
83	+5 VDC	
84	+5 VDC	
85	GND	Ground
86	GND	

Table 5-7

P2 CONNECTOR PIN LIST (Primarily Test Points)

PIN	SIGNAL	FUNCTION
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14	EN ROM	
15		
16	RST CNTRS/	
17		
18	÷349 P INPUT	
19		
20	1.627 μs	
21		
22	CMND STRB/	
23		
24	÷349 CLEAR/	
25		Test Points
26	÷32 OF ÷349	
27		
28	CRT BAUD CLK	
29		
30	DIS 1.627/	

PIN	SIGNAL	FUNCTION
31		
32	DIS CRT BAUD CLK	
33		
34	÷349 LSB RST/	
35		
36	÷349 LSB SET/	
37		
38	19.2 kHz	
39		
40	1760 Hz	
41		
42	DIS 1760 Hz	
43		
44		
45		
46		
47		
48		
49		
50	(NO CONNECTIONS)	
51		
52		
53		
54		
55		
56		
57		
58		
59		
60		

Table 5-8

J1 CONNECTOR PIN LIST

PIN	SIGNAL	FUNCTION
1	————	+5 VDC Via 1K Resistor
2	TTY DSR/	TTY Data Set Ready (TTL)
3	CRT DTR/	CRT Data Terminal Ready (TTL)
4	TTY Tx DATA	TTY Transmit Data Line
5		
6	TTY Tx DATA RET	TTY Data Transmit Return
7		
8	CRT USART RTS/	CRT Request to Send Data (TTL)
9		
10	PROM RD ACK/	PROM Programmer Read Ack.
11		
12	TTY RDR CTL	TTY Reader Control
13		
14	TTY RDR CTL RET	TTY Reader Control Return
15		
16	TTY Rx DAT	TTY Receive Data Line
17	PTR DRV LFT/	PTR Advance Tape To Left
18	TTY Rx DAT RET	TTY Data Receive Return
19	CRT DSR/	CRT Data Set Ready; invert RS232
20	CRT USART CTS/	CRT Clear To Send Data (TTL)
21	TAPE LOW	PTP Status
22	PTR DRV RT/	PTR Advance Tape To Right
23	LPT CTL1/	LPT Control (not normally used)
24	LPT CTL0/	
25	LTP ACK/	LPT Data Acknowledge
26	CRT CLEAR TO SEND	CRT Clear To Send RS232
27	CRT SIG GND 2	Ground
28	CRT Rx DATA/	CRT Receive Data Line
29	CRT SIG GND 1	Ground
30	CRT Tx DATA	Transmit Data Line
31	PTP DAT 7/	PTP Data Output
32	INITIALIZE/	Initialize Pulse
33	PTP DAT 5/	
34	PTP DAT 6/	
35	PTP DAT 4/	
36	PTP DAT 2/	PTP Data Output
37	PTP DAT 3/	
38	PTP DAT Ø/	
39	PTP DAT 1/	
40		
41	OUT DAT 7 RET	
42	OUT DAT 7/	
43	OUT DAT 5 RET	
44	OUT DAT 5/	
45	OUT DAT 2 RET	Data Out Bus to Peripherals
46	OUT DAT 2/	
47	OUT DAT 6 RET	
48	OUT DAT 6/	
49	OUT DAT 4 RET	
50	OUT DAT 4/	

Table 5-8

J1 CONNECTOR PIN LIST (continued)

PIN	SIGNAL	FUNCTION
51	OUT DAT 3 RET	
52	OUT DAT 3/	
53	TTY SIG GND	Ground
54	LPT STAT 1/	LPT Status Bit
55	PROM SIG GND1	Ground
56	LPT BUSY	LPT Busy (Ready/)
57	PROM SIG GND2	Ground
58	OUT DAT 0/	Data Out Bus To Peripherals
59	OUT DATA 0 RET	
60	PTP ADV	PTP Advance Tape
61	OUT DAT 1 RET	Data Out Bus To Peripherals
62	OUT DAT 1/	
63	PTP FOR	Forward Tape Advance
64	PTR DATA 7/	
65	PTR DATA 6/	
66	PTR DATA 5/	
67	PTR DATA 4/	PTR Data Input
68	PTR DATA 3/	
69	PTR DATA 2/	
70	PTR DATA 1/	
71	PTR DATA 0/	
72	PTP SYS RDY/	PTP System Ready
73	PTR SIG GND 4	Ground
74	TAPE CHAD ERR/	PTP Status
75	PTR SIG GND 3	Ground
76	UNUSED GND	Ground
77	PTR SIG GND 2	Ground
78	PTP RDY/	PTP Ready
79	PTR SIG GND 1	Ground
80	PTR SYS RDY/	PTR System Ready
81	PTP SIG GND 3	Ground
82	PTR RDY	PTR Ready
83	PTP SIG GND 1	Ground
84	PTP SIG GND 2	Ground
85	PROM DATA 0/	PROM Data Input
86	PROM DATA 1/	
87	PROM DATA 2/	PROM Data Input
88	PROM DATA 3/	
89	PROM RD DAT/	PROM Read Data
90	PROM RD STAT/	PROM Read Status
91	PROM DATA 5/	
92	PROM DATA 6/	PROM Input Data
93	PROM DATA 7/	
94	PROM DATA 4/	
95	LPT DATA STRB/	LPT Data Strobe
96	PROM WRT DAT PLS/	PROM Write Data Strobe
97	LPT GND	Ground
98	PROM CTL PLS/	PROM High Address-Control Strobe
99	UNUSED GND	Ground
100	PROM ADR PLS/	PROM Low Address Strobe

5.3.3 SUMMARY OF DEDICATED I/O ADDRESSES

Table 5-9 summarizes those I/O addresses which are dedicated to specific functions within the INTELLEC MDS System.

5.4 OPERATING CHARACTERISTICS: MONITOR MODULE

The AC and DC characteristics of all major signals that appear at the edge connectors will be listed in this section. This information, however, will be supplied by Intel.

5.4.1 AC CHARACTERISTICS

See Tables 5-10a and 5-10b.

5.4.2 DC CHARACTERISTICS

See Tables 5-11 and 5-12. Power requirements are cited below:

	TYP	MAX
V_{CC} +5 VDC ±5%	2.13A	2.97A

Table 5-9

SUMMARY OF DEDICATED I/O ADDRESSES

ADDRESS	INPUT	OUTPUT
ØØFF	*Real Time Clk	*Enable RTC
ØØFE	Reserved	*Override
ØØFD	Reserved	*Store Cur Level
ØØFC	*Int Mask	*Int Mask
ØØFB	LPT Status	LPT Control
ØØFA	INT Status	LPT Data
ØØF9	PT Status	PT Control
ØØF8	PTR Data	PTP Data
ØØF7	CRT Status	CRT Control
ØØF6	CRT Data	CRT Data
ØØF5	TTY Status	TTY Control
ØØF4	TTY Data	TTY Data
ØØF3	———	Monitor Int cntrl
ØØF2	———	PROM prog address LSB
ØØF1	PROM prog status	PROM prog high addr/ control
ØØF0	PROM prog data	PROM prog DATA

*Implemented on Front Panel Control Module in INTELLEC MDS system.

Table 5-10a

MONITOR MODULE MDS BUS AC CHARACTERISTICS

PARAMETER	OVERALL MIN	OVERALL MAX	DESCRIPTION INPUT REQUIREMENTS	REMARKS
t_{AS}	50		Address set-up time to command	
t_{AH}	50		Address hold time from command	
t_{DS}	50		Data set-up time to command, WRT	
t_{DHW}	50		Data hold time from command, WRT	
t_{SEP}	141		Command separation	
t_{WC}	t_{ACC}		Command width	
t_{XKCO}	0		Command turn off delay from XACK/	
t_{BCY}	100		Bus Clock cycle time	
t_{BW}	25		Bus Clock low and high periods	
t_{CC}	101.725		Com. clock cycle time ±0.05%	
t_{CW}	25		Com. clock low and high periods	
			OUTPUT LIMITS	
t_{DH1}		76	INH1/ Delay from ADRx/, INH2/	
t_{XKO}		141	XACK turn off delay	
t_{DHR}	0		Data hold from read commend	
t_{ACC}		3424	XACK/ delay from VAL RD DATA	Pulsed output to PROM prgrm or LPT
		90+ t_{ACCPP}		t_{ACCPA}=access by PROM prog.
		1811		Other commands
t_{XKD}	50		XACK/ delay from VAL RD DATA	

Table 5-10b

MONITOR MODULE EXTERNAL INTERFACE AC CHARACTERISTICS

PARAMETER	OVERALL MIN	OVERALL MAX	DESCRIPTION OUTPUT LIMITS	REMARKS
t_{EWD}		95	Delay from IOWC/	
t_{EFSU}	1200		PTP fro set-up to PTPADV↑	
t_{EDRST}		62	PTR DRV reset from PTR RDY/↑	
t_{EDSD}	1236		OUTDATx/ set up to strobe	
t_{ESTB}	746		Strobe width	
t_{EDMO}	697.8		OUTDATx/ hold from strobe	
t_{DII}	0		IORC/ to PROM RD	
t_{AK-AK}		50	PROM ACK Delay	
			INPUT LIMITS	
t_{EDRDY}	1811		PTR RDY/ delay from PTR DRV	
t_{EPRRD}		140	PTR RDY/ off from PTR BRV/↑	
t_{EDSR}		100	Valid Data from IORC/	
t_{EDHI}	100		PROM Data hold	
t_{EDSI}	0		PROM Data set up	
t_{EDHR}	0		Hold from IORC/	
t_{EDVR}	0		Valid after IORC/ lead	

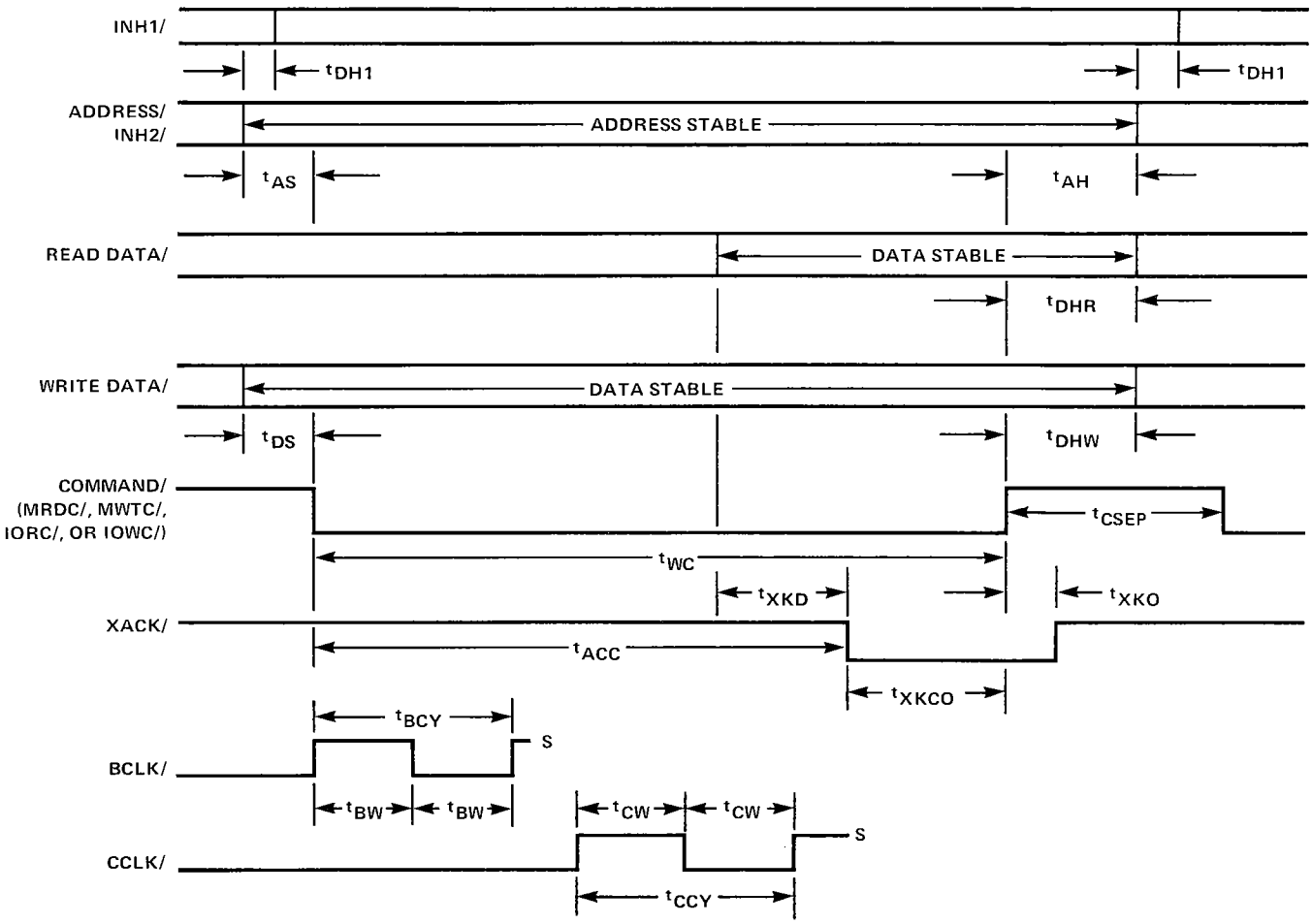


Figure 5-20. Command Timing

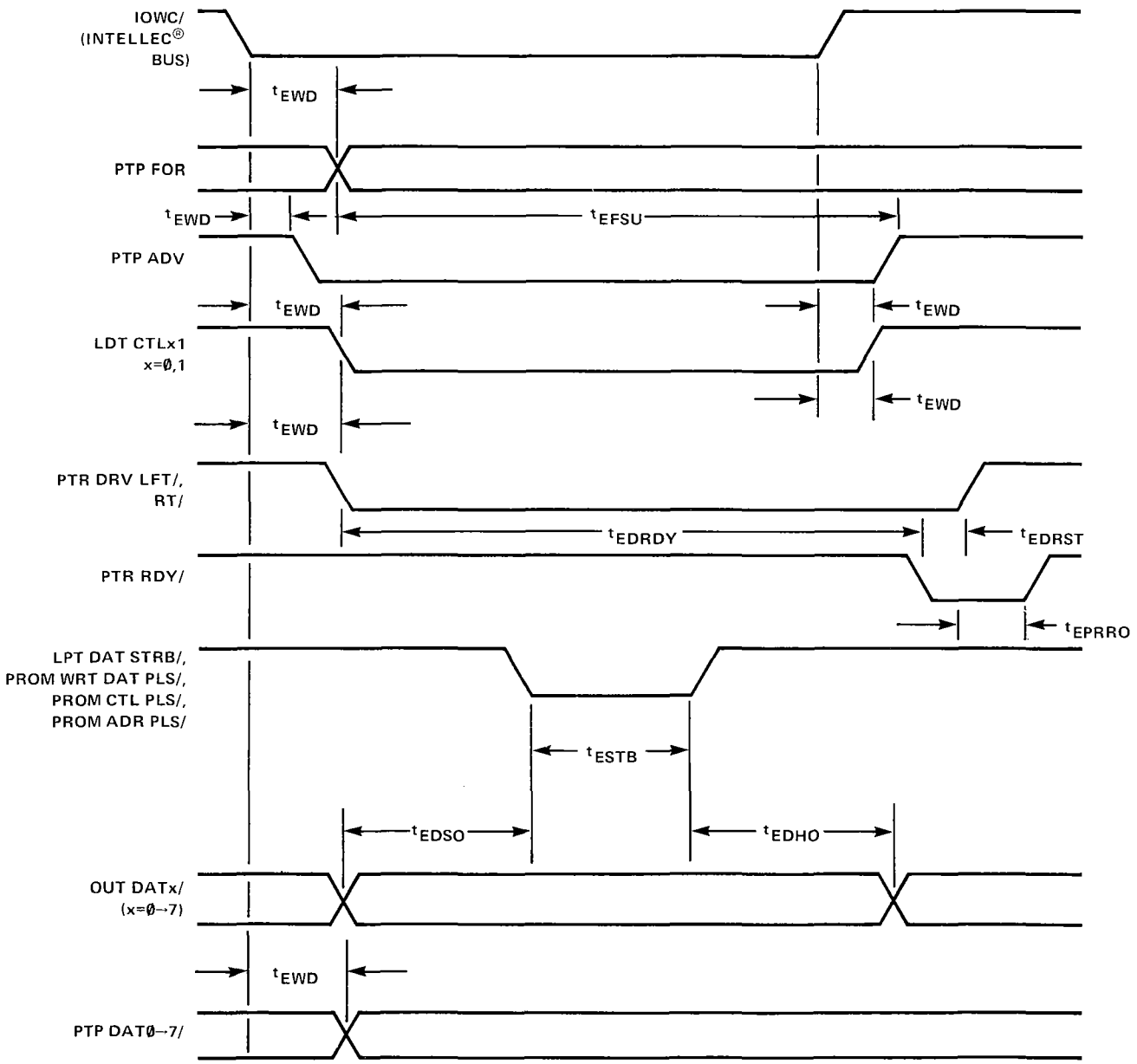


Figure 5-21. External I/O Write Timing

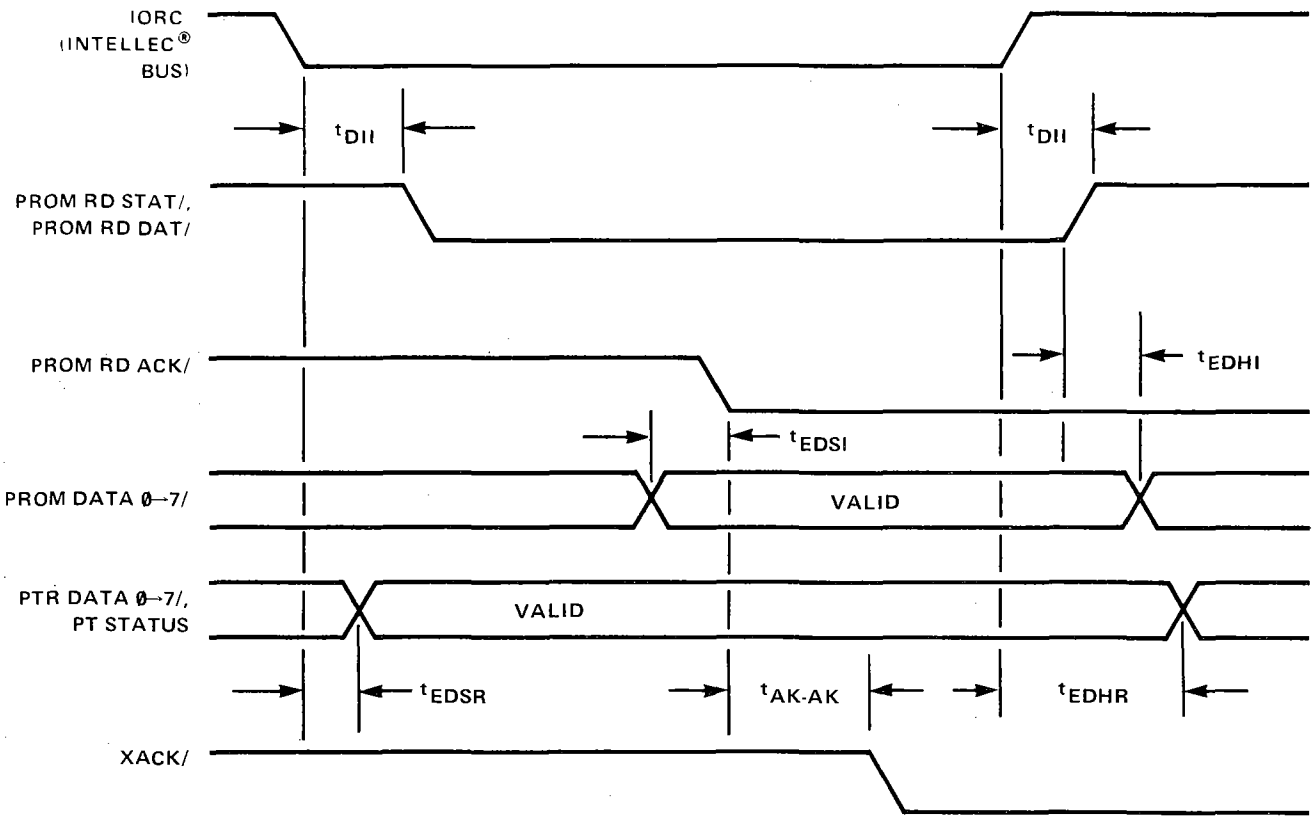


Figure 5-22. External I/O Read Timing

Table 5-11

MONITOR MODULE DC CHARACTERISTICS (INTELLEC® Bus)

SIGNAL	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	PARAMETER			
				MIN	TYP	MAX	UNITS
ADRØ/→ADRF/, INH2/	V_{IL}	Input Low Voltage				0.65	V
	V_{IH}	Input High Voltage		2.2			V
	I_{IL}	Input Current at V_{IL}	V_{IL} = 0.45V			-0.52	mA
	I_{IH}	Input Current at V_{IH}	V_{IH} = 2.4V			40	μF
	C_L	Capacitive Load				30	pF
IOWC/, IORC/	V_{IL}					0.85	V
	V_{IH}			2.2			V
	I_{IL}		V_{IL} = 0.45V			-0.5	mA
	I_{IH}		V_{IH} = 5.25V			20	μF
	C_L					10	pF
XACK/	V_{OL}		I_{OL} = 16 mA	2.4		0.4	V
	V_{OH}		I_{OH} = -5.2 mA				V
	I_{LH}		High Z V_O = 2.4V			40	μA
	I_{LL}		High Z V_O = 0.4V			-40	μA
	C_L					15	pF
INT3/, INH1	V_{OL}		I_{OL} = 16mA			0.4	V
	I_{OH}		V_{OH} = 12V			50	μA
	C_L					15	pF
DATØ/→DAT7/	V_{OL}		I_{OL} = 32mA			0.5	V
	V_{OH}		I_{OH} = -5.2mA	2.4			V
	V_{IL}					0.8	V
	V_{IH}			2.2			V
	I_{IL}		V_{IL} = 0.45V			280	μA
	I_{IH}		V_{IH} = 2.4V			540	μA
	C_L					15	pF
DAT8/→DATF/	V_{OL}		I_{OL} = 32mA			0.4	V
	V_{OH}		I_{OH} = -5.2mA	2.4			V
	I_{IL}		High Z V_O = 0.4			-40	μA
	I_{IH}		High Z V_O = 2.4			40	μA
	C_L					15	pF
CCLK/, INIT/	V_{IL}					0.85	V
	V_{IH}			2.0			V
	I_{IL}		V_{IL} = 0.45V			-0.25	mA
	I_{IH}		V_{IH} = 5.25V			10	μA
	C_L					15	pF

Table 5-12

MONITOR MODULE DC CHARACTERISTICS (EXTERNAL INTERFACE)

SIGNAL	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	PARAMETER			
				MIN	TYP	MAX	UNITS
PTP DATØ→7/,	V_{OL}	Output Low Voltage	I_{OL} = 32mA			0.4	V
OUT DATØ→7/,	V_{OH}	Output High Voltage	I_{OH} = -5.2mA	2.4			V
PROM RD STAT/,	C_L	Capacitive Load				15	pF
PROM PD DAT/, PTP ADV, PTP FOR							
INITIALIZE/	V_{OL}		I_{OL} = 16mA			0.4	V
	V_{OH}		I_{OH} = -5.2mA	2.4			V
	C_L					15	pF
PROM WRT DAT PLS/,	V_{OL}		I_{OL} = 48mA			0.4	V
PROM CTL PLS,	V_{OH}		I_{OH} = -1.2mA	2.4			V
PROM ADR PLS,	C_L					15	pF
LPT DATSTRB, PTR DRV RT, PTR DRV LFT, LPT DTLØ, LPT CTL1							
CRT Tx DATA/	V_{OL}		Jumper POS (7) I_{OL} = 10mA			-5	V
	V_{OH}		Jumper POS (7) I_{OH} = 50mA	5			V
	V_{OL}		Jumper POS (6) I_{OL} = 16mA			0.4	V
	V_{OH}		Jumper POS (6) I_{OH} = -5.2mA	2.4			V
	C_L					15	pF
TTY Tx Data,	I_{OL}	Output Low Current	V_{OL} = -10V, output is off			20	μA
TTY RDR CTL	V_{OH}	Output High Voltage	I_{OH} = -40mA	2.7			V
	C_L					15	pF
PT Status signals,	V_{IL}	Input Low Voltage				0.8	V
LPT ACK/,	V_{IH}	Input High Voltage		2			V
LPT BUSY,	I_{IL}	Input Current at V_{IL}	V_{IL} = 0.4V			-6.4	mA
LPT STAT1,	I_{IH}	Input Current at V_{IH}	V_{IH} = 2.4V			160	μA
PROM RD ACK/	C_L					15	pF
PROM DATA Ø→7/,	V_{IL}					0.8	V
PTR DATA Ø→7/,	V_{IH}			2			V
	I_{IL}		V_{IL} = 0.4V			-1.6	mA
	I_{IH}		V_{IH} = 2.4V			40	μA
	C_L					15	pF

Table 5-12

MONITOR MODULE DC CHARACTERISTICS (EXTERNAL INTERFACE) (continued)

SIGNAL	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	PARAMETER			
				MIN	TYP	MAX	UNITS
CRT Rx DATA/	V_{IL}		Jumper POS ⑦			-3	V
	V_{IH}		Jumper POS ⑦	+3			V
	I_{IL}		Jumper POS ⑦ V_{IL} = -25V			-6	mA
	I_{IH}		Jumper POS ⑦ V_{IH} = 25V			9	mA
	V_{IL}		Jumper POS ⑥			0.6	V
	V_{IH}		Jumper POS ⑥	2			V
	I_{IL}		Jumper POS ⑥ V_{IL} = 0.45V			-6	mA
	I_{IH}		Jumper POS ⑥ V_{IH} = 2.4V			200	μA
	C_L					50	pF
TTY Tx DATA	V_{IL}					-5	V
	V_{IH}			3			V
	I_{IL}		V_{IL} = -12V			-20	mA
	I_{IH}		V_{IH} = +12V			65	mA
	C_L					0.15	μF
	V_{ILZ}	Input Voltage Open Circuit	I_{IL} = 0mA			-6	V