intellec™ 8 Bare Bones 8 and Microcomputer Modules

The widespread usage of low-cost microcomputer systems is made possible by Intel's development and volume production of MCS-8 microcomputer sets. To make it easier to use these sets, Intel now offers complete 8-bit modular microcomputer development systems called Intellec 8.

The Intellec modular microcomputers provide a flexible, inexpensive, and simplified method for developing OEM systems. They are self-contained, expandable systems complete with central processor, memory, I/O, crystal clock, power supplies, standard software, and a control and display console.

The major benefit of the Intellec modular microcomputers is that random access memories (RAMs) may be used instead of read-only-memories (ROMs) for program storage. By using RAMs, program loading and modification is made much easier. In addition, the Intellec front panel control and display console makes it easier to monitor and debug programs. What this means is faster turn-around time during development, enabling you to arrive at that finished system sooner.

The Intellec 8 Eight-Bit Microcomputer Development System. The Intellec 8 is a microcomputer development system designed for applications which require 8-bit bytes of data to perform either binary arithmetic manipulations or logical operations. The Intellec 8 comes complete with power supplies, display and control panel, and finished cabinet. It can directly address up to 16k 8-bit bytes of memory which can be any mix of ROMs, PROMs, or RAMs. The Intellec 8 is designed around the Intel 8008 central processor chip. There are 48 instructions including conditional branching, binary arithmetic, logical, register-to-register, and memory reference operations. I/O channels provide eight 8-bit input ports and twenty-four 8-bit output ports — all completely TTL compatible. The unit has interrupt capability and a two-phase crystal clock that operates at 800kHz providing an instruction cycle time of about 12.5μs.

Bare Bones 8. The Bare Bones 8 has the same capability as the Intellec 8 only it does not include the power supplies, front panel, or finished cabinet. It is designed as a rack-mountable version.

The Intellec 8 system comes with a standard software package which includes a system monitor, resident assembler, and text editor. The programmer can prepare his program in mnemonic form, load it into the Intellec 8, edit and modify it, then assemble it and use the monitor to load the assembled program.

Other development tools for the Intellec 8 include a PL/M compiler, cross assembler, and simulator designed to operate on general-purpose computers. PL/M, a new high-level language, has been developed as an assembly language replacement. A PL/M program can be written in less than 10% of the time it takes to write that same program in assembly language without loss of machine efficiency.

Standard Microcomputer Modules. Microcomputer Modules, standard cards that can be purchased individually so that the designer can develop his system with as little or as much as he needs, are also available.

Additional CPU, Memory, Input/Output, PROM Programmer, Universal Prototype, and other standard modules provide developmental support and systems expansion capability.

MCS-8 MICROCOMPUTER DEVELOPMENT SYSTEMS

- **Intellec 8: Complete MCS-8 Microcomputer Development System**
  - **Central Processor Module**
  - **RAM Memory Module (4096 x 8)**
  - **Input/Output Module (TTL compatible)**
  - **PROM Memory Module (4k x 8 capacity; 1k Resident System Monitor included)**
  - **Control Console and Display**
  - **Power Supplies and Cabinet**
- **Bare Bones 8: MCS-8 System without power supplies, cabinet, or control console**
- **Standard Software**
  - **Resident System Monitor**
  - **Assembler**
  - **Text Editor**

  } Requires 8k of RAM
- **5k bytes of Memory (expandable to 16,384 bytes)**
- **Direct Access to Memory and I/O**
- **Four 8-bit input ports (expandable to eight)**
- **Four 8-bit output ports (expandable to twenty-four)**
- **Universal Asynchronous Transmitter Receiver for serial communications Interface**
- **Real time interrupt capability**
- **Crystal Controlled Master System Clock**

The Intellec 8 is a complete microcomputer development system for MCS-8 microcomputer systems. Its modular design allows the development of any size MCS-8 system, and it has built-in features to make this task easier than it has ever been before.

The basic Intellec 8 consists of four microcomputer modules (CPU, RAM, PROM, and I/O), power supplies, and console and displays in a small compact package. The heart of the system is the imm8-82 Central Processor Module. It is built around Intel's 8008-1, an 8-bit CPU on a chip. It contains all necessary interface to control up to 16k of memory, eight 8-bit input ports, twenty-four 8-bit output ports, and to respond to real time interrupts.

The Intellec 8 has 5k bytes of memory in its basic configuration and may be expanded up to a maximum of 16,384 bytes of memory. Of the basic 5k bytes of memory, 4096 bytes are random access read/write memory located on the imm6-28 RAM Memory Module and are addressed as the lower 4k of memory. This memory may be used for both data storage and program storage. The remaining 1024 bytes of memory are located on the imm6-26 PROM Memory Module and addressed as the upper 1024 bytes of the 16k memory. This portion of memory is a system monitor in four 1702A PROMs. Twelve additional sockets are available on the imm6-28 for monitor or program expansion. When the PROM Programmer Module (imm8-76) is added to the system a fifth 1702A PROM must be used with the monitor for system control.

PROM memory modules and RAM memory modules may be used in any combination to make up the 16k of directly addressable memory. Facilities are built into these modules so that any combination of RAM and ROM or PROM may be mixed in 256 byte increments.

Input and output in the Intellec 8 is provided by the imm8-60 I/O module. It contains four 8-bit input ports, and four 8-bit output ports. In addition it contains a universal asynchronous transmitter/receiver chip as well as a teletype driver, receiver, and reader control. Bit serial communication using only the teletype drivers, receivers, and the I/O port, is also possible with this module.

The universal asynchronous transmitter receiver chip may operate at either 110 baud for standard teletype interface or 1200 baud for communication with a high speed CRT terminal. Additional I/O modules, imm8-60, and output modules, imm8-62, can expand the I/O capability of the Intellec 8 to eight input ports and twenty-four output ports, all TTL compatible.

An interrupt line and an 8-bit interrupt instruction port is built into the imm8-82 Central Processor Module. When an interrupt occurs, the processor executes the instruction which is present at the interrupt instruction port. In the Intellec 8, both the interrupt line and the interrupt instruction port are connected to the console. The processor may be interrupted by depressing the switch labeled INT, and the interrupt instruction is entered in the ADDRESS/INSTRUCTION/DATA switches.

Additional module locations are available in the Intellec 8 so the user may develop his own custom interface using the imm6-70 Universal Prototype Module. All necessary control signals, data, and address buses are present at the connectors of the unused module locations for this expansion. When memory, I/O, and custom interfaces are added to the Intellec 8, care should be taken not to exceed the built-in power supply capability.

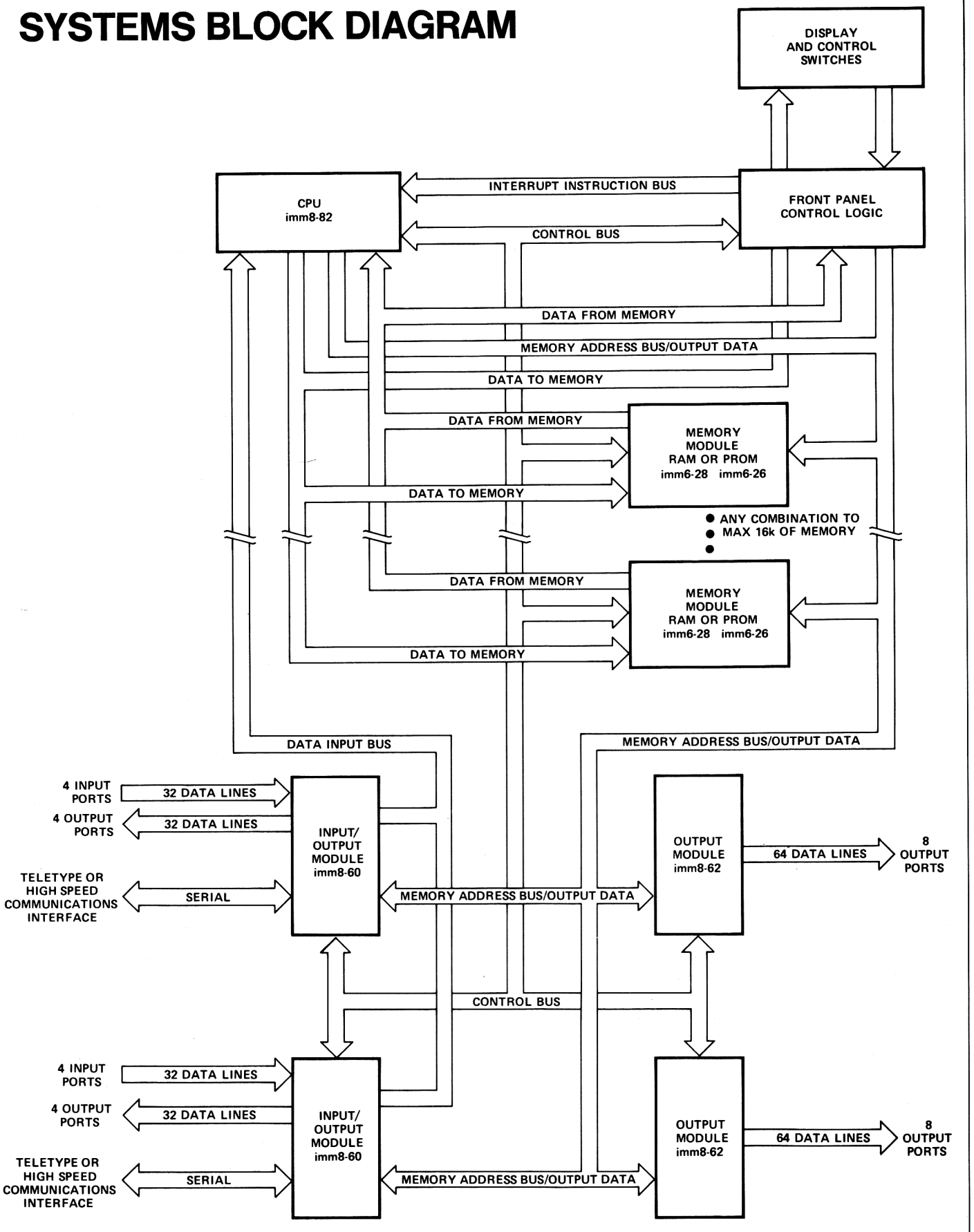
Every Intellec 8 comes with three basic pieces of software, the systems monitor, a resident program located in the upper 1024 bytes of memory, a symbolic assembler and a text editor. The resident systems monitor allows the operator to punch and load tapes, display and alter memory, and execute programs.

With the optional PROM Programmer Module, 1702A PROMs may be programmed and verified under control of the system monitor.

The text editor is a paper tape editor to allow the operator to edit his source code before assembly. The assembler takes this source tape and translates it into object code to run on the Intellec 8 or any MCS-8 system.

The Intellec 8 microcomputer development system is also available in a Bare Bones 8 version. In this version the power supply, chassis, console, and display are removed leaving the user a compact rack mountable chassis to imbed in his own system.

SYSTEMS BLOCK DIAGRAM

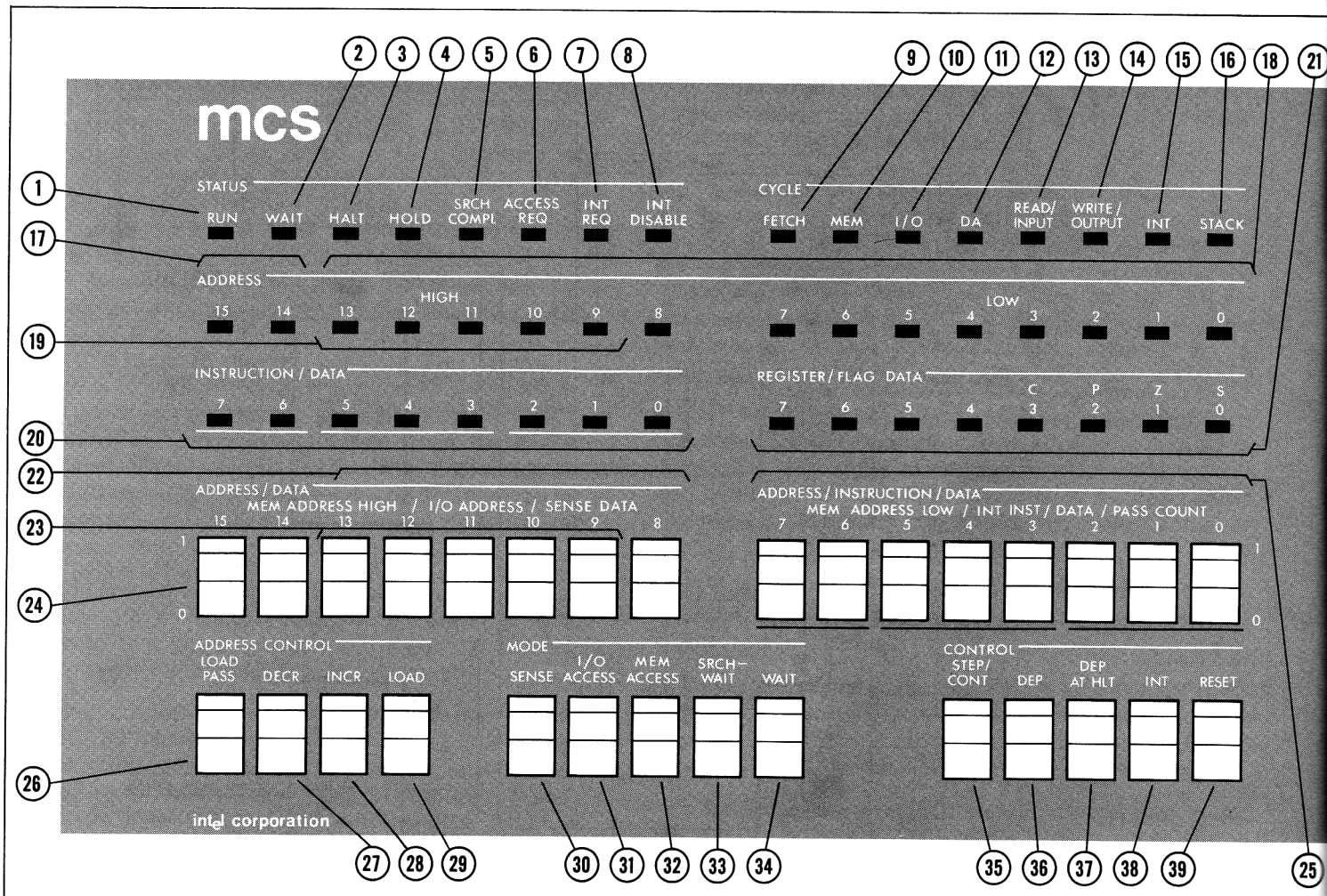


INTELLEC 8 CONTROL CONSOLE AND DISPLAY

The Control Console directs and monitors all activities of the Intellec 8. Complete processor status, machine cycle conditions and operational control of all processor activity are provided, and additional controls facilitating program debugging and hardware checkout are included on the control console.

- **STATUS** is a display of the operating mode of the processor.
  1. **RUN** indicates the processor is running.
  2. **WAIT** indicates the processor is waiting for memory or I/O to be available.
  3. **HALT** indicates the processor is in a stopped state.
  4. **HOLD** indicates the processor is in a HOLD state allowing an I/O or MEM ACCESS to be performed.
  5. **SEARCH COMPL** indicates the processor has executed instructions until the search address and pass counter settings have been reached. (See LOAD PASS 26, and SEARCH-WAIT 33)
  6. **ACCESS REQ** indicates an I/O or memory access is pending from the Control Console.
  7. **INT REQ** indicates an interrupt is pending from the Control Console (see INT 38).
  8. **INT DISABLE** not applicable.

- **CYCLE** provides continuous display of the processor's machine cycle status.
  9. **FETCH** indicates the current machine cycle is fetching an instruction from memory.
  10. **MEM** indicates the processor is executing a memory read (PCR) or memory write (PCW) cycle, or, under manual control, a direct access to memory is in progress.
  11. **I/O** indicates the processor is executing an I/O read or write cycle (PCC) or, under manual control, a direct access to I/O is in progress.
  12. **DA** indicates a direct access to memory or I/O is in progress.
  13. **READ/INPUT** indicates a memory or input read operation is in progress.
  14. **WRITE/OUTPUT** indicates a memory or output write operation is in progress.
  15. **INT** indicates an interrupt cycle is in progress.
  16. **STACK** not applicable.
- **ADDRESS** is a display of memory or I/O address.
  17. **INDICATORS** 14-15 not applicable.
  18. **INDICATORS** 0-13 are a display of the address of memory being accessed during a Fetch, Read, Write, or during manual MEM ACCESS.
  19. **INDICATORS** 9-13 are a display of the I/O address during an input, an output, or during a manual I/O ACCESS.



- **INSTRUCTION/DATA** is a display of the instruction or data.

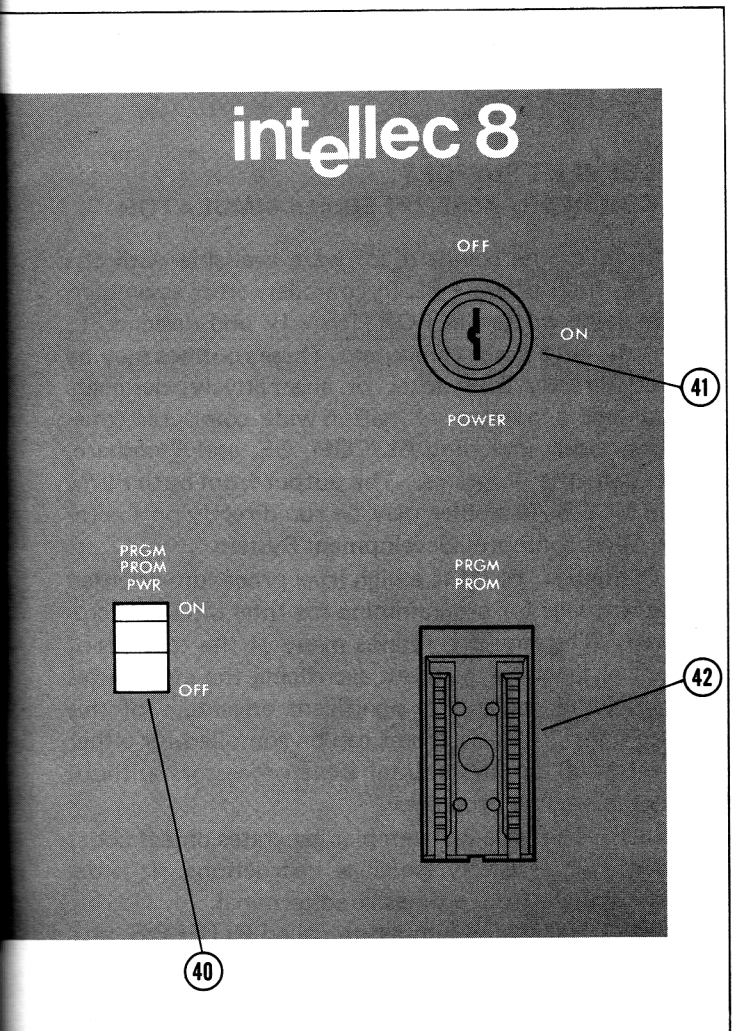
20. INDICATORS 0-7 are a display of the instruction or data between the processor and memory or I/O.

- **REGISTER/FLAG DATA** is the display of the processor data bus during executions of most instructions (display is dependent upon instruction being executed).

21. INDICATORS 0-7 are a display of the contents of the CPU data bus when the instruction is executed. In the case of move instructions, the contents of the source register is displayed. Flags C, P, Z, and S are a special case. The flag status appears in the lower four bits, only when an input instruction is executed.

- **ADDRESS/DATA** These eight switches provide entry of address or data for manual or SENSE operation of the processor (see SENSE 30).

22. MEM ADDRESS HIGH The upper six bits of memory address for direct access or search operations are entered here.
23. I/O ADDRESS The five bit I/O address for manual I/O ACCESS is entered here.
24. SENSE DATA Data to be input during a SENSE mode operation is entered here (see SENSE 30).



- **ADDRESS/INSTRUCTION/DATA** These eight switches provide entry of data, address, and instructions during manual or interrupt operation of the processor.

25. MEM ADDRESS LOW The lower eight bits of memory address for direct access or search mode operation are entered here.
INT INST During an interrupt cycle the interrupt instruction is fetched from here (see INT 38).
DATA Data for deposit to memory or an output port during manual operation is entered here (see DEP 36 , and DEP AT HLT 37).
PASS COUNT Data to be loaded into the pass count register is entered here (see LOAD PASS 26.).

- **ADDRESS CONTROL** These four switches control addressing of memory and I/O and loading of the search address during manual operation of the processor.

26. LOAD PASS Loads pass count into pass count register (PASS COUNT is the number of times the processor will iterate through the search address during a search operation before indicating SEARCH COMPLETE (see SEARCH-WAIT 33 and SEARCH COMPL 5)
27. DECR decrements the loaded address by one (see LOAD 29).
28. INCR increments the loaded address by one (see LOAD 29).
29. LOAD loads contents of address high and low into memory address register for manual direct access to memory or search mode operation (see MEM ACCESS 32 , and SEARCH-WAIT 33).

- **MODE** These five switches select the processor's mode of operation.

30. SENSE causes the processor to input data from the SENSE DATA switches during execution of an input instruction instead of the addressed input port (see SENSE DATA 24).
31. I/O ACCESS provides access to any input port and control of any output port when the processor is in a WAIT mode.
32. MEM ACCESS allows access to and control of any location in memory when the processor is in the WAIT mode.
33. SEARCH-WAIT provides for execution of a program to a specific location, where the processor enters a WAIT state and displays current system conditions.
34. WAIT causes the processor to go into the WAIT state

- **CONTROL** These five switches provide operator control of the processor.

35. STEP/CONT provides single step execution of a program while the processor is in a WAIT mode or continuation of a program from the SEARCH COMPLETE condition, when in a SEARCH-WAIT mode.
36. DEP deposits an 8-bit word to memory or output during a memory or I/O access operation (see DATA 25).
37. DEP AT HLT deposits an 8-bit word to a selected memory location or output automatically during a programmed HALT when I/O ACCESS or MEM ACCESS mode and DEP are previously set. (See DATA 25)
38. INT causes the processor to execute an interrupt cycle, fetching the interrupt instruction from the INT INST switches (see INT INST 25).
39. RESET causes processor to begin execution of program at memory location zero by resetting program counter to zero. All other registers remain unchanged.

- **POWER and PROM PROGRAMMING**

40. PRGM PROM PWR Power switch for high voltage used with PROM programmer.
41. POWER Key operated main power switch
42. PRGM PROM Zero insertion force socket for 1602A or 1702A PROM to be programmed

SYSTEMS SOFTWARE

The Intellec 8 and Bare Bones 8 Microcomputer Development Systems come with three pieces of software: Resident System Monitor, Text Editor and Symbolic Assembler. The Text Editor and Assembler are supplied on paper tape and are loaded with the System Monitor.

SYSTEM MONITOR

- **Loads and punches paper tape**
- **Displays and alters contents of memory**
- **Fills memory with constants**
- **Executes programs in memory**
- **Moves blocks of data in memory**
- **Programs 1602A or 1702A PROMs***

The System Monitor is contained in four 1702A PROMs and is assigned to the upper 1024 words of memory, leaving the lower 15k of memory for program and data storage. This executive software allows the operator to load and punch BNPF or hexadecimal format tapes, display and alter memory, load constants to memory, move blocks of RAM memory, and execute user programs.

The System Monitor is extended by the control software for the imm8-76 programmer module. Included with this module is a fifth 1702A PROM which gives the monitor the ability to program 1602A to 1702A PROMs as well as being able to load memory from already programmed PROMs for duplication and verify the contents of PROMs against master tapes.

**Option with PROM programmer module imm8-76.*

TEXT EDITOR

- **Edits symbolic data from paper tape with data from operator's terminal**
- **Edited output is available via paper tape**
- **Appends text to editor input buffer**
- **Moves pointer to any desired location**
- **Finds and inserts or substitutes strings**
- **Deletes lines selectively**

The Text Editor allows the operator to edit his source code, making corrections and additions. He may append code, delete code, locate strings, insert strings, substitute strings and output edited code via paper tape. The text editor runs on a minimum Intellec 8 system with teletype I/O. (Requires a minimum of 8k x 8 of RAM.)

ASSEMBLER

- **Standard symbolic assembler**
- **Input via prepunched paper tape**
- **Output in 8008 object code**

The Symbolic Assembler is a multiple pass type. During Pass 1 the assembler reads the source code from the paper tape and generates a symbol table for later use. During Pass 2 the assembler generates the assembly listing. Also at this time, any detectable errors such as undefined jumps or missing symbols are indicated by a diagnostic printout on the teletype. Pass 3 may now be run. It generates object code, and punches it on paper tape. (Requires a minimum of 8k x 8 of RAM.)

DEVELOPMENT SUPPORT: PL/M COMPILER, ASSEMBLER and SIMULATOR

In addition to the standard software available with the Intellec 8, Intel offers a PL/M compiler, cross assembler, and simulator written in FORTRAN IV and designed to run on any large scale computer. These routines may be procured directly from Intel, or alternatively, designers may contact a number of nation-wide computer time-sharing services, including AL/COM, GE, and Tymshare, for access to the programs. The output from both PL/M and the MCS-8 Assembler may be run directly on the Intellec 8 Microcomputer Development System.

PL/M Compiler: PL/M is a high level procedure-oriented systems language for programming the Intel MCS-8 microcomputer. The language retains many of the features of a high-level language, without sacrificing the efficiencies of assembly language. A significant advantage of this language is that PL/M programs can be compiled for either the Intel 8008 or future Intel 8-bit processors without altering the original program.

Assembler: The MCS-8 Assembler generates object codes from symbolic assembly language instructions. It is designed to operate from a timeshared terminal.

Simulator: The MCS-8 Simulator, called INTERP/8, provides a software simulation of the Intel 8008 CPU, along with execution monitoring commands to aid program development for the MCS-8.

SYSTEMS SPECIFICATIONS

Word Size:	Data: 8 bits Instruction: 8, 16, or 24 bits
Memory Size:	5k bytes expandable to 16k bytes
Instruction Set:	48, including: conditional branching, binary arithmetic, logical, register-to-register and memory reference operations
Machine Cycle Time:	12.5 μs
System Clock:	Crystal controlled at 800kHz ±0.01%
I/O Channels:	4 expandable to 8 input ports 4 expandable to 24 output ports TTL Compatible
Interrupt:	Single Level
Direct Access to Memory:	Standard via control console
Memory Cycle Time:	900 nanoseconds
Operating Temperature:	0°C to 55°C
DC Power Supplies: (standard Intellec 8)	V_{CC} = 5V, I_{CC} = 12A* V_{DD} = −9V, I_{DD} = 1.8A* V_{GG} = −12V, I_{GG} = 0.06A
DC Power Requirement:	V_{CC} = 5V±5%, I_{CC} = 11A max.,6A typ. V_{DD} = −9±5%, I_{DD} = 1A max., 0.5A typ. V_{GG} = −12V±5%, I_{GG} = 0.03A max., 0.016A typ.
AC Power Requirement: (standard Intellec 8)	50-60Hz, 115/230VAC, 200 Watts *Larger power supplies may be required for expanded systems.
Physical Size:	Intellec 8: 7" x 17 1/8" x 12 1/4" (table top only) Bare Bones 8: 6 3/4" x 17" x 12" (suitable for mounting in standard RETMA 7" x 19" panel space)
Weight:	30 lb.

Standard Software:	System Monitor Resident Assembler Text Editor
Support Software:	PL/M Compiler Cross Assembler Simulator written in FORTRAN IV

STANDARD SYSTEMS and OPTIONAL MODULES

Intellec 8 (imm8-80) Standard System includes the following Modules and Accessories:

- Central Processor Module
- Input/Output Module
- PROM Memory Module
- RAM Memory Module
- Chassis with Mother Board
- Power Supplies
- Control and Display Panel
- Finished Cabinet
- Standard Software:
  - System Monitor
  - Resident Assembler*
  - Text Editor*

Bare Bones 8 (imm8-81) Standard System includes the following Modules:

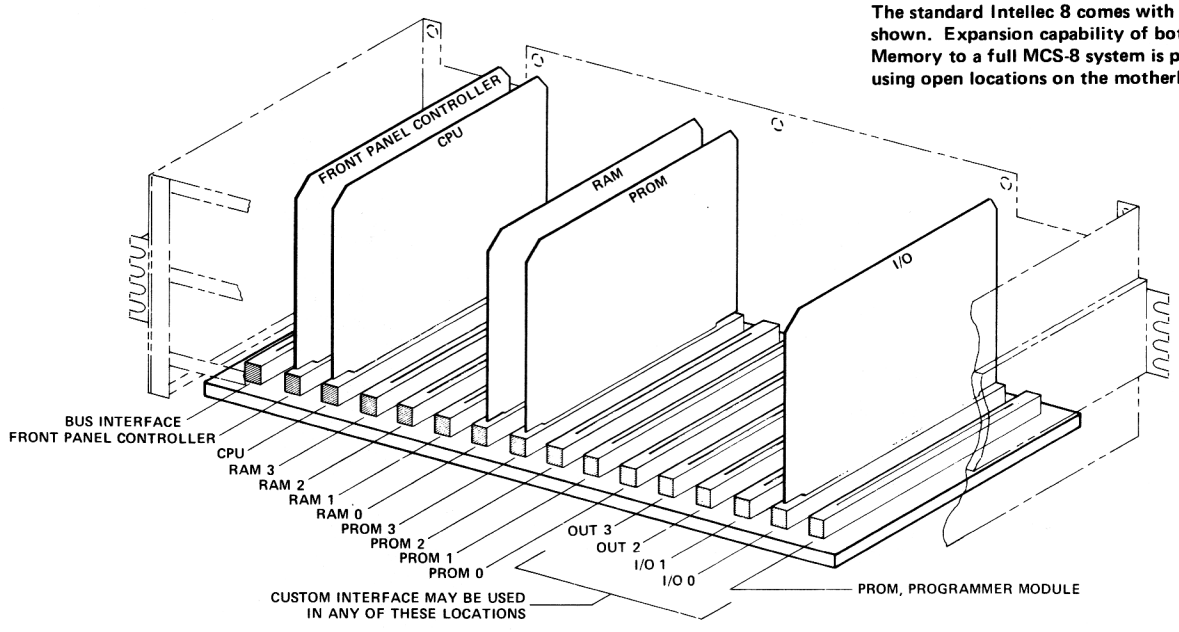
- Central Processor Module
- Input/Output Module
- PROM Memory Module
- RAM Memory Module
- Chassis (rack mountable with Mother Board)
- Standard Software:
  - System Monitor
  - Resident Assembler*
  - Text Editor*

*Requires a minimum of 8k of RAM

Optional Modules available for the Intellec 8 and Bare Bones 8:

- PROM Programmer Module with Control Software
- Additional I/O or Output Modules
- Additional RAM Memory Modules
- Universal Prototype Module
- Module Extender
- Drawer Slides and extenders for Rack Mounting

The standard Intellec 8 comes with the modules shown. Expansion capability of both I/O and Memory to a full MCS-8 system is provided by using open locations on the motherboard.



Intellec 8 and Bare Bones 8 Module Assignments