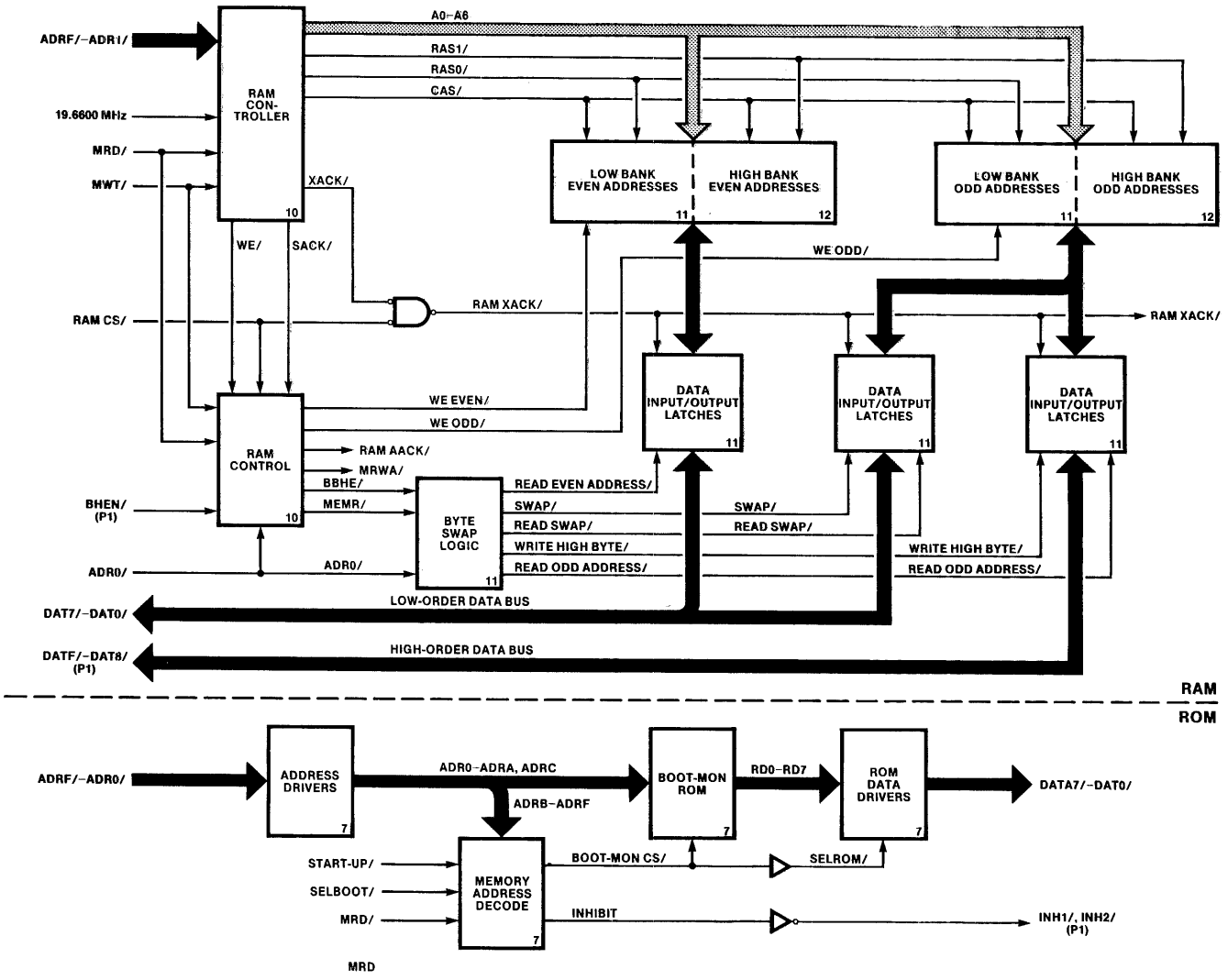

NOTE: The number in the lower right-hand corner of each block identifies the sheet number of the IPC schematic

Figure 3-5. IPC Memory Subsystem Block Diagram 556-19

Monitor program to reenable the diagnostic portion of the boot/diagnostic ROM segment. Entering the Monitor's Z$ command transfers control to the diagnostic (the Z command subroutine reactivates the SEL BOOT/ output by writing 0CH to port FF).

The control port also includes an interrupt enable bit. This bit is cleared (interrupts disabled) when the IPC is initialized and is subsequently set (interrupts enabled) when the Monitor is entered. The Monitor's IOC and PIO interface driver routines automatically clear the interrupt enable bit when called (to prevent an interrupt from being serviced during a sequence-dependent section of code).

The interrupt enable bit is used to enable or deny the interrupt (INTR) output from the system interrupt controller to the master processor. By controlling interrupts in this manner, the system interrupt controller and the master processor's internal interrupt flip-flop are not disturbed when using the Monitor's I/O routines to access system resources. The user program can use the master processor's DI (disable interrupt) and EI (enable interrupt) instructions without regard for Monitor operations.

The input to the control port on sheet 6 is a hexadecimal code appearing on data lines D0/ through D3/. The three least-significant bits of this code select one of four control outputs; the most-significant bit either sets or resets the selected output. The four outputs, the function of each output, and the related hexadecimal codes are outlined in table 3-1.