3.3 IPC INPUT-OUTPUT SUBSYSTEM

The I/O subsystem of the IPC (figure 3-7) provides overall management of all Intellec Series II development system communications with the IPC master processor. Such communications include "system" I/O transfers to or from other optional Multibus boards and "local" I/O transfers. The system I/O transfers are accomplished via the Multibus interface.

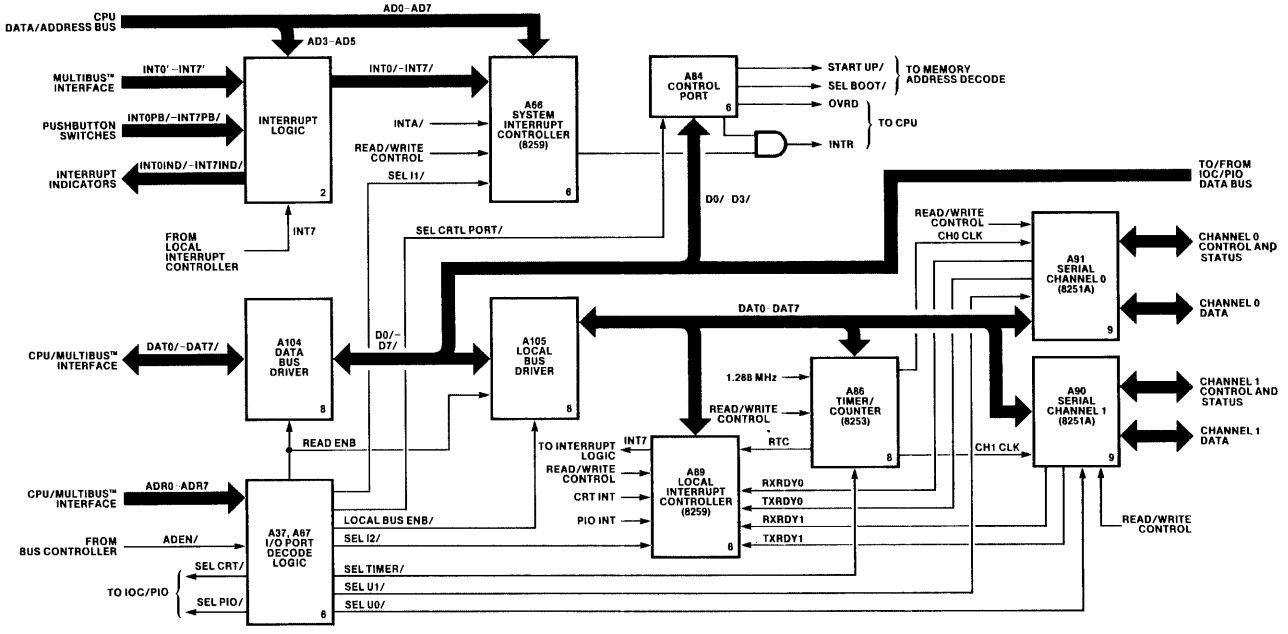
Local I/O transfers use the Multibus, but are accomplished via I/O ports of the master processor. The local I/O transfers are subdivided into external (PIO and IOC) transfers and internal I/O transfers. All internal I/O transfers are between the IPC master processor and the on-board programmable resources of the IPC.

Decoding of the internal and external I/O port addresses is performed by the decode logic on sheet 6. This logic decodes 19 distinct port addresses to produce ten control signals. The port addresses and associated chip select signals for both internal and external I/O control are shown in table 3-3.

One significant factor illustrated in table 3-3 is that the SEL LOCAL signal is generated for each of the port addresses used by both the internal and external I/O control circuits. This signal is applied to the local acknowledge timer (sheet 5). The timer enables master processor program execution 2.0 microseconds after the start of any local I/O transfer or local ROM access. The enabling of the various ROM segments is provided by the memory address decoder (section 3.2.1)

3.3.1 EXTERNAL (PIO/IOC) I/O TRANSFERS

The I/O subsystem of the IPC controls the routing of external I/O transfers to and from the PIO and IOC. In the case of external transfers, the I/O subsystem decodes the I/O port addresses and enables the common data lines of the PIO and IOC. The port addresses also cause the I/O subsystem to generate a select signal for either the PIO or the IOC. The select signals initiate communications between the master processor and the 8041 microprocessor of the PIO or the 8080A-2 microprocessor of the IOC. These external microprocessors are, in turn, responsible for communications with I/O devices (peripherals, integral disk, and CRT/keyboard). The IOC microprocessor is also directly responsible for issuing commands to, and receiving status from, the programmable chips of the IOC. Note that although the PIO and the IOC respond in a similar manner, they are completely independent of one another.



NOTE: The number in the lower right-hand corner of each block identifies the sheet number of the IPC schematic.

Figure 3-7. IPC I/O Subsystem Block Diagram 556-21