CHAPTER 4
IOC I/O INTERFACES

The IOC consists of the hardware and software that are used to establish interfaces between a master processor and both the integral CRT terminal and the integral diskette drive. Modification of the IOC is unnecessary since most IOC functions are integrated with Intel-supplied system software. This chapter provides details of IOC-master processor protocol as a basis for user-designed master programs.

4.1 IOC/MASTER PROCESSOR PROTOCOL

All communications between the IOC and the master processor are accomplished via the data bus buffer (DBB) of the IOC. The DBB is essentially an inter-bus communications facility that stores one input byte, one output byte, and one byte of DBB status. The DBB status bits indicate the presence of data in the input and output buffers, the busy status of the IOC processor relative to command processing, and the type of byte (command or data) present in the input/output buffer.

When the IOC is not busy processing a previously issued command, it is idle only in the sense that the IOC processor is not concerned with inter-processor communications. During this time, RAM refresh and CRT refresh cycles continually occur. Also, if any keyboard entries are made, the character bytes are saved by the keyboard processor. The master processor must periodically poll the IOC to determine if keyboard entries have occurred and then command the IOC to transfer the keyboard characters to the master via the IOC's DBB.

The commands used to input keyboard characters are functionally similar to commands used to update the CRT display or to accomplish diskette data transfers in that any command must be completely processed by the IOC before a new command can be issued. However, keyboard entries may occur at any time irrespective of I/O activities initiated by the master. Any program controlling the IOC must allow time for the acceptance of new keyboard entries during the execution of any I/O operation of long duration. The frequency of keyboard input commands must be sufficient to match the keystroke rate of a fast typist; the keyboard processor provides temporary storage for up to eight characters. Keyboard entries must be handled as unscheduled real-time events by the controlling resident or non-resident program.

4.2 DATA BUS BUFFER

The IPB/IPC (or any other master processor) uses two I/O ports for communications with the IOC. The first of these ports (port C0) is a data port that provides for single byte transfers to or from the IOC. The bytes may contain data to or from a device, status from the IOC or one of its devices, or diagnostic instructions or results from the IOC. The second port (port C1) is a control port that provides for command transfers to the IOC and the return of DBB status. The commands directly control the IOC and identify the type of data, status, or diagnostic information that is to be transferred via the data port. All transfers via the data port require prior master processor issuance of a command to the IOC control port. However, a command does not necessarily result in a data port transfer.

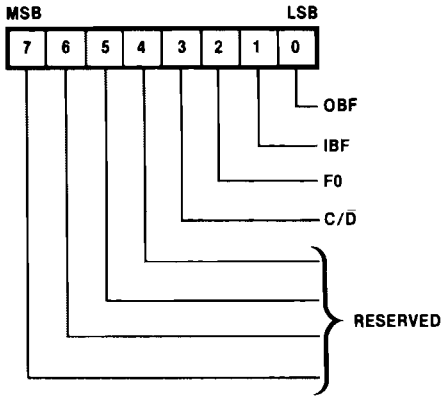
The preceding arrangement allows for the following types of transfers to and from the IOC:

- Direct transfer of DBB status without IOC participation.
- Direct control of the IOC by means of commands that do not result in a data transfer.
- Data transfers to or from a device on command.
- Status transfers from the IOC or a device on command.
- Diagnostic data transfers from the IOC on command.

Two important factors are associated with transfers between a master processor and the IOC. The first factor is that most commands cause the transfer of only one byte of data, status, or diagnostic information via the data port. If a block of information (other than diskette data) is to be transferred, a separate command is required for each byte of the block. The diskette data transfer commands (read and write) cause the transfer of a block of data to or from the master processor. The second factor is that the master processor maintains total control of transfers via the data port. The IOC, when responding to a read command, sets the F0 flag while it is executing the command and then sets the output buffer full (OBF) flag to indicate when the requested byte can be read by the master processor. Accordingly, the master processor must repeatedly access the DBB status byte to determine when the the input data is ready. Similarly, when the IOC is responding to a write command, it sets the F0 flag while it is executing the command and clears the input buffer full (IBF) flag when it accepts the byte (the master

processor sets the IBF flag when it writes the byte to the input buffer). The DBB status byte must also be accessed prior to issuing any command to ensure that the IOC is ready to accept the command (i.e., IOC busy flag F0 must be tested).

The format of the DBB status byte returned during an I/O read of port C1 is as follows:



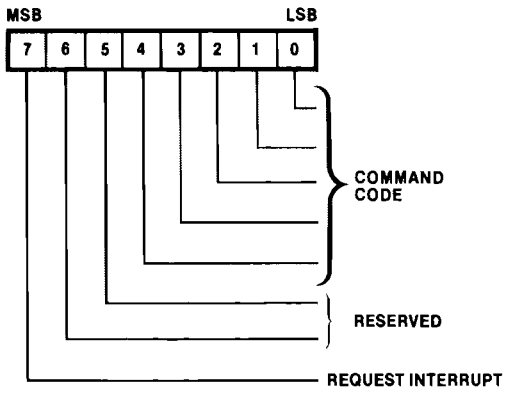
OBF Output Buffer Full. The OBF flag is automatically set (to a "1" state) by the IOC processor when the IOC writes a data byte to the output buffer. The OBF flag is automatically cleared (to a "0" state) when the master processor reads the byte from the output buffer.

IBF Input Buffer Full. The IBF flag is automatically set by the master processor when it writes a data byte to the input buffer. The IBF flag is automatically cleared when the IOC processor reads the byte from the input buffer.

F0 F0 flag. The F0 flag is set by the IOC processor on receipt of a command from the master processor in order to lockout additional command entry. On completion of the command, the IOC processor clears the F0 flag. The master processor monitors the F0 flag to determine when a command has been accepted (F0 flag set) and when command processing is complete (F0 flag clear).

C/$\overline{D}$ Command/Data. The C/$\overline{D}$ flag reflects the state of the master processor's low-order port address bit to differentiate between the writing of a data byte to port C0 (C/$\overline{D}$ = 0) and the writing of a command byte to port C1 (C/$\overline{D}$ = 1). The IOC processor examines this flag to determine if the byte in the input buffer is a command or data. The IOC processor also controls this flag to inform the master processor of the contents of the output buffer (if C/$\overline{D}$ = 0, the output buffer contains the requested data byte; if C/$\overline{D}$ = 1, the output buffer contains a status byte).

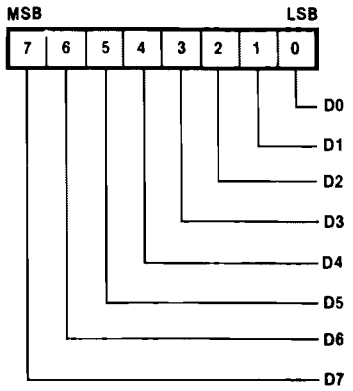
Command bytes transferred to the IOC during an I/O write to port C1 have the following general format:



Command Code is a 5-bit binary value that uniquely identifies each of the commands that may be issued by the master processor.

Request Interrupt is a control bit that informs the IOC that an interrupt is expected at the completion of the operation specified by the command. Commands that make use of the request interrupt bit include all commands that pass data to or from the CRT and the integral diskette.

Data, status and diagnostic bytes transferred via I/O port C0 have no specific format except as required by the associated command. Data bit mnemonics are as follows:



4.3 IOC COMMANDS

Specific commands are used with the diskette drive, the CRT, and the keyboard. The status byte returned by the individual I/O devices serves to verify proper operation of the device. Other commands are not used by a specific device and are known as system commands (all diagnostic commands are system commands). A complete listing of the IOC commands is provided in table 4-1.

4.3.1 SYSTEM COMMANDS

Eleven of the commands that may be issued by a master processor to the IOC are used to control or test subsystem functions that are common to all of the IOC devices. These system commands permit program-controlled hardware resetting, provide for the return of device and subsystem status, control enabling and resetting of interrupts, and enable diagnostic testing of IOC facilities. The following text describes each of the system commands and defines the format of data bytes that are transferred as a result of command execution.

NOTE

Command bit 7 has no function within the system commands (i.e., interrupts cannot be generated by the IOC on execution of a system command).

The PACIFY command is a software reset that terminates any pending I/O operation and reinitializes the IOC hardware and software. No data byte transfer is associated with this command. IOC initialization requires a minimum of 100 milliseconds, and no subsequent commands should be issued during this period.

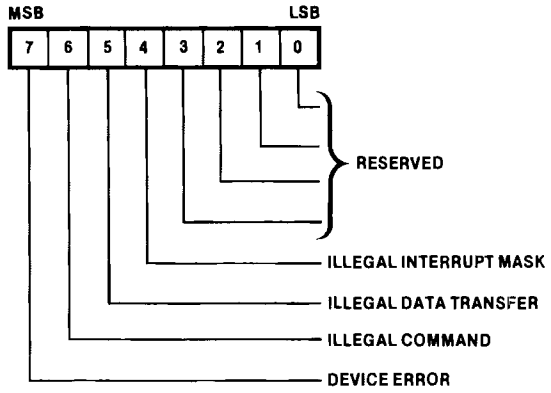
The ERESET command is intended for use with an I/O device that requires a hardware error reset to clear an error condition within the device. Since the

Table 4-1. IOC Command Set

Type	Command Code	Mnemonic	Function
System	00000	PACIFY	Resets IOC and its devices.
	00001	ERESET	Resets device-generated error (not used by standard devices).
	00010	SYSTAT	Returns subsystem status byte to master.
	00011	DSTAT	Returns device status byte to master.
	00100	SRQDAK	Enables input of device interrupt acknowledge mask from master.
	00101	SRQACK	Clears IOC subsystem interrupt request.
	00110	SRQ	Tests ability of IOC to forward an interrupt request to the master.
	00111	DECHO	Tests ability of IOC to echo data byte sent by master.
	01000	CSMEM	Requests IOC to checksum on-board ROM. Returns pass/fail.
	01001	TRAM	Requests IOC to test on-board RAM. Returns pass/fail.
	01010	SINT	Enables specified device interrupt from IOC.
	01011 thru 01111	—	Reserved, causes illegal command error.
CRT	10000	CRTC	Requests data byte output to the CRT monitor.
	10001	CRTS	Returns CRT status byte to master.
Keyboard	10010	KEYC	Requests data byte input from the keyboard.
	10011	KSTC	Returns keyboard status byte to master.
	10100	—	Reserved.
Integral Diskette	10101	WPBC	Enables input of first of five bytes that define current diskette operation.
	10110	WPBCC	Enables input of each of four bytes that follow WPBC.
	10111	WDBC	Enables input of diskette write bytes from master.
	11000	—	Reserved.
	11001	RDBC	Enables output of diskette read bytes to master.
	11010	—	Reserved.
	11011	RRSTS	Returns diskette result byte to master.
	11100	RDSTS	Returns diskette device status byte to master.
	11101 thru 11111	—	Reserved, causes illegal command error.

standard devices of the IOC do not require an error reset signal, the ERESET command is not implemented by IOC firmware.

The SYSTAT command causes the IOC processor to load the system status byte into the output data buffer of the DBB. The IOC processor sets the OBF flag and clears the C/$\overline{D}$ flag to inform the master processor that system status byte can be read from the data port. The format of the system status byte is as follows:



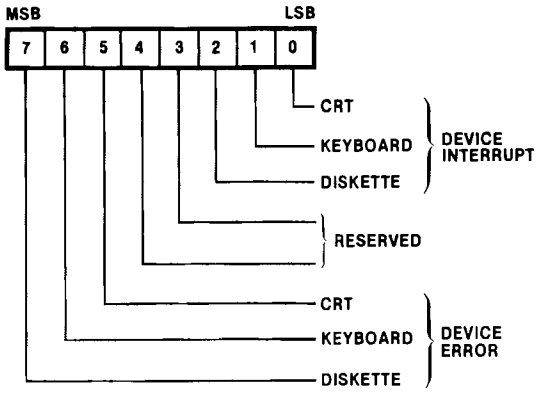
Illegal Interrupt Mask is set when the interrupt reset mask transferred by a SRQDAK command does not correspond to the interrupt bit set in the device status byte. The illegal interrupt mask bit is cleared when the master processor reads the system status byte from the output buffer.

Illegal Data Transfer is set when the master processor loads a data byte into the DBB input buffer without a preceding command. The data byte is not accepted by the IOC. The illegal data transfer bit is cleared when the master processor reads the system status byte from the output port.

Illegal Command is set when the master processor loads an undefined command code into the DBB input buffer (see table 4-1). The command is not executed by the IOC. The illegal command bit is cleared when the master processor reads the system status byte from the output buffer.

Device Error is set when a device fails to respond to a command. The master processor must issue a DSTAT command to determine the individual device responsible for the error. The device error bit is cleared by the DSTAT command.

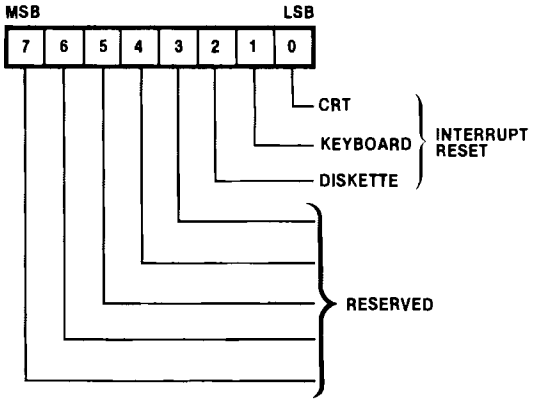
The DSTAT command causes the IOC processor to load the device status byte into the output data buffer of the DBB. The IOC processor sets the OBF flag and clears the C/$\overline{D}$ flag to inform the master processor that the device status byte can be read from the data port. The format of the device status byte is as follows:



A Device Interrupt bit is when the operation specified by a command has been completed and interrupts for the device have been enabled (request interrupt bit in the command byte set or device interrupt previously enabled by a SINT command). A device interrupt bit is cleared by a SRQDAK or SRQACK command.

A Device Error bit is set when the specified device fails to respond to a command issued by the master processor. A device error bit is cleared when the master processor reads the device status byte. More detailed error information is provided by the CRTS command (for CRT errors), the KSTC command (for keyboard errors) or the RDSTS command for diskette errors).

The SRQDAK command is used to clear a device interrupt. The subsequent data byte from the master processor to the input data buffer is as follows:



An Interrupt Reset bit, when set, clears the corresponding interrupt bit in the device status byte (see DSTAT command). Attempting to reset an interrupt bit that is not set causes the illegal interrupt mask bit to be set in the system status byte. Note that the SRQDAK command also clears the hardware interrupt to the IPB/IPC.

The SRQACK command causes the IOC to reset all of the interrupt bits in the device status byte and the hardware interrupt to the IPB/IPC. A data byte transfer is not associated with the SRQACK command.

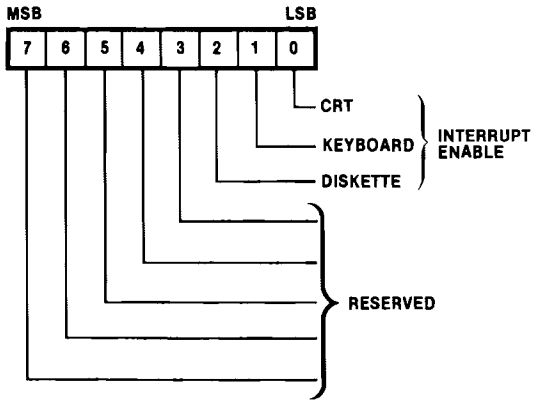
The SRQ command causes the IOC to generate a hardware interrupt to the IPB/IPC. The interrupt bits of the device status byte are not affected, and a data byte transfer is not initiated. This diagnostic command allows any master processor to test the IOC interrupt request line when all other local interrupts of the IPB/IPC are reset. The IOC interrupt request causes a level 7 interrupt request on the Multibus interface. The interrupt request is cleared by a SRQACK command.

The DECHO command causes the IOC processor to accept and return (in complemented form) the next data byte input from the master processor. Although the data byte is sent and received via I/O port C0, the path within the IOC includes a software-controlled transfer of the data byte from the DBB input data buffer to the DBB output data buffer. The entire action constitutes a fairly comprehensive test of the master processor-IOC interface. The IOC response to a DECHO command requires approximately two milliseconds.

The CSMEM command causes the IOC processor to checksum the contents of the IOC ROM and thereby perform a confidence test on the IOC firmware. If the checksum test passes, the IOC processor sets the C/$\overline{D}$ flag to zero and returns a data byte of all zeroes; if the checksum test fails, the IOC processor sets the C/$\overline{D}$ flag to one and returns a data byte of all ones. Command execution requires approximately 100 milliseconds.

The TRAM command causes the IOC processor to perform read-after-write testing of IOC RAM. If a RAM location is found to be faulty, the test is terminated, and the IOC processor sets the C/$\overline{D}$ flag to one and returns a data byte of all ones. If the test passes, the IOC processor sets the C/$\overline{D}$ flag to zero and returns a data byte of all zeros. Faulty locations are not identified. Command execution requires approximately 100 milliseconds.

The SINT command causes the IOC processor to accept an interrupt enable byte at the input data buffer of the DBB. The enabling of any interrupt bit also enables the hardware interrupt line (IOC interrupt) to the IPB/IPC. The interrupt enable bits perform a function identical to the request interrupt control bit (bit 7) of a command byte. Note that once an interrupt is enabled, it remains enabled until a subsequent SINT command is issued to clear the interrupt enable bit. The format of the interrupt enable byte is as follows:



An Interrupt Enable bit, when set, enables the interrupt from the corresponding IOC device. The format of the interrupt enable byte is identical to that of the interrupt reset byte of the SRQDAK command. Note that when any of the interrupts are enabled, the IOC interrupt to the IPB/IPC is also enabled.

4.3.2 CRT COMMANDS

All timing and formatting of the integral CRT display is established by the IOC firmware and the 8275 programmable CRT controller. The presentation of data is accomplished by transferring data from IOC RAM tables to the CRT character generating circuits. Commands from the master processor merely update the data tables. A single type of command is used to write keyboard inputs and to program responses on the CRT. A second CRT-associated command returns CRT status to the master processor.

The CRTC command causes the IOC to use the next data byte appearing at the DBB input data buffer as an input to the CRT display tables located in IOC RAM. The occurrence of the command is totally asynchronous with respect to CRT display raster timing. Furthermore, positioning of characters on the CRT screen is determined solely by a pointer that is maintained by the IOC firmware. Operator keyboard

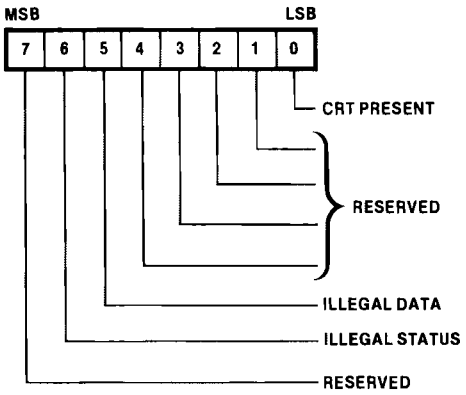
entries can alter the pointer for editing purposes, but the interpretation of the special characters used for this purpose (or any other purpose) is a function of the IOC firmware. The character codes employed are those of the ASCII set.

When operating under ISIS or Monitor, the IPB/IPC polls the DBB to determine when the IOC has accepted the CRT character byte, and interrupts are not employed (the request interrupt bit of the command byte is *not* set). When the request interrupt bit (bit 7) of the CRTC command byte is set (or if CRT interrupts have been previously enabled by a SINT command), the IOC processor will set the CRT interrupt bit in the device status byte when it writes the CRT character byte into IOC RAM and, unless IOC interrupts have been masked out by the master processor, the IOC will interrupt the IPB/IPC. In an interrupt-driven environment, the master processor should clear the CRT interrupt (SRQDAK or SRQACK command) before the next CRT character byte is written.

NOTE

Interrupt-driven programs that make use of the IOC interrupt must access the device status byte (DSTAT command) to determine the source of the interrupt.

The CRTS command causes the IOC processor to load the CRT status byte into the output data buffer of the DBB and to clear the CRT device error bit in the device status byte. The CRTS command is normally issued only in response to a CRT error as indicated by the setting of the device error bit in the system status byte and the setting of the CRT error bit in the device status byte. The format of the CRT status byte is as follows:



CRT Present is set during initialization and indicates that the IOC is operational (i.e., able to respond to commands from a master processor).

Illegal Data is set when the master processor loads a data byte into the DBB input buffer without a preceding CRTC command. The illegal data bit is cleared when the master processor reads the CRT status byte.

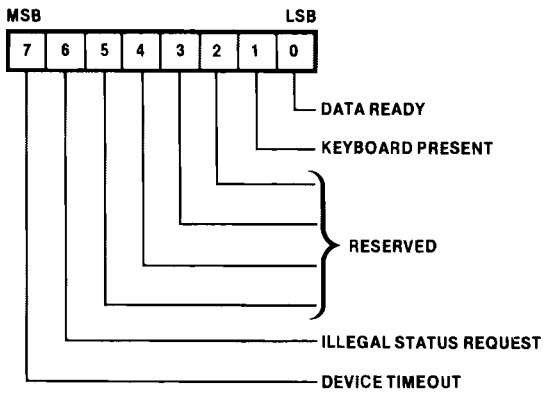
Illegal Status is set when the request interrupt bit (bit 7) of the CRTS command byte is erroneously set by the master processor. (A master processor cannot legally request an interrupt at the completion of a status accessing operation.) The illegal status bit is cleared when the master processor reads the CRT status byte.

4.3.3 KEYBOARD COMMANDS

Two commands are used with the keyboard; one command is used to access keyboard entries, and the other command is used to access keyboard status.

The KEYC command causes the IOC processor to access an ASCII character byte from the keyboard processor and to place this byte in the output data buffer. The KEYC command is the only IOC data transfer command that does not make use of the request interrupt bit in the command byte (to enable keyboard interrupts, the SINT command must be used). The format for the keyboard character bytes is established by the ASCII standard.

The KSTC command causes the IOC to access the keyboard status byte and to place this byte in the output data buffer of the DBB. When operating in the polled mode (interrupts disabled), the master processor first uses the KSTC command to determine when a character has been entered at the keyboard (by testing the data ready bit) and then uses the KEYC command to access the character byte. The KSTC command is also issued in response to a keyboard error (indicated by the setting of the device error bit in the system status byte and the setting of the keyboard device error bit in the device status byte). The format of the keyboard status byte is as follows:



Data Ready is set when a character byte is available from the keyboard processor as a result of keyboard entry.

Keyboard Present is set when the keyboard is connected to the development system. The IPB/IPC examines this bit during initialization to assign the system console device (if the keyboard present bit is set, the keyboard and integral CRT are assigned as the system console; if the keyboard present bit is clear, the device attached to one of the serial I/O channels is assigned as the system console).

Illegal Status Request is set when the request interrupt bit in the KSTC command byte is set (a master processor cannot legally request an interrupt at the completion of a status-access operation) and is cleared when the master processor reads the keyboard status byte.

Device Timeout is set when a KEYC command is issued when a character byte is not available from the keyboard processor (data ready bit clear). The device timeout bit is cleared when the master processor reads the keyboard status byte.

4.3.4 INTEGRAL DISKETTE COMMANDS

The integral diskette of the Intellec Series II development system is a random-access, mass-storage media on which information is formatted to simplify access and to utilize available storage space. Accordingly, a significant amount of control information must be passed to the diskette and its control circuits. Some control information such as sector size may be fixed and can be established during system initialization. Other information, such as the size of a file to be recorded and the availability of storage space, can only be determined immediately prior to recording the file and requires active participation on the part of the master program.

The need to provide for master program control of diskette recording plus the fact that data transfers occur in two directions (diskette read or write) substantially increases the number of commands that must be issued to the IOC. Furthermore, two types of status bytes are returned by the IOC processor; one to indicate the success of IOC/master interactions and the other to indicate the results of IOC/diskette drive interactions. The six commands required to transfer diskette control, data, and status bytes are listed in table 4-1.

Most of the control information supplied to the IOC is provided in the form of five bytes that are referred to as the I/O parameter block (IOPB). These bytes specify the diskette operation to be performed and provide formatting information including the number of records (sectors) to be transferred and the track and sector addresses.

The diskette commands are associated with two interfaces; the interface between the IOC and a master processor and the interface between the IOC processor and the diskette. The diskette read and write commands (RDBC and WDBC) transfer data between the master processor and IOC RAM. Conversely, the parameter block write commands (WPBC and WPBCC) load the I/O parameter block into IOC RAM; the contents of the parameter block are used to define and initiate data transfers between IOC RAM and the diskette. The read drive status command (RDSTS), in addition to defining the current status of the drive, indicates incorrect command entry or execution. The read result status command (RRSTS) is used to verify the result of a diskette operation.

Diskette data transfers must be viewed as two separate operations; the transfer of the data block between a master processor and IOC RAM and the transfer of the data block between IOC RAM and the diskette. Data block transfers between IOC RAM and the diskette are automatically initiated when the last byte of the I/O parameter block is written into IOC RAM. Accordingly, in order to write data on the diskette, the data block must first be written into IOC RAM before the parameter block is written. Conversely, in order to read a data block from the diskette, the parameter block must precede the reading of the data block from IOC RAM. Typical command sequences for diskette read and write operations are outlined in table 4-2.

The WPBC command causes the IOC processor to accept the next data byte at the DBB input data buffer as the first (channel word) byte of a parameter block. The IOC processor writes this data byte into a preassigned location in IOC RAM. The request interrupt bit of the command byte, if set, causes a diskette device interrupt to be generated when the byte is written into RAM. The format and function of the first parameter block byte are discussed following the description of the WPBCC command.

The WPBCC command causes the IOC processor to accept the next data byte at the DBB input data buffer as one of the subsequent I/O parameter block bytes. The IOC processor writes the byte into IOC RAM and, if the request interrupt bit is set in the

Table 4-2. Typical Diskette Read and Write Command Sequences

Read Sequence	
Command	**Action**
RDSTS	Determine if drive is ready
WPBC	Input IOPB Channel Word byte
WPBCC	Input IOPB Diskette Instruction byte
WPBCC	Input IOPB Sector Count byte
WPBCC	Input IOPB Track Address byte
WPBCC	Input IOPB Sector Address byte
RDSTS	Determine when operation is complete (polled mode)
RRSTS	Determine if operation was successful
RDBC	Output data block from IOC RAM
Write Sequence	
Command	**Action**
RDSTS	Determine if drive is ready
WDBC	Input data block to IOC RAM
WPBC	Input IOPB Channel Word byte
WPBCC	Input IOPB Diskette Instruction byte
WPBCC	Input IOPB Sector Count byte
WPBCC	Input IOPB Track Address byte
WPBCC	Input IOPB Sector Address byte
RDSTS	Determine when operation is complete (polled mode)
RRSTS	Determine if operation was successful

NOTE:

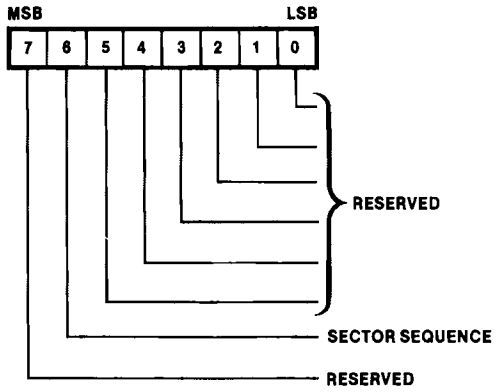
1. First byte of data block input to IOC from master processor contains sector count that is multiplied by 128 by the IOC to determine the number of bytes to be transferred.

command byte, generates a diskette device interrupt when the byte is written. The data byte being written into IOC RAM is either the second, third, fourth or fifth byte of the I/O parameter block. The byte written and the IOC RAM location selected are determined by the occurrence of the WPBC command and any subsequent WPBCC command. In other words, the WPBC command serves as a reference for the I/O parameter block and the following four WPBCC commands load the four remaining parameter bytes in consecutive RAM locations. Accordingly, the parameter block bytes must be presented in sequence, and any detected error requires reentry of the entire I/O parameter block. The sequence in which I/O parameter block bytes are input is indicated in table 4-2.

NOTE

Further details on programming diskette operations are provided in the 8271 Programmable Floppy Disk Controller data sheet.

The format of the I/O parameter block Channel Word byte (byte 1) associated with the WPBC command is as follows:

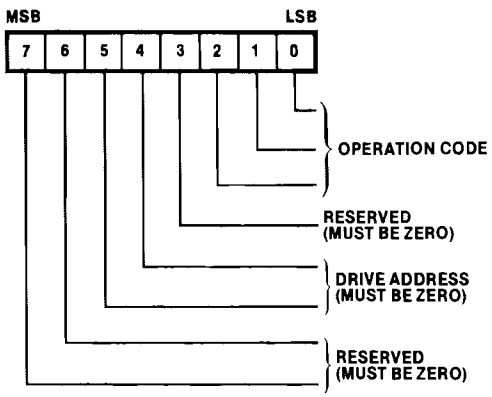


The sector sequence bit (bit 6) is only examined when a format track operation is specified in the diskette instruction byte (byte 2) of the I/O parameter block. When the sector sequence bit is set, the "random" sector format is selected, and the diskette controller

accesses a format table in IOC RAM to determine the order in which logical sector addresses are assigned when formatting the track. The format table consists of 26 data byte pairs. The first byte of each pair is a sector address ranging from 1 to 26 (01H-1AH); the second byte can contain any value and is required only to maintain compatibility with the Intel two-board diskette controllers. The format table must be written into IOC RAM (using the WDBC command) prior to initiating the format track operation. The format table itself begins at the same predefined location in IOC RAM that is used to temporarily store diskette data. The first entry in the table is the sector count byte (see WDBC command description) and contains a value of 01H (the IOC processor multiplies the sector count value by 128 to determine the number of consecutive RAM locations to be written by the WDBC command). During the format track operation, the diskette controller writes the first sector address entry from the table into the ID field of physical sector 01 (the first sector following the index mark), the second sector address table entry into physical sector 02, etc., until all 26 sectors have been written. The track address written into the ID field is taken directly from the track address byte (byte 4) of the I/O parameter block. The sector data marks, CRC characters and gaps are supplied by the diskette controller, and the data field of each sector is filled with 128 bytes of 0E5H.

When the sector sequence bit is clear, the "sequential" sector format is selected. The format track operation follows the random sector format description of the previous paragraph with the exception that the sector addresses are assigned in sequential order (i.e., physical sector 01 is assigned logical sector address 01, physical sector 02 is assigned logical sector 02, etc.) by the diskette controller, and a format table is not required.

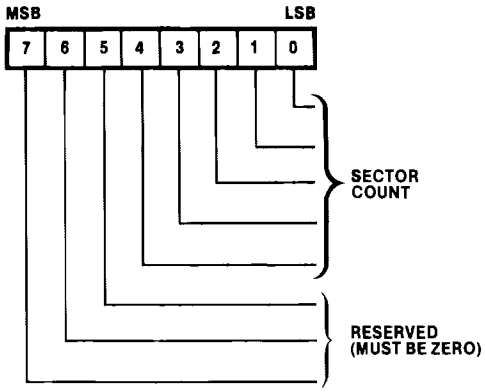
The format of the I/O parameter block Diskette Instruction byte (byte 2) is as follows:



Drive Address. Bits 4 and 5 specify the drive address. The integral drive is assigned unit 0, and bits 4 and 5 must both be zero.

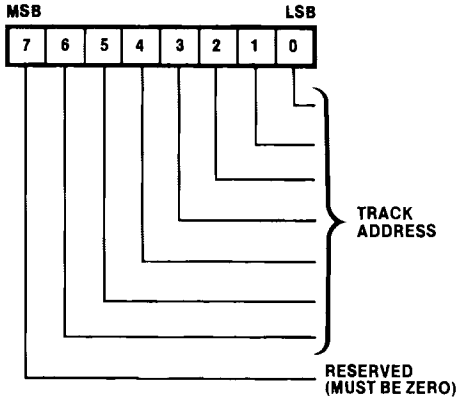
Operation Code. Bits 0, 1 and 2 specify the diskette operation to be performed. Operation code functions are outlined in table 4-3.

The format of the I/O parameter block Sector Count byte (byte 3) is as follows:



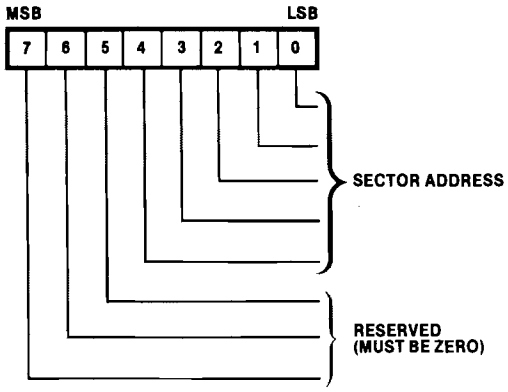
The Sector Count byte specifies the number of sectors to be accessed during a diskette read, write or verify operation. The combined value of the sector count and the (starting) sector address (byte 5 of the I/O parameter block) cannot be greater than 26 (1AH). Note that if the sector count value is 0H, one sector is transferred.

The format of the I/O parameter block Track Address byte (byte 4) is as follows:



The Track Address byte specifies the track to be accessed during a subsequent diskette seek, read or write operation. Since a diskette has 77 tracks, legal values range from 00H to 4CH (tracks 0 through 76).

The format of the I/O parameter block Sector Address byte (byte 5) is as follows:

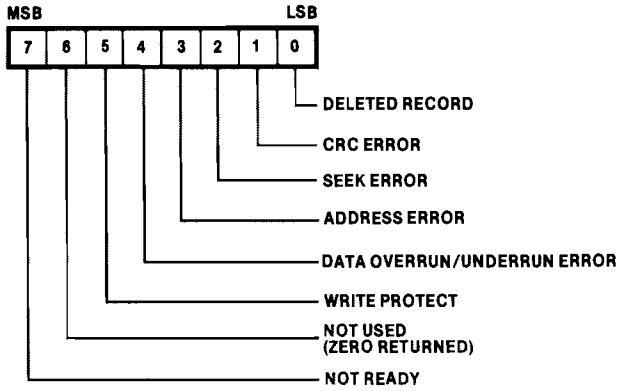


The Sector Address byte specifies the sector or the first of a series of sectors to be accessed during a subsequent diskette read, write or verify operation. Legal values range from 01H to 1AH (1-26).

The WDBC command causes the IOC processor to read-in a block of data bytes through the DBB input data buffer and to write the data bytes into sequential locations in IOC RAM. The WDBC command is used prior to a write data or format track (random format only) diskette operation to load the data to be written on the diskette into IOC RAM. The first byte transferred by the WDBC command is a count byte that specifies the number of 128-byte blocks to follow (the count byte is not written into RAM; the IOC multiplies the value by 128 to determine the extent of the transfer). Note that while the format table associated with the format track operation only requires 52 byte entries, 128 bytes are transferred by the WDBC command. The request interrupt bit of the WDBC command byte, when set, causes a diskette device interrupt to be generated when the specified number of data bytes have been written into IOC RAM.

The RDBC command causes the IOC processor to place sequential data bytes from IOC RAM into the DBB output data buffer and is issued following a read data diskette operation to allow a master processor to access the data read from the diskette. The number of bytes transferred by a RDBC command is dependent on the number of sectors read during the previous read data operation (specified by byte 3 of the associated I/O parameter block). When the request interrupt bit is set in the RDBC command byte, a diskette device interrupt is generated when the master processor reads-in the last data byte from the DBB output data buffer.

The RRSTS command is issued when a diskette device error is indicated in the device status byte and causes the IOC processor to place the diskette controller's result byte in the DBB output data buffer. The diskette device error bit is cleared when the master processor reads the result byte. The individual bits of the result byte are defined as follows:



Deleted Record is set when an attempt is made to read or verify a deleted sector (a sector that has previously been rewritten with a deleted data mark at the beginning of its data field). If the deleted record bit is set, the data is not transferred or verified.

CRC Error is set when the CRC character computed for a read data or verify CRC operation does not match the CRC character generated when the sector was written. Since this error is not detected until the sector is read, the data in IOC RAM must be considered invalid.

Seek Error is set during a read, write or verify operation when the addressed sector cannot be located within one complete revolution or when the track address specified does not match the track address read. If the seek error bit is set, no data is transferred, and a recalibrate operation should be performed to position the drive's read/write head at a known location.

Address Error is set when:

- the track address specified is greater than 76 (4CH).
- a sector address of 00H is specified.
- a sector address greater than 26 (1AH) is specified.
- the sector address and the number of sectors specified is greater than 26 (1AH).

Table 4-3. Diskette Operation Codes

Operation Code Bit 2	Bit 1	Bit 0	Operation	Function
0	0	0	No Operation	No operation. The diskette controller immediately sets the operation complete status bit in the diskette device status byte when the last I/O parameter block is written.
0	0	1	Seek	Initiates a seek operation to the track address specified in byte 4 of the I/O parameter block and sets the operation complete status bit in the diskette device status byte.
0	1	0	Format Track	Initiates a seek operation to the track address specified in byte 4 of the I/O parameter block. When the complete track has been formatted, the diskette controller sets the operation complete status bit.
0	1	1	Recalibrate	Steps the diskette drive's read/write head out until a track 0 indication is received from the drive. When track 0 is located, the diskette controller sets the operation complete status bit.
1	0	0	Read Data	Initiates a seek operation to the track address specified in byte 4 of the I/O parameter block and begins reading the sector ID fields until the sector addressed in byte 5 of the I/O parameter block is located. When the addressed sector is located, transfer the data contents of the number of sectors specified by byte 3 of the I/O parameter block to IOC RAM. When the transfer is complete, the diskette controller sets the operation complete status bit.
1	0	1	Verify CRC	Identical to the read data operation except that no data is transferred to IOC RAM. If an error is detected (i.e., if the data read does not match the data previously written), the diskette controller sets the CRC error bit in the result status byte. The operation complete status bit is set when the operation is complete (or if an error is detected).
1	1	0	Write Data	Initiates a seek operation to the track address specified in byte 4 of the I/O parameter block and begins reading the sector ID fields until the sector addressed in byte 5 of the I/O parameter block is located. When the addressed sector is located, reads in the data from IOC RAM and serially writes the data into the sector's data field. When the number of sectors specified by byte 3 of the I/O parameter block have been written, the diskette controller sets the operation complete status bit.
1	1	1	Write Deleted Data	Identical to the write data operation except that a deleted data mark is written in place of the data address mark at the beginning of the data field.

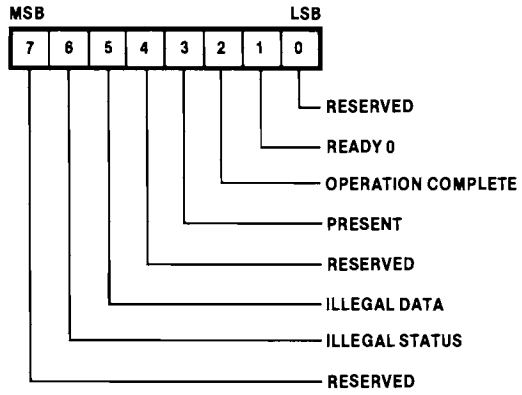
Data Overrun/Underrun Error is set when the diskette controller is unable to write a data byte to RAM before it is overwritten or when the requested data byte is not received from RAM in time to be written on the diskette.

Write Protect is set when an attempt is made to format or write to a write-protected diskette. When this bit is set, the operation is prevented, and no data is written on the diskette.

Not Ready is set when the diskette drive is not ready to perform a seek, read or write operation (i.e., the door is open or a diskette is not installed).

The RDSTS command causes the IOC processor to place the diskette status byte in the DBB output data buffer. The RDSTS command is used prior to a diskette operation to determine if the drive is ready

and is used in the polled mode (interrupts disabled) to determine when the operation has been completed. The format of the diskette status byte is as follows:



Ready 0 is set when the diskette is ready to perform a seek, read or write operation (i.e., the diskette is in place and up to speed).

Operation Complete is set when the specified operation has been completed or when the operation cannot be completed as a result of an error condition. When this bit is set, the device status byte and/or the controller's result byte should be examined.

Present is set when the integral diskette drive is physically connected to the IOC circuit board.

Illegal Data is set when the master processor loads a data byte into the DBB input data buffer without a preceding integral diskette command.

Illegal Status is set when the request interrupt bit (bit 7) of an RDSTS or RRSTS command is set by a master processor (a master processor cannot request an interrupt at the completion of a status-access operation).