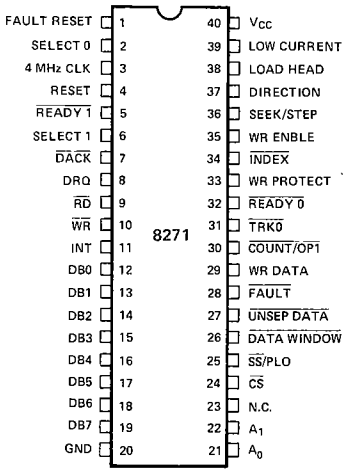
8271
PROGRAMMABLE FLOPPY DISK CONTROLLER

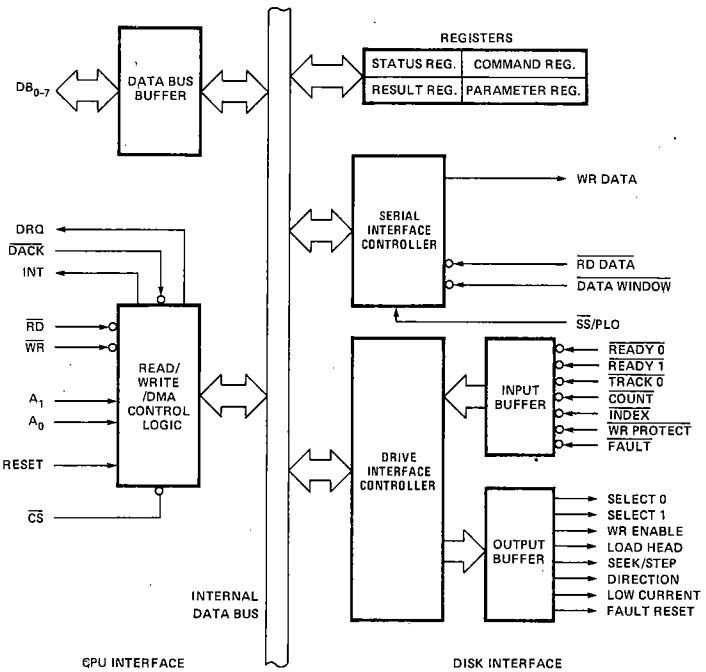
- IBM 3740 Soft Sectored Format Compatible
- Programmable Record Lengths
- Multi-Sector Capability
- Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives
- Automatic Read/Write Head Positioning and Verification
- Internal CRC Generation and Checking
- Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count
- Fully Compatible with 8080 CPU
- Single +5Volt Supply
- 40 Pin Package

The 8271 Floppy Disk Controller (FDC) is a single chip device designed to interface from one to four floppy disk drive to the 8080 microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk interface.

PIN CONFIGURATION



BLOCK DIAGRAM



General

The 8271 Floppy Disk Controller (FDC) LSI component is designed to interface from one to four floppy disk drives to an eight bit microcomputer.

The FDC supports a soft sectored format that is IBM 3740 compatible. This component is a high level controller that relieves the CPU (and user) of many of the control tasks associated with implementing a floppy disk interface. The FDC supports a variety of high level instructions which allow the user to store and retrieve data on a floppy disk without dealing with the low level details of the disk operation.

In addition to the standard read/write commands a scan command is supported. The scan command allows the user program to specify a data pattern and instruct the FDC to search for that pattern on a track. Any application that is required to search the disk (such as point of sale price lookup, disk directory search, etc.) for information may use the scan command to reduce the CPU overhead. Once the scan operation is initiated, no CPU intervention is required.

Hardware Description

The 8271 is packaged in a 40 pin DIP. The following is a functional description of each pin.

Pin Name	I/O	Description
V_{CC}	PWR	+5V supply
GND	PWR	Ground
4MHz Clock	I	A 4MHz ±1% square wave clock
Reset	I	A high signal on the reset input will force the 8271 to an idle state. The 8271 will remain idle until a command is issued by the CPU. The drive interface output signals are forced low.
$\overline{CS}$	I	The I/O Read and I/O Write inputs are enabled by the chip select signal.
DB_7-DB_0	I/O	The Data Bus lines are bidirectional three-state lines (8080 data bus compatible).
$\overline{WR}$	I	The Write signal is used to signal the control logic that a transfer of data from the data bus to the 8271 is required.
$\overline{RD}$	I	The Read signal is used to signal the control logic that a transfer of data from the 8271 to the data bus is required.
INT	O	The interrupt signal indicates that the 8271 requires service.
A_1–A_0	I	These two lines are used to select the destination of source of data to be accessed by the control logic.
DRQ	O	The DMA request signal is used to request a transfer of data between the 8271 and memory.
$\overline{DACK}$	I	The DMA ACK signal notifies the 8271 that a DMA cycle has been granted.
Select 1– Select 0	O	These lines are used to specify the selected drive.
Fault Reset	O	The fault reset line is used to reset an error condition which is latched by the drive.
Write Enable	O	This signal enables the drive write logic.
Seek/Step	O	This multi-function line is used during drive seeks.
Direction	O	The direction line specifies the seek direction.
Load Head	O	The load head line causes the drive to load the Read/Write head load pad against the diskette.
Low Current	O	This line notifies the drive that track 43 or greater is selected.
$\overline{\text{Ready 1}}$, $\overline{\text{Ready 0}}$	I	These two lines indicate that the specified drive is ready.
$\overline{Fault}$	I	This line is used by the drive to specify a file unsafe condition.
$\overline{Count/OP1}$	I	If the seek / direction / count seek mode is selected, the count pin is pulsed for each track. Otherwise this pin is user specified optional input.
$\overline{\text{Write Protect}}$	I	This signal is used to specify if the drive/diskette may be written.
$\overline{TRK0}$	I	This signal indicates when the R/W head is positioned over track zero.
$\overline{Index}$	I	The index signal gives an indication of the relative position of the diskette.
$\overline{SS/PLO}$	I	This pin is used to specify the type of data separator used.
Write Data	O	Composite write data.
$\overline{\text{Unseparated}}$ $\overline{\text{Data}}$	I	This input is the unseparated data and clocks.
$\overline{\text{Data Window}}$	I	This is a data window established by the single-shot or phase-locked oscillator data separator.

Principles of Operation

The 8271 is fully compatible with the 8080 system Bus. As an 8080 peripheral device, it accepts commands from the CPU, executes these Commands and provides a Result back to the 8080 CPU at the end of execution.

Communication with the CPU are through the activating of $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ pins. The A_1,A_0 select the appropriate registers on chip:

A1	A0	CS RD	CS WR
0	0	Status Reg	Command Reg
0	1	Result Reg	Parameter Reg

The FDC chip operation is composed of the following general sequence of events:

The Command Phase

During the Command Phase, the CPU issues a command byte to the 8271. The command byte provides a general description of the type of operation requested. Many operations require more detailed information about the comand. In such case, from zero to five parameters are written following the command byte to provide such information. The various commands that the 8271 can recognize are listed in the Software Operation Section.

The Execution Phase

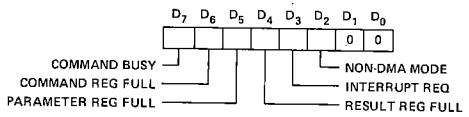
Soon as the last parameter is written into the 8271, the FDC enters the Execution Phase. During this phase there is no need for CPU involvement. The FDC may optionally interface with the 8257 (DMA controller) for high speed data transfers (See System Diagram).

The Result Phase

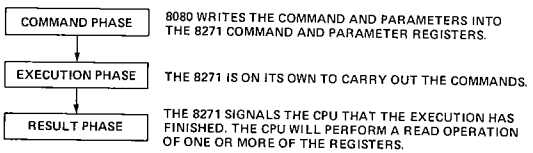
During the Result Phase, the FDC chip notified the CPU of the outcome of the command execution. This phase may be initiated by:

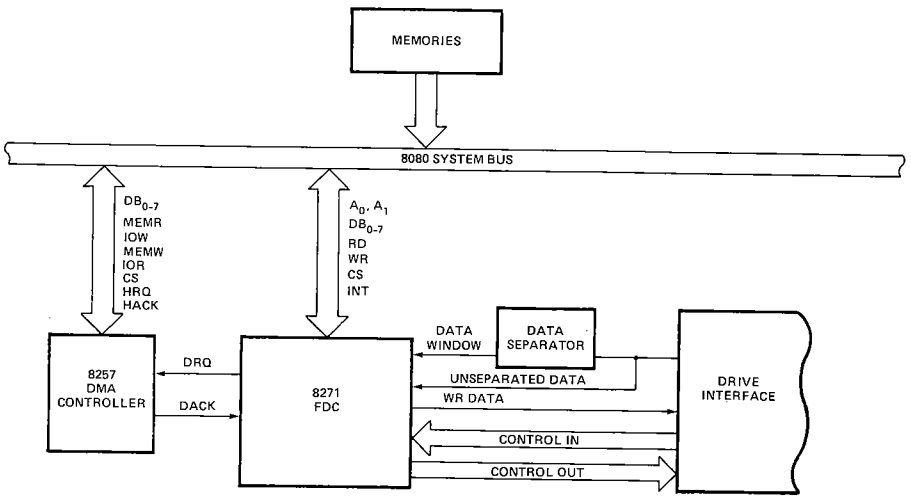
1. The successful completion of an operation.
2. An error detected during an operation.
3. An illegal command or parameter detected during the Command Phase.

In the Result Phase, the CPU Reads the Status Register which provides the following information:



After reading the Status Register, the CPU then Reads the Result Register for more information.





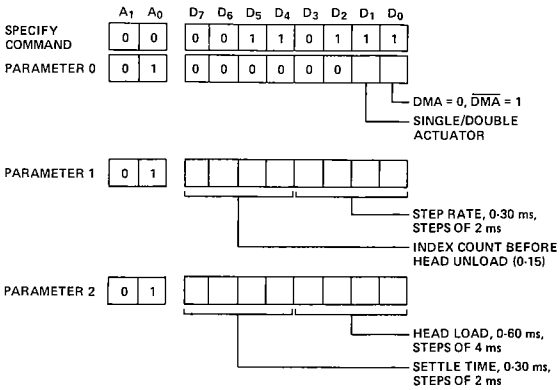
8271 SYSTEM DIAGRAM

Software Operation

The 8271 can accept many powerful commands from the CPU. The following is a list of Basic Commands (associated Parameters not shown).

- SCAN DATA
- SCAN DATA AND DELETED DATA
- WRITE DATA
- WRITE DATA AND DELETED DATA
- READ DATA
- READ DATA AND DELETED DATA
- READ ID
- VERIFY DATA AND DELETED DATA
- FORMAT
- RECALIBRATE
- SEEK
- READ DRIVE STATUS
- LOAD BAD TRACKS
- SPECIFY
- RESET

As an example, the SPECIFY command is associated with 3 parameters:



EXECUTION PHASE BASIC CHARACTERISTICS

The following table summarizes the various commands with corresponding execution phase characteristics.

	1	2	3	4	5	6	7	8
COMMANDS	**Deleted Data**	**Head**	**Ready**	**Write/ Protect**	**Seek**	**Seek Check**	**Result**	**Completion Interrupt**
SCAN DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
SCAN DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
WRITE DATA	x	LOAD	√	√	YES	YES	YES	YES
WRITE DEL DATA	x	LOAD	√	√	YES	YES	YES	YES
READ DATA	SKIP	LOAD	√	x	YES	YES	YES	YES
READ DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
READ ID	x	LOAD	√	x	YES	NO	YES	YES
VERIFY DEL DATA	XFER	LOAD	√	x	YES	YES	YES	YES
FORMAT	x	LOAD	√	√	YES	NO	YES	YES
RECALIBRATE	x	–	x	x	YES	NO	YES	YES
SEEK	x	–	x	x	YES	NO	YES	YES
READ DRIVE STAT	x	–	x	x	NO	NO	YES	NO
LOAD BAD TRACKS	x	–	x	x	NO	NO	YES	NO
SPECIFY	x	–	x	x	NO	NO	NO	NO
RESET	x	UNLOAD	x	x	NO	NO	NO	NO

Note: 1. "x" → DON'T CARE
2. "√" → check
3. "–" → No change