

ISBC 254™ BUBBLE MEMORY BOARD

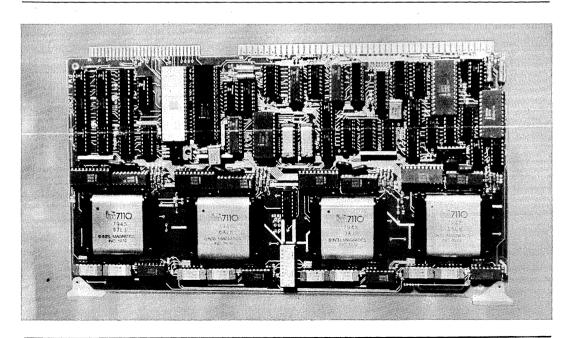
- 128K Byte to 512K Byte Capacity on Single iSBC™ Board
- 48MS Average Access Time
- Low Power Consumption35 Watts for 512 KB Version

- Non-Volatile Storage
- Multiple I/O Modes, Including DMA
- Driver Software for Operation with RMX 80/86

The iSBC 254[™] is a non-volatile memory utilizing the Intel 7110 one-megabit bubble memory element. The board is offered in three capacities: 128K, 256K, or 512K bytes.

The iSBC 254 can be operated in three I/O modes: polled status, interrupt-driven, or DMA. The 128K byte version can operate at a maximum transfer rate of 12.5K bytes per second. The multiple bubble elements of the 256K byte and 512K byte versions can be accessed in parallel to achieve maximum transfer rates of 25K and 50K bytes per second, respectively.

The physical outline of the iSBC 254 is the standard 12 inch by 6.75 inch iSBC card format. The depth of the board, however, is 0.62 inches, requiring two normally spaced card slots for adequate mechanical clearance. Power requirements for the iSBC 254 are 4 Amps at +5 volts and 1.2 Amps at +12 volts, maximum.



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OPERATIONAL DESCRIPTION

Three distinct modes of operation relate to the transfer of data. Each is briefly described below.

Data Transfer

In DMA (Direct Memory Access) Mode, the iSBC 254 board utilizes the Intel 8257 DMA Controller, in conjunction with the 7220 Bubble Memory Controller, to perform three distinct types of DMA operation: DMA Read, DMA Write, and DMA Verify. In a DMA Read operation, data is transferred from memory to the FIFO (first-in/first-out RAM) of the 7220 BMC (Bubble Memory Controller). In a DMA Write operation, data is transferred from the 7220 BMC FIFO to memory. In a DMA Verify operation, the iSBC 254 board gains control of the bus, but no actual transfer of data takes place. DMA Read and DMA Write operations are used for high-speed data transfers involving bus accessible memory; DMA Verify operations are typically used to maintain control of the system bus while verification tasks, such as checking newly acquired data, are being performed.

In Polled Mode, the CPU periodically checks the Status Register of the 7220 BMC. The Status Register can indicate a variety of conditions, one of which is that the BMC FIFO is ready to receive data or that the FIFO contains data to be read.

In DRQ (Data Request) Mode, when the FIFO of the 7220 BMC is half empty (during a write operation) or half full (during a read operation), the DRQ pin becomes active and an interrupt is issued, signalling that data may be written (bus to iSBC 254 board) or read (iSBC 254 board to bus).

Two distinct modes of operation relate to monitoring the bubble memory board status (via the 7220 Bubble Memory Controller). Each is briefly described below.

Status Monitoring Modes

In Interrupt Mode, a change in the 7220 BMC Status Register will cause an interrupt to occur, and the host processor will then look at that register to see what change has occurred. Any of the following may be indicated: the BMC sequencer is busy; an operation has been completed; an operation has failed; a timing error has occurred; and/or a correctable, uncorrectable, or parity error has occurred.

In Polled Mode, as described above under Data Transfer, the CPU periodically checks the Status Register of the 7220 BMC. The Status Register can indicate a variety of conditions: that the BMC Sequencer is busy; that an operation is complete; that an operation has failed; that a timing error has occurred; that a correctable, uncorrectable, or parity error has occurred; or, in terms of data transfer, that the BMC FIFO is ready to receive data or that the FIFO contains data to be read.

SOFTWARE DESCRIPTION

The iSBC 254 board can run under either the iRMX/80 or the iRMX/86 operating system.

Under the iRMX/80 operating system, the Bubble Manager (BMGR), a software task that runs with the iRMX/80 operating system, keeps track of free or available space on the Magnetic Bubble Memory. Another task, Bubble I/O (BUBIO), controls all iSBC 254 board operations. Bubble I/O can run with or without the Bubble Manager.

Under the iRMX/86 operating system, the iSBC 254 board is supported as an integral part of the I/O system software, which is part of the iRMX/86 operating system. (The iRMX/86 operating system device driver for the iSBC 254 board is linked with the I/O system software, which is in turn linked with the iRMX/86 operating system.) Because the iRMX/86 operating system.) Because the iRMX/86 operating system all devices "look" the same when running under this operating system, and because of a variety of built-in features, the the iRMX/86 operating system provides great flexibility.

Software programs on both single- and double-density diskettes are provided with the iSBC 254 board. EX-254 is a set of programs that demonstrates how to use the various iSBC 254 board software commands.



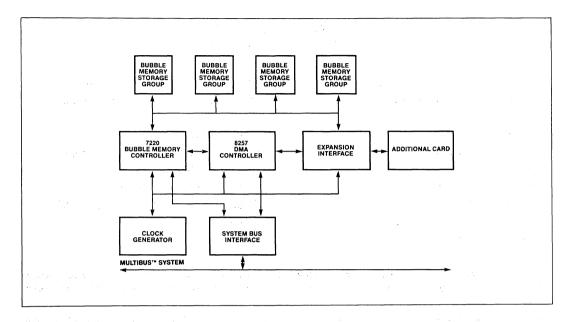


Figure 1. iSBC 254™ Board, Block Diagram

SPECIFICATIONS

Memory Size

128K, 256K, or 512K bytes

Interface

All address, data, and control signals are TTL-compatible and Intel MULTIBUS system compatible.

Electrical Characteristics

D.C. Power

+5 volts D.C. ±5%, 3.0A (max.)

+12 volts D.C. ±5%, 1.4A (max.)

Performance

Rotating Field Rate: 50KHz

Maximum Data Rate: 50K bytes/second

Average Access Time: 48ms

Connector

86-pin double-sided PC edge connector with 0.40 cm

(0.156 in.) contact centers.

Mating Connector: Control Data VFB01E43D0A1 or

Vikina 2VH43/1ANE5.

Physical Characteristics

Length: 30.48 cm (12 in.) Height: 17.15 cm (6.75 in.)

Depth: 1.57 cm (0.62 in.)

Note: Because of its depth, the iSBC 254 board requires

two card slots.

Environment

Board Operating Temperature: 0-55°C

Equipment Supplied

iSBC 254 Bubble Memory Board

iSBC 254 Operation Manual

iSBC 254 Software (single- and double-density

diskettes)