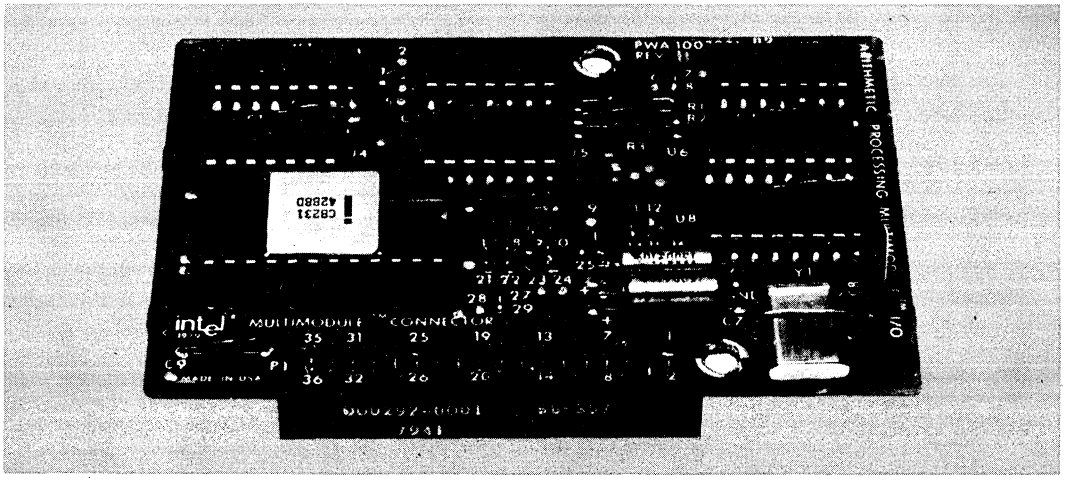
iSBX™ 331
FIXED/FLOATING POINT MATH MULTIMODULE BOARD

- **iSBX™ bus compatible high speed fixed/floating point math expansion**
- **4 MHz operation**
- **Fixed point single and double precision (16/32-bit)**
- **Floating point double precision (32-bit)**
- **Binary data formats**
- **Add, subtract, multiply and divide**
- **Trignometric and inverse trigonometric functions**
- **Square root, log, and exponential functions**
- **Float-to-fixed and fixed-to-float conversions**
- **End of operation interrupt**
- **Software reset control**
- **Low power requirements**
- **iSBX™ bus on-board expansion eliminates MULTIBUS® system bus latency and increases system throughput**

The Intel® iSBX 331 Fixed/Floating Point Math MULTIMODULE Board is a member of Intel's new line of iSBX bus compatible MULTIMODULE products. The iSBX MULTIMODULE board plugs directly into any iSBX bus compatible host board offering low cost incremental on-board expansion. As a result, any iSBX bus compatible host board may be expanded to perform high speed math computations, affording up to a 40× improvement in speed compared to software math. The iSBX 331 module performs single/double (16/32-bit) precision fixed point plus double (32-bit) precision floating point arithmetic operations. In addition, the module performs transcendental, data manipulation, and fixed to float/float to fixed point conversion operations. The command operations run entirely independent of the host board permitting efficient concurrent processing. The iSBX board is closely coupled to the host board through the iSBX bus, and as such, offers maximum on-board performance and frees MULTIBUS system traffic for other system resources. Incremental power dissipation is minimal requiring only 2.73 watts.



FUNCTIONAL DESCRIPTION

The iSBX 331 module uses the Intel 8231 Arithmetic Processing Unit (APU) to accomplish high speed (4 MHz) math operation. The system software may communicate with the iSBX 331 module across the iSBX bus using I/O read/write commands. All transfers, including operand, result, status, and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and commands are issued to perform operations on the data. Results are then available from the stack. A status byte may be read to monitor execution completion and the nature of the result (zero, sign, or errors). In addition, control logic is included on the iSBX 331 module to facilitate single instruction software reset control.

Command Functions

The iSBX 331 module commands fall into three categories: double precision floating point, single precision fixed point, and double precision fixed point (see Table 1). There are four arithmetic operations that can be performed in either fixed or floating point numbers: add, subtract, multiply, and divide. These operations require two operands. The 8231 assumes these operands are located in the internal stack as Top of Stack (TOS) and Next on Stack (NOS). The result will always be returned to TOS. There are four types of transcendental operations that can be performed in floating point numbers: trigonometric functions, logarithms, exponentials, and square roots. The results of these operations will be returned to TOS. There are four types of data manipulation operations that can be performed in either fixed or floating point numbers: sign change of TOS, exchange of TOS and NOS and copying or popping operands onto or off of TOS. Fixed to floating point conversion can be performed on floating point instructions and floating point to fixed point conversion can be performed on fixed point instructions.

The execution times of the commands are shown in Table 2.

Interrupt Requests

There is one interrupt line from the APU that may generate an interrupt request to the host: END (MINTRI). The END interrupt line is active upon command completion. The END signal is cleared by a reset or status register read.

Installation

The iSBX 331 module plugs directly into the female iSBX connector on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figures 1 and 2).

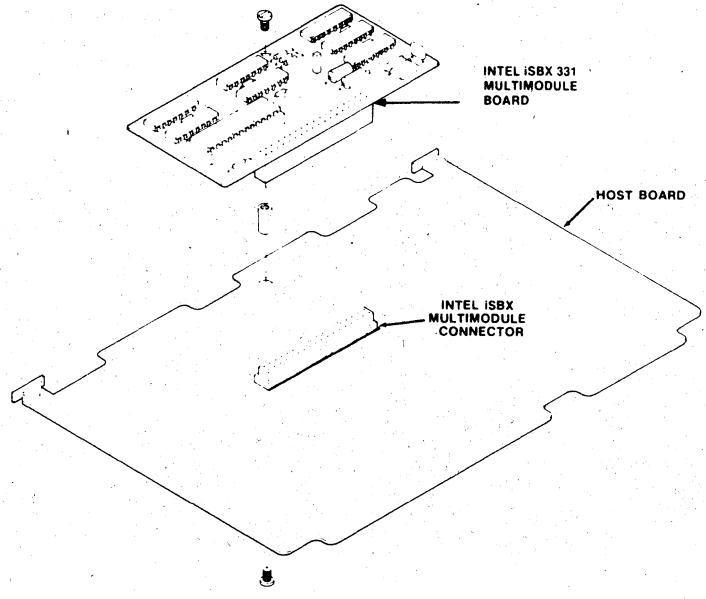


Figure 1. Installation of iSBX™ 331 Module on a Host Board

Table 1. Command Summary

Double Precision Floating Point Instructions (32-Bit)

Instruction	Description	Hex Code	Stack Contents After Execution[1] A B C D	Status Flags Affected[3]
ACOS	Inverse Cosine of A	0 6	R U U U	S, Z, E
ASIN	Inverse Sine of A	0 5	R U U U	S, Z, E
ATAN	Inverse Tangent of A	0 7	R B U U	S, Z
CHSF	Sign Change of A	1 5	R B C D	S, Z
COS	Cosine of A (radians)	0 3	R B U U	S, Z
EXP	e^A Function	0 A	R B U U	S, Z, E
FADD	Add A and B	1 0	R C D U	S, Z, E
FDIV	Divide B by A	1 3	R C D U	S, Z, E
FLTD	32-Bit Fixed to Floating Point Conversion	1 C	R B C U	S, Z
FLTS	16-Bit Fixed to Floating Point Conversion	1 D	R B C U	S, Z
FMUL	Multiply A and B	1 2	R C D U	S, Z, E
FSUB	Subtract A from B	1 1	R C D U	S, Z, E
LOG	Common Logarithm (base 10) of A	0 8	R B U U	S, Z, E
LN	Natural Logarithm of A	0 9	R B U U	S, Z, E
POPF	Stack Pop	1 8	B C D A	S, Z
PTOF	Stack Push	1 7	A A B C	S, Z
PUPI	Push π onto Stack	1 A	R A B C	S, Z
PWR	B^A Power Function	0 B	R C U U	S, Z, E
SIN	Sine of A (radians)	0 2	R B U U	S, Z
SQRT	Square Root of A	0 1	R B C U	S, Z, E
TAN	Tangent of A (radians)	0 4	R B U U	S, Z, E
XCHF	Exchange A and B	1 9	B A C D	S, Z

Double Precision Fixed Point Instructions (32-Bit)

Instruction	Description	Hex Code	Stack Contents After Execution[1] A B C D	Status Flags Affected[3]
CHSD	Sign Change of A	3 4	R B C D	S, Z, O
DADD	Add A and B	2 C	R C D A	S, Z, C, E
DDIV	Divide B by A	2 F	R C D U	S, Z, E
DMUL	Multiply A and B (R = lower 32 bits)	2 E	R C D U	S, Z, O
DMUU	Multiply A and B (R = upper 32 bits)	3 6	R C D U	S, Z, O
DSUB	Subtract A from B	2 D	R C D A	S, Z, C, O
FIXD	Floating to Fixed Point Conversion	1 E	R B C U	S, Z, O
POPD	Stack Pop	3 8	B C D A	S, Z
PTOD	Stack Push	3 7	A A B C	S, Z
XCHD	Exchange A and B	3 9	B A C D	S, Z

Table 1. Command Summary (continued)

Single Precision Fixed Point Instructions (16-Bit)

Instruction	Description	Hex Code	Stack Contents After Execution[2] A_U A_L B_U B_L C_U C_L D_U D_L	Status Flags Affected[3]
CHSS	Change Sign of A_U	7 4	R A_L B_U B_L C_U C_L D_U D_L	S, Z, O
FIXS	Floating to Fixed Point Conversion	1 F	R B_U B_L C_U C_L U U U	S, Z, O
POPS	Stack Pop	7 8	A_L B_U B_L C_U C_L D_U D_L A_U	S, Z
PTOS	Stack Push	7 7	A_U A_U A_L B_U B_L C_U C_L D_U	S, Z
SADD	Add A_U and A_L	6 C	R B_U B_L C_U C_L D_U D_L A_U	S, Z, C, E
SDIV	Divide A_L by A_U	6 F	R B_U B_L C_U C_L D_U D_L U	S, Z, E
SMUL	Multiply A_L by A_U (R = lower 16 bits)	6 E	R B_U B_L C_U C_L D_U D_L U	S, Z, E
SMUU	Multiply A_L by A_U (R = upper 16 bits)	7 6	R B_U B_L C_U C_L D_U D_L U	S, Z, E
SSUB	Subtract A_U from A_L	6 D	R B_U B_L C_U C_L D_U D_L A_U	S, Z, C, E
XCHS	Exchange A_U and A_L	7 9	A_L A_U B_U B_L C_U C_L D_U D_L	S, Z
NOP	No Operation	0 0	A_U A_L B_U B_L C_U C_L D_U D_L	

NOTES:

1. The stack initially is composed of four 32-bit numbers (A, B, C, D). A is equivalent to Top Of Stack (TOS) and B is Next On Stack (NOS). Upon completion of a command the stack is composed of: the result (R); undefined (U); or the initial contents (A, B, C, or D).
2. The stack initially is composed of eight 16-bit numbers (A_U, A_L, B_U, B_L, C_U, C_L, D_U, D_L). A_U is the TOS and A_L is NOS. Upon completion of a command the stack is composed of: the result (R); undefined (U); or the initial contents (A_U, A_L, B_U, B_L,...).
3. Nomenclature: Sign (S); Zero (Z); Overflow (O); Carry (C); Error Code Field (E).

Table 2. Command Execution Times

Command Mnemonic	μSeconds	Command Mnemonic	μSeconds
SADD	4.25	ASIN	1917
SSUB	7.5	ACOS	1933.5
SMUL	21-23.5	ATAN	1501.5
SMUU	20-24.5	LOG	1118.5-1783
SDIV	21-23.5	LN	1074.5-1739
DADD	5.25	EXP	948.5-1219.5
DSUB	9.5	PWR	2072.5-3008
DMUL	48.5-52.5	NOP	1
DMUU	45.5-54.5	CHSS	5.75
DDIV	52	CHSD	6.75
FIXS	23-54	CHSF	4.5
FIXD	25-86.5	PTOS	4
FLTS	24.5-46.5	PTOD	5
FLTD	24.5-94.5	PTOF	5
FADD	13.5-92	POPS	2.5
FSUB	17.5-92.5	POPD	3
FMUL	36.5-42	POPF	3
FDIV	38.5-46	XCHS	4.5
SQRT	200	XCHD	6.5
SIN	1116	XCHF	6.5
COS	1029.5	PUPI	4
TAN	1438.5		

NOTE: Assumes 4 MHz operation.

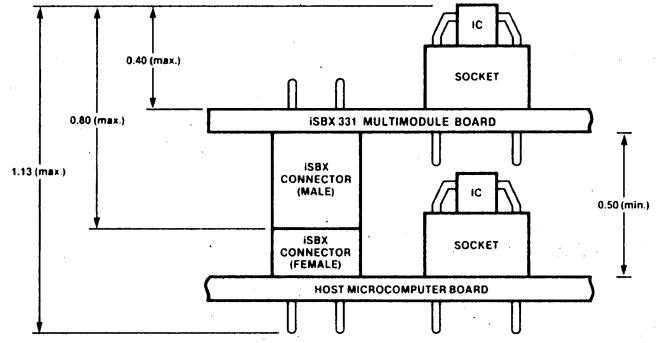


Figure 2. ISBX 331 MULTIMODULE Board Mounting Clearances (inches)

SPECIFICATIONS

Word Size

Data—8 bits.

On-Board Clock Rate

4.0 MHz ±0.1%.

I/O Addressing

Function	Type of Operation	iSBX Connector Port Address
Data Transfer	Read or Write	X0, X2, X4, or X6
Command Transfer	Write	X1, X3, X5, or X7
Status Transfer	Read	X1, X3, X5, or X7
Reset	Write	X8 through XF

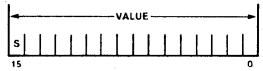
NOTE:
The port addresses are determined on the host iSBC microcomputer. Refer to the Hardware Reference Manual for your host iSBC microcomputer to determine the first digit (X) of the connector port addresses.

Arithmetic Functions

See Table 1.

Data Formats

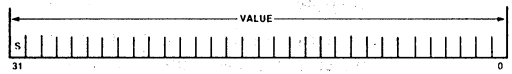
Single Precision Fixed Point (16 bits)



Bit 15: S = Sign of the operand. Positive values are represented by a sign bit of zero (S = 0). Negative values are represented by the two's complement of the corresponding positive value with a sign bit equal to 1 (S = 1).

Bits 0-14: Values in the range from −32, 768 to +32, 767.

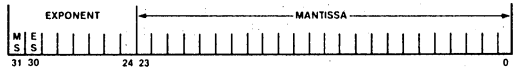
Double Precision Fixed Point (32 bits)



Bit 31: S = Sign of operand. Positive values are represented by a sign of zero (S = 0). Negative values are represented by the two's complemet of the corresponding positive value with a sign bit equal to 1 (S = 1).

Bits 0-30: Values in the range from −2, 147, 483, 648 to +2, 147, 483, 647.

Double Precision Floating Point (32 bits)



Bit 31: MS = Sign of the mantissa. 1 represents negative and 0 represents positive.

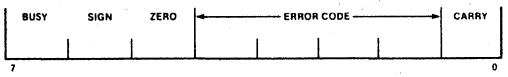
Bits 24-30: ES = the exponent expressed as a two's complement 7-bit value having a range of −64 to +63.

Bits 0-23: The mantissa is expressed as a 24-bit (fractional) value. The 8231 APU requires that floating point data be represented by a fractional mantissa value between 0.5 and 1 multiplied by 2 raised to an appropriate power (exponent). This is expressed as follows:

$$\text{Value} = \text{mantissa} \times 2^{\text{exponent}}$$

Device Status

Device status is provided by means of an internal status register whose format is shown below:



BUSY: Indicates that 8231 is currently executing a command (1 = Busy)

SIGN: Indicates that the value on the top of stack is negative (1 = Negative)

ZERO: Indicates that the value on the top of stack is zero (1 = Value is zero)

ERROR CODE: This field contains an indication of the validity of the result of the last operation. The error codes are:

0000 — No error
1000 — Divide by zero
0100 — Square root or log of negative number
1100 — Argument of inverse sine, cosine, or e^x too large
XX10— Underflow
XX01— Overflow

CARRY: Previous operation resulted in carry or borrow from most significant bit. (1 = Carry/Borrow, 0 = No Carry/No Borrow.)

If the BUSY bit in the status register is a one, the other status bits are not defined; if zero, indicating not busy, the operation is complete and the other status bits are defined as given above.

Access Time

Read—1900 ns (max.)
Write—1900 ns (max.)

NOTE:
Actual transfer speed is dependent upon the cycle time of the host microcomputer. The listed times assume no operation in progress. If an operation is executing when an access is attempted, the command execution time must be added to the above times for all accesses except status read.

Interrupts

One interrupt request may originate from the APU indicating command completion (END).

Interface

iSBX Bus—All signals TTL compatible

Physical Characteristics

Width—6.35 cm (2.50 in.)
Length—9.40 cm (3.70 in.)
Height*—2.04 cm (0.80 in.) iSBX 331 Board
—2.86 cm (1.13 in.) iSBX 331 Board + Host Board
Weight—51 gm (1.79 oz)

*See Figure 2.

Electrical Characteristics

DC Power Requirements

$V_{CC} = +5V \pm 5\%$ $I_{CC} = 365$ mA max.
$V_{DD} = +12V \pm 5\%$ $I_{DD} = 75$ mA max.

Environmental

Operating Temperature—0°C to 55°C

Free moving air across the base board and iSBX board.

Reference Manual

142668-01—iSBX 331 Floating Point Math MULTIMODULE Board (NOT SUPPLIED)

Reference manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBX 331	Fixed/Floating Point Math MULTIMODULE Board