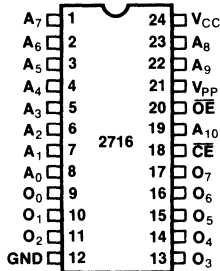# intel®

2716
16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time**
  - **— 2716-1: 350 ns Max.**
  - **— 2716-2: 390 ns Max.**
  - **— 2716: 450 ns Max.**
  - **— 2716-5: 490 ns Max.**
  - **— 2716-6: 650 ns Max.**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— Active Power: 525 mW Max.**
  - **— Standby Power: 132 mW Max.**

- **Pin Compatible to Intel 2732A EPROM**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible During Read and Program**
- **Completely Static**

The Intel 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single-address programming. It makes designing with EPROMs fast, easy and economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with high-performance +5V microprocessors such as Intel's 8085 and 8086. Selected 2716-5s and 2716-6s are also available for slower speed applications. The 2716 also has a static standby mode which reduces power consumption without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 uses a simple and fast method for programming—a single TTL-level pulse. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Programming of any location at any time—either individually, sequentially or at random is possible with the 2716's single-address programming. Total programming time for all 16,384 bits is only 100 seconds.

Pin		Pin	
A_7	1	24	V_{CC}
A_6	2	23	A_8
A_5	3	22	A_9
A_4	4	21	V_{PP}
A_3	5	20	$\overline{OE}$
A_2	6	19	A_{10}
A_1	7	18	$\overline{CE}$
A_0	8	17	O_7
O_0	9	16	O_6
O_1	10	15	O_5
O_2	11	14	O_4
GND	12	13	O_3

PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
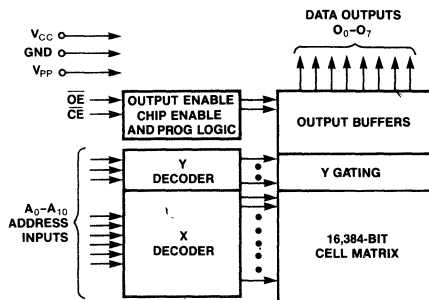
Figure 1. Pin Configuration

Figure 2. Block Diagram

intel   2716

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +125°C
All Input or Output Voltages with
  Respect to Ground .... +6V to −0.3V
V_{PP} Supply Voltage with Respect
  to Ground During Program .... +26.5V to −0.3V

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND A.C. OPERATING CONDITIONS DURING READ

	2716	2716-1	2716-2	2716-5	2716-6
Temperature Range	0°C–70°C	0°C–70°C	0°C–70°C	0°C–70°C	0°C–70°C
V_{CC} Power Supply[1,2]	5V ±5%	5V ±10%	5V ±5%	5V ±5%	5V ±5%
V_{PP} Power Supply[2]	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

READ OPERATION
D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

A.C. CHARACTERISTICS

Symbol	Parameter	Limits (ns)										Test Conditions†
		2716		2716-1		2716-2		2716-5		2716-6		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay		450		350		390		450		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390		490		650	$\overline{OE} = V_{IL}$
t_{OE}[4]	Output Enable to Output Delay		120		120		120		160		200	$\overline{CE} = V_{IL}$
t_{DF}[4,6]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	100	0	100	0	100	0	100	0	100	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

CAPACITANCE[4] (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Typ.[3]	Max.	Units	Test Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

†A.C. TEST CONDITIONS

Output Load . . . . 1 TTL gate and
C_L = 100 pF
Input Rise and Fall Times . . . . ≤20 ns
Input Pulse Levels . . . . 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs . . . . 0.8V and 2V
Outputs . . . . 0.8V and 2V
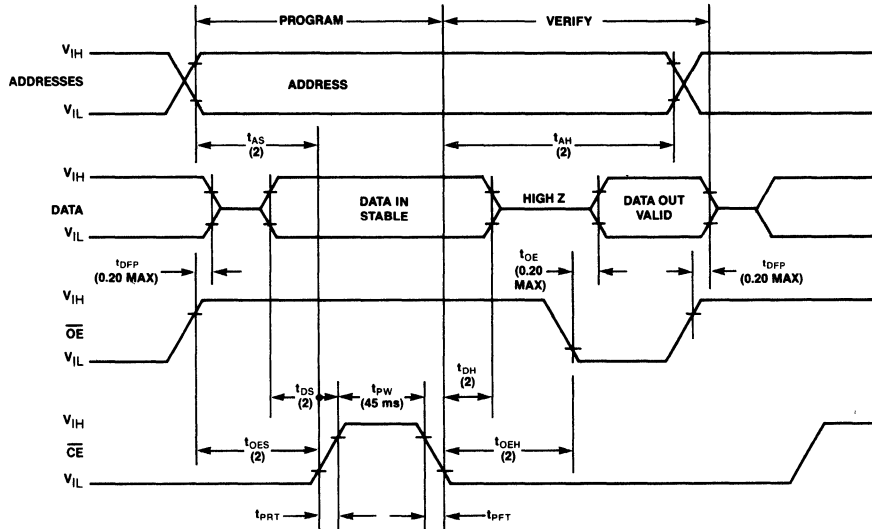
A.C. WAVEFORMS[1]
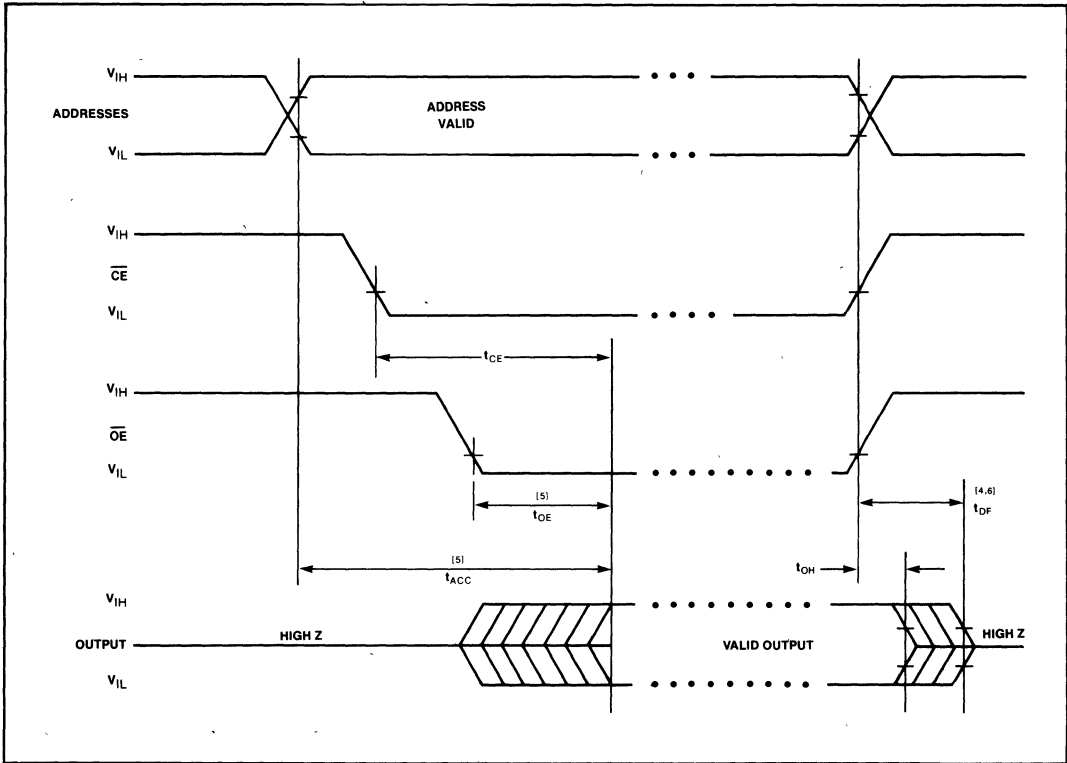
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. $\overline{OE}$ may be delayed up to t_{ACC}–t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
6. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first

AFN-00811B

PROGRAMMING WAVEFORMS

PROGRAM   VERIFY

V_{IH}

ADDRESSES   ADDRESS

V_{IL}

t_{AS} (2)

t_{AH} (2)

V_{IH}

DATA   DATA IN STABLE   HIGH Z   DATA OUT VALID

V_{IL}

t_{DFP} (0.20 MAX)

t_{OE} (0.20 MAX)

t_{DFP} (0.20 MAX)

V_{IH}

$\overline{OE}$

V_{IL}

t_{DS} (2)

t_{PW} (45 ms)

t_{DH} (2)

V_{IH}

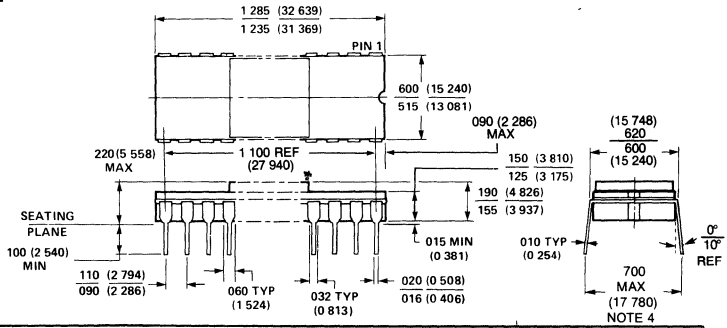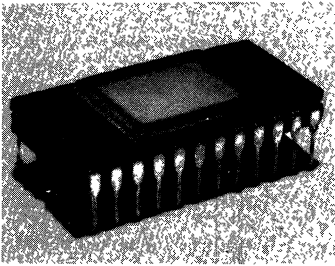$\overline{CE}$

t_{OES} (2)

t_{OEH} (2)

V_{IL}

t_{PRT}

t_{PFT}

NOTE
1 ALL TIMES SHOWN IN PARENTHESIS ARE MINIMUM TIMES AND ARE μ SEC UNLESS OTHERWISE NOTED
2 t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER

CERAMIC DUAL IN-LINE PACKAGE TYPE B

24–LEAD HERMETIC DUAL IN–LINE
PACKAGE TYPE B

1 285 (32 639)
1 235 (31 369)

PIN 1

600 (15 240)
515 (13 081)

090 (2 286)
MAX

(15 748)
620
600
(15 240)

220 (5 558)
MAX

1 100 REF
(27 940)

150 (3 810)
125 (3 175)

190 (4 826)
155 (3 937)

SEATING
PLANE

100 (2 540)
MIN

110 (2 794)
090 (2 286)

060 TYP
(1 524)

032 TYP
(0 813)

020 (0 508)
016 (0 406)

015 MIN
(0 381)

010 TYP
(0 254)

700
MAX
(17 780)
NOTE 4

0°
10°
REF

CERAMIC LEADLESS CHIP CARRIERS

18-LEAD CERAMIC LEADLESS
PACKAGE TYPE F

067 (1 701)
055 (1 397)

250 (6 350)
240 (6 096)
—B—

079 (2 006)
065 (1 651)

050 (1 270)
040 (1 016)
TYP 2 PLCS

130 (3 302)
120 (3 048)

390 (9 906)
380 (9 652)
—A—

440 (11 176)
420 (10 668)
⊕ A 010

050 (1 270) BSC

200 (5 080)
⊕ A 006

PIN 1

028 (0 711)
022 (0 558)
18 PLCS

011 (0 279)
007 (0 177)
TYP
R

118 (2 997)
107 (2 717)

150 (3 810)
BSC

18 1

305 (7 747)
280 (7 112)
⊕ B 016

PIN 1 INDEX CORNER
015 (0 381)
005 (0 127)
TYP 4 PLCS
R

088 (2 235)
077 (1 955)
TYP 2 PLCS

073 (1 854)
062 (1 574)

⊕ B 006