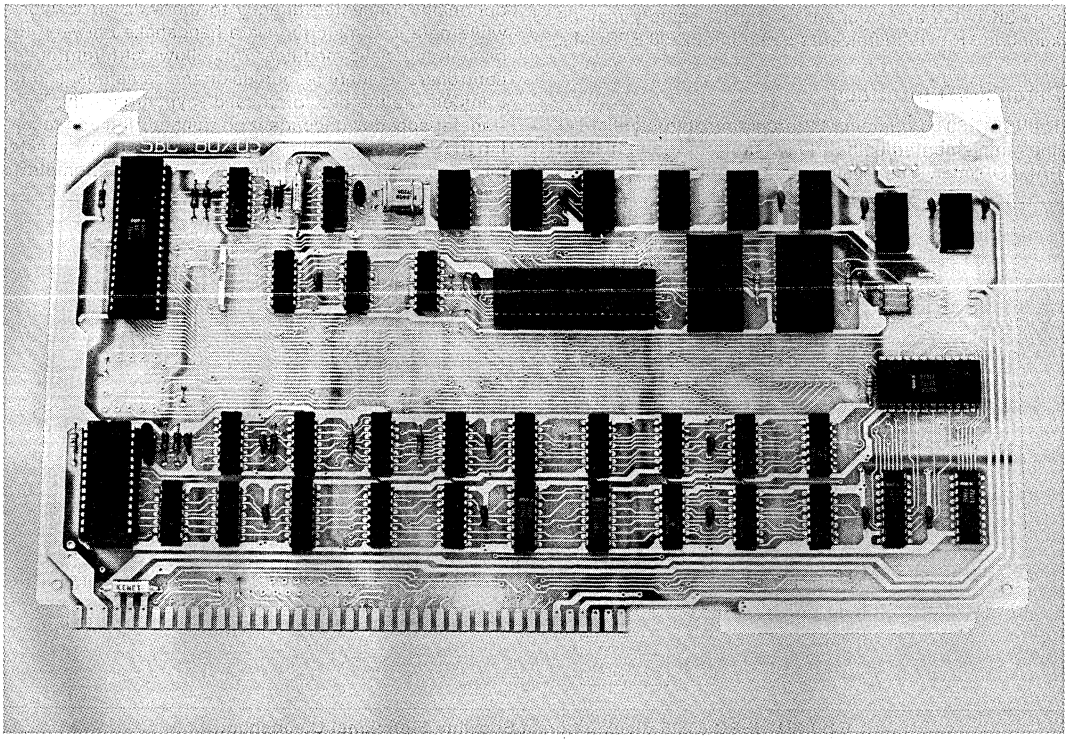
iSBC 80/05 (or pSBC 80/05*) SINGLE BOARD COMPUTER

- 8085A CPU used as central processor
- 512 bytes of static read/write memory
- Sockets for 4K bytes of erasable reprogrammable or masked read only memory
- 22 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators
- Full MULTIBUS control logic allowing up to 16 masters to share system bus
- Programmable 14-bit binary timer
- TTL serial I/O interface with sockets for RS232C line drivers and receivers
- Four-level vectored interrupt
- Fully compatible with optional iSBC expansion boards and peripherals
- Single +5V power supply

The iSBC 80/05 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/05 is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial interface, priority interrupt logic, programmable timer, MULTIBUS control logic, and bus expansion buffers all reside on the board.



*Same product, manufactured by Intel Puerto Rico, Inc.

FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel 8085 CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/05. The 8085A CPU is directly software compatible with the popular Intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum on-board instruction execution time is 2.03 microseconds. A block diagram of iSBC 80/05 functional components is shown in Figure 1.

Memory Addressing

The 8085A CPU has a 16-bit program counter which allows direct addressing of up to 65,536 bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The iSBC 80/05 contains 512 bytes of read/write memory using Intel's low power static RAMs. Two sockets for up to 4K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 2K-byte increments using Intel 2716 erasable and electrically reprogrammable ROMs (EPROMs). Optionally, if only 2K bytes are required, read only memory may be added in 1K-byte increments using Intel 2708 EPROMs.

Parallel I/O Interface

The iSBC 80/05 contains 22 programmable parallel I/O lines implemented using the I/O ports of the Intel 8155 RAM/IO/Timer. The system software is used to configure the I/O lines in any combination of unidirectional input or output ports as indicated in Table 1. The I/O interface may, therefore, be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 22 programmable I/O lines and signal ground lines are brought out to a 40-pin edge connector that mates with flat, woven, or round cable.

Multimaster Capability

The iSBC 8085A is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share systems tasks with communication over the system bus), the iSBC 80/05 provides full MULTIBUS arbitration control logic. This control logic allows up to three bus masters (i.e., any combination of iSBC 80/05, iSBC 80/20-4, DMA controller, diskette controller, etc.) to share the system bus in serial (daisy-chain) priority fashion, and up to 16 masters may share the MULTIBUS with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the iSBC 80/05 or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and for transfers via the bus to proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to

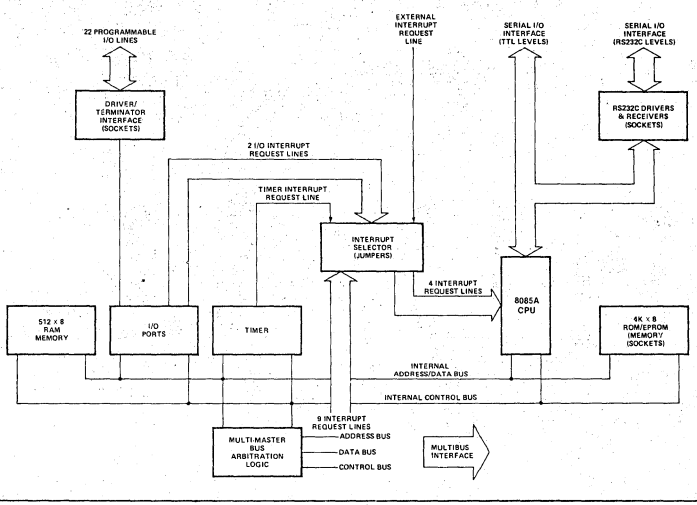


Figure 1. iSBC 80/05 Block Diagram Showing Functional Components

Table 1. Input/Output Modes of Operation

Port	Lines (qty)	Mode of Operation				Control
		Unidirectional				
		Input		Output		
		Unlatched	Latched & Strobed	Latched	Latched & Strobed	
1	8	X	X	X	X	
2	8	X	X	X	X	
3	3	X		X		X[1]
4	3	X		X		X[2]

Notes

1. Port 3 must be used as a control port when port 1 is used as a latched and strobed input or a latched and strobed output port.
2. Port 4 must be used as a control port when port 2 is used as a latched and strobed input or a latched and strobed output port.

gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct-memory-access (DMA) operations and high speed peripheral control, but are by no means limited to these three.

Programmable Timer

The iSBC 80/05 provides a fully programmable binary 14-bit interval timer utilizing the Intel 8155 RAM/IO/Timer. The system designer simply configures the timer via software to meet system requirements. Whenever a given time delay is needed, software commands to the programmable timer select the desired function. Four functions are available as shown in Table 2. The contents of the timer counter may be read at any time during system operation.

Serial I/O Interface

The iSBC 80/05 provides serial I/O capability through the serial input data (SID) and serial output data (SOD) functions of the Intel 8085A CPU. These functions are controlled exculsively by software through execution of the 8085A RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for execution of serial I/O support software. Hence, the maximum baud rate supported by the iSBC 80/05 is solely dependent on the overall system real-time software requirements. Serial I/O signals are TTL compatible and sockets are provided on the board for optional connection of RS232C line drivers and receivers.

Interrupt Capability

The iSBC 80/05 takes advantage of the powerful interrupt processing capability of the 8085A CPU. Interrupt requests are routed to the four interrupt inputs of the 8085A CPU (i.e., TRAP, RST 7.5, RST 6.5, and RST 5.5 in order of priority, TRAP highest), and each input generates a unique memory address (i.e., TRAP: 24_{16}, RST 7.5: $3C_{16}$, RST 6.5: 34_{16}, RST 5.5: $2C_{16}$). A single 8085A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory. All interrupt inputs with the exception of one (TRAP) may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085A CPU.

Table 2. Programmable Timer Functions

Function	Operation
Programmable pulse	Timer out goes low during the second half of count. Therefore, the count loaded in the count length register should be twice the pulse width desired.
Square wave rate generator	Timer out will remain high until one-half the count has been completed, and go low for the other half of the count. The count length is automatically reloaded when terminal count is reached.
Rate generator	Divide by N counter. A repetitive timer out low pulse is generated and new timeout initiated every time terminal count is reached.
Programmable strobe	A single low pulse is generated upon reaching terminal count. This function is extremely useful for generation of real-time clocks.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the iSBC 310A High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding

single or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are available to support multiboard systems.

Systems Development Capability

The development cycle of iSBC 80/05-based products may be significantly reduced using an Intellec microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of iSBC 80/05 system software. An optional diskette operating system provides a relocating macroassembler, a relocating loader and linkage editior, and a library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 80/05.

Programming Capability

PL/M-80 — Intel's high level programming language, PL/M, is also available as a resident Intellec microcomputer development system option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits
Data — 8 bits

Cycle Time

Basic Instruction Cycle — 2.03 μs, ± 0.1%

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

ROM/EPROM — $0\text{-}0FFF_H$
RAM — $3E00_H$

Memory Capacity

On-Board ROM/EPROM — 4K bytes (with Intel 2716) or 2K bytes (with Intel 2708)

On-Board RAM — 512 bytes

Off-Board Expansion — Up to 65,536 bytes in user specified combination of RAM, ROM, and PROM

I/O Addressing

On-Board Programmable I/O — see Table 1

Port Control	8155 Port 1	8155 Port 2	8155 Ports 3 & 4	8155 Port	8155 Timer Low-Order Byte	8155 Timer High-Order Byte
Address	00	01	02	03	04	05

I/O Capacity

Parallel — 22 programmable lines (see Table 1)

Note

The iSBC 80/05 may be expanded to 1102 programmable input/output lines by using optional iSBC 80 I/O boards.

Serial Communications Characteristics

SID and SOD functions of the 8085A CPU are used for serial I/O. They are controlled by software through RIM and SIM instructions of the 8085A CPU. Baud rate is determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements.

Interrupts

Four-level interrupt routed to 8085A CPU interrupt inputs. Each interrupt automatically vectors the processor to a unique memory location.

Interrupt Input	Memory Address	Priority	Type
TRAP	24_{16}	Highest	Non-maskable
RST 7.5	$3C_{16}$	↑	Maskable
RST 6.5	34_{16}	↓	Maskable
RST 5.5	$2C_{16}$	Lowest	Maskable

Timer

Input Frequency Reference — 122.88 kHz ± 0.1% (8.14 μs period nominal)

Output Frequencies/Timing Intervals

Function	Timer/Counter	
	Min	Max
Programmable pulse	8.14 μs	66.67 ms
Square wave rate generator	7.50 Hz	61.44 kHz
Rate generator	7.50 Hz	61.44 kHz
Programmable strobe	8.14 μs	133.33 ms

Interfaces

Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Interrupt Request — All TTL compatible (active-low)
Serial I/O — TTL; sockets available for RS232C line drivers and receivers

System Clock (8085A CPU)

1.966 MHz ± 0.1%

Interface	Lines (qty)	Centers (in.)	Mating Connector
Bus	86 double-sided	0.156	Viking 2KH43/9AMK12
Parallel I/O	50 double-sided	0.100	3M 3415-000
Serial I/O[1]	7 single-sided	0.156	Molex 09-66-1071 Connector Molex 09-50-7071 Connector
			AMP 87194-6 Connector AMP 3-87025-4 Connector

Note

1. Connectors and pins from one vendor may only be used with connectors and pins from the same vendor.

Line Drivers and Terminators

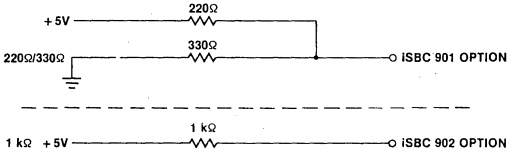
I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/05:

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators — Intel provides 220Ω/330Ω divider and 1 kΩ pull-up resistive terminator packs for termination of I/O lines programmed as inputs. These options are as follows:



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

RS232C Drivers and Receivers

The following RS232C drivers and receivers are compatible with the RS232C socket on the iSBC 80/05:

RS232C Driver — National DS1488 or TI SN75188
RS232C Receiver — National DS1490 or TI SN75189

Physical Characteristics

Width — 12.00 in. (30.49 cm)
Height — 6.75 in. (17.15 cm)
Depth — 0.50 in. (1.27 cm)
Weight — 12.0 oz (339.8 gm)

Electrical Characteristics

DC Power Requirements

Voltage (±5%)	Without PROM[1] (max)	With 2716 EPROM[2] (max)	With 8708 EPROM[3] (max)
V_{CC} = +5V	I_{CC} = 1.80 mA	2.65A	2.45A
V_{DD} = +12V[4]	I_{DD} = 0	7 mA[5]	137 mA
V_{BB} = −5V[4]	I_{BB} = 0	0	90 mA
V_{AA} = −12V[5]	I_{AA} = 0	23 mA[5]	23 mA[5]

Notes

1. Does not include power required for optional EPROM/ROM, I/O drivers, and I/O terminators.
2. With two Intel 2716 EPROMs and 220Ω/330Ω terminators installed for 22 input ports; all terminator inputs low.
3. With two Intel 2708 EPROMs and 220Ω/330Ω terminators installed for 22 input ports; all terminator inputs low.
4. Required for 2708 EPROMs.
5. Required only when RS232C capability required.

Environmental Characteristics

Operating Temperature — 0°C to +55°C.

Reference Manual

9800483D — iSBC 80/05 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/05	Single Board Computer