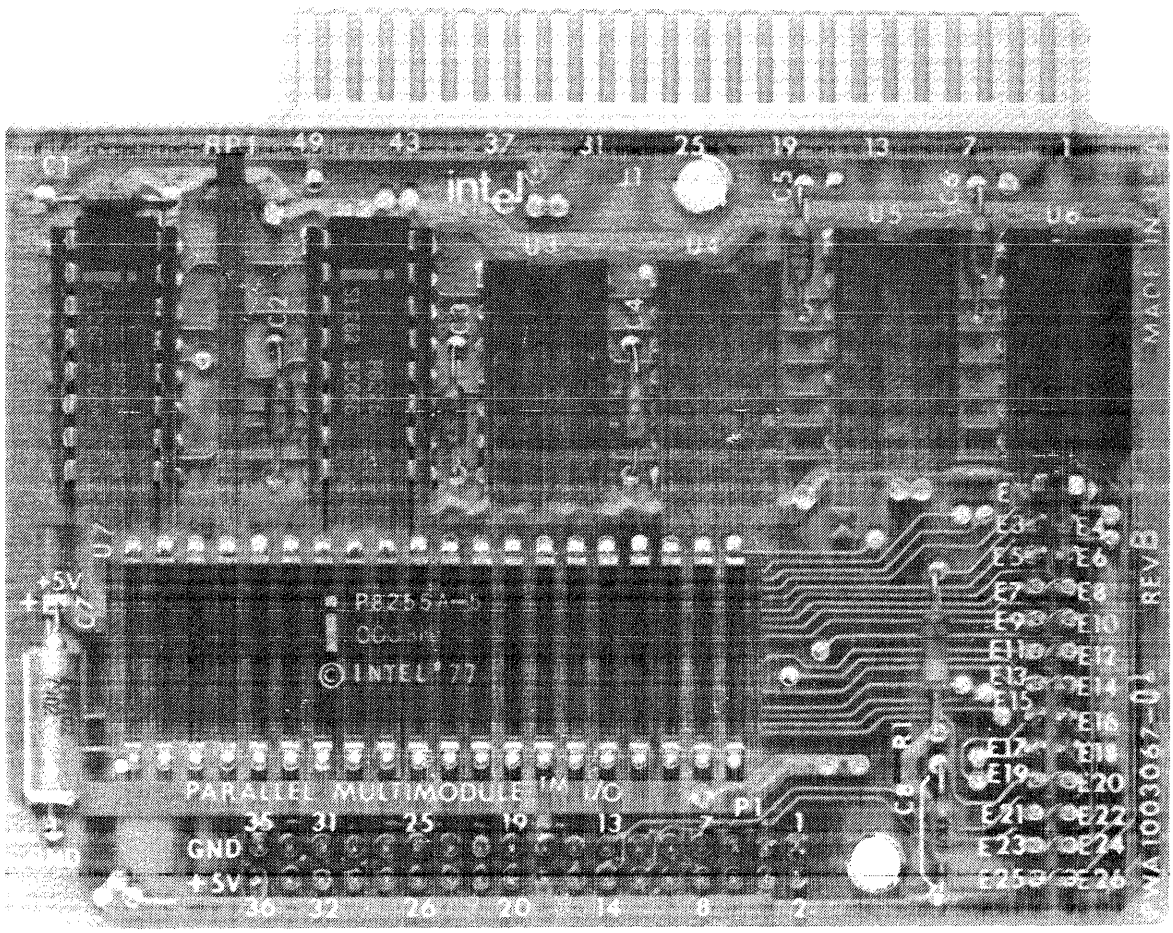
iSBX™ 350 PARALLEL MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa, Clara, California 95051

Order Number: 9803191-02

iSBX 350™ PARALLEL MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, installation, programming information, principles of operation, and service information for the Intel iSBX 350 Parallel Multimodule Board. Additional information is available in the following documents:

- *Intel MCS-85 User's Manual,* Order No. 9800366
- *Intel Peripheral Design Handbook,* Order No. 9800676
- *Intel 8080/8085 Assembly Language Programming Manual,* Order No. 9800301
- *Intel 8255A Programmable Peripheral Interface,* Application Note AP-15
- *Intel MULTIBUS Interfacing,* Application Note AP-28
- *Intel MULTIBUS Specification,* Order No. 9800683

CONTENTS

TABLES

ILLUSTRATIONS

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBX 350 Parallel Multimodule Board (hereafter referred to as the Multimodule board) is a member of Intel's growing line of expansion Multimodule boards designed to increase the capabilities of any iSBC microcomputer that contains a Multimodule connector. This manual describes the general information, preparation for use, programming, principles of operation, and service information for the Multimodule board.

1-2. DESCRIPTION

Figure 1-1 shows the iSBX 350 Parallel Multimodule Board. The Multimodule board provides expansion capability of 24 programmable parallel I/O lines for a host iSBC microcomputer. The additional I/O lines are configurable via the system software and the line driver/receiver devices on the Multimodule board. The Multimodule board contains an 8255A-5 Programmable Peripheral Interface (PPI) device that may be initialized in one of 3 modes; MODE ZERO - the basic input/output mode, MODE ONE - the strobed input/output mode, and MODE TWO - the bidirectional bus interface mode. The board also includes two socketed 8226 Bidirectional Bus Driver devices for interfacing to external devices.

1-3. EQUIPMENT SUPPLIED

The following are supplied with each iSBX 350 Parallel Multimodule Board:

a. Schematic Diagram, dwg. no. 2003069
b. Assembly Diagram, dwg. no. 1003067
c. 1 spacer, plastic, ½ x 6/32
d. 2 screws, plastic, ¼ x 6/32.

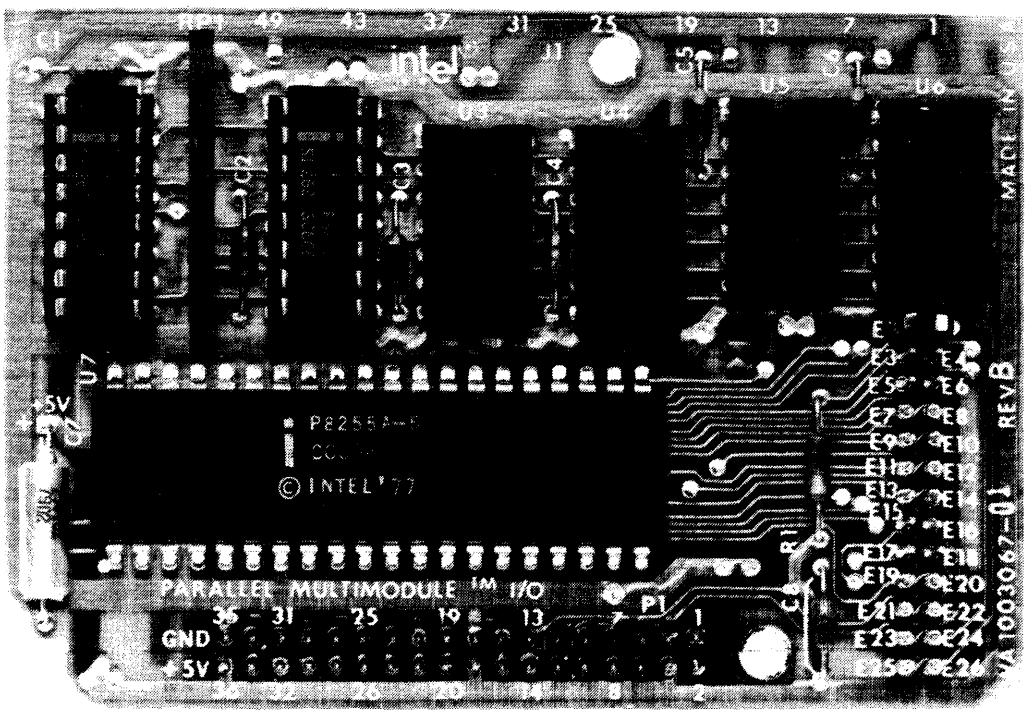


Figure 1-1. iSBX 350™ Parallel Multimodule™ Board

In addition, the user must supply a host iSBC microcomputer; line driver/terminator devices for Multimodule sockets XU3, XU4, XU5, and XU6, if required by the application; and an interconnecting cable and connector.

1-4. COMPATIBLE EQUIPMENT

The Multimodule board must be used with a host Intel iSBC microcomputer that includes a compatible mating connector.

1-5. SPECIFICATIONS

The specifications for the iSBX 350 Parallel Multimodule Board are listed in table 1-1.

Table 1-1. Specifications

I/O ADDRESSING

All addressing for the Parallel I/O Ports is contingent on the Multimodule connector used on the host iSBC microcomputer. Reference table 3-1.

INTERFACE COMPATIBILITY

Parallel Interface

24 programmable lines (8 lines per port); one port includes bidirectional bus drivers. DIP sockets included for user installation of line drivers and/or I/O terminators, as required by the application.

System Bus

Compatible with the iSBX bus specifications.

PARALLEL INTERFACE CONNECTORS

Interface	No. of Pins	Pin Centers		Mating Connectors
		in.	mm	
J1 Channel	25/50	0.1	2.54	AMP-88083-1 3M-3415-0000

POWER REQUIREMENTS

Power Requirement	Configuration
+5V @ 320 mA	Sockets XU3, XU4, XU5, and XU6 empty (As-shipped).
+5V @ 500 mA	Sockets XU3, XU4, XU5, and XU6 contain 7438 buffers.
+5V @ 620 mA	Sockets XU3, XU4, XU5, and XU6 contain iSBC 901 Termination devices.

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0° to 55°C (32° to 131°F).

Relative Humidity: To 90% without condensation.

PHYSICAL CHARACTERISTICS

Width: 7.24 cm (2.85 inches).

Length: 9.40 cm (3.70 inches).

Thickness: 2.03 cm (0.80 inch) Multimodule board only.
2.82 cm (1.13 inches) Multimodule and iSBC board.

Weight: 51 gm (1.79 ounces).

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides information on preparing and installing the iSBX 350 Parallel Multimodule Board. Included are instructions on unpacking and inspection; installation considerations, such as physical, power, cooling, and mounting requirements; jumper configurations; ac and dc characteristics; connector assignments; and installation procedures.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The iSBX 350 Parallel Multimodule Board is designed to interface with all Intel iSBC Single Board Computers that contain the I/O interface connector required to support Multimodule boards. Other installation considerations such as power, cooling, mounting, and physical size requirements, are outlined in the following paragraphs.

2-4. POWER REQUIREMENT

The power requirements for the Multimodule board vary depending on the configuration of the board. The Multimodule board with no user-installed buffers (sockets XU3 through XU6) requires +5V (±0.25V) at 320 mA (maximum).

With four 7438 buffers installed in sockets XU3 through XU6, the board requires +5V (±0.25V) at 500 mA (maximum).

If iSBC 901 termination packages are used, the board requires +5V (±0.25V) at 620 mA (maximum).

All power for the Multimodule board is derived from the host iSBC microcomputer and drawn through the iSBX bus (P1) on the Multimodule board. Table 1-1 contains these power requirements in tabular form.

NOTE

If modification of a Multimodule board is required, ensure that none of the Multimodule specifications and standards are violated in doing so.

2-5. COOLING REQUIREMENT

The iSBX 350 Parallel Multimodule Board dissipates 44.1 gram-calories/minute (0.18 BTU/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F).

2-6. MOUNTING REQUIREMENT

The Multimodule boards will mount onto any iSBC microcomputer containing an iSBX bus connector. Figure 2-1 shows the P1 connector and mounting hole location on the Multimodule board. The mounting hardware supplied as part of the Multimodule board includes:

a. 1 plastic spacer, ½ inch x 6/32, separate from the board.

b. 36-pin connector P1, factory-installed onto the board.

c. 2 plastic screws, ¼ inch x 6/32, separate from board.

NOTE

Plan your cardcage space allocation. The Multimodule board, when installed onto a host microcomputer, occupies an additional card slot adjacent to the component side of the host microcomputer in an iSBC 604/614 Cardcage.

2-7. DIMENSIONS

Figure 2-1 shows the dimensions for the Multimodule board, and figure 2-2 shows the clearances for a Multimodule board mounted onto a host iSBC microcomputer. The physical dimensions of the Multimodule board are as follows:

a. Width: 7.27 cm (2.85 inches).

b. Length: 9.40 cm (3.70 inches).

c. Thickness: 2.05 cm (0.80 inch) Multimodule board only; 2.82 cm (1.13 inches) Multimodule and iSBC board.

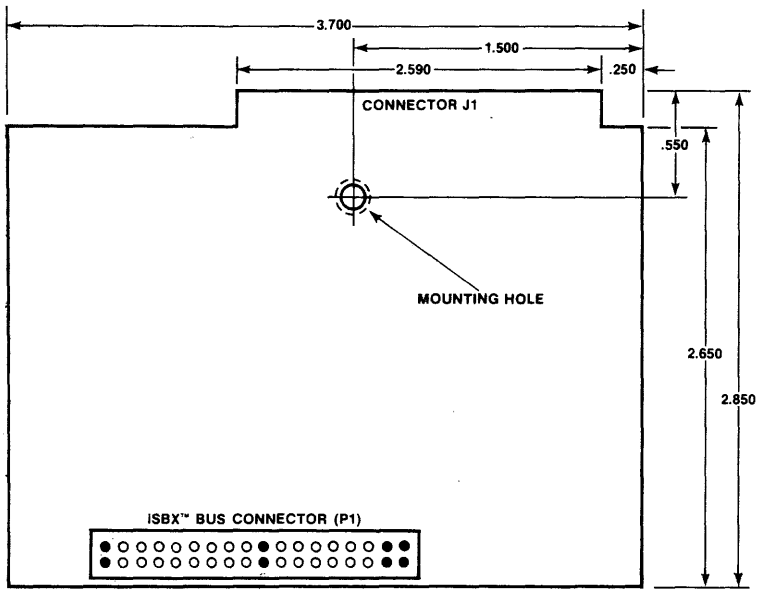


Figure 2-1. Board Dimensions (Inches)

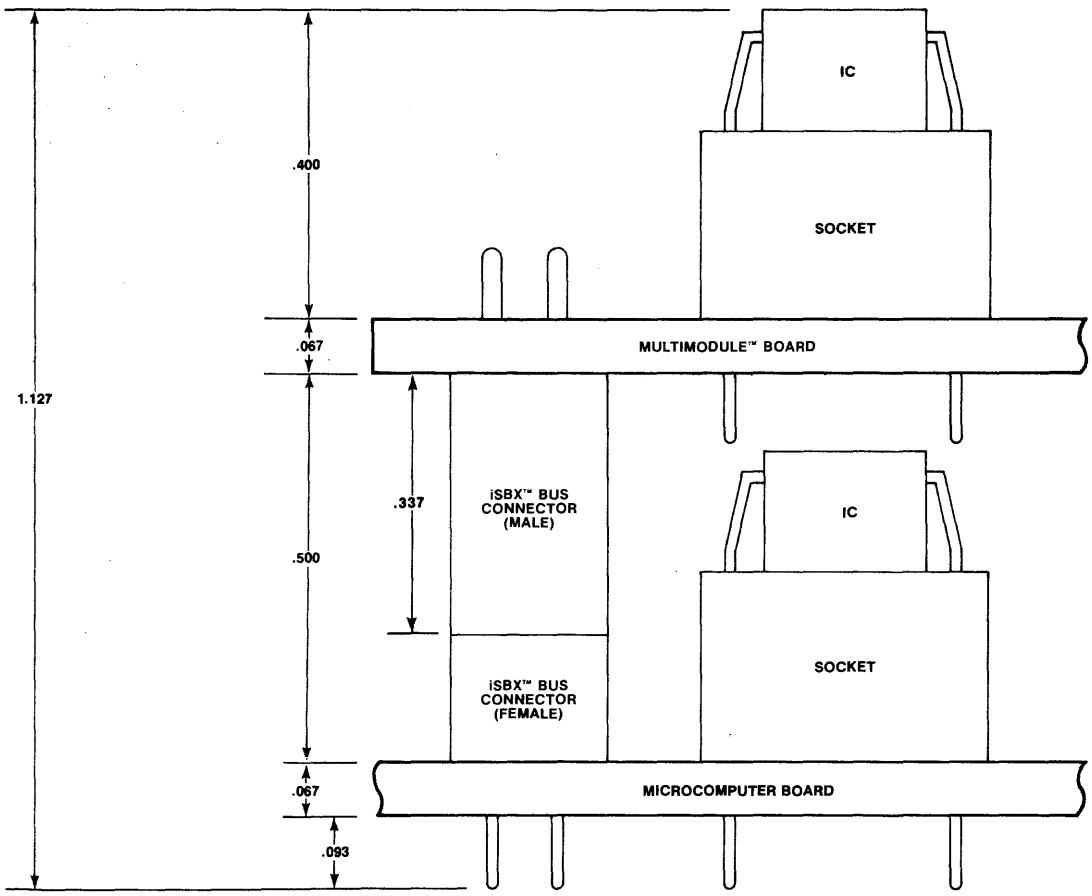


Figure 2-2. Mounting Clearances (Inches)

2-8. DC INTERFACE CHARACTERISTICS

The dc characteristics of the Multimodule board at the J1 connector are listed in table 2-1.

2-9. CONNECTOR CONFIGURATION

The Multimodule board is designed to mount onto a Multimodule connector on a host iSBC microcomputer. Connector P1 interfaces all data and control signals between the host iSBC microcomputer and the Multimodule board. The signals found on each pin of the P1 connector are listed in table 2-2. Reference chapter 4 for signal descriptions.

Connector J1 on the Multimodule board handles parallel I/O communication between the Multimodule board and an external device. The signals found on each pin of the J1 connector are listed in table 2-3.

Table 2-1. DC Characteristics

Output Signal	Type Drive	I_{OL} MAX (mA)	V_{OL} MAX (I_{OL}=MAX)	I_{OH} MAX (μA)	V_{OH} MIN (I_{OH}=MAX)	C_O MIN (pf)
Port A	TTL	20	0.45	-10mA	2.4	18
Input Signal	**Type Receiver**	**I_{IL} MAX (mA) (V_{IL}=.45**	**V_{IL} MAX**	**I_{IH} MAX (mA) (V_{IH}=2.4)**	**V_{IH} MIN**	**C_I MAX (pf)**
Port A	TTL	-5.2	0.80	-2.2	2.0	18
Port B & C: 1K Pull-Up	TTL	-5.0	0.80	-2.2	2.0	20
Port B & C: 220/330 Terminator	TTL	-21.00	0.80	-3.0	2.0	20
EXT INTR (J1 Pin 50)	TTL	-6.5	0.50	-2.2	2.4	40

NOTES:
TTL = Standard Totem Pole Output
Reference table 2-6 for Port B and C output characteristics.
Capacity values are approximations.

Table 2-2. Connector P1 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	SIGNAL GROUND	36	+5V	+5 Volts
33	MD0	MDATA BIT 0	34	—	RESERVED
31	MD1	MDATA BIT 1	32	—	RESERVED
29	MD2	MDATA BIT 2	30	OPT0	OPTION 0
27	MD3	MDATA BIT 3	28	OPT1	OPTION 1
25	MD4	MDATA BIT 4	26	—	RESERVED
23	MD5	MDATA BIT 5	24	—	RESERVED
21	MD6	MDATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	MDATA BIT 7	20	—	RESERVED
17	GND	SIGNAL GROUND	18	+5V	+5 Volts
15	IORD/	IO READ COMMAND	16	—	RESERVED
13	IOWRT/	IO WRITE COMMAND	14	MINTR0	M INTERRUPT 0
11	MA0	M ADDRESS 0	12	MINTR1	M INTERRUPT 1
9	MA1	M ADDRESS 1	10	—	RESERVED
7	—	RESERVED	8	MPST/	M PRESENT
5	RESET	RESET	6	—	RESERVED
3	GND	SIGNAL GROUND	4	+5V	+5 Volts
1	—	RESERVED	2	—	RESERVED

Table 2-3. Connector J1 Pin Assignments

Pin	Signal	Pin	Signal
1	Ground	2	PORT B - BIT 7
3	Ground	4	PORT B - BIT 6
5	Ground	6	PORT B - BIT 5
7	Ground	8	PORT B - BIT 4
9	Ground	10	PORT B - BIT 3
11	Ground	12	PORT B - BIT 2
13	Ground	14	PORT B - BIT 1
15	Ground	16	PORT B - BIT 0
17	Ground	18	PORT C - BIT 3
19	Ground	20	PORT C - BIT 2
21	Ground	22	PORT C - BIT 1
23	Ground	24	PORT C - BIT 0
25	Ground	26	PORT C - BIT 4
27	Ground	28	PORT C - BIT 5
29	Ground	30	PORT C - BIT 6
31	Ground	32	PORT C - BIT 7
33	Ground	34	PORT A - BIT 7
35	Ground	36	PORT A - BIT 6
37	Ground	38	PORT A - BIT 5
39	Ground	40	PORT A - BIT 4
41	Ground	42	PORT A - BIT 3
43	Ground	44	PORT A - BIT 2
45	Ground	46	PORT A - BIT 1
47	Ground	48	PORT A - BIT 0
49	Ground	50	Optional *

* Optional = +5V or GND or External Interrupt input; reference paragraph 2-10 for caution.

Table 2-4 contains a listing of some of the details for compatible connectors that may be user-supplied to interface to the J1 connector on the Multimodule board.

2-10. JUMPER CONFIGURATION

The Multimodule board contains 26 wirewrap posts (E1 through E26). These may be user-configured to provide the flexibility needed to support all three modes of operation of the PPI. Table 2-5 lists the functions of each jumper.

Port Enables. Each of the Port C I/O lines contains enable/disable jumper options (E7-E14 and E19-E26). Additional jumpers (E15-E18) provide ability to input or output four other signals (MINTR0, MINTR1, OPT0, OPT1) via Port C; thus the user can buffer these signals to the interface.

Interrupt/Options. E6 provides a convenient method to send the MINTR0, MINTR1, OPT0, or OPT1 signal to pin 50 of the J1 connector. E6 may also be jumpered to +5 volts when the application dictates. Reference to table 2-5.

CAUTION

If E6 is wired to +5V, ensure that the connector is installed properly onto J1; the +5V signal must always interface to pin 50 of J1. Failure to do so could result in damage to the terminator/driver devices in XU1 through XU6.

Driver Control. E2 provides direction control for the bidirectional bus drivers, and may be jumpered to E1 or any of the Port C control lines.

The schematic drawing of the Multimodule board (reference figure 5-2) shows the "as shipped" configuration of the jumpers, including connections from E1 to E2, E7 to E8, E9 to E10, E11 to E12, E13 to E14, E19 to E20, E21 to E22, E23 to E24, and E25 to E26.

Table 2-4. Compatible J1 Connector Details

Function	No. Of Pairs/ Pins	Centers (inches)	Connector Type	Vendor	Vendor Part No.
Parallel I/O Connector	25/50	0.1	Female, Flat Crimp	3M 3M AMP ANSLEY SAE	3415-0000 WITH EARS 3415-0000 W/O EARS 88083-1 609-5015 SD6750 SERIES
Parallel I/O Connector	25/50	0.1	Female, Soldered	AMP VIKING TI	2-583485-6 3VH25/1JV5 H312125
Parallel I/O Connector	25/50	0.1	Female, Wirewrap	TI VIKING ITT CANNON	H311125 3VH25/1JND5 EC4A050A1A

Table 2-5. Port Configuration Jumpers for Multimodule™ Board

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration			Restrictions	
			Delete	Add	Effect	Port	
X0	0 Input	8226: U1, U2	*E1-E2	E3-E2	8226 = input enabled.	X1	None; can be in Mode 0 or 1, input or output.
						X2	None; can be in Mode 0, input or output, unless Port X1 is in Mode 1.
X0	0 Output (latched)	8226: U1, U2		*E1-E2	8226 = output enabled.	X1	None; can be in Mode 0 or 1, input or output.
						X2	None; can be in Mode 0, input or output, unless Port X1 is in Mode 1.
X0	1 Input (strobed)	8226: U1, U2 T: XU3 D: XU4	*E1-E2	E3-E2	8226 = input enabled.	X1	None; can be in Mode 0 or 1, input or output.
				*E19-E20	Connects J1-26 to STB_A/ input.	X2	Port X2 bits perform the following: • Bits 0, 1, 2 — Control for Port X1 if Port X1 is in Mode 1. • Bit 3 — Port X0 Interrupt (PA INTR) to interrupt jumper matrix. • Bit 4 — Port X0 Strobe (STB/) input. • Bit 5 — Port X0 input Buffer Full (IBF) output. • Bits 6, 7 — Port X2 input or output (both must be in same direction).
			*E21-E22 and *E13-E14	E21-E14	Connects IBF_A output to J1-18		
				E13-E16 or E13-E18	Connects INT_A output to MINTR1 or MINTR0.		

*Default jumper connected at the factory.

Table 2-5. Port Configuration Jumpers For Multimodule™ Board (Continued)

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration				Restrictions
			Delete	Add	Effect	Port	
X0	1 Output (latched)	8226: U1, U2 T: XU3 D: XU4		*E1-E2	8226 = output enabled.	X1	None; can be in Mode 0 or 1, input or output.
				*E23-E24	Connects J1-30 to ACK_A/ input.	X2	Port X1 bits perform the following: • Bits 0, 1, 2 — Control for Port X1 if Port X1 is in Mode 1. • Bit 3 — Port X0 interrupt (PA INTR) to interrupt jumper matrix. • Bits 4, 5 — Port X2 input or output (both must be in same direction). • Bit 6 — Port X0 Acknowledge (ACK/) input. • Bit 7 — Port X0 Output Buffer Full (OBF/) output.
			*E13-E14 and *E25-E26	E25-E14	Connects OBF_A output to J1-18.		
				E13-E16 or E13-E18	Connects INT_A output to MINTR1 or MINTR0.		
X0	2 (bi-directional)	8226: U1, U2 T: XU3 D: XU4	*E1-E2	E4-E2	Allows ACK_A/ input to control 8226 in/out direction.	X1	None; can be in Mode 0 or 1, input or output.
				*E19-E20	Connects J1-26 to STB_A/ input.	X2	Port X2 bits perform the following: • Bits 0, 1, 2 — Can be used for input or output if Port X2 is in Mode 0. • Bit 3 — Port X0 interrupt (PA INTR) to interrupt jumper matrix. • Bit 4 — Port X0 Strobe (STB/) input. • Bit 5 — Port X0 input Buffer Full (IBF) output. • Bit 6 — Port X0 Acknowledge (ACK/) input. • Bit 7 — Port X0 Output Buffer Full (OBF/) output.
			*E7-E8 and *E21-E22	E21-E8	Connects IBF_A output to J1-24.		
				*E23-E24	Connects J1-30 to ACK_A/ input.		
			*E13-E14 and *E25-E26	E25-E14	Connects OBF_A/ output to J1-18.		
				E13-E16 or E13-E18	Connects INT_A output to MINTR1 or MINTR0.		
X1	0 Input	T: XU5, XU6	None	None		X0	None.
						X2	None; Port X2 can be in Mode 0, input or output, if Port X0 is also in Mode 0.
*Default jumper connected at the factory.							

Table 2-5. Port Configuration Jumpers For Multimodule™ Board (Continued)

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration				Restrictions
			Delete	Add	Effect	Port	
X1	0 Output (latched)	D: XU5, XU6	None	None		X0	None
						X2	None; Port X2 can be in Mode 0, input or output, if Port X0 is also in Mode 0.
X1	1 Input (strobed)	T: XU3, XU5, XU6 D: XU4		*E9-E10	Connects IBF_B output to J1-22.	X0	None.
			*E25-E26 *E11-E12 *E7-E8	E26-E11	Connects J1-32 to STB_B/ input.	X2	Port X2 bits perform the following: • Bit 0 — Port X1 interrupt (PB INTR) to interrupt jumper matrix. • Bit 1 — Port X1 Input Buffer Full (IBF) output. • Bit 2 — Port X1 Strobe (STB/) input. • Bits 3, 4, 5, 6, 7 — Depends on Port X0 mode.
				E7-E16 or E7-E18	Connects INT_B output to MINTR1. Connects INT_B output to MINTR0.		
X1	1 Output (latched)	T: XU3 D: XU4, XU5, XU6		*E9-E10	Connects OBF_B/ output output J1-22.	X0	None.
			*E11-E12 and *E25-E26 *E7-E8	E11-E26	Connects J1-32 to ACK_B/ input.	X2	Port X2 bits perform the following: • Bit 0 — Port X1 interrupt (PB INTR) to interrupt jumper matrix. • Bit 1 — Port X1 Output Buffer Full (OBF/) output. • Bit 2 — Port X1 Acknowledge (ACK/) input. • Bits 3, 4, 5, 6, 7 — Depends on Port X0 mode.
				E7-E16 or E7-E18	Connects INT_B output to MINTR1. Connects INT_B output to MINTR0.		
X2 (upper)	0 Input	T: XU3	None	*E19-E20 *E21-E22 *E23-E24 *E25-E26	Connects bit 4 to J1-26. Connects bit 5 to J1-28. Connects bit 6 to J1-30. Connects bit 7 to J1-32.	X0	Port X0 must be in Mode 0 for all four bits to be available.
						X1	Port X1 must be in Mode 0 for all four bits to be available.
X2 (lower)	0 Input	T: XU4	None	*E7-E8 *E9-E10 *E11-E12 *E13-E14	Connects bit 0 to J1-24. Connects bit 1 to J1-22. Connects bit 2 to J1-20. Connects bit 3 to J1-18.	X0	Port X0 must be in Mode 0 for all four bits to be available.
						X1	Port X1 must be in Mode 0 for all four bits to be available.

*Default jumper connected at the factory.

Table 2-5. Port Configuration Jumpers For Multimodule™ Board (Continued)

Port	Mode	Driver (D)/ Terminator (T)	Jumper Configuration				Restrictions
			Delete	Add	Effect	Port	
X1 (upper)	0 Output (latched)	D: XU3	None	Same as for Port X2 (upper) mode 0 Input.		X0	Same as for Port X2 (upper) Mode 0 Input.
X1 (lower)	0 Output (latched)	D: XU4	None	Same as for Port X2 (lower) Mode 0 Input.		X2	Same as for Port X2 (lower) Mode 0 Input.
*Default jumper connected at the factory.							

2-11. LINE DRIVERS AND I/O TERMINATORS

All 24 I/O lines on the Multimodule board can be buffered with drivers or terminators at sockets XU1, XU2, XU3, XU4, XU5, and XU6 on the board. The 24 I/O lines may be divided into three groups of eight. The group labeled Port A is connected to the socketed 8226 Bidirectional Bus Driver devices. Unlike Port B and Port C, Port A may be used in the "as-shipped" configuration with no additional components.

NOTE

The 8226's are inverting devices. You may wish to substitute Intel 8216 non-inverting bidirectional bus driver devices, as required by the application.

Port B and Port C each interface to two sockets compatible with any 7400 pinout type driver. Table 2-6 lists some of the common drivers and their characteristics.

Table 2-6. Compatible Line Drivers

Driver	Characteristic[1]	I_{OL} (mA)[2]	I_{OH} (mA)[3]
7438	I,OC	48	—
7437	I	48	-1.2
7432	NI	16	-0.8
7426	I,OC	16	—
7409	NI,OC	16	—
7408	NI	16	-0.8
7403	I,OC	16	—
7400	I	16	-0.4

NOTES:
1. I = Inverting; OC = Open Collector; NI = Non Inverting.
2. I_{OL} specified for V_{OL} = 0.4 Volt.
3. I_{OH} specified for V_{OH} = 2.4 Volts.

The Port B and Port C sockets are also compatible with two special terminator resistor packs available through Intel; the iSBC 901 Terminator and the iSBC 902 Pull-Up. The packs are shown in figure 2-3 and useful in interfacing to the Intel 8255A-5 PPI device in an input application.

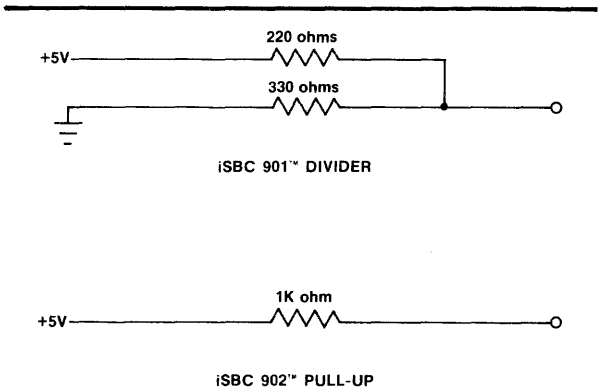


Figure 2-3. Compatible I/O Terminators

Each of the Port C lines also includes two wirewrap posts that provide the flexibility needed to support all three modes of operation of the PPI. Uses for the wirewrap posts are contained in section 2-10.

2-12. INSTALLATION PROCEDURE

The Multimodule board mounts onto the host iSBC microcomputer. Install the board as follows:

a. With a non-metal ¼ inch x 6/32 screw, secure the ½ inch plastic spacer to the host iSBC microcomputer as shown in figure 2-4.

b. Locate pin 1 on the iSBX bus connector (P1) and align it with pin 1 of the iSBX bus connector on the host iSBC microcomputer.

c. Align the Multimodule board mounting hole with the spacer on the host iSBC microcomputer; reference figure 2-1.

d. Gently press the two boards together until the connector seats.

e. Secure the Multimodule board to the top of the spacer with the other ¼ inch x 6/32 screw.

NOTE

The placement of an installed Multimodule board and the host board connector number may vary according to the type of host iSBC microcomputer that is used.

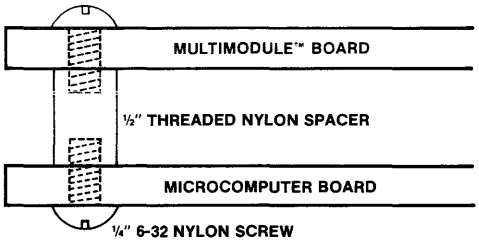


Figure 2-4. Mounting Technique

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter describes the programming of the iSBX 350 Parallel Multimodule Board, which entails programming the 8255A-5 Programmable Peripheral Interface (PPI). Three basic modes of operation for the PPI are supported; the basic Input/Output mode (Mode 0), the strobed Input/Output mode (Mode 1), and the Bidirectional Bus mode (Mode 2).

3-2. PPI PROGRAMMING

The PPI programming presented in the following text consists of sections on addressing, control word format, initialization, and operation of the PPI. Examples are included for a typical PPI port READ and port WRITE subroutine.

3-3. ADDRESSING

The PPI uses four consecutive addresses either X0 through X3 or X4 through X7 for the Multimodule board for data transfer and for port control. (Refer to table 3-1.) In some instances there may be more than one connector for a Multimodule board on the host iSBC microcomputer; each connector requires its own port address. In the examples in the following text, the first digit of the port address (X) is determined by the host iSBC microcomputer.

Table 3-1. Port Addresses

8255 Ports	Multimodule™ Connector Address
Port A	X0 or X4
Port B	X1 or X5
Port C	X2 or X6
Control	X3 or X7
Reserved	X8 to XF

NOTE: The first digit of each port I/O address is listed as "X" since it will change dependent on the type of host iSBC microcomputer used. Refer to the Hardware Reference Manual for your host iSBC microcomputer to determine the first digit of the port address.

NOTE

Note that addresses X8 through XF on the host microcomputer are reserved for the Multimodule board and must not be used by another device when the Multimodule board is installed onto the host iSBC microcomputer.

3-4. CONTROL WORD FORMAT

The control word format shown in figure 3-1 is used to initialize the PPI to define the operating mode of the three ports. Note that the ports are separated into two groups. Group A (control word bits 3

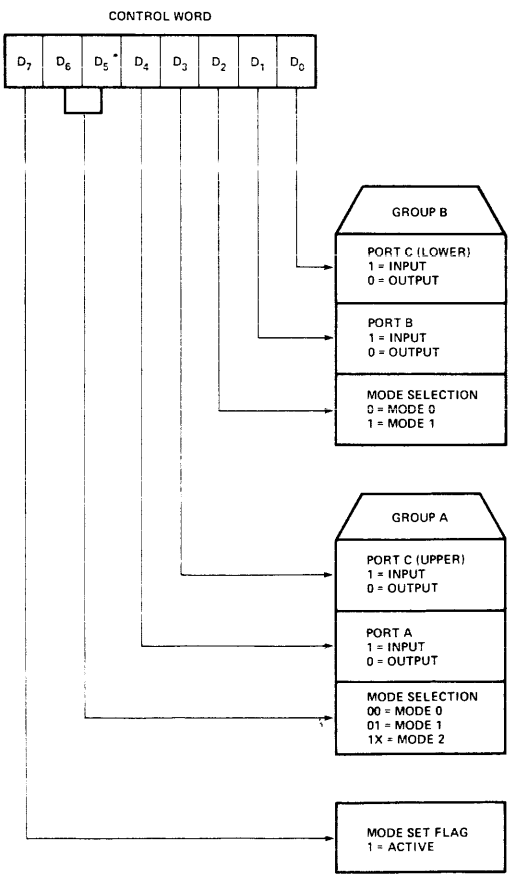


Figure 3-1. PPI Control Word Format

through 6) defines the operating mode for Port A (address X0 or X4) and the upper four bits of Port C (address X2 or X6). Group B (control word bits X0 through X2) defines the operating mode for Port B (address X1 or X5) and the lower four bits of Port C (address X2 or X6). Bit 7 of the control word reflects the mode set flag.

3-5. INITIALIZATION

To initialize the PPI, write a control word to port address X3 (or X7). Refer to figure 3-1 and table 3-2 and assume that the control word is 92 (hexadecimal). This initializes the PPI as follows:

a. Mode Set Flag active
b. Port A (X0 or X4) set to Mode 0 Input
c. Port C (X2 or X6) upper set to Mode 0 Output
d. Port B (X1 or X5) set to Mode 0 Input
e. Port C (X2 or X6) lower set to Mode 0 Output

3-6. OPERATION

After the PPI has been initialized, the operation is simply performing a READ or a WRITE to the appropriate port.

3-7. READ OPERATION. A typical read subroutine for Port A is given in table 3-3.

3-8. WRITE OPERATION. A typical write subroutine for Port C is given in table 3-4. As shown in figure 3-2, any of the Port C bits can be selectively set or cleared by writing a control word to address X3.

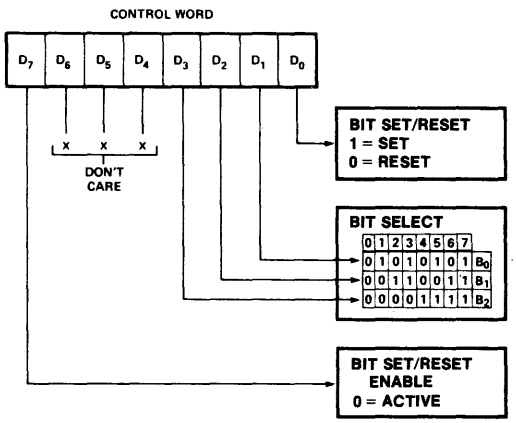


Figure 3-2. PPI Port C Bit Set/Reset Control Word Format

Table 3-2. Typical PPI Initialization Subroutine

```
;INT PAR INITIALIZES PARALLEL PORTS.
;USES-A: DESTROYS-A.
-
INT PAR:  MVI     A,92H          ;MODE WORD TO PPI PORT A & B IN, C OUT
          OUT     BASAD + 3      ;BASE ADDRESS + 3
          RET

          END
```

Table 3-3. Typical PPI Port READ Subroutine

```
;AREAD READS A BYTE FROM PORT A INTO REG A.
;USES-A; DESTROYS-A.

AREAD:    IN      BASAD          ;INPUT BYTE (BASE ADDRESS)
          RET

          END
```

Table 3-4. Typical PPI Port WRITE Subroutine

```
;COUT OUTPUTS A BYTE FROM REG A TO PORT C.
;USES-A; DESTROYS-NOTHING.

COUT:     OUT     BASAD + 2      ;OUTPUT BYTE (BASE ADDRESS + 2)
          RET

          END
```

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter presents the principles of operation of the iSBX 350 Parallel Multimodule Board. Included are sections covering the interfaces between the host microcomputer and the Multimodule board and between the parallel I/O lines and the Multimodule board. The interfaces to the Multimodule board and the interrupt system are detailed in the following text.

4-2. iSBX™ BUS INTERFACE

The interface to the host iSBC microcomputer consists of several signals which control the Multimodule board functions. Each signal is described in the following paragraphs and shown in the schematic diagram, included as figure 5-2.

RESET (Reset). This active high signal to the PPI provides initialization for the chip, resets the control register, and conditions all 8255A-5 ports to the input mode. RESET is derived from the microprocessor reset signal in the host iSBC microcomputer.

IOWRT/ (Write). This active low input to the Multimodule board indicates that data or a command is to be written into the PPI from the iSBX bus (MD0-MD7). Reference table 4-1.

IORD/ (Read). This active low input indicates that data is to be read from the PPI and made available on the iSBX bus (MD0-MD7). Reference table 4-1.

MCS0/ (Chip Select). This active low input selects the PPI, enabling communication between the PPI and the host iSBC microcomputer. Reference table 4-1.

MA0, MA1 (Address lines). The active high inputs to the Multimodule board, in conjunction with the IORD/ and IOWRT/ lines, control selection of one of three ports or the Control Word Register in the PPI. Reference table 4-1.

MD0-MD7 (Bidirectional Data Bus). These active high lines provide the interface for data and command transfer between the PPI and the host iSBC microcomputer.

MPST/ (Module present). This active low output signal indicates to the host iSBC microcomputer that a Multimodule board has been installed.

OPT0, OPT1 (Option signals). These user-defined signals are included to provide application flexibility for the Multimodule board. These signals, if required by the application, must be user-configured via jumpers.

MINTR0, MINTR1 (Interrupt signals). These signals are included to provide interrupt generation on the Multimodule board. These signals, if required by the application, must be user-configured via jumpers.

Table 4-1. PPI Operations

MA1	MA0	IORD/	IOWRT/	MCS0/	INPUT OPERATION (READ)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Illegal Condition
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus - 3-State
X	X	1	1	X	Data Bus - 3-State

4-3. PORT INTERFACE

The parallel port I/O (via connector J1) on the Multimodule board consists of three 8-bit ports that may be configured in one of several modes, as listed in table 4-2. The eight bits of Port A and eight bits of Port B must be configured as units to either input or output mode, but Port C may be broken into two groups of four, either of which can be used in input and/or output mode.

Data I/O through Port A passes through two 8226 Bidirectional Bus Drivers (U1 and U2) which control the direction of data flow according to the condition of DIEN/, the signal on jumper post E2. When DIEN/ is low, data flows from the PPI to the port data lines. Conversely, when DIEN/ is high, data flows from the port data lines to the PPI.

Four 14-pin DIP sockets are provided for user-supplied line driver/receiver device installation onto the Port B and Port C data lines. The type of line driver/receiver device is determined by the application.

Table 4-2. Mode Definition Summary Table

	Mode 0		Mode 1		Mode 2
Port/Bit	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	Bidirectional
PA_1	IN	OUT	IN	OUT	Bidirectional
PA_2	IN	OUT	IN	OUT	Bidirectional
PA_3	IN	OUT	IN	OUT	Bidirectional
PA_4	IN	OUT	IN	OUT	Bidirectional
PA_5	IN	OUT	IN	OUT	Bidirectional
PA_6	IN	OUT	IN	OUT	Bidirectional
PA_7	IN	OUT	IN	OUT	Bidirectional
PB_0	IN	OUT	IN	OUT	—
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	OBF_B/	I/O
PC_2	IN	OUT	STB_B/	ACK_B/	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	STB_A/	I/O	STB_A/
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	ACK_A/	ACK_A/
PC_7	IN	OUT	I/O	OBF_A/	OBF_A/

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, and service and repair assistance instructions for the iSBX 350 Parallel Multimodule Board.

5-2. REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the Multimodule board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column in table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML"; every effort should be made to procure these parts from a local (commercial) distributor.

5-3. SERVICE DIAGRAMS

The parts location diagram and schematic diagram for the Multimodule board are provided in Figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g. MCS0/) is active low. Conversely, a signal mnemonic without a slash (e.g. OPT0) is active high.

Table 5-2. Manufacturer Codes

Mfr. Code	Manufacturer	Address
AMP	AMP, Inc.	Harrisburg, PA
INTEL	Intel Corporation	Santa Clara, CA
TI	Texas Instruments	Dallas, TX
COML	Any Commercial Source Order By Description (OBD)	

5-4. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the MCSD Technical Support Center in Santa Clara, California at one of the following numbers:

Telephone:

From Alaska, Arizona, or Hawaii call:
(602) 869-4600

From all other U.S. locations call toll free:
(800) 528-0595

TWX Number: 910-951-1330

Table 5-1. Replaceable Parts

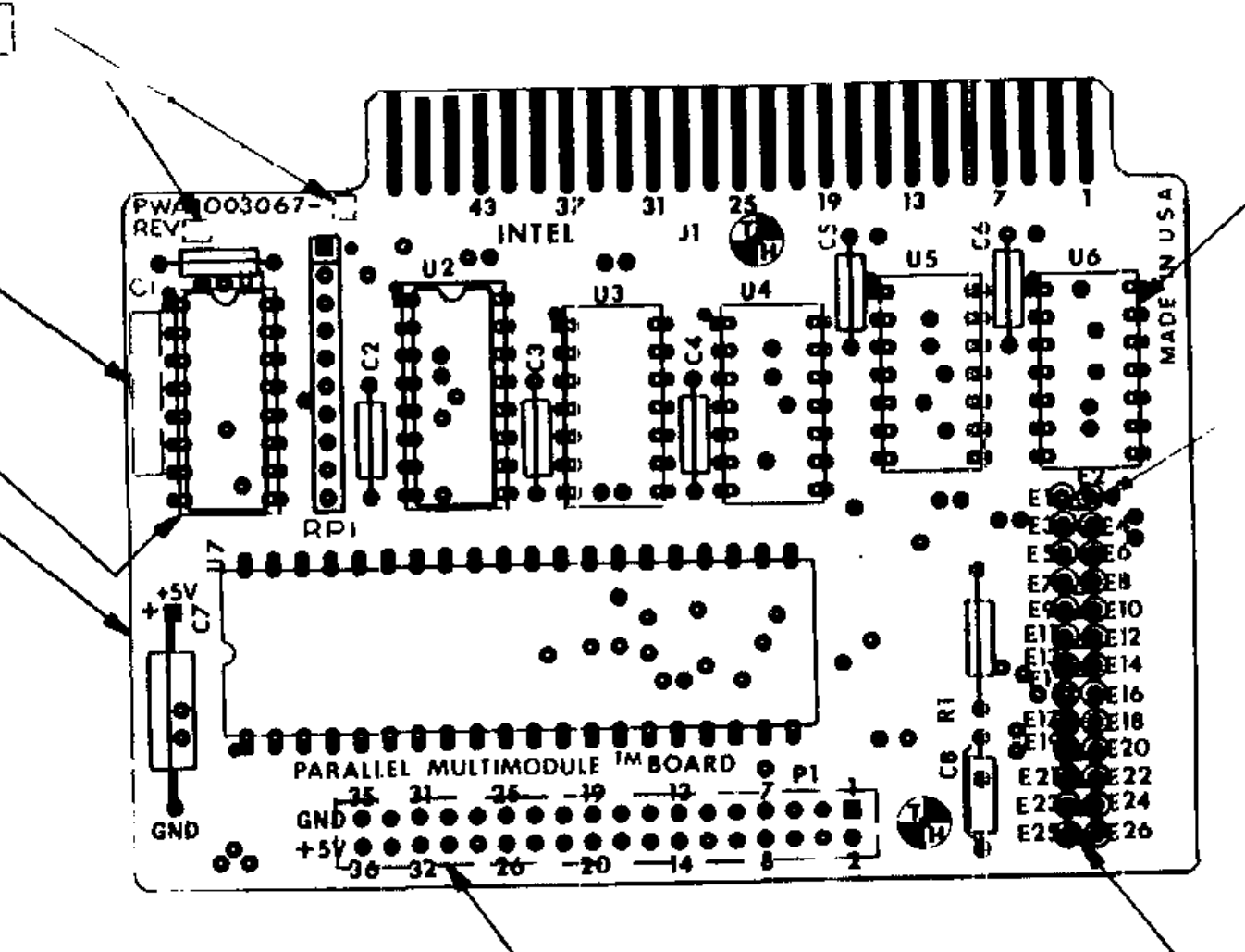
Reference Designation	Description	Mfg. Part No.	Mfr. Code	Qty.
U1, U2	IC, 8226 Bidirectional Data Buffer	8226	INTEL	2
XU3,XU4,XU5,XU6	Socket, 14-pin DIP	C93-14-02	TI	4
U7	IC, 8255A-5 Programmable Peripheral Interface	P8255A-5	INTEL	1
R1	Resistor, 1K, ¼W, 5%	OBD	COML	1
RP1	Resistor Pack, 10-pin, 1K 2%	OBD	COML	1
C7	Capacitor, tant, 22μf, 15V, 10%	OBD	COML	1
C1,C2,C3,C4, C5,C6,C8	Capacitor, 0.1μf, 50V +80% -20%	OBD	COML	7
P1	Connector, 36 pin, male	103109-001	INTEL	1
E1-E26	Post, Wire wrap	87022-1	AMP	26
XU1,XU2	Socket, 16-pin DIP	C93-16-02	TI	2

Always contact the MCSD Technical Support Center before returning a product to Intel for service or repair. You will be given a "Repair Authorization Number", shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment from Intel, or if the product is out of warranty, a purchase order is necessary in order for the MCSD Technical Support Center to initiate the repair.

In preparing the product for shipment to the MCSD Technical Support Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by MCSD Technical Support Center personnel.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.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INTEL
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PARALLEL MULTIMODULE ™ BOARD
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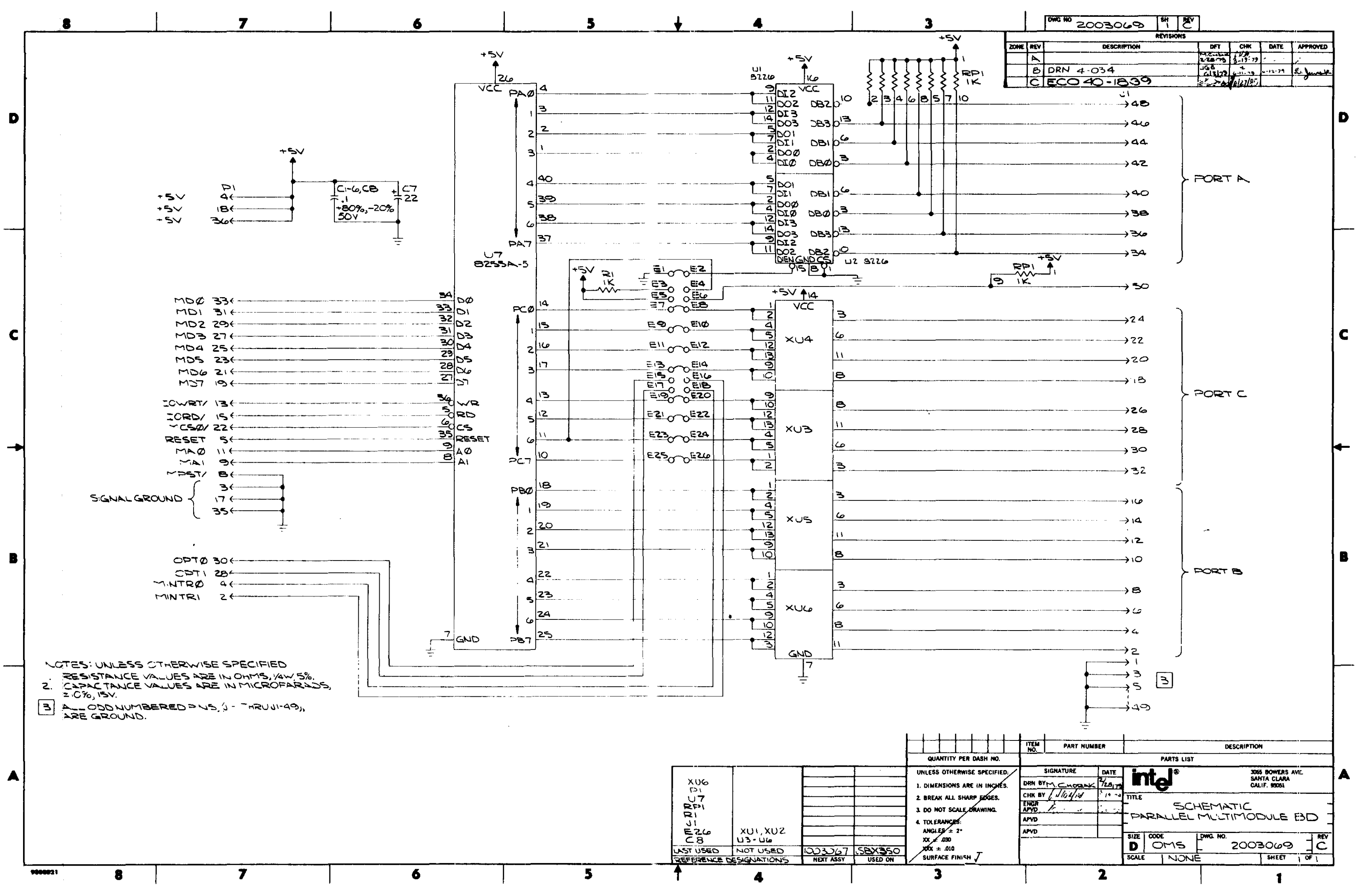

DWG NO 2003069 SH 1 REV C
REVISIONS
ZONE | REV | DESCRIPTION | DFT | CHK | DATE | APPROVED
A
B DRN 4-034
C ECO 40-1839
+5V
RP1 1K
U1 8226
U2 8226
VCC
DI2 DO2 DI3 DO3 DO1 DI1 DOØ DIØ
DB2 DB3 DB1 DBØ
DIEN GND CS
U7 8255A-5
PAØ PA7 PCØ PC7 PBØ PB7
DØ D1 D2 D3 D4 D5 D6 D7
WR RD CS RESET AØ A1 GND
MDØ 33
MD1 31
MD2 29
MD3 27
MD4 25
MD5 23
MD6 21
MD7 19
IOWRT/ 13
IORD/ 15
MCSØ/ 22
RESET 5
MAØ 11
MA1 9
MPST/ 8
SIGNAL GROUND 3 17 35
OPTØ 30
OPT1 28
MINTRØ 4
MINTR1 2
P1
+5V 4
+5V 18
+5V 36
C1-6,C8 .1 +80%,-20% 50V
C7 22
R1 1K
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20 E21 E22 E23 E24 E25 E26
XU4 XU3 XU5 XU6
J1
PORT A
PORT C
PORT B
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS, 1/4W 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 15V.
3 ALL ODD NUMBERED PINS, (J1 THRU J1-49), ARE GROUND.
XU6 P1 U7 RP1 R1 J1 E26 C8
LAST USED
XU1, XU2 U3-U6
NOT USED
REFERENCE DESIGNATIONS
1003067 NEXT ASSY
SBX350 USED ON
QUANTITY PER DASH NO.
UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ± 2° .XX ± .030 .XXX ± .010
SURFACE FINISH
ITEM NO. | PART NUMBER | DESCRIPTION
PARTS LIST
SIGNATURE DATE
DRN BY M. CHODNIK
CHK BY
ENGR APVD
APVD
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intel
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