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APPLICATION NOTE

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Designing With Intel's 8022 Microcomputer

Will Ittner
MCO Applications

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"MCS-48 Family of Single Chip Microcomputers User's Manual"

"Crystals: Specifications for Intel Components"

"Application Techniques for the MCS-48 Family"

"Keyboard/Display Scanning with Intel's MCS-48 Microcomputers"

"MCS-48 and UPI-41 Assembly Language Manual

Designing With Intel's 8022 Microcomputer

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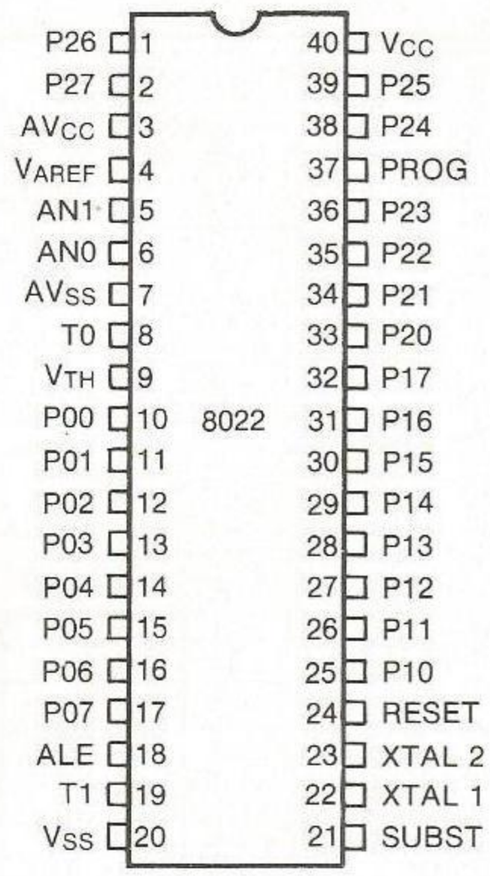


Figure 1. Pin Configuration

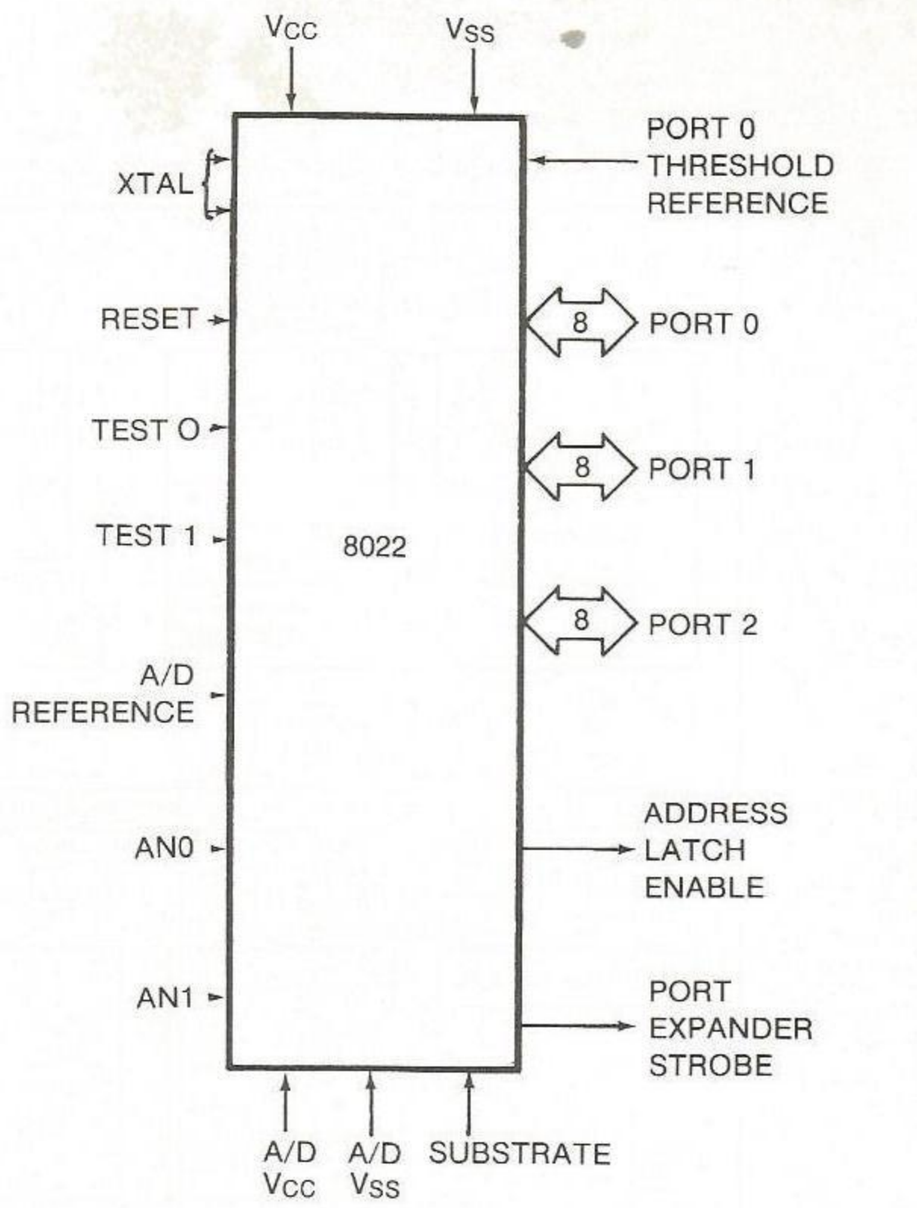


Figure 2. Logic Symbol

INTRODUCTION

Taking advantage of the latest advances in silicon technology, Intel has developed a complete control system on a chip, the 8022, the first 8-bit microcomputer with an A/D converter on-chip. Whereas in the past microcomputers relied on external circuits for analog interfacing, it is now possible to build a one chip control system with analog interfacing, digital interfacing, and computer processing capabilities. Tackling the high volume, low cost controller market, the Intel 8022 microcomputer fits cost and space sensitive applications such as automobiles, appliances, and consumer products previously dominated by electromechanical controls. Its use, however, is not confined only to these applications. In medium volume applications, the 8022 provides the system designer with a simplified solution to many control problems. No longer is it necessary to expend valuable engineering time designing wheel spokes and axles; the whole cart is available.

This note is intended to answer some design questions concerning the 8022 and to suggest to the reader possible applications and system configurations. The reader should refer to the 8022 Data Sheet for electrical specifications and details. It is also suggested that the reader consult with the MCS-48 User's Manual (July 1978 or later) for a complete description of the entire MCS-48 family of microprocessors of which the 8022 is the newest member.

The note is divided into two main sections. The first is a product description of the 8022, including a detailed discussion of the main features, their characteristics and how to use them, The second section discusses several possible applications, their configurations and design considerations.

Product Overview

The heart of the 8022 is the Intel 8021, a general purpose single chip microcomputer, which is a lower performance, lower cost version of the 8048. Added to this central core are interrupts, additional I/O, and linear functions. Like the 8021, the 8022 is designed to operate over a power supply range of 4.5 to 6.5 volts.

The 8022 instruction set contains over 70 instructions and is a subset of the 8048 instruction set. To conserve memory and maximize throughput, most instructions are single-byte, single-cycle. No instructions are longer than two-byte, two-cycle. The instruction cycle time is 10 microseconds at a 3MHz clock rate. Extensive conditional branch logic is built into the processor to increase the overall efficiency of the instruction set for control applications. As examples, the DJNZ instruction (decrement register and jump if not zero) allows loops to be formed in just one instruction and the MOVP A, @A allows single instruction table look-up of constants from program storage. Program storage in the 8022 consists of 2048 eight bit bytes of mask programmable ROM.

Hardware stack and data memory are integrated in the 64 byte RAM to enhance processing flexibility and memory utilization. The first eight RAM locations are designated as working registers and are directly addressable by any of the 11 direct register instructions. Besides increasing the variety of operations that can be performed on data in memory, this approach further reduces the number of instruction bytes required for processing. In addition to being used as working registers, Registers 0 and 1 can be used as Pointer registers to indirectly address all locations in memory using the indirect register instructions.

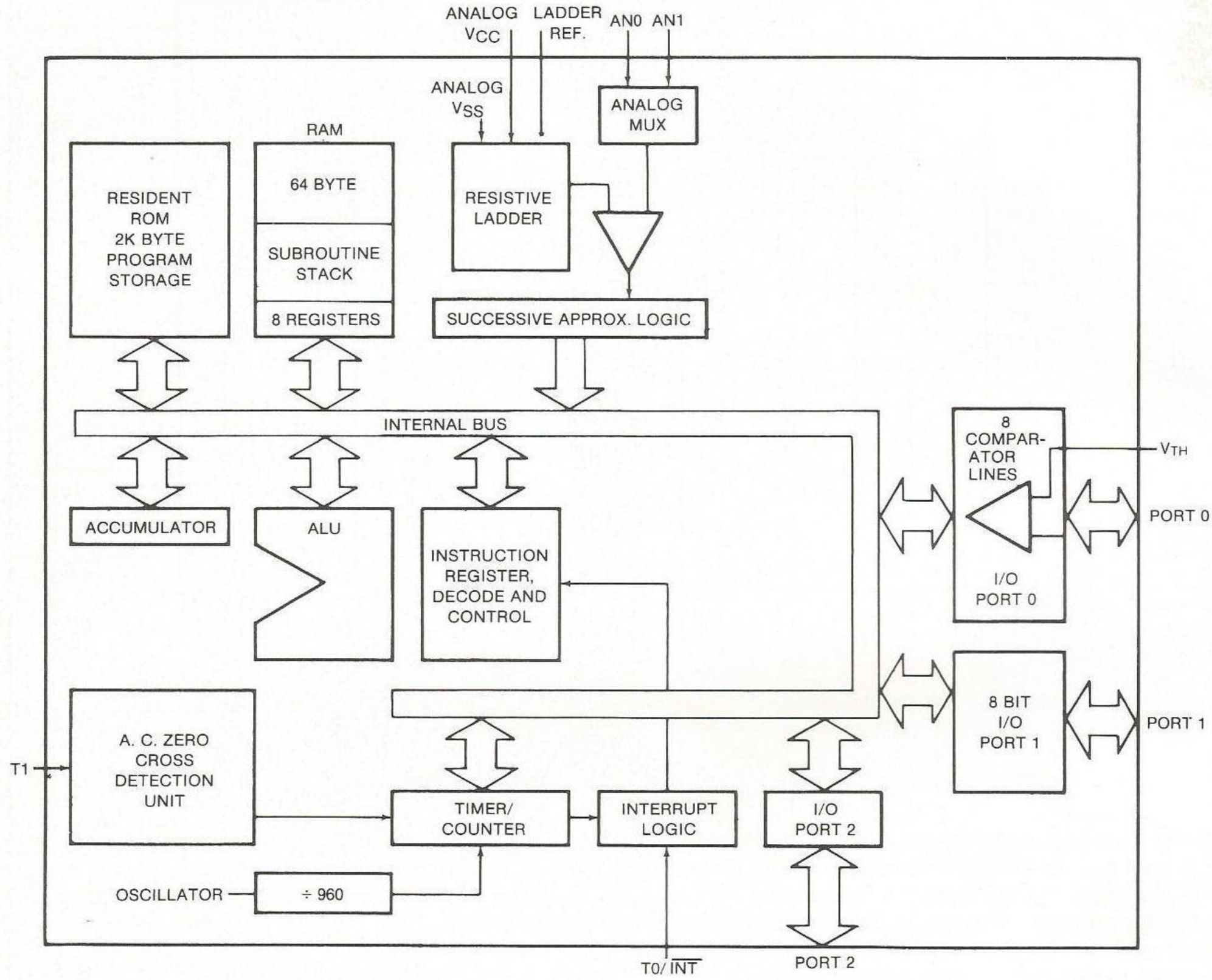


Figure 3. 8022 Block Diagram

The next 16 bytes of RAM may be used as the address stack to enable the processor to keep track of the return addresses generated from instructions and in handling interrupts. Since two bytes are needed to store each address, the 16 bytes of address stack allow up to a total of eight levels of subroutine nesting. A 3-bit stack pointer supplies the address of the locations to be loaded with the next return address generated. This stack pointer is incremented when a return address is stored and decremented when an address is fetched during a subroutine or interrupt return. If all eight levels of subroutine nesting are not required by an application, the unused portion of the address stack may be used as standard RAM.

The 8022 has an extremely flexible and powerful I/O structure. The 26 digital I/O lines are configured into three 8-bit general-purpose ports and two test pins, T0 and T1. All three ports are quasi-bidirectional, meaning all lines are useable as inputs or outputs on a line-by-line basis under software control.

To increase the user's flexibility, any line of Port 0 can also be designated an open drain output by removing the pullup device present on the line via mask option. This is useful in driving analog circuits and interfacing to high impedance digital I/O. In addition to the open drain option, Port 0 has voltage comparator inputs with a common reference pin (V_{TH}). In appliance control and other applications, this allows direct glass touchpanel interfacing with relatively low voltage (10-15V) drive, thus limiting product liablility problems and easing U.L. approval. The Port 0 comparator inputs are also generally useful in many other ways from expanding analog inputs to maximizing margin on noisy signals.

To further increase user flexibility and reduce system cost, two I/O pins (P10 and P11) have been designated as high current drive pins with the ability to sink 7ma each, instead of the standard TTL load of 1.6ma. This can eliminate the need for discrete drive transistors in many applications.

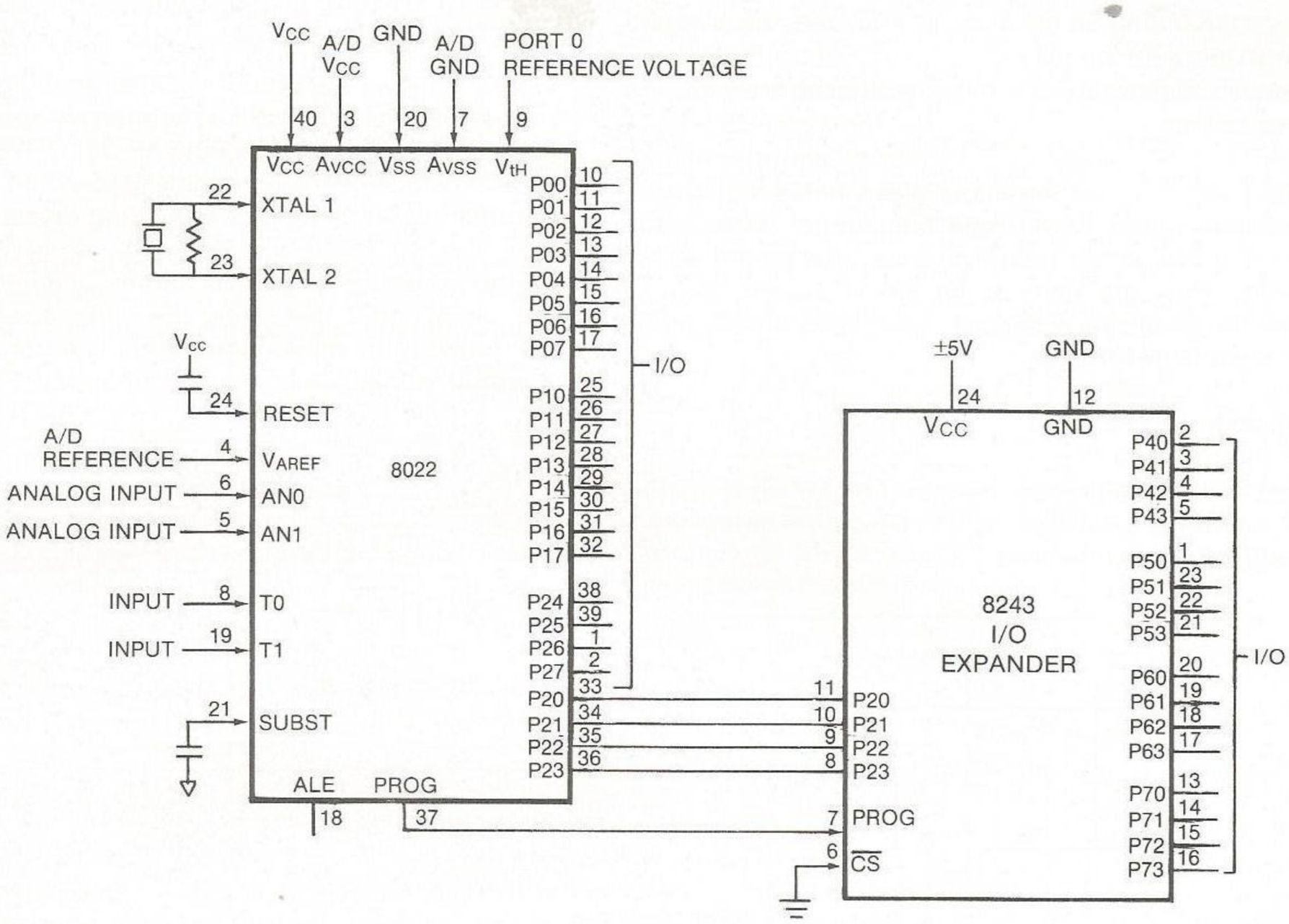


Figure 4. Adding an I/O Expander to the 8022

The lower half of Port 2, in addition to serving as a general-purpose I/O port, is used as a "bus" for attaching the Intel 8243 I/O expander units. The Port Expander Strobe is used in conjunction with Port 2 to synchronize the 8243 operations. Figure 4 shows such a configuration.

Note that the quasi-bidirectional structure and the Port 2 expansion bus are consistent with all MCS-48 products and are fully described in the MCS-48 User's Manual.

Frequently in control applications, the state of one or two signals must be monitored so that a fast response can be accomplished. The 8022's two test pins offer this capability. Both test pins, T0 and T1, are directly testable via two conditional branch instructions. The T0 pin can also cause an interrupt. The T1 pin, in addition to being directly testable, has the ability to detect the zero crossing of slowly moving AC inputs. This is useful in controlling 50/60Hz power. It also enables the 8022 to precisely control phase sensitive devices, such as triacs and SCRs. Again external circuitry is reduced.

The 8022 contains its own clock and oscillator circuitry and requires only an external timing control element to generate all internal timing signals. An inductor, a crystal, or an external clock may be used as the timing control device.

The programmable 8-bit timer/event counter enables the user to accurately monitor elapsed time by providing a hardware replacement for software overhead such as timing loops. Total count capacity is 8192 instruction cycles or 81.9 msec at a 10 microsecond cycle time. The timer may also be used as an event counter where the Test 1 input serves as a counter input. After a STRT CNT command, low to high transitions on the T1 pin will cause the timer/counter to be incremented. When the timer counter overflows (FFH to 00), the timer flag will be set and an interrupt generated if enabled.

The analog to digital converter is designed to simplify and cost reduce interfacing to analog sources. All parts of the converter are integrated onto the chip, with the exception of the voltage reference. Conversion is completely hardware controlled using a successive approximation technique and occurs in four instruction cycles or 40 microseconds. Three single byte instructions, SEL AN0 (select analog input 0), SEL AN1 (select analog input 1), and RAD (read A/D conversion result) are added to the 8021 instruction set to allow the programmer to interface to the converter conveniently.

Product Features

This next section will delve deeper into some of the functions which comprise the 8022 architecture. Chip architecture will be discussed along with design considerations, software routines, and hardware configurations. The specific items covered are CPU timing, the Timer/Counter, the TEST and Interrupt inputs, Zero Cross detection, the A/D converter, and the Port 0 comparator inputs.

System Clock

One of the first considerations in the system design is what frequency source should be used. The on-board oscillator can use a variety of elements to determine system fre-

quency. Depending on the accuracy needed, the element can be an inductor and capacitor, or a crystal and resistor. If necessary, the oscillator inputs can also be driven by an external source.

It should be noted that the values given in this section are approximate values based on a sampling of parts. In no case are these to be interpreted as guaranteed specifications. They are here as an aid in system design. Consult the final Data sheet or contact Intel direct if more information is needed for a critical design.

Inductor Mode

Figure 5 shows the proper configuration for the inductor mode. A parallel capacitor of 20 to 50pf is recommended for best frequency tolerance.

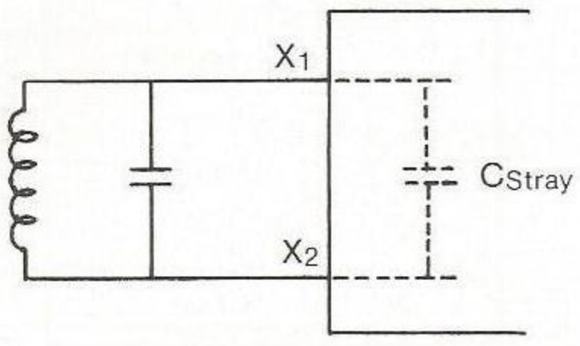


Figure 5.

Table 1 shows the effects of changes in parameters based on a sampling of parts. Part to part input capacitance differences (Cstray) will effect the tolerance. A less than 0.2% part to part tolerance can be expected with a parallel capacitance of 50pf. (see fig. #5). An additional 0.5% variation comes about when only 20pf is used in the tank circuit. This is because the stray capacitance in the 8022 and the PCB becomes a larger proportion of the total capacitance.

Vcc =	4.5v	5.5v	6.5v
f =	$\pm$0.2%	0	$\approx$0.2%
Temp =	-40°C	25°C	85°C
f =	$\pm$0.6%	0	$\approx$0.6%

Table 1. Inductor Mode

To determine the inductance and capacitance required for a given frequency, the equation

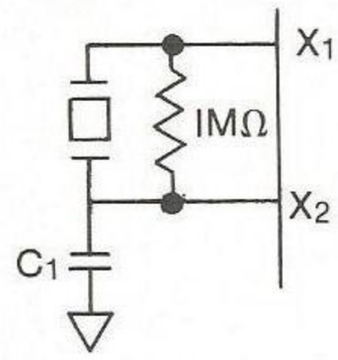
$$f = \frac{1}{2\pi\sqrt{LC}}$$

can be used. Due to the effects of stray capacitance the calculated frequency may be slightly high. It should be noted that the tolerances given in Table 1 do not include the tolerances of the inductor and capacitor used in the system. Mathematical analysis of the above equation will show that the frequency will change roughly proportional to the tolerances of L and C on a worst case situation. That is if both L and C are ±5% parts, the frequency will vary approximately ±5%.

Crystal Mode

Figure 6 shows the proper installation of a crystal. A one meg-ohm parallel resistor is required for operation with an 8021 or 8022. Application note AP-35 "CRYSTALS: Specifications for Intel Components" should be consulted for information on using and specifying crystals.

A 20pf capacitor is optional, but recommended, on X2. It has been found that using the capacitor increases the immunity of the microcomputer to line transient noise or spurious signals which may find their way into the system.



C_1 is an optional 20pf capacitor

Figure 6.

Which One?

Which timing source to use is dependent on several factors. In most applications cost is of primary importance. The lowest cost device, but one which still gets the job accomplished, is the logical choice. Selecting the device which gets the job accomplished is the next task.

A Case Study

To exemplify the design tradeoffs in choosing a timing element consider the detection of 50Hz or 60Hz line frequency as may be needed in many consumer products being sold in the U.S. and overseas. Traditionally two products are produced, one for the U.S. market and one for the overseas market. A jumper selection to tell the processor which frequency source is being used is the only difference. This costs one I/O pin plus the costs of insertion and inventorying two products. All of these costs can be saved by allowing the processor to compute which frequency is coming in on the T1 pin. Figure 7 lists the software which could be used during a power-up routine to determine whether 50Hz or 60Hz timing should be used.

The timer is used to time the interval of one line cycle. If everything were perfectly accurate, one count would equal 50Hz while another count would equal 60 Hz, but it's not. The power company frequency may shift slightly, plus the 8022 oscillator may drift as discussed earlier. The maximum allowable oscillator change must be calculated from the input source. Assuming the power companies may drift ±2 cycles, then the processor must be able to detect a difference of 58Hz-52Hz = 6Hz or less than 10.3% change. This means that the oscillator frequency itself cannot change more than 10.3% or ±5.15%. The crystal would definitely work but may be overkill. The Inductor/capacitor combination could be the most economical solution.

The equation

$$\frac{\frac{1}{LF}}{\frac{1 \times 30 \times 32}{f}} = \text{count}$$

where LF = line freq,
f = osc. freq.

will give the value of the time at the end of one line cycle. Plugging in the values for an oscillator of 3MHz ±5% and a ±2 cycle deviation in line freqency, the counter will yield counts of:

47–56 = 60Hz
57–68 = 50Hz

Inductor and capacitor components could be picked to yield the required tolerance, saving the costs previously mentioned.

Timer/Counter

An 8-bit interval timer/counter is available to enable the user to keep track of time elapsed or number of events occured while normal program execution and flow continues. The Auto 50/60Hz detection routine previously discussed is one of many possible applications of the timer/counter.

The timer/counter consists of a divide by 32 prescaler (only used in the timer mode) and an eight bit main timer. The STRT T command clears the prescaler and thereafter it increments once each 30 input clocks (once each single cycle instruction, twice each double cycle instruction). At the (11111) to (00000) transition the timer is incremented. A timer overflow from (FFH) to (00H) will set the timer flag along with the timer interrupt, if enabled (see below). A conditional branch instruction (JTF) is available for testing

```
LOC  OBJ          LINE        SOURCE STATEMENT

                     1 ;
                     2 ;       AUTO 50/60HZ DETECTION ON POWER UP
                     3 ;       ==================================
                     4 ;
                     5 PWRUP:
0000 27              6         CLR     A         ;CLEAR ACCM
0001 0414            7         JMP     PWRDET    ;JUMP AROUND INTERRUPT ROUTINES
                     8 ;
                     9 ;
                    10 ;       INTERRUPT ROUTINES HERE
                    11 ;
                    12 ;
0014                13         ORG     20
                    14 ;
                    15 ;       MEASURE ONE LINE CYCLE
                    16 ;       ----------------------
                    17 ;
                    18 PWRDET:
0014 5614           19         JT1     PWRDET    ;WAIT FOR NEXT RISING EDGE
                    20 LINLOW:
0016 4616           21         JNT1    LINLOW    ;WAIT FOR NEXT RISING EDGE
0018 62             22         MOV     T,A       ;CLEAR TIMER
0019 55             23         STRT    T         ;START TIMER
                    24 LINEHI:
001A 561A           25         JT1     LINEHI    ;WAIT HERE FOR LINE TO GO LOW
                    26 RISEDG:
001C 461C           27         JNT1    RISEDG    ;WAIT HERE FOR RISING EDGE
001E 65             28         STOP    TCNT      ;STOP TIMER AT END OF ONE LINE CYCLE
001F 42             29         MOV     A,T       ;READ TIMER VALUE
0020 03D1           30         ADD     A,#-47    ;SUBTRACT 47
0022 E62C           31         JNC     ORANGE    ;ERROR-NOT WITHIN RANGE
0024 03F6           32         ADD     A,#-10    ;SUBTRACT 10
0026 E62C           33         JNC     HZ60      ;JUMP TO 60HZ ROUTINE
0028 03F4           34         ADD     A,#-12    ;SUBTRACT 12
002A F62C           35         JC      ORANGE    ;ERROR-NOT WITHIN RANGE
                    36 HZ50:
                    37                           ;SET 50HZ FLAG
                    38 HZ60:
                    39                           ;SET 60HZ FLAG
                    40 ORANGE:
                    41                           ;LINE FREQUENCY ABNORMAL TRY AGAIN
                    42
                    43
                    44
                    45
```

Figure 7.

this flag, the flag being reset each test. This instruction must also be used to initialize the timer overflow flag after a RESET, as RESET does not perform this function. Total count capacity for the timer is $2^5 \times 2^8 = 8192$ or 81.9 ms at a 10 micro second cycle time. Contents of the timer are moved to the accumulator by the MOV A,T instruction without disturbing the counting process. Conversely, the MOV T,A instruction loads the timer with the contents of the accumulator. Notice that the 8-bit timer can be read from and written to. The prescaler, however, can not. It is a separate 5-bit counter which is cleared only by a STRT T command.

The timer may also be used as an event counter. After a STRT CNT command the 8022 will respond to low-to-high transitions on the Test 1 pin by incrementing the timer. Transitions can occur no faster than once each three instruction cycles (every 30 microseconds when using a 3 MHz clock)—there is no minimum frequency. In this mode the prescaler is not used. The timer will contain the number of positive transitions occuring on T1 since a STRT CNT command.

The timer and event counter functions are mutually exclusive. Counting or timing may be started (STRT CNT, STRT T) or stopped (STOP TCNT) under program control.

The T1 pin, besides being an input to the counter, can also function as a testable input, detect the zero crossing of an AC signal, and interrupt processing. These functions, as well as those of the Test 0 pin and the interrupt structure, will be discussed in the next section.

Test And Interrupt Inputs

In addition to the 24 general purpose I/O lines which comprise ports 0, 1, and 2, the 8022 has two special inputs, T0 and T1, which are testable via conditional jump instructions. These pins allow inputs to cause program branches without the necessity to load an input port into the accumulator. The instructions JT0, JNT0, JT1, JNT1 will cause program flow to be modified depending on the state of the T0 or T1 pin. For instance, JT0 will cause a jump to the specified address if the T0 pin is high (a 1 level). Conversely, JNT0 will jump if T0 is low (a 0 level). If the jump does not occur, program flow continues with the next instruction.

The Test 0 pin serves as an external interrupt input as well as a testable input. An interrupt sequence is initiated by applying a low "0" level input to the T0 pin when the external interrupt is enabled (EN I). The interrupt is level triggered and active low to allow "WIRE ORING" of several interrupt sources at the input pin. When an interrupt is detected it causes a "call to subroutine" to location 3 in program memory as soon as all other cycles of the current instruction are complete. At this time, the program counter contents are saved in the program counter stack, but the remaining status of the processor is not.

Unlike the 8048, the 8022 does not contain a program status word. Thus, when appropriate, the carry and auxiliary carry flags must be saved by the software, as must be the accumulator. The routine shown below saves the accumulator and the carry flags.

```
Instructions    Comments
MOV R6,A        ;save accumulator in register 6
CLR A           ;clear accumulator
DA A            ;convert carry flags into sixes
MOV R7,A        ;save representation of carry flags
```

The end of an interrupt service subroutine is marked by the execution of a Return from Interrupt instruction (RETI). Prior to returning from the interrupt subroutine however, the status of the accumulator and the carry flags must be restored. The following routine restores the status of the accumulator and the carry flags, which were previously saved by the above program segment.

```
Instructions    Comments
MOV A,R7        ;restore carry flags status to
ADD A,#0AAH     ;accumulator and set/clear
                ;carry flags
MOV A,R6        ;restore accumulator
RETI            ;return from interrupt
```

An interrupt or CALL to a subroutine causes the contents of the program counter to be stored in one of the eight register pairs of the Program Counter Stack. During a CALL instruction the program counter, when saved, points to the second byte of the CALL instruction (or the return address minus one). The stack contents are then incremented before being loaded into the program counter during a return (RET) from subroutine. During an interrupt the program counter, when saved, points directly to the return address. Thus, during a return (RETI) from interrupt, the stack contents are not incremented but loaded directly into the program counter. This difference makes it imperative to use only RETI's to return from interrupts, and RET's to return from subroutines.

The interrupt system is single level in that once an interrupt is detected all further interrupt requests are ignored until execution of a RETI re-enables the interrupt input logic. This sequence holds true also for an internal interrupt generated by timer overflow. If an external interrupt and an internal timer/counter generated interrupt are detected at the same time, the external source will be recognized first, if enabled. The timer/counter interrupt will be recognized, if enabled, after the return (RETI) from the external interrupt. Timer/counter generated internal interrupts and T0 generated external interrupts have separate vector locations. The external interrupt will vector to location 3, whereas an internal interrupt will vector to location 7.

If needed, a second external interrupt can be created by enabling the timer/counter interrupt (EN TCNTI), loading FFH into the counter (one less than terminal count) and enabling the event counter mode (STRT CNT). A low-to-high transition on the T1 input will then cause an interrupt vector to location 7.

Zero Cross Detect

The Test 1 pin, in addition to being a testable input and a counter input, also serves one other important function. It can be used to detect the zero crossing point of slow moving AC signals. Execution of the STRT CNT instruction puts the T1 pin in the counter input mode by connecting T1 to the counter and enabling the counter. Subsequent low-to-high transitions on T1 will cause the counter to increment. Note that this operation differs from the rest of the MCS-48 devices, which increment the counter on high-to-low transitions. This change was made on the 8022 to take advantage of the accuracy of the rising edge detection on the zero cross circuitry.

When driven directly, this pin responds as a normal digital input. To utilize the zero cross detection mode, an AC signal of approximately 1-3 VAC p-p magnitude and a maximum frequency of 1kHz is coupled through an external capacitor (1 microfarad) to the T1 pin. The internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one. This is accomplished by the self-biasing high gain amplifier which is included in the T1 input. This circuit biases the T1 input exactly at its switching point, such that a small change will cause a digital transition to occur. This digital transition takes place within 5 degrees of the zero point.

The digital value of T1 remains a one until the falling edge of the AC input drops approximately 100mV below the switching point of the rising edge (100mV below the zero point, if the digital transition occured exactly at the zero point). The 100 mV offset is created by hysterisis and eliminates chattering of the internal signal caused by external noise.

The accuracy of the zero crossing will be a function of the capacitor used (see Fig. 10). On critical systems the capacitor can be adjusted to improve overall accuracy.

NOTE:

1. WHEN INTERRUPT IN PROGRESS f/f IS SET ALL FURTHER INTERRUPTS ARE LOCKED OUT INDEPENDENT OF STATE OF EITHER INTERRUPT ENABLE f/f.

2. WHILE TIMER INTERRUPTS ARE DISABLED TIMER OVERFLOW f/f WILL NOT STORE ANY OVERFLOW THAT OCCURS. TIMER FLAG WILL BE SET, HOWEVER.

Figure 8. Interrupt Logic

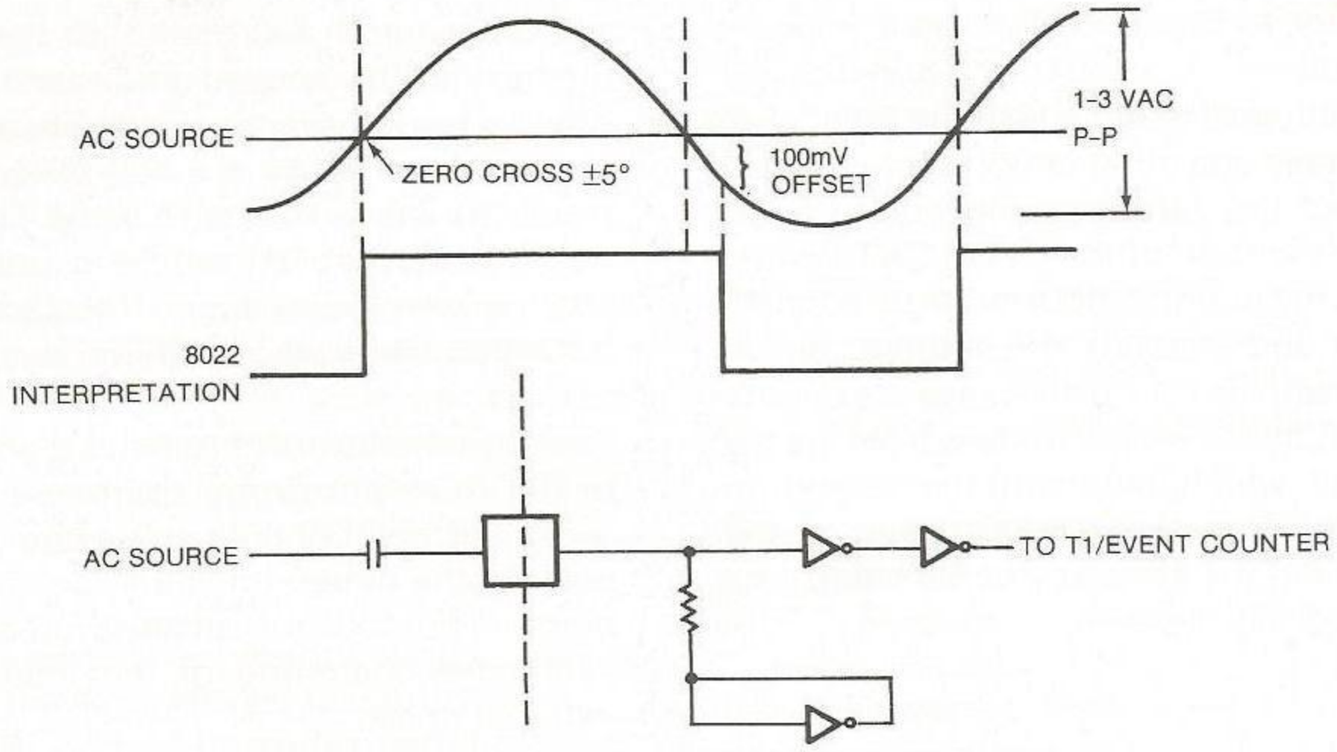


Figure 9. Zero Cross Detection

The phase angle at the T1 input can be expressed as

$$\Theta = \arctan \frac{X_C}{R}$$

where $X_C = \frac{1}{2\pi fC}$

$R = 150K\Omega$ (see fig. 10)

Solving the equation using the recommended one microfarad capacitor and 60Hz

$$X_C = \frac{1}{2\pi\ (60)\ (1\mu f)}$$

$$= 2652.6$$

$$\Theta = \arctan \frac{2652.6}{150K\Omega}$$

$$= -1.01^0$$

shows the voltage at the pin slightly leading the true AC voltage. Internally the circuit adds up to another five degrees before the processor can detect that a zero crossing occured. Software can also add several degrees before outputing a signal. To compensate for all of this delay, a smaller capacitor could be chosen to give a -5 degree shift in hardware before the processor.

The zero cross detection capability allows the user to make the 50/60 Hz power signal the basis for his system timing. All timing routines, including time-of-day, can be implemented using the zero cross detection capability of T1 and its conditional jump instructions. In addition, the zero cross detection feature can be used in conjunction with the timer interrupt, as discussed earlier, to interrupt processing at the zero voltage point. This enables the user to control voltage phase sensitive devices such as triacs and SCRs, and to use the 8022 in applications such as shaft speed and angle measurement.

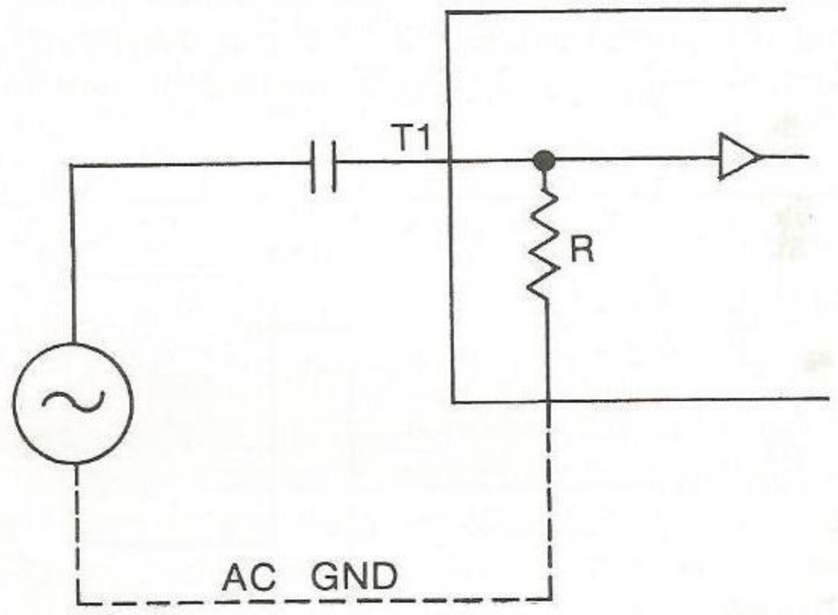


Figure 10. AC Equivalent of Zero Cross Input

Analog To Digital Converter

The T1 zero cross function is only one of the linear functions incorporated into the 8022 architecture. The most noted linear function is that of a complete analog to digital converter.

The analog to digital converter is a complete successive approximation converter with two multiplexed input channels. Either channel is selected by software with the SEL AN0 or SEL AN1 instruction. These instructions also restart the conversion sequences. A valid digital value can be read with the RAD (read A/D) instruction during the fourth instruction cycle following a select instruction. Conversions occur continuously, and RAD may be executed at any time with confidence that the sample is no more than 40 microseconds old.

The converter hardware has three parts as shown in Figure 11, a series string of resistors, a voltage comparator, and successive approximation logic. A series string of 256 matched resistors divides the voltage between AVss and V_{AREF} (the reference pin) into 256 voltage steps. This configuration gives the converter its inherent monotonicity.

The voltage tap on the series resistor string is selected by

the resistor ladder decoder. This decoder is driven by the 8-bit successive approximation register (SAR). Each bit of the SAR is set in succession MSB to LSB and a voltage comparison between the selected resistor ladder voltage and the analog input voltage is performed after the setting of each bit. The result of each comparison determines whether the particular bit will remain set or be reset. All

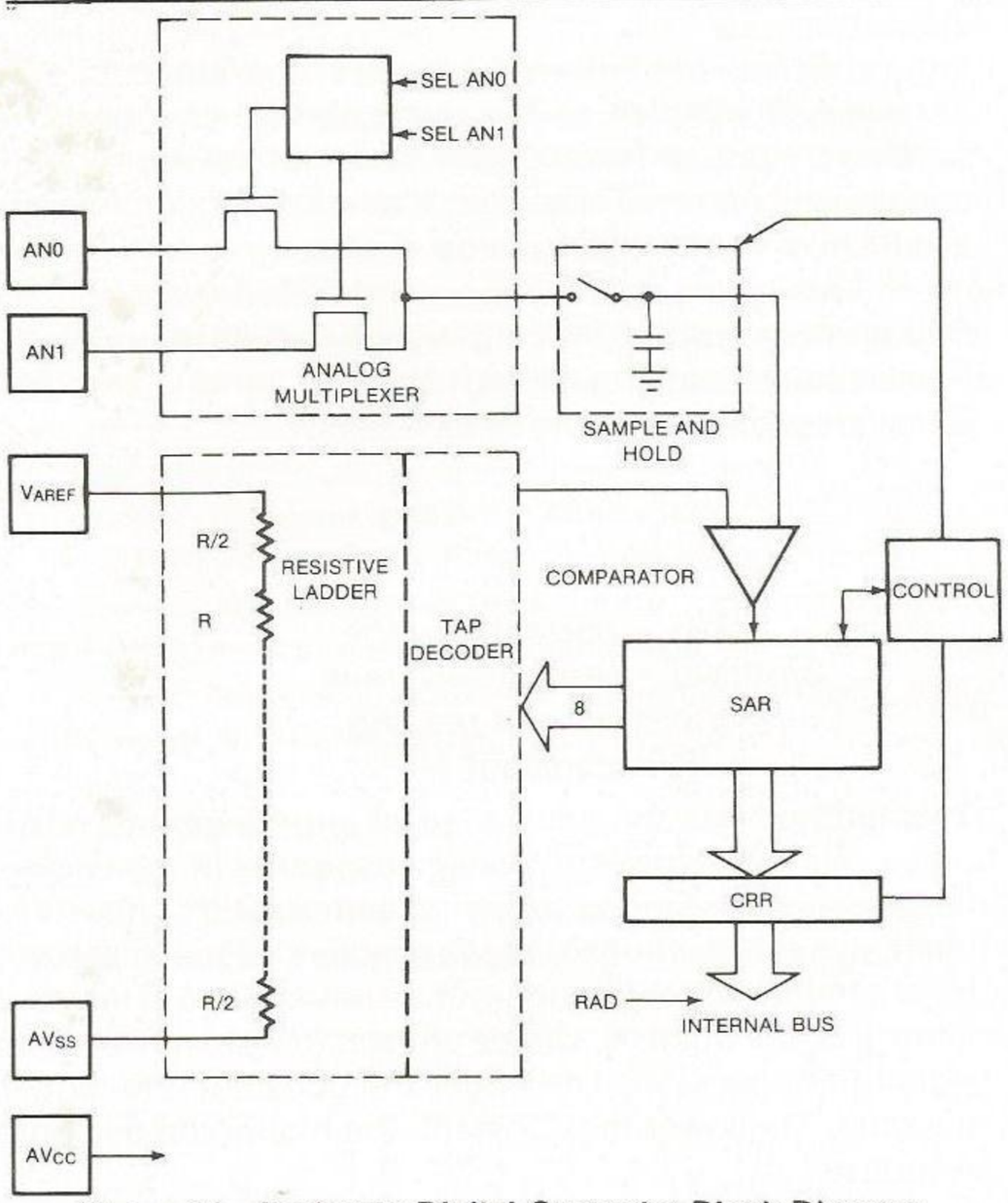


Figure 11. Analog to Digital Converter Block Diagram

comparisons are performed automatically by the on-chip A/D hardware. At the end of eight comparisons the SAR contains a valid digital representation of the analog voltage. This result is then latched into the conversion result registor (CRR). The RAD instruction can then load the conversion result from the CRR to the accumulator.

To insure maximum accuracy from the A/D converter, separate power supply pins (Avcc and Avss) and a substrate pin (SUBST) have been provided. Unless there is excessive noise on the digital power supply, both Vcc and Avcc can be tied together and still maintain maximum accuracy. Figure 12 shows a typical analog configuration for sensing temperature in two thermistors. The substrate has both low frequency and high frequency bypass for noise immunity. The power supply pins (Vcc, Avcc) are bypassed with a .01 microfarad capacitor close to the chip. All other analog signals are bypassed with .001 microfarad capacitors for added noise rejection. (See also Software Noise Rejection)

As figure 11 shows, VAREF is connected to the top of the resistive ladder. When the selected analog channel is equal to or greater than VAREF the conversion result will equal 255 decimal (FF hexadecimal). The VAREF voltage can be generated in a number of ways depending on the

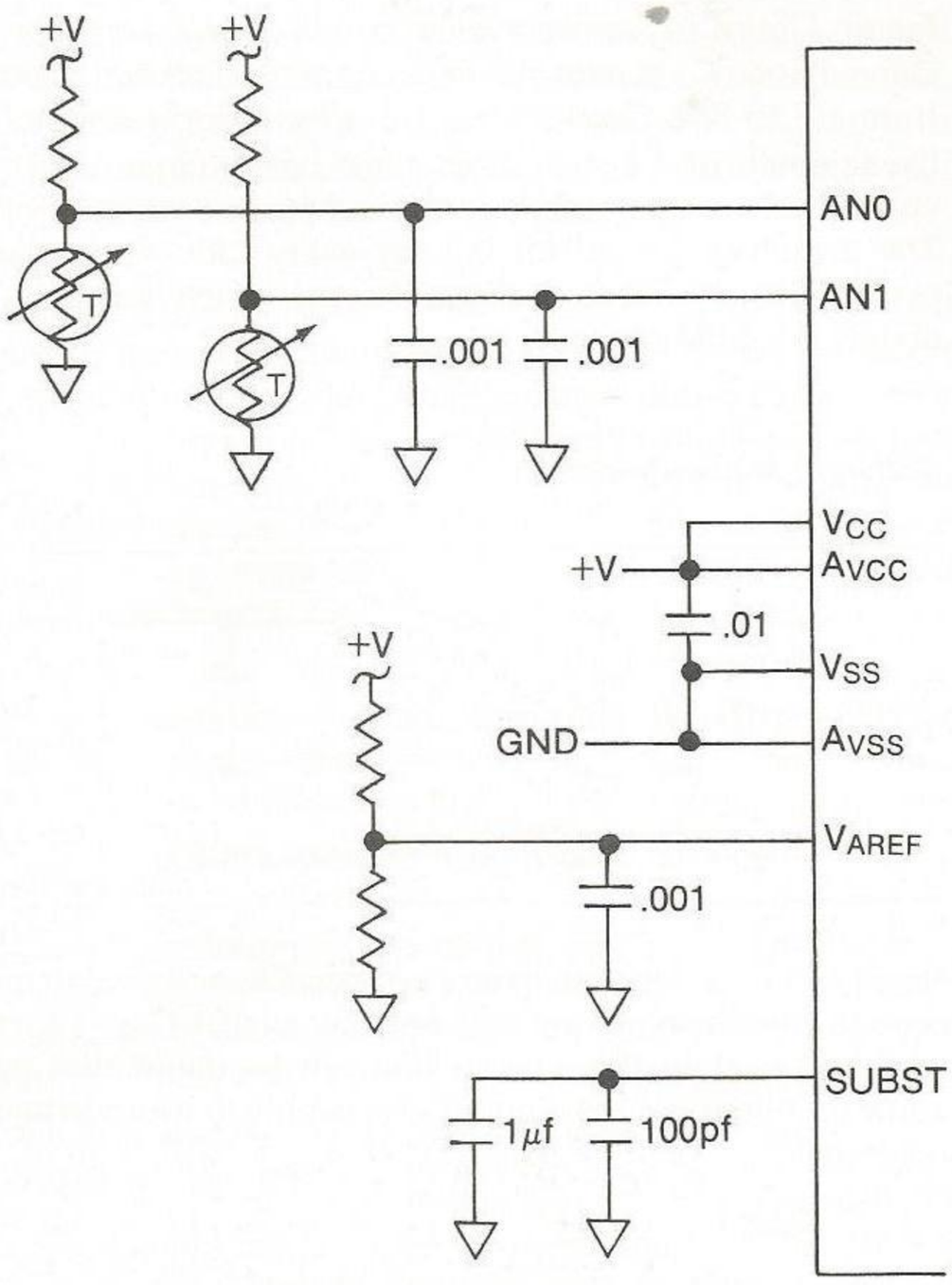


Figure 12. Typical Analog Schematic

system. It could be connected directly to Vcc giving a A/D range of GND to Vcc, or a simple resistor divider could be used to balance the reference voltage with the analog signals as in Figure 12. In calculating the impedance of the divider, the ladder impedance must be considered (see Figure 13). The total impedance of the ladder ranges from approximately 15K to 20K. This includes part to part differences and variance as a function of temperature. The resistor impedance should be chosen such that the 15K ohm parallel resistance is a small percentage of the divider impedance.

Input impedance of the converter can also be an important

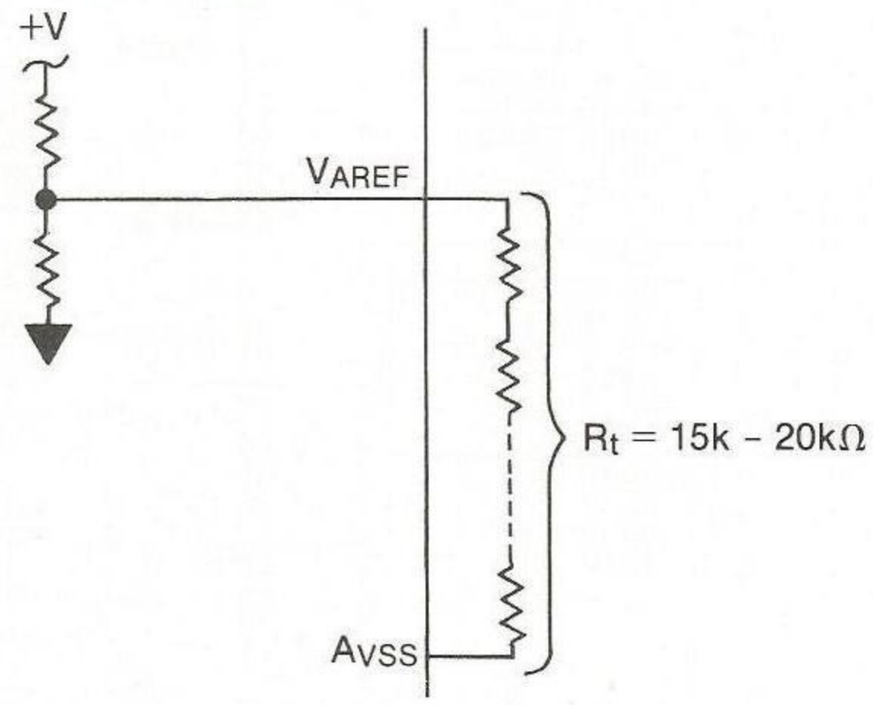


Figure 13. Ladder Impedance

factor. Figure 14 is an equivalent circuit of an analog input. Capacitance C1 is package capacitance which may range from 1pf to 3pf. Capacitance C2 is the sample and hold capacitance of 1.2pf to 1.4pf. This capacitance is only connected into the circuit by the sample and hold switch. The switch is closed for 0.3 tcy every four instruction cycles. Resistor R1 is package leakage which is approximately 2.5-5.0M ohms.

Software Noise Rejection

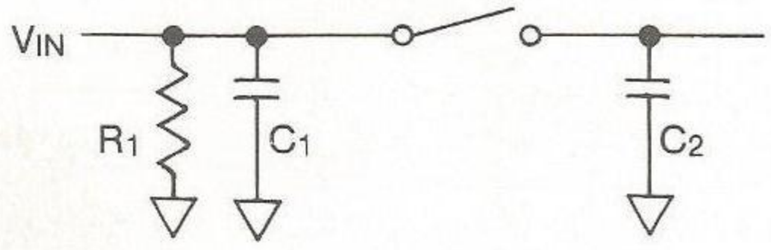


Figure 14. Analog Input Equivalent Circuit

Noise can be a problem in any system. Capacitors can be used to filter the noise but may not filter all of it. Capacitors also add cost to the system but can be eliminated by software filtering. One technique is simply to average two readings:

$$\frac{V_{IN1} + V_{IN2}}{2} = V_{OUT}$$

or keep a running average by averaging each reading with the previous average:

```
SEL AN0         ;Start conversion
MOV R0,#30      ;Point to storage location
RAD             ;Read current A/D sample
ADD A,@R0       ;Add current sample to previous average
RRC A           ;Divide by two
MOV @R0,A       ;Store new average
```

This method will eliminate small fluctuations in the input voltage and reduce the effect of large fluctuations. Often, however, noise may be more severe. Excessive noise may require averaging of many readings taken over a short period of time.

$$\frac{V_{IN1} + V_{IN2} + \ldots + V_{IN16}}{16} = V_{OUT}$$

Figure 15 lists the software required to average 16 successive A/D samples, as the above equation suggests. In such averaging, it is necessary to select the appropriate channel only once. Thereafter, a new conversion result is available every four instruction cycles.

Still another type of filtering is "exponential averaging." Similar to the running average method, current readings are averaged with the previous average.

$$\frac{V_{IN} - Voldavg}{K} + Voldavg = Vavg$$

Where Vavg = current average
Voldavg = previous average
Vin = current reading
K = constant

This method has the advantage of large signal to noise ratios, but has slower dynamic response. In many systems, especially those involving temperature measurement, dynamic response is not a problem. Signal noise will be of a much higher frequency than any change in temperature. The constant, K, can be chosen to yield any desired signal to noise ratio. The larger the constant, the higher the ratio. The lower the constant, the higher the dynamic response.

To increase the effectiveness in reducing line generated noise, any of the above methods should be synchronized to the line frequency. As previously discussed, an interrupt can be generated when the 50Hz or 60Hz line frequency crosses AC zero. The A/D filtering routine should be part of the interrupt routine. Reading of the A/D will then occur at the same point of each line cycle, thus ignoring any line generated fluctuations in the analog inputs.

```
LOC  OBJ          LINE        SOURCE STATEMENT

                    47 ;
                    48 ;        AVERAGE 16 A/D READINGS
                    49 ;        ======================
                    50 ;
                    51 AVG16:
002C BC00           52          MOV     R4,#00  ;CLEAR TEMP. MSB RESULT REGISTER
002E B81A           53          MOV     R0,#26  ;SET UP POINTER
0030 B000           54          MOV     @R0,#00 ;CLEAR RESULT REGISTER
0032 85             55          SEL     AN0     ;SELECT AND START CONVERSION
0033 BA10           56          MOV     R2,#16  ;16 READINGS
                    57 LOOP:
0035 80             58          RAD             ;READ RESULT
0036 60             59          ADD     A,@R0   ;LSB
0037 A0             60          MOV     @R0,A   ;SAVE NEW LSB
0038 27             61          CLR     A
0039 7C             62          ADDC    A,R4    ;ADD CARRY TO MSB
003A AC             63          MOV     R4,A    ;SAVE NEW MSB
003B EA35           64          DJNZ    R2,LOOP ;NEXT READING
003D 47             65          SWAP    A       ;MSB INTO MSN
003E 20             66          XCH     A,@R0
003F 47             67          SWAP    A       ;DIVIDE BY 16
0040 30             68          XCHD    A,@R0   ;LOCATION 26 NOW CONTAINS
                    69                          ;THE AVERAGE
                    70
                    71
                    72
```

Figure 15.

Port 0 Comparator Inputs

Intel, in its commitment to add analog features to microcomputers, did not stop with A/D conversion and zero cross detection. Also added to the 8022 were eight comparators for easing the interface to non-digital inputs.

Port 0 has been modified from the standard quasi-bidirectional structure to allow an optional open drain configuration with comparator inputs. The low impedance pullup device has been eliminated and the high impedance pullup is optional. Thus, the user can choose via a mask programmable selection each line of Port 0 to be either quasi-bidirectional with a high impedance or true open-drain. The open drain configuration allows the line to sink current through the low impedance pulldown device or to float in the high output state. More importantly, the open drain configuration makes Port 0 very easy to drive when it is used as inputs. The input circuitry for each line of Port 0 includes a voltage comparator which amplifies the voltage difference between the input port line and the Port 0 threshold reference pin (V_{TH}). The voltage gain of the comparator is sufficient to sense a 100mV input differential within the range Vss to Vcc/2.

If V_{TH} is allowed to float, it will bias itself to the digital switch point of the other ports, and Port 0 behaves as a set of normal digital inputs. However, by biasing V_{TH}, the switch point can be both tightly controlled and adjusted. Common uses for this would include unusual logic level inputs as from a diode isolated keyboard, analog channel expansion, and direct capacitive touchpanel interface. The comparator action is automatic and the port is read just as any other port.

A typical use for Port 0 is in the interfacing with capacitive touch panels on microwave ovens and other new appliances. A touch-panel switch consists of two capacitors in series. One lead is attached to a high voltage buffer (10 to 30 volts). The other is attached to the Port 0 sense input. As a finger touches the common point, the drive signal is shunted by body capacitance, attenuating the signal reaching the input.

Low-voltage touch-panel operation (less than 30V) is possible, since the comparators allow small voltage changes to be detected. Most of the present touch-panel designs require a 50–100V drive on the touch panel.

Capacitive touch panels can be multiplexed in the same manner as mechanical keyboards (Fig. 16). The vacuum flourescent display and the touch panel drivers are integrated to optimize hardware through shared high voltage buffers.

Figure 17 lists the software necessary to refresh the display and scan the touch-panel matrix. This routine could be adapted to serve as part of a timer/interrupt

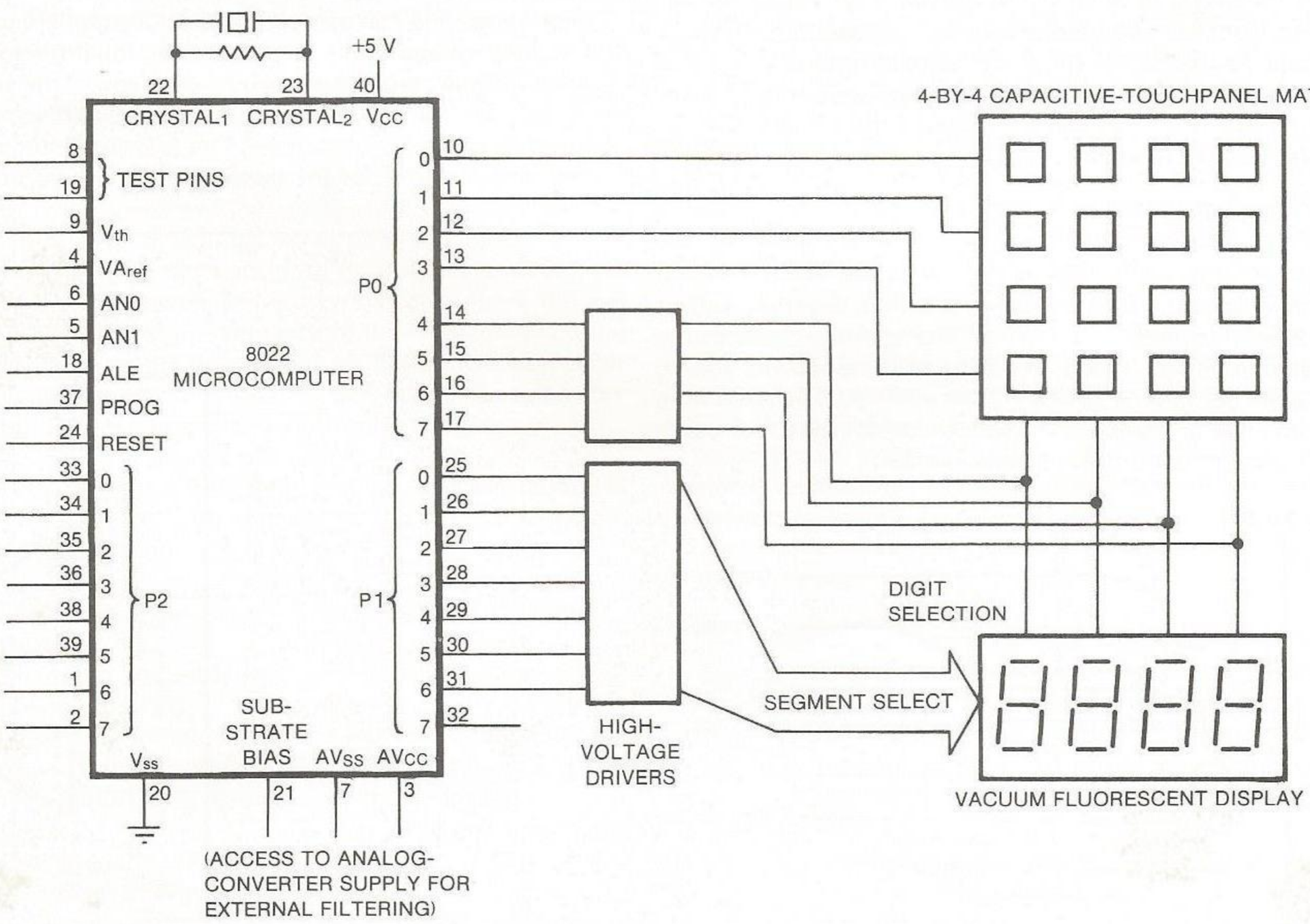


Figure 16. Typical Keyboard/Display Schematic

```
LOC  OBJ          LINE        SOURCE STATEMENT

                    74 ;
                    75 ;        KEYBOARD DISPLAY ROUTINE
                    76 ;        ========================
                    77 ;
003C                78 D4       EQU     3CH     ;MSD OF DISPLAY
                    79 KEYDIS:
0041 27             80          CLR     A
0042 39             81          OUTL    P1,A    ;TURN OFF SEGMENT DRIVERS
0043 90             82          OUTL    P0,A    ;TURN OFF DIGIT DRIVERS AND
                    83                          ;PANEL STROBES
                    84                          ;INITIALIZE SENSE INPUTS TO GND
0044 230F           85          MOV     A,#0FH
0046 90             86          OUTL    P0,A    ;FLOAT SENSE INPUTS
0047 4B             87          ORL     A,R3    ;NEW STROBE POSITION
0048 90             88          OUTL    P0,A    ;TURN ON STROBE
0049 08             89          IN      A,P0    ;READ SENSE INPUTS
004A AC             90          MOV     R4,A    ;SAVE SENSE INPUTS
004B B83B           91          MOV     R0,#D4-1        ;RAM LOCATION OF MSB OF 7-SEG PATTERN
004D FB             92          MOV     A,R3    ;STROBE POSITION INTO A
004E 90             93          OUTL    P0,A    ;GND SENSE INPUTS
                    94 LOOP1:
004F F7             95          RLC     A       ;ROTATE DIGIT STROBE INTO CARRY
0050 18             96          INC     R0      ;NEXT DIGIT LOCATION
0051 E64F           97          JNC     LOOP1   ;LOOP UNTIL CARRY
0053 F0             98          MOV     A,@R0   ;RETRIEVE PATTERN FROM RAM
0054 39             99          OUTL    P1,A    ;OUTPUT NEW PATTERN
                   100
                   101
```

Figure 17.

scheme that would generate an interrupt at precise intervals for a flicker-free display. Another portion of the software would check for any touched input pads, test for valid entry, and enter key-depression codes into the main program.

Correcting Pad Imbalance

A common problem with capacitive touch panels is their imbalance. Layout, process, aging, and surface impurities all cause the capacitance to vary from touch pad to touch pad, resulting in a family of curves (Fig. 18) of voltage levels from each column of touch pads reaching the sense inputs. As the curves show, if threshold voltage Vth1 alone were used, one column would always appear touched; if Vth2 were used exclusively three of the columns would never appear touched.

To compensate for such varying capacitance levels, the on-chip analog input circuit may be used to allow multiple input voltage levels. Figure 19 depicts the 8022 version of such a circuit. AN0 and V_{TH}, are tied together with a capacitor to line 0 of Port 0. The pull-up resistor and capacitor are used on line 0 to provide an RC timing network connected to ANO, VTH, and P00. The remaining seven lines of Port 0 are the sense lines for the touch panel and use the open drain output option.

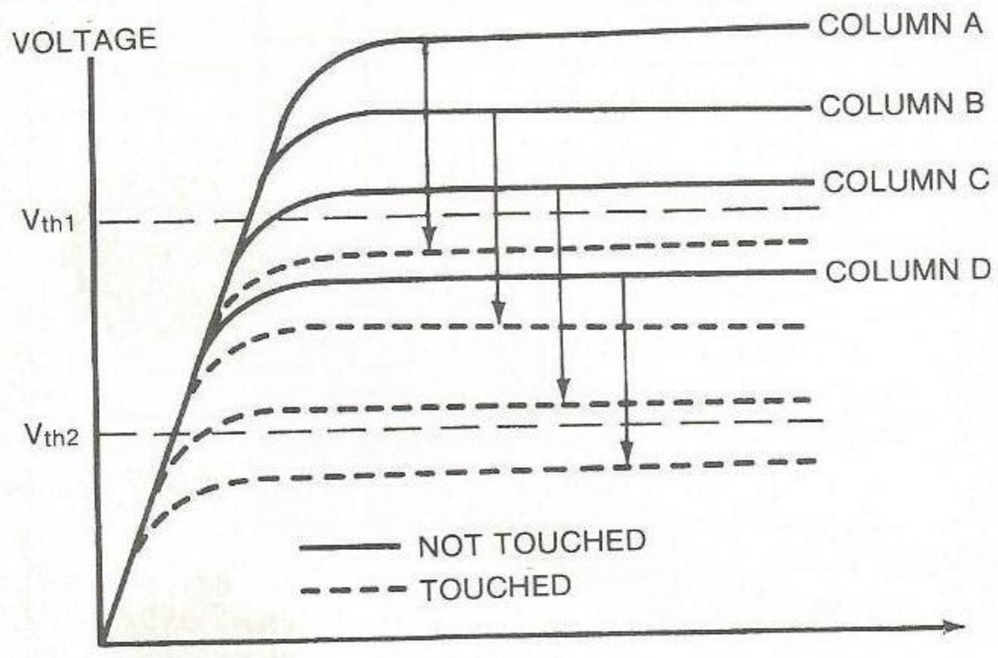


Figure 18.

Handling the different voltage levels would begin with initializing the data by plotting the family of curves with the AN0 input. This is done by writing a 0 to P00 (grounding P00) which initializes V_{TH} to 0v. A logic 1 is then written to P00, which begins to pull the RC network toward 5 v. As V_{TH} ramps upward, the sense lines are monitored for input changes, which will go from 1 to 0 as the not-touched voltage curve for each input is intersected. As the changes occur, the A/D value for each input is intersected. As the changes occur, the A/D value for each sense line can be read and stored. Thus the threshold reference voltage for each sense line can be determined by establishing the not touched voltage levels and by placing the threshold reference voltage below this level. As each row of the keyboard is scanned, the RC network is initialized to 0 v and ramps upward, varying the V_{TH} level. The A/D converter monitors this level looking for the calculated threshold points. As

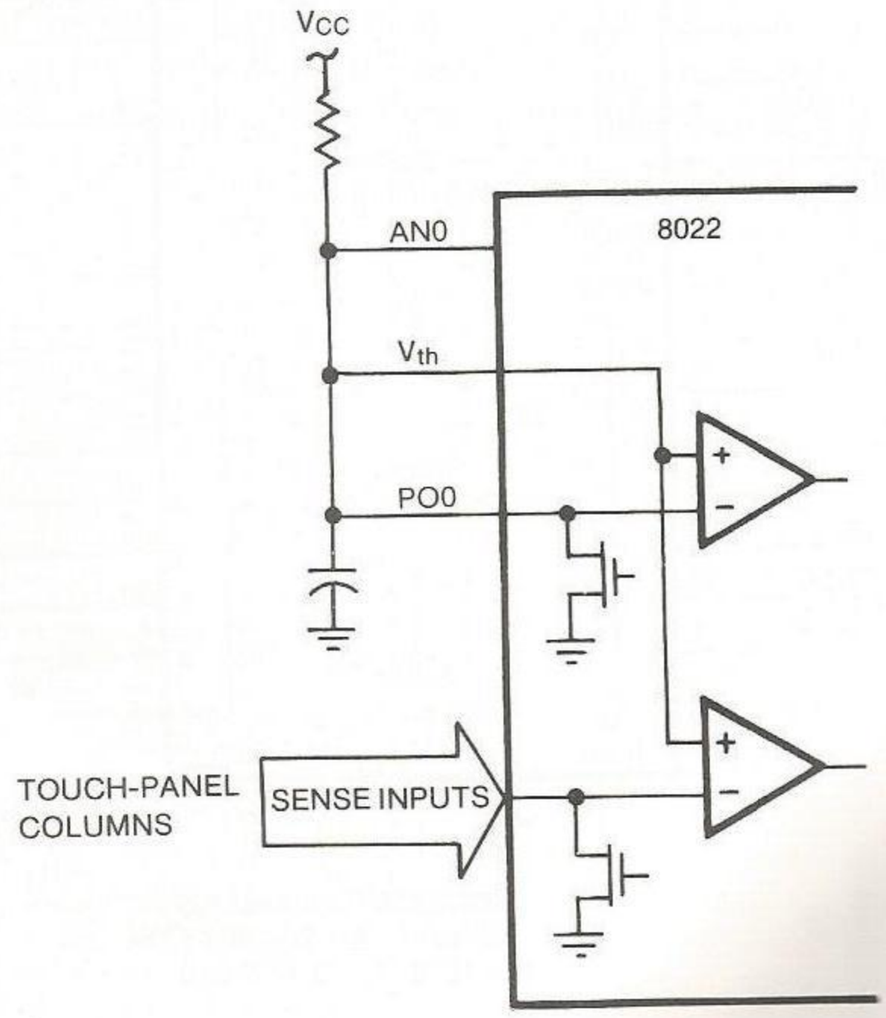


Figure 19.

the points are intersected, the corresponding sense inputs are read, with a 0 indicating a touched input and a 1 indicating a not-touched input. Thus, a multiplexed capacitive touch panel can be scanned and balanced without adding external components to the inputs.

For systems requiring more than two analog inputs to the 8022, Port 0 comparator inputs may be reconfigured to permit formation of pseudo-analog inputs from variable threshold digital inputs. The hardware configuration can be identical to that of Fig. 19. In this scheme, sense inputs act as additional analog inputs of less accuracy than AN0 and AN1 (about 6 bits).

The sequence for implementing the extension is essentially the same found in the variable-threshold touch panel. As V_{TH} ramps upward, a Port 0 bit is monitored for a change from 1 to 0. At the change, AN0 is read corresponding to the value of the analog input into Port 0 (with some error due to the time lag, which can be subtracted). This configuration can be utilized when it is possible to trade off accuracy for such cost improvements: one analog input with 8-bit accuracy and seven analog inputs with 6-bit accuracy. Such may be the case in a range controller that monitors temperature in two ovens, a meat probe, and two of the four burners, all to an accuracy within 10° F.

Application Ideas

This section will discuss some possible applications of the 8022. These applications are discussed in general terms and are believed to be feasible applications of the 8022. None of these applications, however, have been built and checked out.

Power Supply Controller

The three terminal voltage regulator, with its built-in current limiting and overload protection, has vastly simplified the task of designing small power supplies. Power supplies for large systems, with requirements for brown out protection, power fail warnings, etc., have not yet yielded to the design simplicity of the integrated voltage regulator. The combination of an 8022 microcomputer and these same regulators, however, may make it feasible to simplify these larger power supply systems.

There are several requirements of larger power supplies which have to be met outside of the regulation itself. Typical of these are:

1. Sequencing the turn on and shut down of several supplies.
2. Providing an early warning to the system that power is failing.
3. The ability to hold the system in a reset state during power supply sequencing.
4. Generation of a line frequency clock to the system.
5. Provisions for remote start up and shut down.
6. Sufficient energy storage to keep the system running long enough to provide an orderly shut down.
7. High efficiencies to minimize power requirements and heat dissipation.

These requirements can be met by a combination of raw DC supply, multiple three-terminal regulators, and an 8022 microcomputer. Figure 20 shows a raw supply which is capable of generating DC voltages suitable for regulation to five, plus twelve, and minus twelve voltages. (These are arbitrary, but common voltages). In addition, a separate winding is provided which generates a five-volt supply which will be used to supply power to the 8022 itself. The normal rectifiers in the RAW5 and RAW12 supplies are replaced by silicon controlled rectifiers which will be phase angle controlled by the 8022.

Figure 21 shows the connections to the 8022. The RAW5 and RAW12 supplies are applied to simple voltage dividers which feed the analog inputs of the 8022. The signal

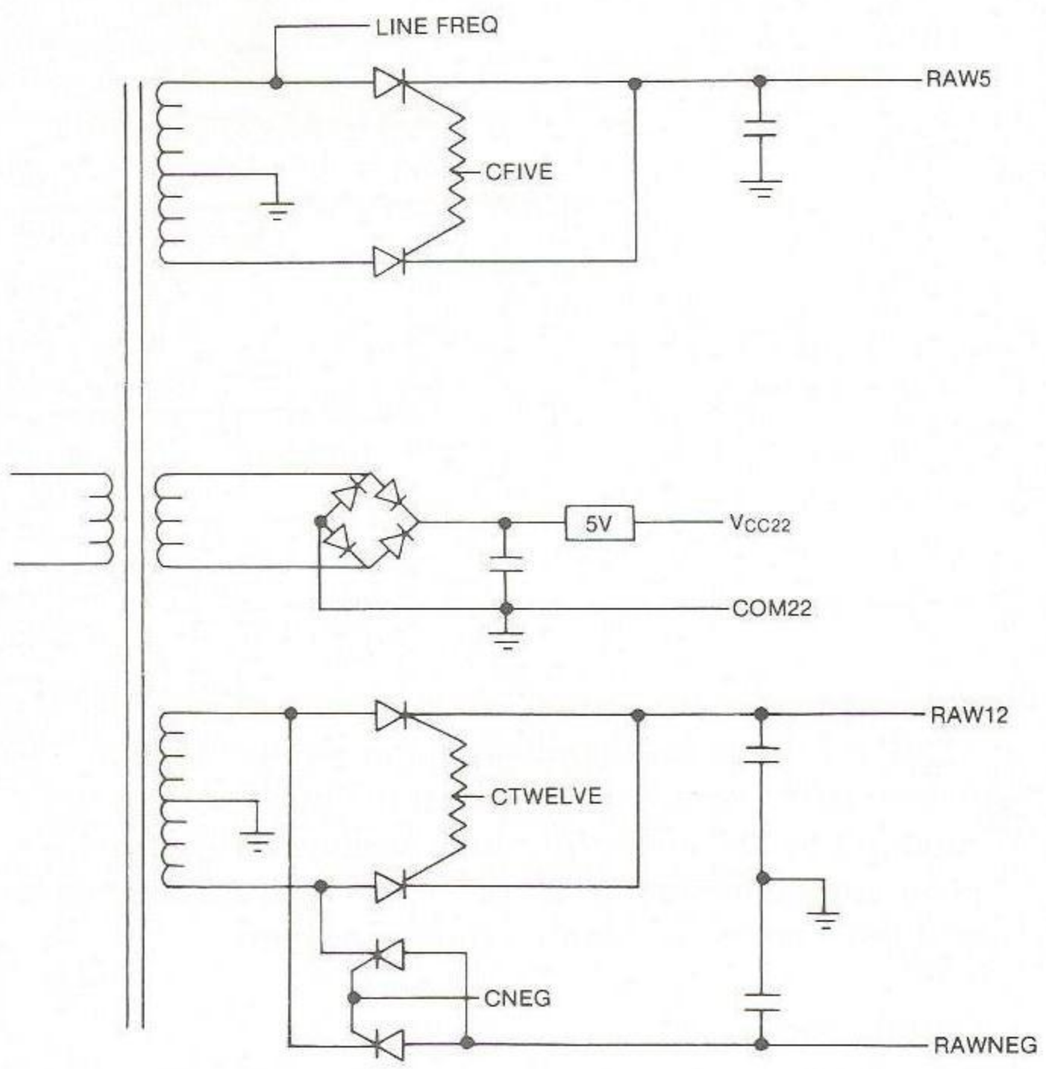


Figure 20.

LINEFREQ is taken from a convenient winding of a transformer, divided down, and applied to the zero cross input of the 8022. A strap is provided to configure the unit for 50/60 Hz operation. In addition to being connected to the basic power supply, the 8022 is also connected to the system receiving the power. The on/off switch becomes an input to the 8022. The 8022 provides outputs for a 10Hz interrupt, a power fail interrupt, cold/warm indicator and system reset.

The 8022 can perform many of the functions normally done by hardware sequencers in the power supply. On power-up, it can hold off the three main supplies until the main supply is firmly established. This prevents the system from responding to short power restorations which frequently occur during power outages. Having determined that it is safe to power up the system, the 8022 can assert the reset signal and the cold start signal. The cold start indication tells the system that power was interrupted at the mains rather than by the OFF switch—a useful function if any amount of battery backed up RAM exists in the system. Having set up these signals, the 8022 waits for

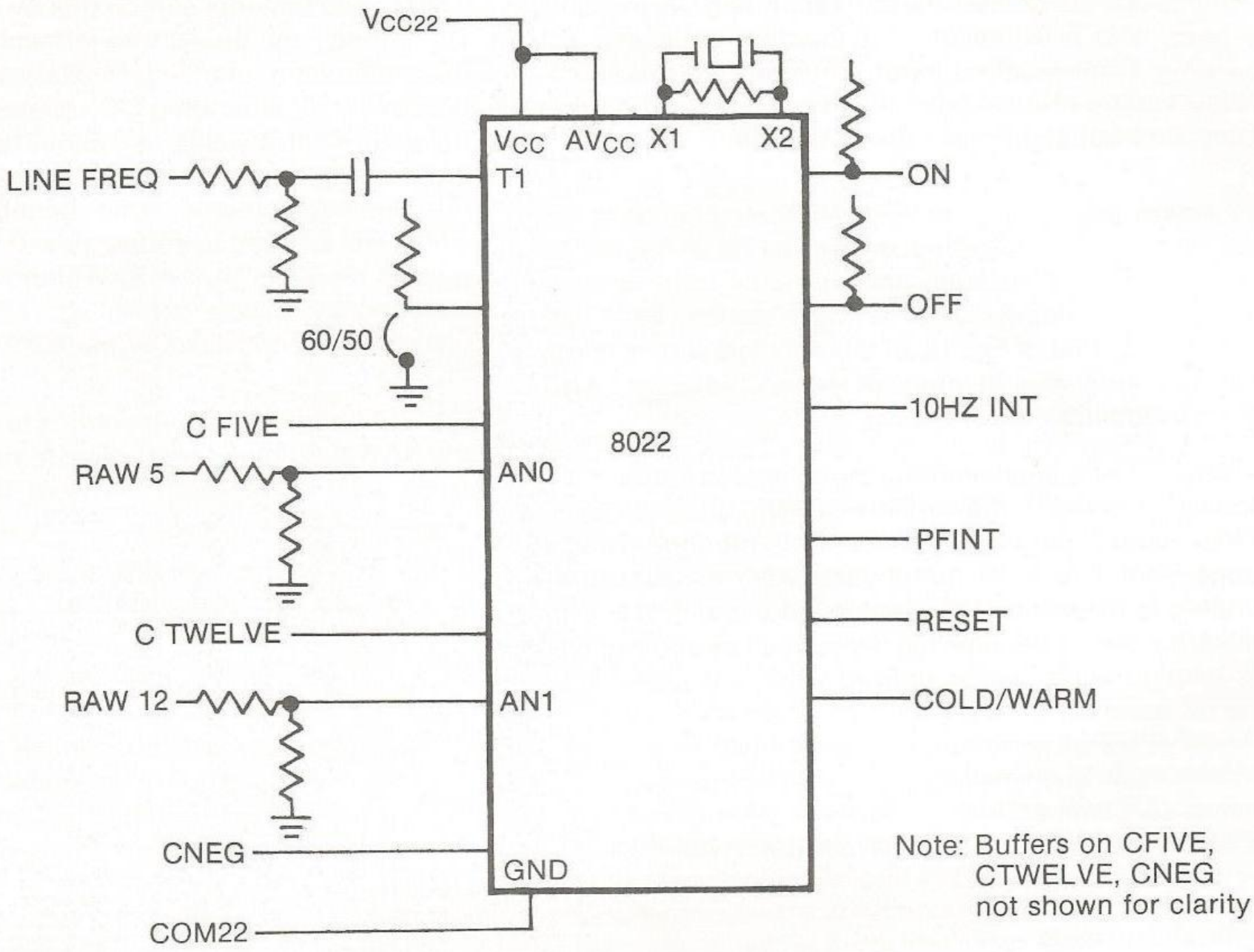


Figure 21.

a zero crossing (to minimize inrush) and then turns on the SCRs for the three supplies one at a time (again to minimize inrush). Any sequencing of the three supplies that is required by the system can also be allowed for. After some programmable time delay, the reset signal can be released and the system allowed to start operation.

During normal operation the 8022 can monitor the two major raw supplies and use phase angle control of the SCRs to regulate them. The regulation would be used to ensure that the three terminal regulators had minimum input voltage requirements met under all line voltage variations while at the same time minimizing the voltage drop across them. This increases the efficiency of the power supply and allows it to be capable of handling brown outs without dissipating excessive power in the regulators.

The line frequency input is used not only for the basis for the phase angle control, but also for two other functions; power fail detect and generation of the 10 Hz interrupt. The 10Hz interrupt can be generated by simply dividing the power line frequency by 5 for 50 Hz and 6 for 60 Hz operation. Performing this division in the power supply itself allows the system to be run on 50 or 60 cycle power with no change external to the power supply. In some situations it should even be possible to have the power supply adapt to either of these inputs by measuring the period of the incoming power on startup (see section "Which One?"). This would be an easy function to incorporate in the software and would require no additional hardware since provision is already made for zero cross detect.

Power fail detection can be done by running the timer while waiting for the line to zero cross. If an excessive time elapses it can be assumed that the power has failed and the power fail interrupt asserted. Note that this will detect total power failure but not a dip in the line voltage below the specifications of the power supply. This condition can be detected by keeping track of the phase angle that is required to maintain the RAW supplies at the proper level. If the SCR's have to be turned on for too high a portion of the total line cycle it is an indication of a brown-out condition and the powerfail interrupt should be generated. Whenever the powerfail interrupt is generated the 8022 should turn on the SCRs continuously to ensure maximum possible energy storage in the filter capacitors. After generation of the powerfail interrupt, the 8022 can again delay (depending, of course, on the energy storage of the power supply) and then assert reset. Once reset is asserted the SCRs are turned off, and left off, until the supplies have dropped down to a point which guarantees that any reset circuitry residing outside of the power supply will see a full power transition when power is reapplied. If the power is shut down by the 8022 in response to the on/off switch, the sequence would be similar except that the cold/warm start signal would indicate a warm start.

The above discussion should make it clear that the 8022 would make the task of designing a power supply system far easier, particularly for those designers more familiar with digital than analog design. If, in addition, the 8022 supply were put on a battery back-up, it would be possible to add many features to the system at virtually zero cost. The 8022 could be programmed to become the system clock and send, perhaps in serial ASCII, the time of day

and the date to the main system on demand or periodically. This function would require that a crystal be used as a timing reference to the 8022 so that the power supply could still track real time even if the incoming power fails. Other possibilities would have the system shut down unless some external event required its attention, or the incorporation of system diagnostic checks within the code of the 8022. The comparator inputs on PORT 0 of the 8022 would even allow some capability of parametric testing as part of these diagnostics. The possibilities bring a new dimension to the term "Programmable Power Supply".

DC Motor Control

Figure 22 shows the 8022 used to control the speed of a permanent magnet DC motor. A seven segment display and keyboard are provided which allow the user to enter the parameters required by the control algorithm. The display is also used to display the speed of the motor during operation. Other data (for example root mean squared error) could also be displayed upon demand. The motor is driven by a constant frequency pulse width modulated signal which is generated programatically. Port 11 (which is one of the two high current outputs) is used to drive a photoisolator which provides level shifting as well as isolation. The circuit shown allows both the speed and torque of the motor to be measured for use by the control algorithm. The torque generated by a PM DC motor is proportional to the armature current. This current, and hence the torque, can be measured by reading the voltage drop across the shunt resistor. The voltage generated across the motor is the sum of the IR drop in the armature and a term which is proportional to the angular speed of the motor. The armature current is already known from the torque measurement, so the speed can easily be determined from the two analog measurements shown. The DC resistance of the armature, the speed constant, and torque constant would, of course, have to be known or entered by the operator.

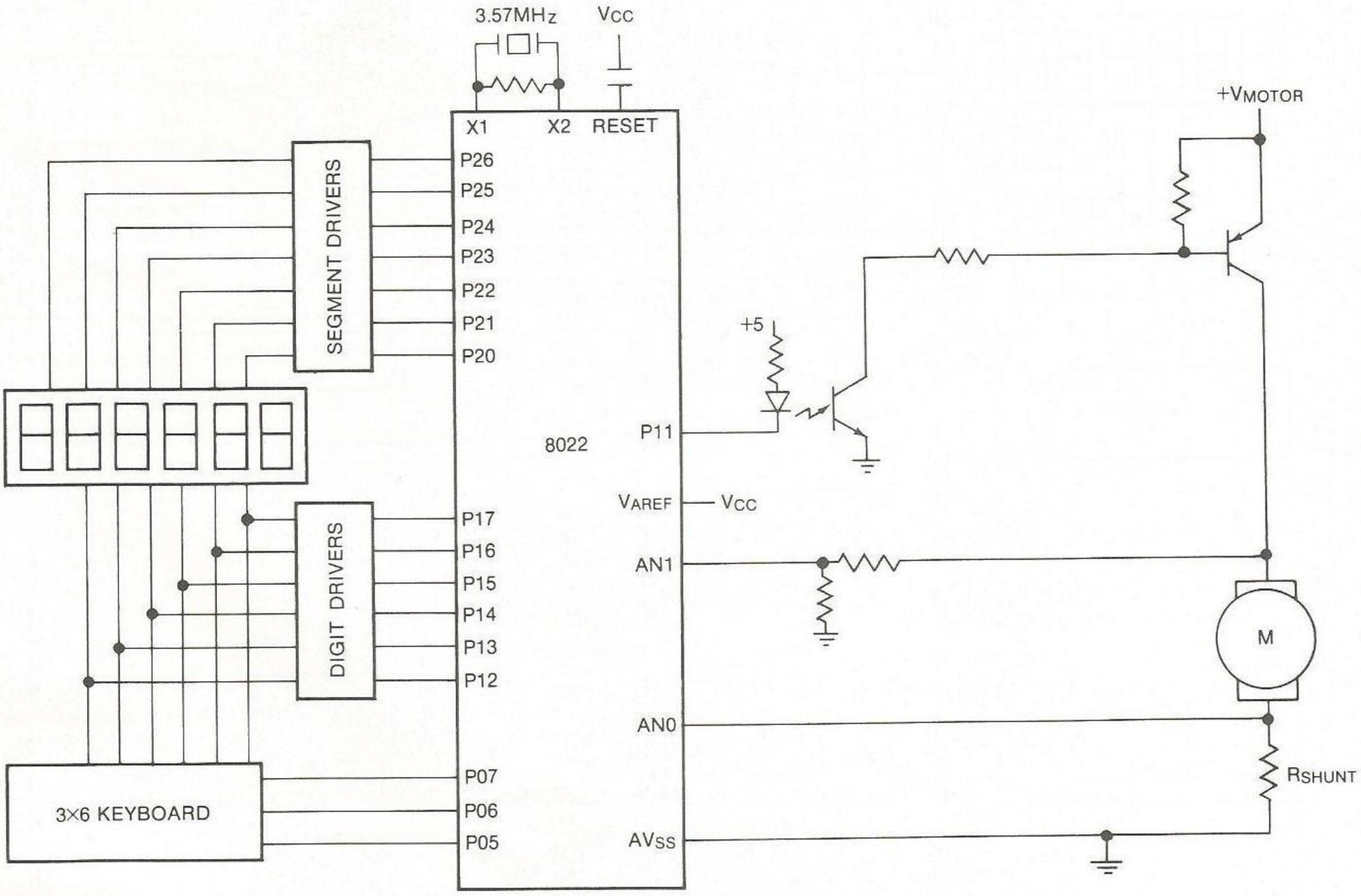


Figure 22. DC Motor Control

Automotive Dashboard

Figure 23 shows an automotive dashboard controlled by the 8022. Provisions are made to measure the oil pressure, water temperature, and vehicle speed. A connection to the distributor points allows the engine RPM and point dwell to be measured. Outputs are provided to control the ignition and starter (allowing the ignition switch to be eliminated in favor of a combination lock). Drive to a vacuum servo is also possible to allow cruise control to be cheaply implemented. The display can be used for a speedometer, tachometer, oil pressure guage, or water temperature guage depending on the current desire of the driver. There are several uncommitted I/O pins which could be used to implement functions such as intermittent action windshield wipers or delayed action light circuits.

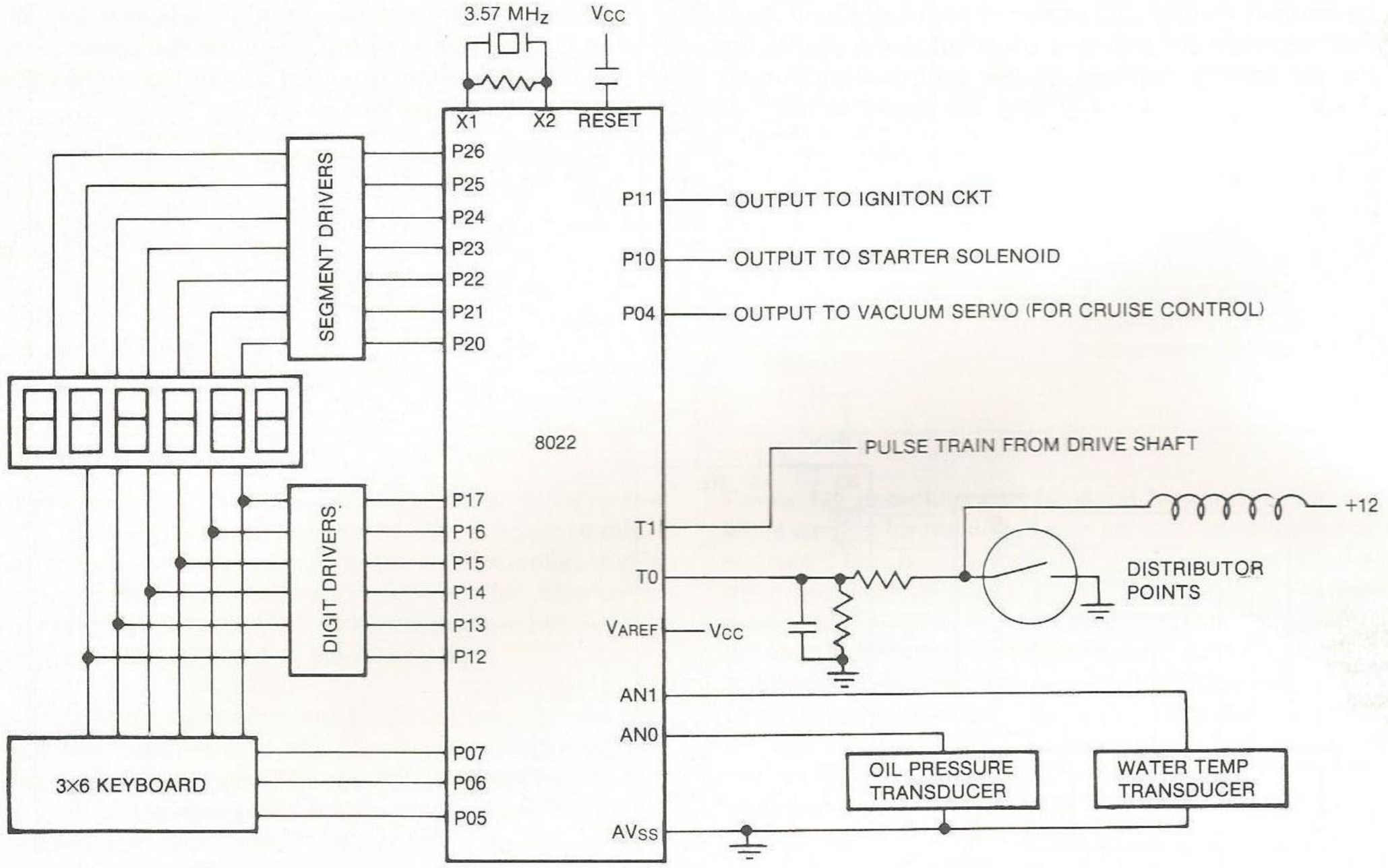


Figure 23. Automotive Dashboard

Darkroom Timer

A darkroom timer based on the 8022 is shown in Figure 24. In addition to the keyboard and display this diagram incorporates drive to two TRIACs, an input to monitor the line frequency crossings, and two analog measurements. The analog inputs are used to monitor and display the temperature of the chemical bath and the light output of the enlarger, both of which can be controlled by the microcomputer. The 8022 could be used to run several timers concurrently while also maintaining the temperature of the chemical bath at the required level. Several uncommited I/O pins are available for additional functions.

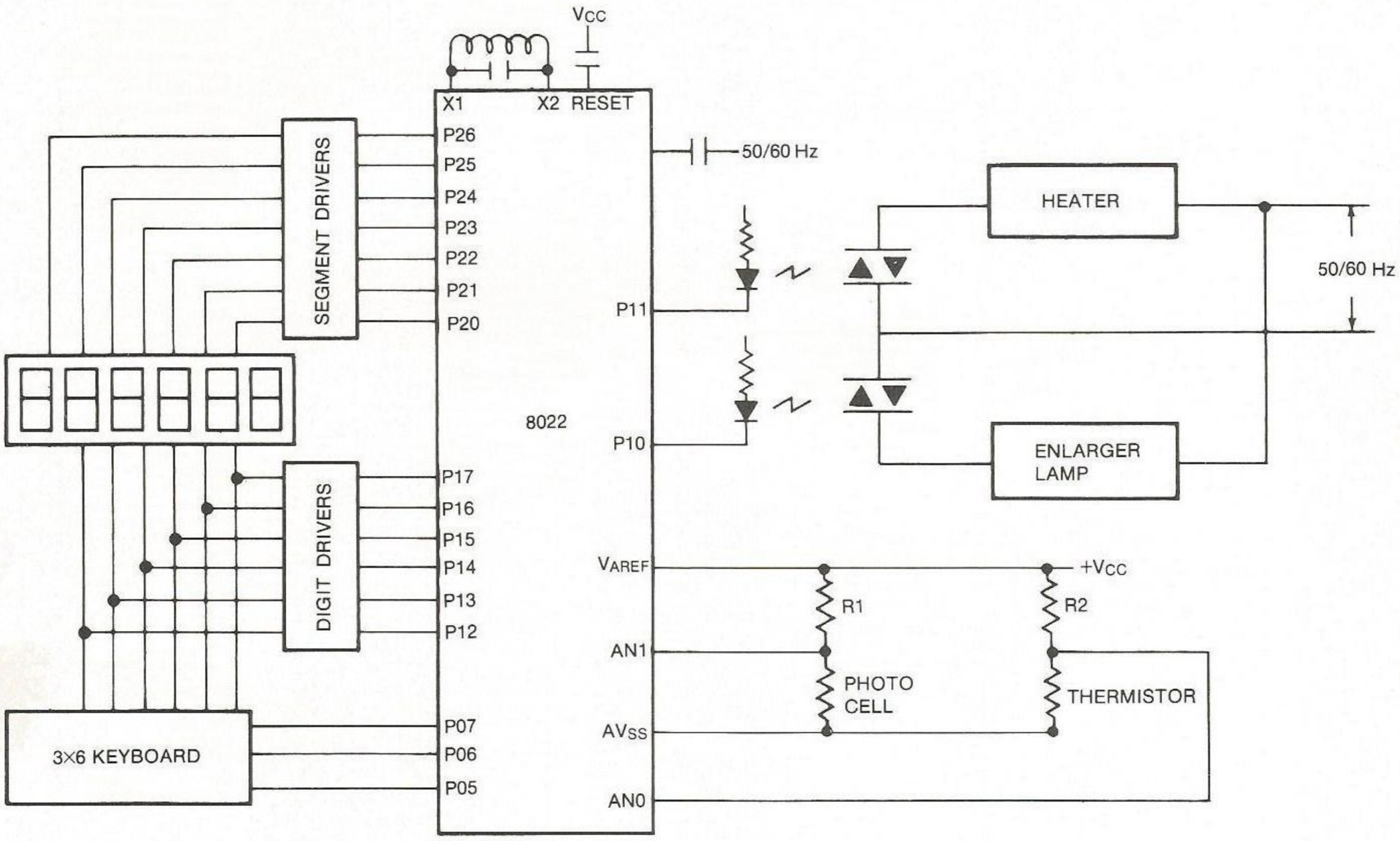


Figure 24. Darkroom Timer/Control

Conclusions

This application note has introduced the reader to the Intel 8022 microcomputer. It has described the main features of the 8022 and discussed some of the design considerations encountered in designing with the 8022.

The reader has also been exposed to several possible applications which show the versatility and cost effectiveness of a microcomputer with on-board analog features.

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8245 Nieman Road, Suite #100
Lenexa 66214
Tel: (913) 888-0212, 3, & 4
TWX: 910-749-6412

KENTUCKY
†Lowry & Associates, Inc.
3351 Commodore
Lexington 40502
Tel: (606) 269-6329

MARYLAND
Intel Corp.*
7257 Parkway Drive
Hanover 21076
Tel: (301) 796-7500
TWX: 710-862-1944

Glen White Associates
57 W. Timonium Road, Suite 307
Timonium 21093
Tel: (301) 252-6360

†Mesa Inc.
11900 Parklawn Drive
Rockville 20852
Tel: Wash. (301) 881-8430
Balto. (301) 792-0021

MASSACHUSETTS
Intel Corp.*
187 Billerica Road, Suite 14A
Chelmsford 01824
Tel: (617) 667-8126
TWX: 710-343-6333

†Computer Marketing, Inc.
257 Crescent Street
Waltham 02154
Tel: (617) 894-7000

MICHIGAN
Intel Corp.
26500 Northwestern Hwy.
Suite 401
Southfield 48075
Tel: (313) 353-0920
TWX: 910-420-1212
TELEX: 2 31143

†Lowry & Associates, Inc.
135 W. North Street
Suite 4
Brighton 48116
Tel: (313) 227-7067

MINNESOTA
Intel Corp.
8200 Normandale Avenue
Suite 422
Bloomington 55437
Tel: (612) 835-6722
TWX: 910-576-2867

†Dytek North
1821 University Ave.
Room 163N
St. Paul 55104
Tel: (612) 645-5816

MISSOURI
Technical Representatives, Inc.
320 Brookes Drive, Suite 104
Hazelwood 63042
Tel: (314) 731-5200
TWX: 910-762-0618

NEW JERSEY
Intel Corp.
1 Metroplaza Office Bldg.
505 Thornall St.
Edison 08817
Tel: (201) 494-5040
TWX: 710-480-6238

NEW MEXICO
BFA Corporation
P.O. Box 1237
Las Cruces 88001
Tel: (505) 523-0601
TWX: 910-983-0543

BFA Corporation
3705 Westerfield, N.E.
Albuquerque 87111
Tel: (505) 292-1212
TWX: 910-989-1157

NEW YORK
Intel Corp.*
350 Vanderbilt Motor Pkwy.
Suite 402
Hauppauge 11787
Tel: (516) 231-3300
TWX: 510-227-6236

Intel Corp.
80 Washington St.
Poughkeepsie 12601
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TWX: 510-248-0060

Intel Corp.
474 Thurston Road
Rochester 14619
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Syracuse 13206
Tel: (315) 463-8592
TWX: 710-541-0554

†T-Squared
2 E. Main
Victor 14564
Tel: (716) 924-9101
TELEX: 97-8289

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Highpoint 27260
Tel: (919) 883-9125

Glen White Associates
4021 Barrett Dr.
Suite 12
Raleigh 27609
Tel: (919) 787-7016

OHIO
Intel Corp.*
8312 North Main Street
Dayton 45415
Tel: (513) 890-5350
TWX: 810-450-2528

Intel Corp.*
Chagrin-Brainard Bldg. #201
28001 Chagrin Blvd.
Cleveland 44122
Tel: (216) 464-2736

Lowry & Associates, Inc.
24200 Chagrin Blvd.
Suite 320
Cleveland 44122
Tel: (216) 464-8113

†Lowry & Associates, Inc.
1524 Marsetta Drive
Dayton 45432
Tel: (513) 429-9040

†Lowry & Associates, Inc.
1050 Freeway Dr., N.
Suite 209
Columbus 43229
Tel: (614) 436-2051

OREGON
ES/Chase Company
4095 SW 144th St.
Beaverton 97005
Tel: (503) 641-4111

PENNSYLVANIA
Intel Corp.*
275 Commerce Dr.
200 Office Center
Suite 212
Fort Washington 19034
Tel: (215) 542-9444
TWX: 510-661-2077

†Lowry & Associates, Inc.
Seven Parkway Center
Suite 455
Pittsburgh 15520
Tel: (412) 922-5110

†Q.E.D. Electronics
300 N. York Road
Hatboro 19040
Tel: (215) 674-9600

TENNESSEE
Glen White Associates
Rt. #12, Norwood S/D
Jonesboro 37659
Tel: (615) 477-8850

Glen White Associates
2523 Howard Road
Germantown 38138
Tel: (901) 754-0483

Glen White Associates
6446 Ridge Lake Road
Hixon 37343
Tel: (615) 842-7799

TEXAS
Intel Corp.*
2925 L.B.J. Freeway
Suite 175
Dallas 75234
Tel: (214) 241-9521
TWX: 910-860-5487

Intel Corp.*
6776 S.W. Freeway
Suite 550
Houston 77074
Tel: (713) 784-3400

Mycrosystems Marketing Inc.
13777 N. Central Expressway
Suite 405
Dallas 75243
Tel: (214) 238-7157
TWX: 910-867-4763

Mycrosystems Marketing Inc.
6610 Harwin Avenue, Suite 125
Houston 77036
Tel: (713) 783-2900

Mycrosystems Marketing Inc.
Koger Executive Center
Suite 207
San Antonio 78228
Tel: (512) 735-5073

UTAH
†Westek
3788 Brockbank Drive
Salt Lake City 84117
Tel: (801) 278-6920

VIRGINIA
Glen White Associates
P.O. Box 1104
Lynchburg 24505
Tel: (804) 384-6920

Glen White Associates
Rt. #1, Box 322
Colonial Beach 22443
Tel: (804) 224-4871

WASHINGTON
Intel Corp.
300 120th Avenue N.E.
Bldg. 2, Suite 202
Bellevue 98005
Tel: (206) 453-8086

E.S./Chase Co.
P.O. Box 80903
Seattle 98198
Tel: (206) 762-4824
TWX: 910-444-2298

WISCONSIN
Intel Corp.
4369 S. Howell Ave.
Milwaukee 53207
Tel: (414) 747-0789

CANADA
Intel Corp.
Suite 233, Bell Mews
39 Highway 7, Bell Corners
Ottawa, Ontario K2H 8R2
Tel: (613) 829-9714
TELEX: 053-4419

Intel Corp.
6205 Airport Rd.
Bldg. B, Suite 205
Mississauga, Ontario
L4V 1E3
Tel: (416) 671-0611
TELEX: 06983574

Multilek, Inc.*
15 Grenfell Crescent
Ottawa, Ontario K2G 0G3
Tel: (613) 226-2365
TELEX: 053-4585

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†These representatives do not offer Intel Components, only boards and systems.

INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, CA 95051 (408) 987-8080

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