iSBC 032/048/064
RANDOM ACCESS MEMORY
BOARDS

HARDWARE
REFERENCE MANUAL

Manual Order Number: 9800488B

intel®

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Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

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PREFACE

This manual provides general information, installation, principles of operation, and service information for the iSBC 032/048/064 Random Access Memory Boards. Additional information is available in the following document: *Intel MULTIBUS Interfacing*, Application Note AP-28.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 032, 048, and 064 Random Access Memory (RAM) Boards provide, respectively, 32K, 48K, and 64K bytes of dynamic random access memory for Intel iSBC 80/86 Series Single Board Computers and System 80/86 Series Microcomputers. These RAM boards, which interface directly with the CPU (or bus master) via the system bus (i.e., the Intel Multibus), differ only in the memory capacity and the manner in which the RAM arrays are configured.

On-board refresh circuits initiate periodic refresh cycles to maintain the integrity of the RAM data. An auxiliary bus connector provides battery-backup power to RAM and to the refresh circuits. A typical iSBC RAM board is shown in figure 1-1.

1-2. PHYSICAL DESCRIPTION

All circuit components are mounted on a single printed circuit board (figure 1-1) that is physically and electrically compatible with the Multibus. Depending upon the RAM capacity, the RAM array is composed of intel 2117 chips (16,384 by 1 bit), Intel 2109 chips (8,192 by 1 bit), or a combination of the two of which includes eight RAM chips. In the 8-bit mode, a Read or Write operation accesses a single 8-bit byte by addressing one storage location in each of the eight chips in the selected bank. In the 16-bit mode, two banks are selected.

On-board jumpers are used to establish the RAM base address and address boundaries. The base address also serves as the board select address. The various RAM chip and jumper configurations are described in Chapter 2 of this manual.

All electrical connections are implemented via edge connectors P1 and P2. Connector P1 (86 pins) connects to the Multibus and accommodates all of the power and signal lines including the address and data buses. The data lines terminate at a memory buffer comprising Intel 8226 Parallel Bidirectional Bus Drivers. Connector P2 accommodates the lines pertaining to the auxiliary power feature.

1-3. MODES OF OPERATION

The iSBC 032/048/064 is capable of both 8 bit and 16 bit operation under the control of the current bus master. Board modifications are not required to convert between 8 and 16 bit operations. Refer to paragraph 3-7 for a more detailed description of data transfers.

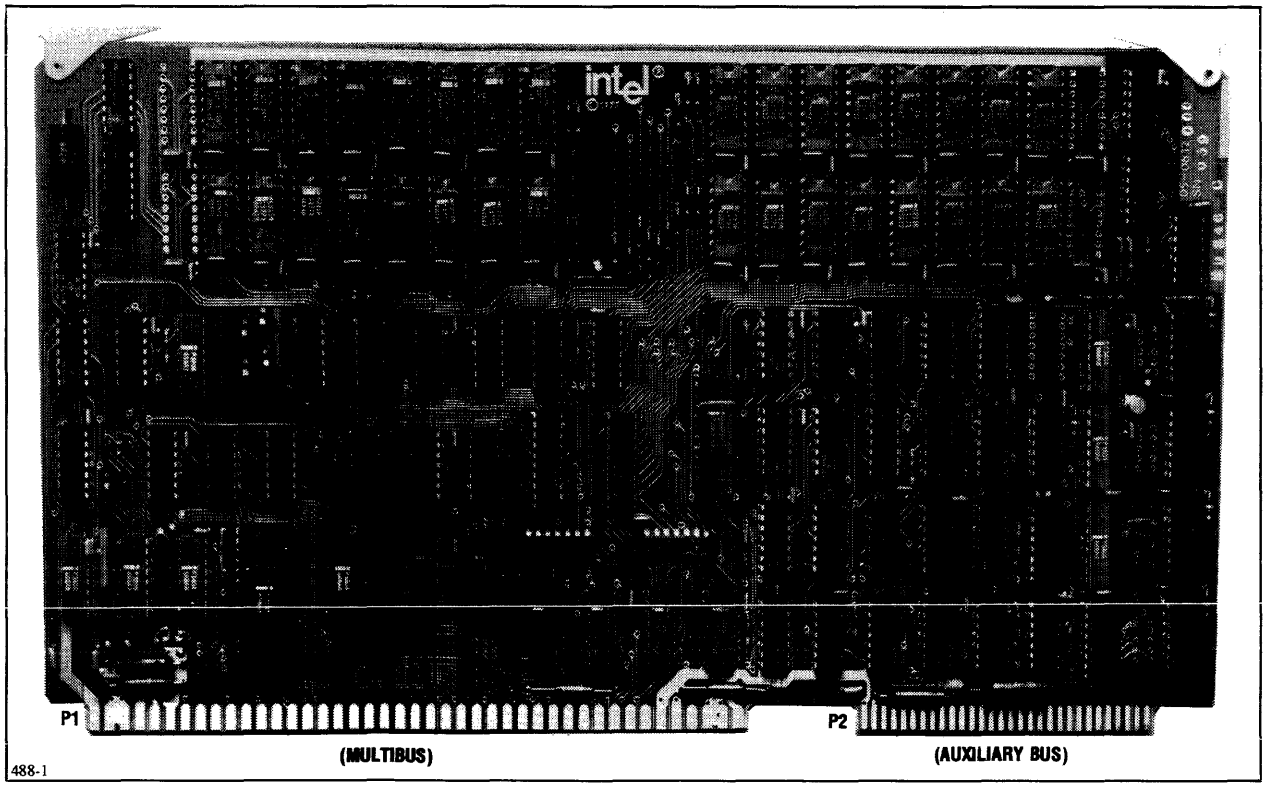


Figure 1-1. Typical iSBC Random Access Memory (RAM) Board

1-4. DOCUMENTATION SUPPLIED

The following documentation is supplied with the iSBC 032/048/064 RAM Boards:

a. Schematic Diagram, dwg. no. 01-0632-000
b. Assembly Drawing, dwg. no. 05-0632-000

1-5. SPECIFICATIONS

Specifications for the iSBC 032/048/064 are listed in table 1-1.

Table 1-1. Specifications

CAPACITY	
iSBC 032:	32,768 8-bit bytes or 16,384 16-bit words.
iSBC 048:	49,152 8-bit bytes or 24,576 16-bit words.
iSBC 064:	65,536 8-bit bytes or 32,768 16-bit words.
MULTIBUS INTERFACE:	All address, data, and command signals are TTL compatible.
ADDRESS SELECTION	
iSBC 032:	32K by 8-bit segments starting at any jumper-selectable base address on a 16K byte boundary; or 16K words (16 bit).
iSBC 048:	48K by 8-bit segments starting at any jumper-selectable base address on a 16K byte boundary; or 24K words (16 bit).
iSBC 064:	64K by 8-bit segments starting at any jumper-selectable base address on a 16K byte boundary; or 32K words (16 bit).
ACCESS TIME:	450 nsec.
CYCLE TIMES	
Read:	700 nsec, maximum.
Write:	700/1240* nsec, maximum.
Refresh:	585 nsec, maximum.
PHYSICAL CHARACTERISTICS	
Width:	30.48 cm (12.00 inches).
Depth:	17.15 cm (6.75 inches).
Thickness:	1.27 cm (0.50 inch).
Weight:	397 gm (14 ounces).

POWER REQUIREMENTS:

Voltage	Current (Without Battery)	Current (With Battery)
V_{CC} = +5V ±5%	I_{CC} = 2.0A typ. = 3.2A max.	I_{CC} = 1.0A typ. = 1.7A max.
V_{DD} = +12V ±5%	I_{DD} = 400 mA typ. = 600 mA max.	I_{DD} = 100 mA typ. = 200 mA max.
V_{BB} = −5V ±5%	I_{BB} = 30 mA typ. = 40 mA max.	I_{BB} = 30 mA typ. = 40 mA max.
**V_{BB} = −10V ±5%	I_{BB} = 50 mA typ. = 60 mA max.	I_{BB} = 50 mA typ. = 60 mA max.

*1240 nsec = Advance Write selected.
**Intellec uses −10V rather than −5V supply.

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBC 032/048/064 RAM Boards. These instructions include unpacking and inspection; installation considerations such as power and cooling requirements, physical dimensions, and bus interface requirements; jumper configurations; optional battery backup and memory protect connections; board installation; and programming considerations.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shiping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel MCSD Technical Support Center (see paragraph 4-3) to obtain a Repair Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The iSBC 032/048/064 RAM Boards are designed for interface with an Intel iSBC 80/86 Single Board Computer based system or an Intel Intellec Microcomputer Development System (MDS). Important installation and interfacing criteria are presented in the following paragraphs.

2-4. POWER REQUIREMENT

Power requirements for the iSBC 032/048/064 RAM Boards are specified in table 1-1. For installation in an iSBC 80/86 Single Board Computer based system, ensure that the system power supply has sufficient +5V, -5V, and +12V current capacity to accommodate the additional requirement. For installation in an Intellec MDS, calculate the total +5V, +12V, and -10V current requirements for the standard modules and all installed optional modules. Ensure that the additional current requirement will not exceed the capacity of the MDS power supply.

2-5. COOLING REQUIREMENT

The iSBC 032/048/064 RAM Boards dissipate 274 gram-calories/minute (1.1 Btu/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). The Intel System 80/86 enclosures and the Intellec MDS include fans to provide adequate intake and exhaust of ventilating air.

2-6. PHYSICAL DIMENSIONS

Physical dimensions of the iSBC 032/048/064 are as follows:

a. Width: 30.48 cm (12.00 inches)
b. Depth: 17.15 cm (6.75 inches)
c. Thickness: 1.27 cm (0.50 inch)

2-7. BUS INTERFACE REQUIREMENTS

The iSBC 032/048/064 RAM Boards are designed for installation in a standard Intel iSBC 604/614 Cardcage or in the Intellec MDS motherboard. As shown in figure 1-1, edge connector P1 provides interface to the Multibus. Connector P1 pin assignments are listed in table 2-1 and descriptions of the signal functions are given in table 2-2. Edge connector P2 is an auxiliary battery backup and memory protect interface as described in paragraph 2-16. Alternative mating connectors for P1 and P2 are listed in table 2-3.

The ac and dc characteristics of the RAM boards are presented in tables 2-4 and 2-5, respectively. The bus exchange timing for RAM Read and Write operations is shown in figure 2-1.

2-8. JUMPER CONFIGURATIONS

Instructions for configuring jumpers for the memory address block, page address assignment, delayed/advanced write and Advanced Acknowledge (AACK/) functions are provided in the following paragraphs.

2-9. PAGE SELECT

Each iSBC memory board in a one megabyte system may be assigned to a specific 64K byte block of memory called a "page." In such a system there is a total of 16 pages, each page occupying 64K bytes of system memory. The pages are designated, in hexadecimal notation, 0 through F, with page 0 being the lower page and page F being the upper or top page.

Page addressing is accomplished with Multibus address lines ADR10-ADR13. The address on these lines is decoded by the A79 circuit.

Three jumper plugs are used to assign the iSBC 032/048/064 Board page. The board is shipped from the factory assigned to page 0 (0-64K). In this configuration, the W7 jumper plug is installed between E8 and E18, the W6 jumper plug is installed between E7 and E17, and the W5 jumper plug is installed between E5 and E21.

To assign the iSBC 032/048/064 Board to another page, several jumper plug changes are required. All jumper plug connections are outlined in table 2-6. The required jumper plugs should be installed according to the following procedure:

Table 2-1. Multibus Connector P1 Pin Assignments

PIN*	SIGNAL	FUNCTION	PIN*	SIGNAL	FUNCTION
1	GND	Ground	44	ADRF/	Address bus
2	GND		45	ADRC/	
3	+5 VDC	Power input	46	ADRD/	
4	+5 VDC		47	ADRA/	
5	+5 VDC		48	ADRB/	
6	+5 VDC		49	ADR8/	
7	+12 VDC		50	ADR9/	
8	+12 VDC		51	ADR6/	
9	−5 VDC		52	ADR7/	
10	−5 VDC		53	ADR4/	
11	GND	Ground	54	ADR5/	
12	GND		55	ADR2/	
13			56	ADR3/	
14	INIT/	System Initialize	57	ADR0/	Equivalent to BLEN
15			58	ADR1/	
16			59	DATE/	Data bus
17			60	DATF/	
18			61	DATC/	
19	MRDC/	Memory Read Command	62	DATD/	
20	MWTC/	Memory Write Command	63	DATA/	
21			64	DATB/	
22			65	DAT8/	
23	XACK/	Transfer Acknowledge	66	DAT9/	
24	INH1/	Inhibit RAM	67	DAT6/	
25	AACK/	Advanced Acknowledge	68	DAT7/	
26			69	DAT4/	
27	BHEN/	Byte High Enable	70	DAT5/	
28	ADR10/		71	DAT2/	
29			72	DAT3/	
30	ADR11/		73	DAT0/	
31			74	DAT1/	
32	ADR12/		75	GND	Ground
33			76	GND	
34	ADR13/		77	−10 VDC	Power Input**
35			78	−10 VDC	
36			79		
37			80		
38			81	+5 VDC	Power input
39			82	+5 VDC	
40			83	+5 VDC	
41			84	+5 VDC	
42			85	GND	Ground
43	ADRE/	Address Bus	86	GND	

*All unassigned pins are reserved.
**Intellec MDS only.

Table 2-2. Multibus Signal Functions

SIGNAL	FUNCTIONAL DESCRIPTION
AACK/	*Advanced Acknowledge.* An early indication to the bus master that iSBC RAM Board has accepted the command and is executing the specified Memory Read or Memory Write operation.
ADR0/-ADRF/	*Address.* These 16 lines transmit the address of the specific RAM location to be accessed within the 64K byte page.
ADR10/-ADR13/	*Page Address.* Selects one of the 16 pages within the one megabyte system.
BHEN/	*Byte High Enable.* Enables DAT8/-DATF/ byte transfer.
DAT0/-DATF/	*Data.* These 16 bidirectional lines transmit and receive data to and from the specific RAM locations. Prevents the iSBC RAM Board from responding when the bus master addresses a higher priority device that has the same address as the iSBC RAM Board.
INIT/	*Initialize.* Resets the iSBC RAM Board circuits to a known internal state.
MRDC/	*Memory Read Command.* Initiates the reading of data from the RAM location specified on the Multibus address lines onto the Multibus data lines.
MWTC/	*Memory Write Command.* Initiates the writing of data from the Multibus data lines into the RAM location specified on the Multibus address lines.
XACK/	*Transfer Acknowledge.* Indicates to the bus master that the iSBC RAM Board has completed the specified Memory Read or Memory Write operation. That is, data has been placed onto or accepted from the Multibus data lines.

Table 2-3. Mating Connectors

INTERFACE	NO. OF PAIRS/PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR PART NO.
Multibus (P1)	43/86	0.156 in.	Soldered	CDC Micro Plastics ARCO Viking	VPB01E43D00A1[2] MP-0156-43-BW-4 AE443WP1 Less Ears 2VH43/1AV5
Multibus (P1)	43/86	0.156 in.	Wirewrap	CDC CDC Viking	VFB01E43D00A1[2] VPB01E43A00A1 2VH43/1AV5
Auxiliary[1] (P2)	30/60	0.1 in.	Soldered	Viking TI	3VH30/1JN5 H312130
Auxiliary[1] (P2)	30/60	0.1 in.	Wirewrap	CDC TI	VPB01B30A00A2[2] H311130

NOTES:
1. Connector dimensions vary from vendor to vendor. Review vendor specifications to ensure that connector heights and wirewrap pin lengths conform to your system packaging requirements.
2. CDC VPB01 . . . , VPB02 . . . , VPB04 . . . , etc., are identical connectors with different electroplating thickness or metal surfaces.

Table 2-4. iSBC 032/048/064 AC Characteristics

PARAMETER	MINIMUM (nsec)**	MAXIMUM (nsec)**	DESCRIPTION	REMARKS
t_{AS}	50		Address setup to command	From data to command
t_{DS}	−100		Write data setup to command	Normal write
t_{AAK}	89	139	Command to advanced acknowledge time	For AACK/ setting of T50
*t_{ACK}		506	Command to transfer acknowledge time	
t_{AH}	0		Address hold time	
t_{DH}	0		Write data hold time	
t_{DH}	0		Read data hold time	
t_{TO}		65	Acknowledge turnoff delay	
*t_{ACC}		450	Access time to read data	
t_{IH}	150		Inhibit hold time command	Blocks AACK if t_{IS}> t_{IS} min.
t_{IPW}	100		Inhibit pulse width	
*$t_{CY(D)}$		700	Minimum cycle time	Delayed write
*$t_{CY(A)}$		1240	Minimum cycle time	Advanced write
*t_{RD}		582	Refresh delay time	
t_{RI}	12.7 μsec	15.6 μsec	Refresh interval	128 row refresh
t_{DSAW}		500	Write data delay from command	For MDS advanced write
t_{IS}	0		Inhibit setup to command	Blocks RAM cycle and t_{ACK}

*When an asynchronous refresh cycle occurs, t_{RD} is added to these parameters.
**Except where noted.

Table 2-5. iSBC 032/048/064 DC Characteristics

SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
MRDC/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.45V		−3.0	mA
	I_{IH}	Input Current at High V	V_{IN}=2.4V		90	μA
	C_L	Capacitive Load			13	pF
MWTC/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.5V		−3.6	mA
	I_{IH}	Input Current at High V	V_{IN}=2.4V		90	μA
	C_L	Capacitive Load				pF
INIT/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.4V		−1.6	mA
	I_{IH}	Input Current at High V	V_{IN}=2.4V		40	μA
	C_L	Capacitive Load				pF
AACK/ XACK/	V_{OL}	Output Low Voltage	I_{OL}=16 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH}=5.2 mA	2.4		V
	C_L	Capacitive Load				pF
INIH/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.4V		−2.25	mA
	I_{IH}	Input Current at High V	V_{IN}=2.4V		60	μA
	C_L	Capacitive Load		7 (typ)		pF
ADR0/- ADR13/ BHEN/	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.45V		−0.25	mA
	I_{IH}	Input Current at High V	V_{IN}=5.25V		10	μA
	C_L	Capacitive Load		7 (typ)		pF
DAT0/- DATF/	V_{IL}	Input Low Voltage			0.85	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN}=0.45V		−0.35	mA
	I_{IH}	Input Current at High V	V_{IN}=5.25V		110	μA
	C_L	Capacitive Load		13 (typ)		pF
	V_{OL}	Output Low Voltage	I_{OL}=15 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH}=−1 mA	3.60		V

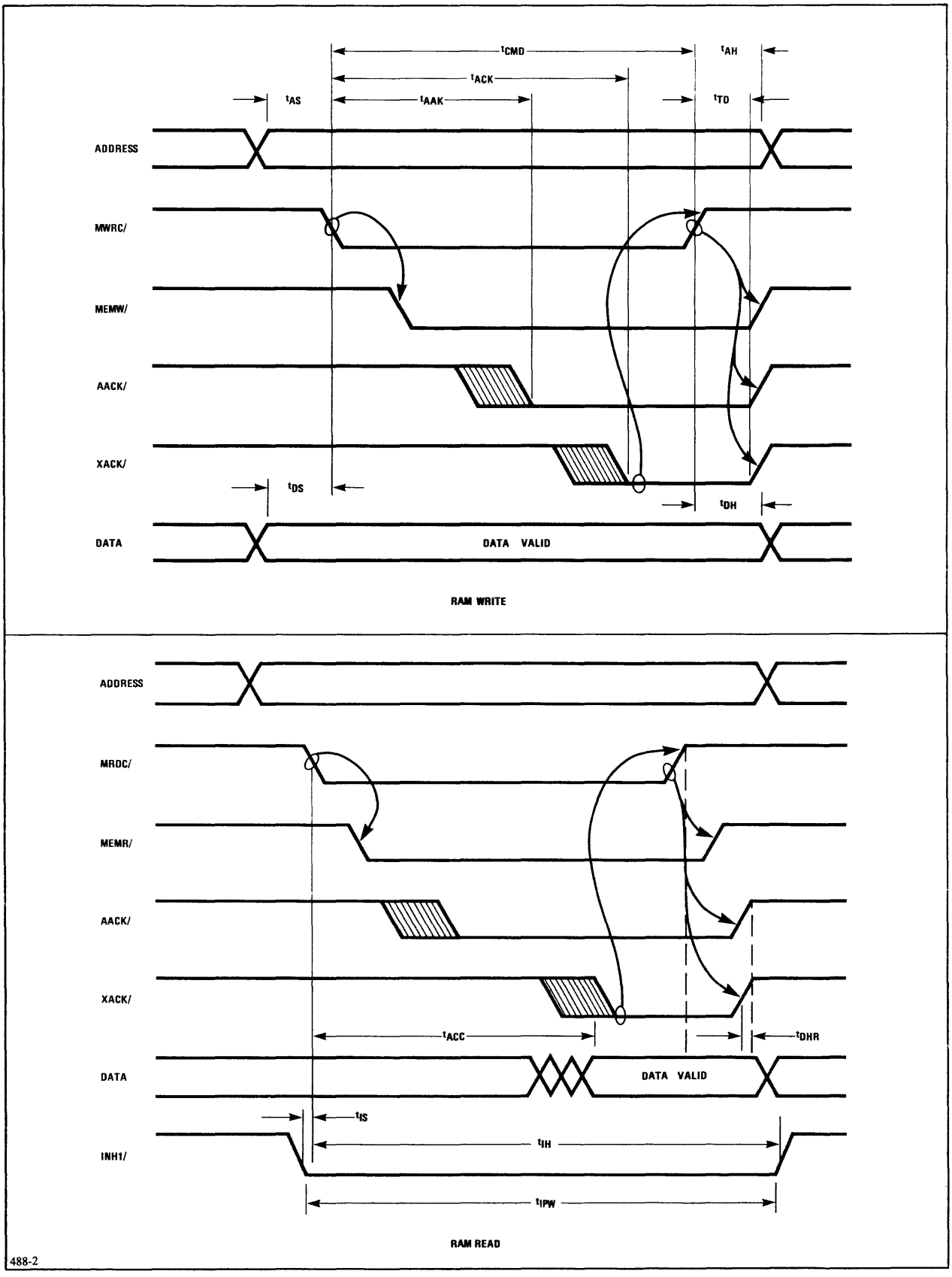


Figure 2-1. Bus Exchange Timing

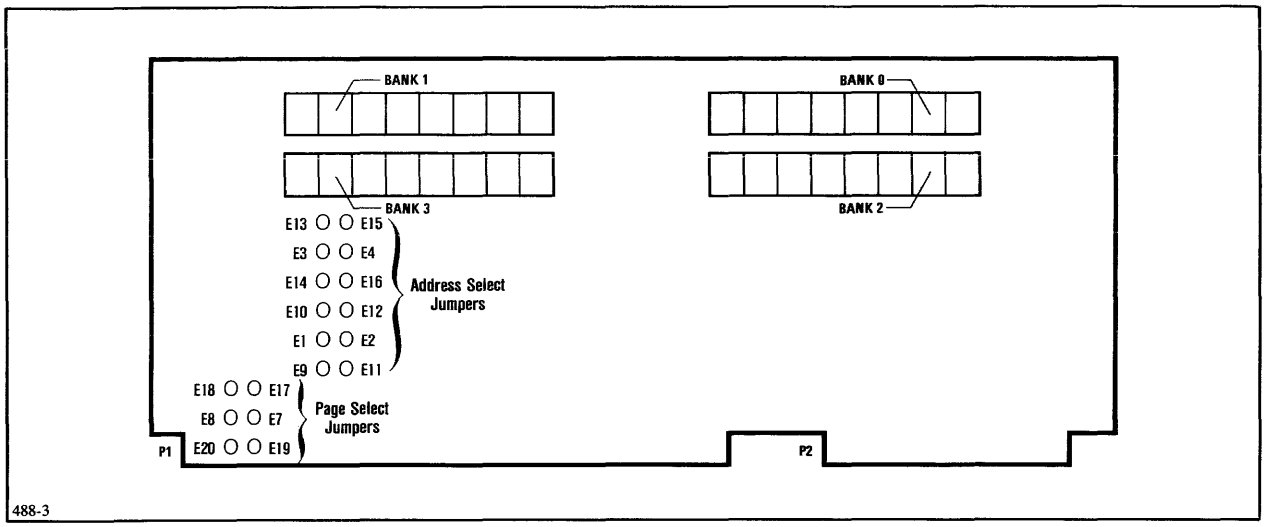


Figure 2-2. RAM Array Banks and Address Block Jumper Terminals

Table 2-6. Page Select Jumper Connections

SELECTED PAGE (RANGE)	JUMPER PLUG	FROM	TO
0 (0 — 64K) or 8 (512 — 576K)	W5	E5	E21
1 (64 — 128K) or 9 (576 — 640K)	W5	E5	E22
2 (128 — 192K) or A (640 — 704K)	W5	E5	E23
3 (192 — 256K) or B (704 — 768K)	W5	E5	E24
4 (256 — 320K) or C (768 — 832K)	W5	E6	E25
5 (320 — 384K) or D (832 — 896K)	W5	E6	E26
6 (384 — 448K) or E (896 — 960K)	W5	E6	E27
7 (448 — 512K) or F (960 — 1024K)	W5	E6	E28
PAGES 0 — 7 (0 — 512K)	W6	E7	E17
	W7	E8	E18
PAGES 8 — F (512 — 1024K)	W6	E7	E19
	W7	E8	E20

Table 2-7. RAM Address Block Assignment Jumper

NOTE	JUMPER	TERMINAL FROM	TERMINAL TO	SELECTED BANKS	ADDRESS BLOCKS
*	W1	E1	E9	0,1	0 – 16K
	W1	E3	E13	2,3	0 – 16K
*	W2	E2	E12	0,1	16K – 32K
	W2	E4	E16	2,3	16K – 32K
*	W3	E1	E10	0,1	32K – 48K
	W3	E3	E14	2,3	32K – 48K
*	W4	E2	E11	0,1	48K – 64K
	W4	E4	E15	2,3	48K – 64K

NOTE:
Connect only one.

1. Determine whether the board is to reside in the lower half (pages 0 through 7) or the upper half (pages 8 through F) of system memory. If the board is to remain in the lower half, as configured at the factory, no change is required for jumper plugs W6 and W7. If the board is to reside in the upper half, jumper plugs W6 and W7 must be removed and re-installed as indicated in table 2-6.
2. To select the specific 64K byte page the board is to reside in, install the W5 jumper plug as indicated in table 2-6.

Example: The board is to be assigned to page A of system memory (640-704K). Since page A resides in the upper half of memory, jumper plug W6 will be installed between E7 and E19; jumper plug W7 will be installed between E8 and E20. Jumper plug W5 will then be installed between E5 and E23.

2-10. MEMORY ADDRESS BLOCK ASSIGNMENT

The iSBC 032/048/064 RAM Boards includes 32 Intel dynamic RAM chips configured in four banks numbered 0 through 3. (Refer to figure 2-2.) The address boundaries of the arrays are established using jumpers to connect the address decoder outputs such that each jumper controls the assignment of a 16K block of memory address. Table 2-7 shows the correlation between the jumpers, jumper terminals, selected banks, and address blocks.

2-11. iSBC 032 RAM BOARD. The iSBC 032 RAM Board includes eight Intel 2109 8K Dynamic RAM chips in each of the four banks. To assign the 32K address locations, two address blocks of 16K each must be established. Proceed as follows:

NOTE

Banks 0 and 1, as well as banks 2 and 3, operate as a pair. Do not separate banks 0 and 1 nor separate banks 2 and 3.

a. Determine which two 16K blocks of addresses are to be assigned. (The blocks need not be contiguous.)
b. Refer to table 2-7 and connect any two jumpers (W1 through W4) that select the two desired 16K address blocks. Make certain that one jumper assigns a 16K block of addresses to banks 0 and 1, and the other jumper assigns the remaining 16K block of addresses to banks 2 and 3.

For example, to select 32K memory locations with one 16K block assigned addresses 0 to 16K and the other 16K block assigned addresses 16K to 32K, proceed as follows:

a. Connect jumper W1 between terminals E1 and E9 (assigns banks 0 and 1 to addresses 0 to 16K); connect jumper W2 between terminals E4 and E16 (assigns banks 2 and 3 to addresses 16K to 32K).

–OR–

b. Connect jumper W1 between terminals E3 and E13 (assigns banks 2 and 3 to addresses 0 to 16K); connect jumper W2 between terminals E2 and E12 (assigns banks 0 and 1 to addresses 16K to 32K).

As mentioned previously, the 16K blocks need not be contiguous. For example, banks 0 and 1 can be assigned to addresses 16K to 32K, and banks 2 and 3 can be assigned to addresses 48K to 64K.

2-12. iSBC 048 RAM BOARD. The iSBC 048 RAM Board includes 16 Intel 2109 and 16 Intel 2117 Dynamic RAM chips. The Intel 2117 16K chips comprise banks 0 and 1 and the Intel 2109 8K chips comprise banks 2 and 3. To assign the 48K address locations, three address blocks of 16K must be established. Proceed as follows:

NOTE

Banks 0 and 1, as well as banks 2 and 3, operate as a pair. Do not separate banks 0 and 1 nor separate banks 2 and 3.

a. Determine which three 16K blocks of addresses are to be assigned. (The 16K block contained in banks 2 and 3 need not be contiguous to the two 16K blocks contained in banks 0 and 1.)
b. Refer to table 2-7 and connect a jumper (W1 through W4) to assign one of the 16K address blocks to banks 2 and 3.
c. Connect two of the remaining jumpers to assign the other two 16K blocks to banks 0 and 1.

For example, to select 48K memory locations in 16K blocks with addresses 0 to 16K, 16K to 32K, and 32K to 48K, proceed as follows:

a. Connect jumper W1 between terminals E1 and E9 (assigns banks 0 and 1 to addresses 0 to 16K).
b. Connect jumper W2 between terminals E2 and E12 (assigns banks 0 and 1 addresses 16K to 32K).
c. Connect jumper W3 between terminals E3 and E14 (assigns banks 2 and 3 to addresses 32K to 48K).

As mentioned previously, the 16K blocks need not be contiguous. For example, banks 0 and 1 can be assigned to addresses 0 to 32K and banks 2 and 3 can be assigned to addresses 48K to 64K.

2-13. iSBC 064 RAM BOARD. The iSBC 064 RAM Board includes eight Intel 2117 16K Dynamic RAM chips in each of the four banks. To assign the 64K address locations, four address blocks of 16K each must be established. Proceed as follows:

NOTE

Banks 0 and 1, as well as banks 2 and 3, operate as a pair. Do not separate banks 2 and 3.

a. Refer to table 2-7 and connect any two jumpers (W1 through W4) to assign two 16K address blocks to banks 0 and 1.

Table 2-8. Advanced Acknowledge (AACK/) Delay Jumpers

JUMPER CONNECTION FROM	JUMPER CONNECTION TO	COMMAND TO AACK/ DELAY (nsec)	AACK/ TO READ DATA DELAY (nsec)
L1	T50	89 min. 139 max.	373
L1	T100	139 min. 189 max.	323
L1	E46	179 min. 229 max.	283
L1	T200/	243 min. 313 max.	214
L1	T240	297 min. 350 max.	181
L1	T300	354 min. 413 max.	124
L1	T340	392 min. 455 max.	86
L1	T400	449 min. 518 max.	29

b. Connect the other two jumpers to assign the remaining two 16K blocks to banks 2 and 3.

For example:

a. Connect jumper W1 between terminals E1 and E9 (assigns banks 0 and 1 to addresses 0 to 16K).

b. Connect jumper W2 between terminals E2 and E12 (assigns banks 0 and 1 to addresses 16K to 32K).

c. Connect jumper W3 between terminals E3 and E14 (assigns banks 2 and 3 to addresses 32K to 48K).

d. Connect jumper W4 between terminals E4 and E15 (assigns banks 2 and 3 to addresses 48K to 64K).

2-14. DELAYED/ADVANCED WRITE

Most systems operate in the delayed write mode. That is, the Memory Write Command is issued a minimum of 50 nanoseconds *after* the write data and RAM address are placed on the Multibus. When an iSBC 032/048/064 is to be used in this type of system environment, connect a jumper between terminals E29 and E30.

In systems that operate in the advance write mode, the bus master issues the Memory Write Command approximately 500 nanoseconds *before* the write data and RAM address are placed on the Multibus. Systems employing the advance write mode include the Intel Intellec Microcomputer Development System 800 (MDS 800) and any system in which there is an Intellec In-Circuit Emulator 80 (ICE 80) module. In this type of system environment, connect a jumper between terminals E29 and E31.

2-15. ADVANCED ACKNOWLEDGE

After the bus master has issued a Read or Write Command, it requires a Transfer Acknowledge (XACK/) or Advanced Acknowledge (AACK/) signal response from the iSBC 032/048/064 RAM Board. The response (XACK/ or AACK/) informs the bus master of the status of the read or write operation.

All systems can operate using the XACK/ signal. However, in some systems the XACK/ signal occurs so long after the command is issued that the bus master must idle in one or more wait states before proceeding with the sequence that completes the data transfer. In such systems, the access time can be enhanced by employing the AACK/ signal. The AACK/ signal can be user selected to occur 80 to 430 nanoseconds before the XACK/ signal, and thus can eliminate the need for bus master wait states (except when a refresh cycle is in progress at command time).

The AACK/ signal can be used only in those systems in which the timing cycle of the bus master makes its use feasible. In systems in which there are more than one bus master, the AACK/ signal must be generated at a time that is compatible with the cycle of the fastest bus master in the system.

Any one of several outputs from the iSBC RAM Board's basic clock can be used to trigger the circuits that generate the AACK/ signal. The triggering pulse is connected to the AACK/ circuits by a user-installed jumper. The jumpered clock pulse determines at what point in the iSBC RAM Board's operating cycle the AACK/ signal is generated. Table 2-8 lists the clock outputs and the time at which the AACK/ signal is generated with relation to: (1) the issuance of the bus master command (which coincides with the availability of Write data) and (2) the time that data is available on the Multibus during Read operations.

2-16. BATTERY BACKUP/MEMORY PROTECT

In systems employing the battery backup and/or memory protect feature, a mating connector must be installed in the Intellec MDS chassis, iSBC 604, or iSBC 614 to accommodate auxiliary connector P2. (Refer to figure 1-1.) The mating connector for P2 must be wired to deliver the necessary battery backup voltages and the memory protect (MPRO/) signal. Table 2-3 lists and describes some 60-pin connectors that may be used for this purpose; both solder and wirewrap connectors are listed. Table 2-9 correlates the signals and pins on the connector.

Table 2-9. Auxiliary Connector P2 Pin Assignments

PINS	FUNCTION
1 and 2	Ground
3 and 4	+5V (Battery)
7 and 8	−5V (Battery)
11 and 12	+12V (Battery)
20	MPRO/
*25	TREFON/
*TREFON/ is a factory test signal; this signal is active low when the selected board is in a refresh cycle.	

Procure the appropriate mating connector for P2 and secure it in place as follows:

a. Position holes in P2 mating connector over mounting holes that are in line with corresponding P1 mating connector.

b. From top of connector, insert two 0.5-inch #4-40 pan head screws down through connector and mounting holes.

c. Install a flat washer, lock washer, and star-type nut on each screw; then tighten the nuts.

When the P2 mating connector has been secured in place, wire the backup battery voltages and the memory protect (MPRO/) signal to the appropriate pins of the connector as listed in table 2-9. Loading requirements for the backup batteries are detailed in table 1-1. If the battery backup voltages are to be used, disconnect the system power inputs from the board as follows:

a. Disconnect system +12V source by removing jumper between terminals E32 and E33.

b. Disconnect system +5V source by removing jumper between terminals E34 and E35.

c. Disconnect system −5V source by removing jumper between terminals E36 and E37.

2-17. BOARD INSTALLATION

Always turn off the computer power (and battery backup power if used) before installing or removing the iSBC 032/048/064 RAM Board. Failure to take this precaution can result in damage to the board.

In an iSBC 80/86 Single Board Computer based system, install the board in any slot that has not been wired for a dedicated function. In an Intellec Microcomputer Development System, install the board in any slot except slots 1 and 2. Ensure that auxiliary connector P2 (if used) mates with the user-supplied mating connector.

2-18. PROGRAMMING CONSIDERATIONS

Because the iSBC 032/048/064 RAM Board represents a portion of system memory, the addresses assigned to the iSBC RAM Board must not overlap addresses assigned to other blocks of system RAM memory. For example, if the memory locations on an iSBC 104 Combination Memory and I/O Board were assigned to a 4K byte segment within one of the 16K blocks of an iSBC 032/048/064 Board, both boards will respond when the addresses are called. If the iSBC 032/048/064 RAM Board is assigned the same addresses as PROM or other higher-priority device in the system, the higher-priority device will activate the Multibus inhibit (INH1/) line when the addresses are called.

When active, INH1/ essentially disconnects the iSBC RAM Board from the system by disabling the iSBC RAM Board's memory buffers and XACK/ and AACK/ signals. Consequently, the higher-priority device will function normally, but the iSBC RAM Board will not respond to the bus master command.

There are certain instances in which the latter situation can be used advantageously. For example, a PROM board equipped with RAM inhibit (e.g., iSBC 416 PROM) having the same address as the iSBC 032/048/064 can be connected to the Multibus for maintenance purposes. When the maintenance tasks have been performed and the PROM board is removed from the Multibus, the iSBC 032/048/064 will function again as an extension of system memory.

Paragraphs 2-9 through 2-13 explain how the iSBC 032/048/064 memory address and page boundaries are established.

CHAPTER 3
PRINCIPLES OF OPERATION

3-1. INTRODUCTION

This chapter details the iSBC 032/048/064 RAM Board with reference to block, logic, and timing diagrams that are interspersed with the text, and to the iSBC 032/048/064 schematic diagram located at the end of chapter 4.

Both active-high (positive-true) and active-low (ground-true) signals appear on the schematics and drawings. To avoid confusion when referring to these signals, the following convention is used. The mnemonic for each active-low signal is terminated by a slash (e.g., REFON/). Such references indicate that the signal level is low when the condition is true (active). A mnemonic without a slash (e.g., CASTM) refers to an active-high signal. These references indicate that the signal level is high when the condition is true (active).

3-2. FUNCTIONAL DESCRIPTION

The iSBC 032/048/064 RAM Board (figure 3-1) is divided into four functional areas: address decoders, RAM array, memory buffers, and control and refresh logic. Upon command from the bus master, the iSBC RAM Board reads data from or writes data into its RAM storage. Except for the direction of data flow, both operations are performed in a similar manner.

All data is transferred between the iSBC RAM Board and the bus master via the Multibus. Data is channelled between the data bus and RAM via the memory buffers. These buffers are composed of line receivers and line drivers to maintain compatibility between the Multibus and the RAM board logic. Timed signals from the control logic activate the drivers in the memory buffers during read operations, and activate the receivers in the memory buffers during write operations. When the iSBC RAM Board is not selected, the memory buffers are essentially disconnected from the data bus.

All timing and control signals required for data transfers are generated by the iSBC RAM Board's control logic. The control sequences that produce these signals are initiated by Read and Write Commands from the bus master.

Before issuing a Read or Write Command, the bus master first addresses the RAM locations to or from which data will be transferred. The bus master issues the address of the desired page and memory location over the address bus that is common to all system devices. When the iSBC RAM Board decodes its address, it initializes the control logic to receive the forthcoming Read or Write Command.

A minimum of 50 nanoseconds after the address is placed on the bus, the bus master issues the Read or Write Command via the control bus. If the command is a Read, the iSBC RAM Board's control logic performs the sequence of operations that reads the data byte from the addressed RAM location and places it on the data bus. When the data has stabilized on the bus, the control logic issues the transfer acknowledge (XACK/) signal. In response to XACK/, the bus master removes the Read Command and the iSBC RAM Board address from the control and address busses to terminate the read operation.

If the command is a Write, the bus master places the write data byte on the data bus coincident with the issuance of the address. With the arrival of the Write Command, the iSBC RAM Board performs the sequence of operations that write the data byte into the addressed RAM location. Systems employing the advance write features issue the Write Command approximately 0.5 microsecond before the data is made available. In such systems, the iSBC RAM Board delays until the data is made available before initiating the write sequence. In either case, the control logic sends XACK/ to the bus master when write operation is completed.

In response to XACK/, the bus master deactivates the Write Command. A minimum of 50 nanoseconds after deactivating the Write Command, the bus master removes the write data byte from the data bus and removes the address from the address bus.

The refresh logic refreshes one row of memory cells every 15 microseconds. In addition, the refresh logic decides which operation to execute if the bus master issues a Read or Write Command when a refresh cycle is due. Refresh cycles are never delayed to accommodate more than one read or write cycle.

The optional auxiliary bus provides battery backup power to the memory array and all circuits associated with the refresh operation. This feature maintains the integrity of the RAM data in the event of a main power failure.

The auxiliary bus also carries the memory protect (MPRO/) signal from the bus master. When asserted, MPRO/ denies access to RAM and also protects the RAM contents during system power-fail sequences.

3-3. ADDRESSING AND DATA ROUTING

The following paragraphs describe the manner in which RAM is addressed and how data is routed between RAM and the data bus.

3-4. BOARD SELECTION AND MEMORY PARTITIONING

Two high-order address bits (ADRE/ and ADRF/) serve two major functions: board selection and memory partitioning. High-order decoder A45 decodes ADRE/ and ADRF/ to produce one of four outputs. (Refer to figure 3-2.) Each of the four outputs relate to the starting address of one 16K block of memory, for a total of 64K possible addresses. Address bits ADR10/ through ADR13/ are used for page selection. A page is one 64K byte block of system memory, within a 1 megabyte address space.

On iSBC 032 Boards, two jumpers select two of the four

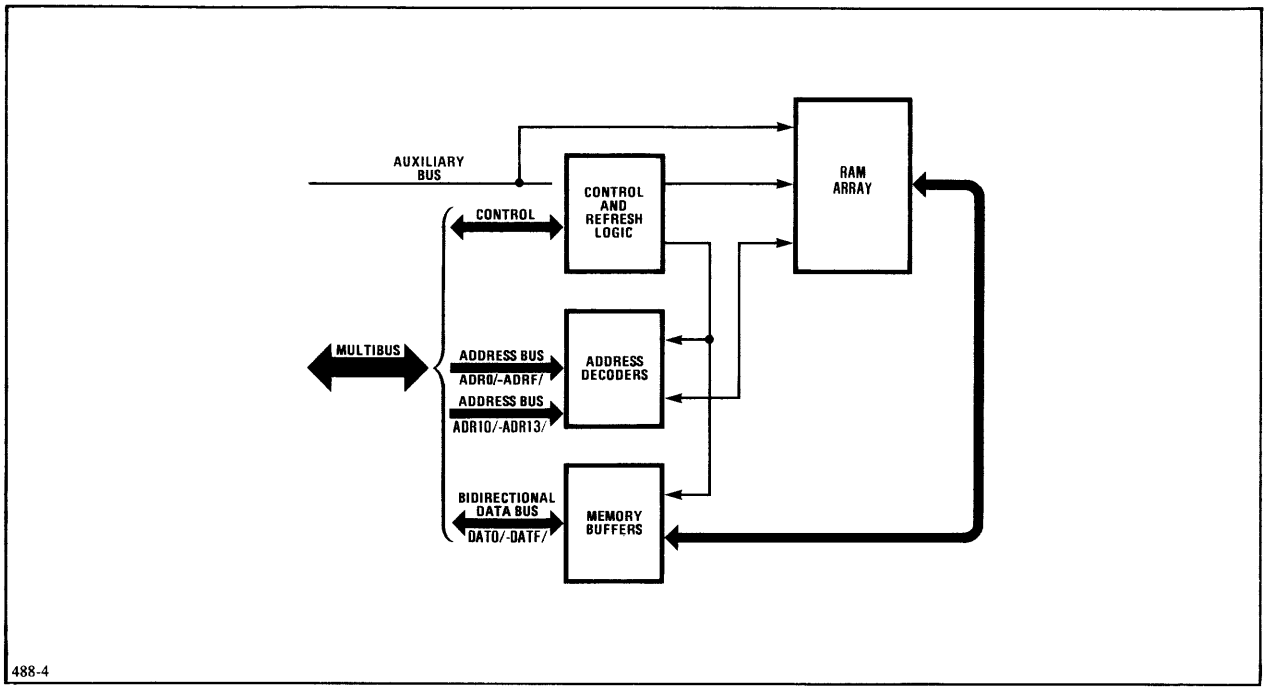


Figure 3-1. iSBC 032/048/064 Functional Block Diagram

decoder outputs (32K addresses). On iSBC 048 Boards, three jumpers select three of the four decoder outputs (48K addresses). On iSBC 064 Boards, four jumpers select all four of the decoder outputs (64K addresses). The jumpers determine which 16K blocks of addresses are assigned to the board's RAM. Together the jumpers select from two (iSBC 032) to four (iSBC 064) 16K blocks of RAM within the 64K addressable locations of system memory.

When any of the jumpered lines from the A79/45 decoders are active, gate A41-6 generates the card select (CDSEL) signal. When active, CDSEL permits control logic of the iSBC RAM Board to respond to Read and Write Commands from the bus master.

The jumper-selected outputs from the A45 decoder also function as control inputs to the RAS generator. This generator produces the RAS0/ through RAS3/ signals that partition the RAM array into four areas or banks of addresses. There are two even banks (0 and 2) and two odd banks (1 and 3).

On iSBC 032 Boards, each bank consists of 8K locations for a total of 32K locations. On iSBC 064 Boards, each bank consists of 16K locations for a total of 64K locations. On iSBC 048 Boards, banks 0 and 1 each consist of 16K locations and banks 2 and 3 each consist of 8K locations for a total of 48K locations.

Consecutive bytes of a data transfer are not stored in contiguous locations of the same bank of the RAM array. Rather, bytes with even addresses are stored in an even array, and bytes with odd addresses are stored in an odd array. The function of selecting alternate arrays and of determining which even and which odd array is to be used is implemented by the RAS generator. The RAS generator, in turn, is controlled by inputs from the A45 decoder, swap byte control, and transfer control logic.

The manner in which the even and odd bytes are routed between the RAM banks and the data bus is described in the following paragraphs. The precise timing of read and write transfers is discussed in paragraph 3-9.

3-5. EVEN ADDRESS BYTE TRANSFER

Consider the transfer of an 8-bit byte that has an even address. The least significant bit (ADR0/) of an even address is false (high). ADR0/ and BHEN/ are applied to swap byte control A78/A43/A44. For 8-bit byte operations, BHEN/ is always false. Under these conditions, the swap byte control logic applies a signal to the RAS generator (A44/A47/A48) that allows the generator to activate either the RAS0/ or RAS2/ signal.

The RAS generator makes the decision to activate RAS0/ or RAS2/ based upon which of the jumpered outputs from the high-order decoder is active. (Only one of the outputs can be active for a given address.) When active, RAS0/ initializes the row selection circuits in RAM bank 0 and RAS2/ initializes the row selection circuits in RAM bank 2. From a timing standpoint, RAS0/ or RAS2/ becomes active when the RASTM signal is sent from the iSBC RAM Boards control logic.

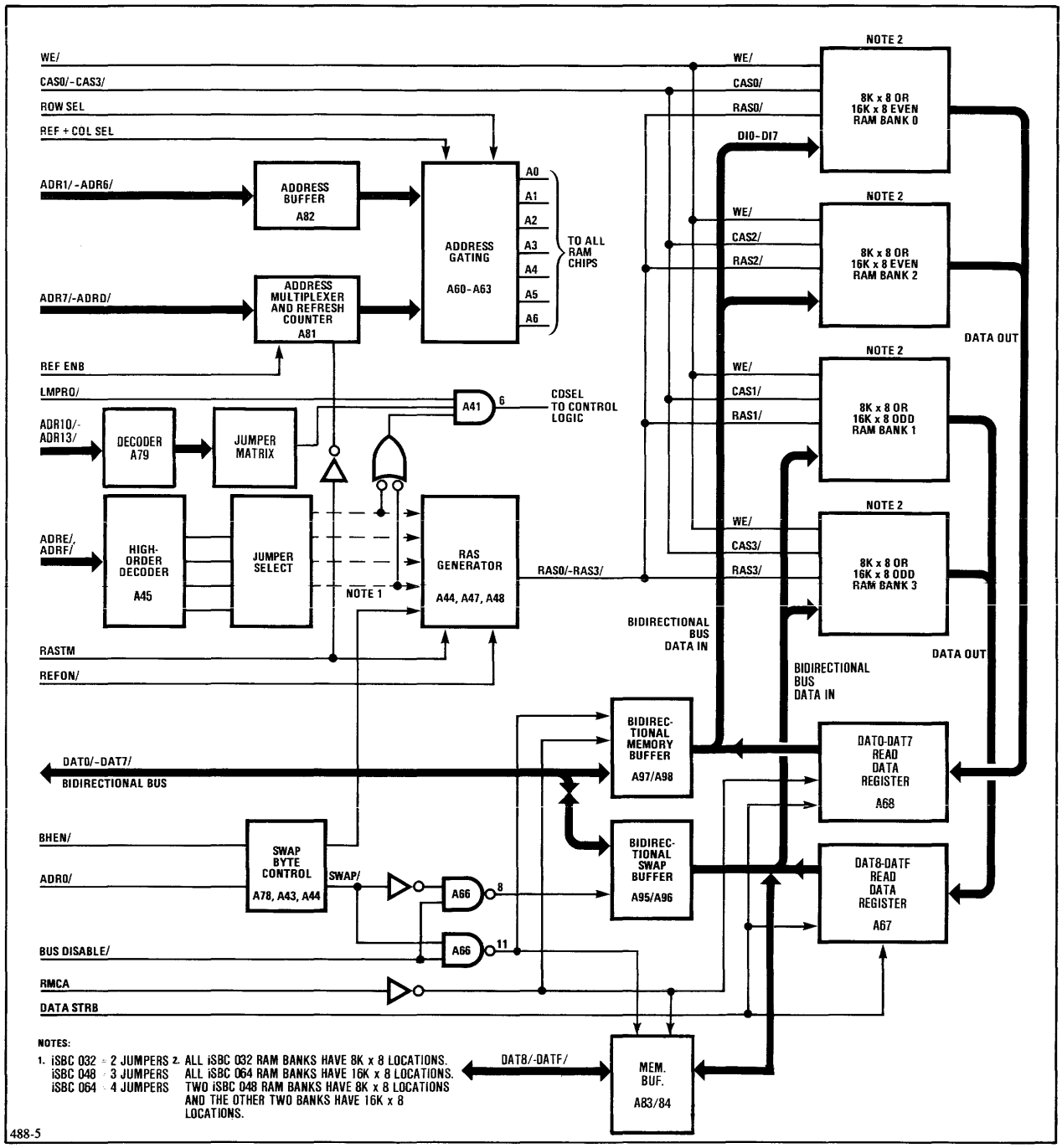


Figure 3-2. Addressing and Memory Buffer Circuits

The address of the specific row of memory cells to be selected is defined by address bus lines ADR1/ through ADR6/. This address is gated to all of the RAM chips by the ROW SEL signal from the control logic. Only the RAM bank whose RAS/ line is active processes the row address.

Some time later in the iSBC RAM Board cycle, the control logic activates the CAS0/ through CAS3/ lines to the RAM banks. These signals cause the RAM chips to begin processing the column address. The column address, which is specified by address lines ADR7/ through ADRD/ (ADR7/ through ADRE/ for 2117 chips), is gated to the RAM chips by the REF + COL SEL signal from the control logic.

Although the address column is enabled in every RAM chip, the addressed row is enabled only in the eight chips of the bank whose RAS signal is active. Consequently, only one 8-bit byte location is selected. In this example, the selected location is in the even bank whose RAS/ signal (RAS0/ or RAS2/) is active.

If the operation is a read transfer, the byte from the selected

8-bit RAM location is latched into read data register A68 by DATA STRB from the control logic. From A68 the byte is routed through the memory buffer drivers and onto Multibus data bus lines DAT0/ through DAT7/. (The buffer drivers are enabled by the RMCA signal from the control logic.)

If the operation is a write transfer, the data to be stored is sent via data bus lines DAT0/ through DAT7/ to the two even RAM banks through the memory data buffer receivers. (The buffer receivers are enabled by the RMCA signal from the control logic.) The byte is written into the even RAM bank whose RAS signal is active. The writing is effected by the write enable (WE/) signal from the control logic.

3-6. ODD ADDRESS BYTE TRANSFER

Consider the transfer of an 8-bit byte that has an odd address. In this case the least significant address bit (ADR0/) is true (low). (See figure 3-2.) When BHEN/ is false, the output from the swap byte control causes the RAS generator to activate the RAS1/ or RAS3/ signal. Whether RAS1/ or RAS3/ is activated depends upon which of the jumpered outputs from the high-order decoder is active.

When active, RAS1/ initializes the row selection circuits in RAM bank 1 and RAS3/ initializes the row selection circuits in RAM bank 3.

The data on address bus lines ADR1/ through ADR6/ is used as described previously to select a specific row in the odd RAS-selected RAM bank. CAS0/ through CAS3/ and the data on address lines ADR7/ through ADRD/ (ADR7/ through ADRE/ for 2117 chips) select the RAM columns. Together these signals select the desired 8-bit RAM location in the odd RAM bank.

If the operation is a read transfer, the byte from the selected 8-bit location is latched into read data register A67 by DATA STRB from the control logic. The contents of A67 are routed to data bus lines DAT0/ through DAT7/ via bidirectional swap buffer A95/A96. The data routing function of the swap buffer is controlled by the swap byte control.

Because ADR0/ is true, signifying an odd address, the swap byte control generates the SWAP/ signal. SWAP/ is inverted and used in conjunction with the false BUS DISABLE/ signal from the control logic to enable gate A66-8. When enabled, A66-8 activates the bidirectional swap buffer.

At the same time, SWAP/ forces the output from gate A66-11 high. This high level disables the bidirectional memory buffer and disconnects the buffer from the data bus.

If the operation is a write transfer, the data to be stored in the selected RAM location is sent via data bus lines DAT0/ through DAT7/. As during a read operation, the swap byte control disables the bidirectional memory buffer and enables the bidirectional swap buffer. When enabled, the swap buffer channels the data from data bus lines DAT0/ through DAT7/ to the odd RAM banks. When the control logic generates write enable (WE/), the data is written into the addressed RAM location.

3-7. 16-BIT WORD TRANSFER

The 16-bit word transfer is controlled by two Multibus signals: Byte High Enable (BHEN/) and Byte Low Enable (BLEN). Byte Low Enable is equivalent to ADR0/ (note that the active state of these two signals is opposite).

When BHEN/ is true (low) data is transferred from an odd data bank, via lines DAT8/ - DATF/. When BLEN is true (high), data is transferred from an even bank via lines DAT0/ - DAT7/. When both signals are false, the swap buffer (A95/96) is activated, enabling data from an odd bank onto the DAT0/ - DAT7/ lines. Table 3-1 gives the complete truth table for the different transfer methods.

3-8. REFRESH CYCLE ADDRESSING

The iSBC 032/048/064 RAM Boards employ a RAS/ only type of refresh cycle. This type of cycle can be considered a semi-read cycle. That is, a specific row address is applied simultaneously to every chip in the memory array. This initiates a read of all 128 cells in the addressed row of each chip. However, no column selection is initiated.
In normal read cycle, the column address selects one of the cells in each of the selected rows as outputs. Because no column is selected in a refresh cycle, there is no output from memory. However, as in a normal read, the data that was read out of the rows of cells is written back into the cells as a function of the internal chip operation. This read/write cycle constitutes a refresh operation.

During a refresh cycle, the row address is generated in the A81 address multiplexer and refresh counter. (Refer to figure 3-2.) During a read or write operation, A81 channels the column address from address bus lines ADR7/ through ADRD/ to the memory array (via the address gating). During a refresh cycle, A81 channels the contents of its internal refresh counter to the memory array. The multiplexing of the contents of the refresh counter from A81 is initiated by the REF ENB signal, which is applied to A81 from the refresh cycle control logic. (Refresh cycle timing is discussed in paragraph 3-11.)

The refresh counter output from A81 is gated to all of the chips in the memory array through the address gating (A60-A63). The gating signal, REF + COL SEL, is generated in the control logic. At the end of each refresh cycle, the control logic generates the REFON/ signal that increments the refresh counter by one. Consequently, the next refresh cycle refreshes the row of cells with the next higher consecutive address.

The Intel 2117 RAM chips used in the iSBC 048 and iSBC 064 Boards have 128 rows of cells (128 rows times 128 columns equal 16K cells). Therefore, the refresh counter is a 7-stage counter capable of counting to 128. Because the Intel 2109 RAM chips used in the iSBC 032 Boards have only 64 rows (64 rows times 128 columns equal 8K cells), the entire contents of the iSBC 032 are refreshed after 64 refresh cycles.

3-9. TIMING AND CONTROL

Each operating cycle is initiated under the control of Intel 3222 Refresh Controller A69. The controller initiates an operating cycle as the result of: (1) a bus master Memory Read Command (MRDC/), (2) a bus master Memory Write Command MWTC/), or (3) a memory refresh request.

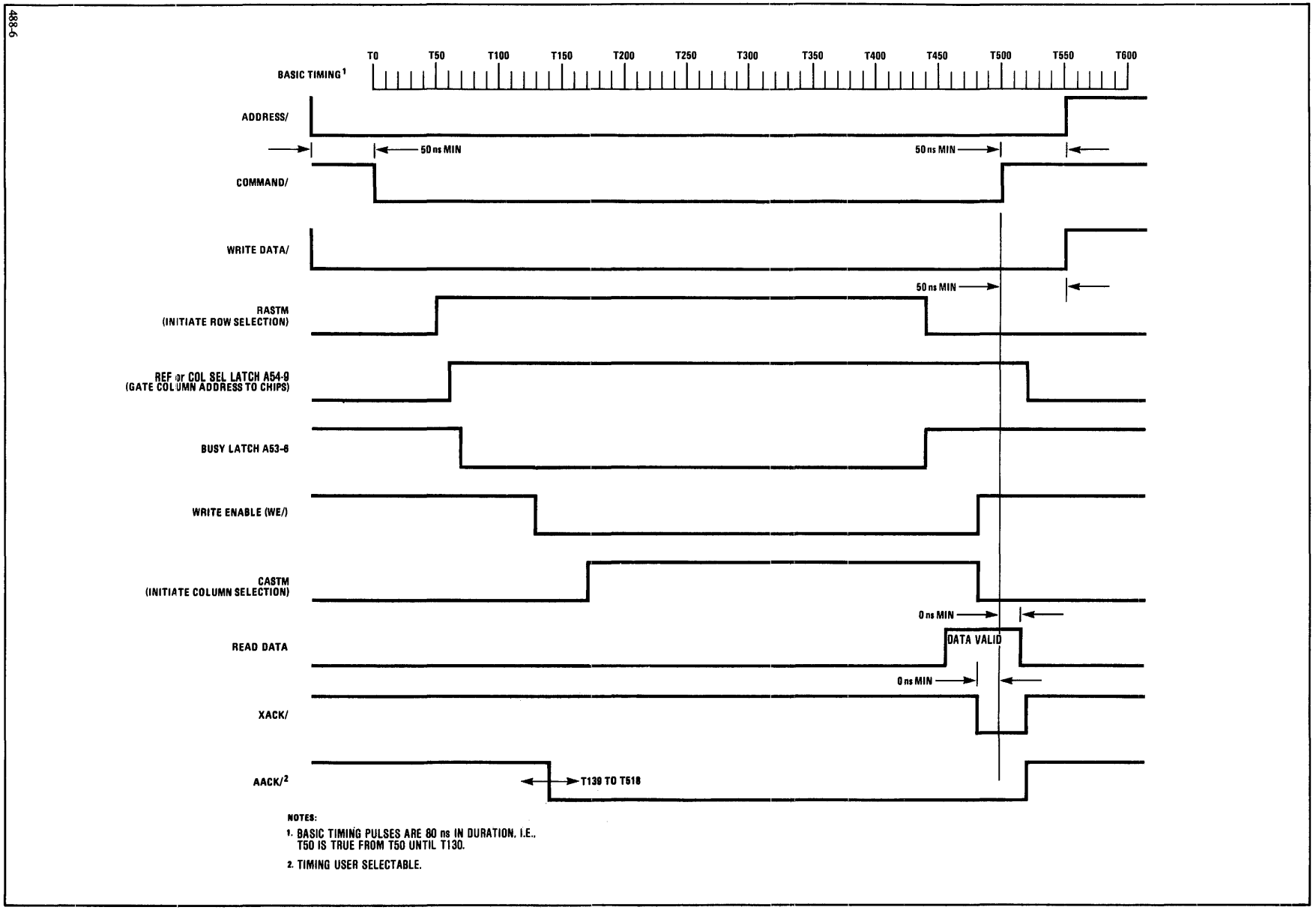


Figure 3-3. Data and Control Timing Diagram

Table 3-1. Data Transfer Methods

BHEN/	BLEN (ADR0/)	Source of: DAT0/ - DAT7/	Source of: DAT8/ - DATF/	Transfer Type
False (1)	True (1)	Even RAM Bank	Undefined	Even Address — Low Byte
False (1)	False (0)	Odd RAM Bank	Undefined	Odd Address — Low Byte
True (0)	True (1)	Even RAM Bank	Odd RAM Bank	16 Bit Word
True (0)	False (0)	Undefined	Odd RAM Bank	Odd Address — High Byte

When a bus master command and a refresh request occur at approximately the same time, the A69 controller must determine the order in which to respond. If the bus master command precedes the refresh request by more than 2 nanoseconds, the controller initiates a command cycle. Then, when the command cycle is completed, the controller initiates a refresh cycle. If the bus master command precedes the refresh request by less than 2 nanoseconds, the controller initiates a refresh cycle and then responds to the bus master's request for a command cycle.

Paragraphs 3-10 and 3-11 describe in detail the operation of the control logic during read, write, and refresh cycles. Figure 3-3 depicts the period of data availability and the timing of the major control signals associated with these operating cycles.

3-10. TYPICAL READ/WRITE CYCLE

When a Memory Read (MRDC/) or a Memory Write (MWTC/) Command is sent from the bus master, gate A87-8 forces pin 3 of refresh controller A69 low if: (1) the iSBC RAM Board has been selected (CDSEL high), (2) no refresh cycle is in progress, and (3) no acknowledge signal is being sent to the bus master as the result of a previous cycle. When A69-3 goes low, A69-4 sets cross-coupled latch A52-6/8.

The output from A52-6/8 triggers the delay comprising A59, A77, A94, and A106. Together, these components provide a delay of 600 nanoseconds. They are tapped at various points to provide the timing pulses that are required throughout the control logic. The T80 (80-nsec delay) output from the delay line is used to reset the cross-coupled latch (A52-6/8). Consequently, whenever the refresh controller initiates a cycle, an 80-nsec pulse begins moving down the delay line.

At T50, RASTM latch A54-5 is set. It is conditioned for setting by the fact that no advance write condition exists (A92-6 high). (Advance write is described in paragraph 3-13). When set, RASTM latch A54-5 generates RASTM which gates the active row address select signals (RAS0/ — RAS3/) to the RAM array. These select signals initiate row select operations in the memory banks.

Address bits ADRE/ and ADRF/ are also latched into A80 by RASTM via A55-1. This ensures that the RAS generator logic will be stable during the entire memory cycle.

Because latch A54-9 begins each operating cycle in the reset state, the ROW SEL signal is now active. (Latch A54-9 is not set by the T50 trigger because pin 19 of refresh controller A69 is high from approximately T45 of a read or write cycle). The ROW SEL signal gates the row address (from ADR1/ — ADR6/ and buffer A82) to the RAM chips. The RAM chips whose RAS signal is active select the row of memory cells specified by the row address.

At T60, busy latch A53-6 is preset, activating the BUSY/ signal. When active, BUSY/ prevents the refresh controller from initiating a refresh cycle. In addition, it forces the refresh controller output at pin 20 low. This signal disables gate A87-8, preventing the controller response to subsequent commands.

At T130, latch A54-9 is set, generating the REF + COL SEL signal. This signal gates the column address (from ADR7/ - ADRD/ and multiplexer A81) to the RAM chips.

At T170, latch A73-5 generates the CASTM signal which, in turn, activates the CAS0 through CAS3 signals. These signals initialize the selection of the column of memory cells whose address is specified by address bus bits ADR7/ through ADRD/. At this time, all addressing data (row and column) required for the selection of a specific data byte is present at the RAM array.

If the operation is a write transfer, gate A90-11 generates write enable signal WE/ when write latch A73-9 is set at T130. This signal initializes the RAM chip write circuits. Consequently, data is written into the addressed RAM location with the arrival of the CAS signals at T170.

During a read operation, gate A74-6 generates the DATA STRB signal coincident with the generation of CASTM (T170). DATA STRB gates the data read from RAM through data out buffers A67 and A68 to the data bus. The data is latched into the data out buffers when CASTM latch A73-5 is reset at T480 of the cycle. The iSBC RAM Board's access time is enhanced by the fact that the data is available as soon as DATA STRB is generated as opposed to when the data is latched into the data out buffers.

At T480 (trailing edge of T400), XACK latch A91-5 is set, activating the XACK/ signal to the bus master. The latch is conditioned for setting by gate A74-11 because: (1) the cycle in progress is not a refresh cycle, and (2) there is not an active advance write condition. If the operation is a write, XACK/ informs the bus master that the data on the data bus has been written into the addressed RAM location. If the operation is a read, XACK/ informs the bus master that the data requested from RAM is available on the data bus.

XACK latch A91-5 and AACK latch A91-9 are reset when

end-of-command latch A103-5 and end-of-busy latch A101-9 are set. A103-5 is set when the bus master responds to XACK/ by removing the Read or Write Command from the system bus. A101-9 is set when busy latch A53-6 is reset at the trailing edge of T440 (T520). Latches A101-9 and A103-5 are cleared after latches A91-5 and A91-9 are cleared.

The iSBC RAM Board cycle terminates when latches A54-5, A54-9, and A53-6 are reset at T440; and when latches A73-5 and A73-9 are reset at T480.

3-11. REFRESH CYCLE

Memory refresh cycles occur as a function of a timer internal to the A69 refresh controller. If the bus master issues no read or write commands, a refresh cycle will occur every 15 microseconds when the timer output at pin 1 of A69 forces pin 2 low. When A69-2 goes low, the resultant low at A69-4 and the T80 timing pulse toggle cross-coupled latch A52-6/8. As during a bus master command cycle, the toggling of A52-6/8 starts an 80-nsec pulse moving down delay line A59, A77, A94, A106.

Because the cycle is a refresh cycle rather than a command cycle, pin 19 of refresh controller A69 goes low instead of high by approximately T45. This low signal is inverted and applied to the D-input of refresh enable latch A53-9. As a result, A53-9 cannot be reset by the trailing edge of T50 as during a cycle initiated by the bus master. (A53-9 is preset at T440 of every cycle.) Because A53-9 remains set throughout the refresh cycle, the REF ENB signal remains high. When high, REF ENB conditions the A81 multiplexer and refresh counter (figure 3-2) so that the contents of the refresh counter is routed to the RAM array. The refresh counter specifies the address of the row of RAM cells that are to be refreshed.

Latch A54-5 does not set at T50 as in a system cycle because REFON/ (A69-19) is low causing A74-11 to be low. A54-5 is not set until T70 when its preset input (pin 4) is activated. This delayed RASTM signal allows the refresh address to stabilize. As explained in the discussion of addressing (paragraph 3-4), the RASTM signal causes the RAS generator to enable the appropriate RAS signal as determined by the RAM address. The bank of the RAM array that receives the active RAS signal refreshes the cells in the row specified by the refresh counter.

Most of the operations performed during a cycle initiated by the bus controller are inhibited by the fact that pin 19 of refresh controller A69 is low during a refresh cycle. For example, the low at A69-19 inhibits the generation of the XACK/, AACK/, CASTM, and DATA STROBE signals.

As during a cycle initiated by the bus master, busy latch A53-6 is set from T60 until the trailing edge of T440 (T520). When set, A53-6 prevents the refresh controller from responding to commands from the bus master. When A53-6 is reset at T520, pin 19 of refresh controller A69 goes high, forcing the REFON/ signal high. The positive transition of REFON/ steps the refresh counter in A81. As a result, the next refresh cycle refreshes the cells of the rows having the next higher consecutive address.

3-12. ADVANCED ACKNOWLEDGE

The Advanced Acknowledge (AACK/) signal is generated 80 to 430 manoseconds before the normal Transfer Acknowledge signal XACK/. The AACK/ signal informs the bus master that the read or write transfer in progress will be completed early enough so that the bus master can proceed with its basic timing sequence. Were it not for AACK/, the bus master would not be informed of the status of the data transfer until the arrival of XACK/. In some systems, the XACK/ signal occurs so late in the current timing state that the bus master would enter one or more wait conditions before proceeding to the next timing state. In such systems, the access time of the system is enhanced by employing the AACK/ signal to eliminate the need for a wait condition. It can only be employed in systems in which the bus master cycle timing makes its use feasible.

During a command cycle, the D-input to AACK/ latch A91-9 is held high by the pin 19 output from refresh controller A69. With the D-input high, the AACK/ latch is set when triggered. Depending upon the system timing requirements, eight of the timing pulses, T50 through T400, can be wired to trigger the latch. When set, AACK/ latch A91-9 enables one input of the gate (A74-8) that generates the AACK/ signal. The other input of the gate is enabled by the set output from latch A101-5.

Usually, latch A101-5 is preset when XACK/ latch A91-5 is set near the end of each cycle (T480). Therefore, gate A74-8 normally generates AACK/ whenever AACK latch A91-9 is set. Gate A74-8 cannot generate the AACK/ signal if latch A101-5 is in the reset state.

The D-input to latch A101-5 is controlled such that the latch is reset when the busy latch is reset (T520) if: (1) there is an active bus master command but an inhibit (INH1/) condition exists (inhibit is explained in paragraph 3-13), or (2) a bus master command is issued during a refresh cycle. When either of these situations occur, the AACK/ signal of the following cycle is delayed to coincide with the XACK/ signal.

The AACK/ signal is deactivated when AACK latch A91-9 is reset when gate A100-8 is enabled. Gate A100-8 is enabled when: (1) latch A101-9 is set by the output from busy latch A53-6 at T520, and (2) latch 103-5 is set by the deactivation of the command from the bus master.

3-13. ADVANCE WRITE

In systems employing the advance write feature, the bus master issues a Write Command 0.5 microsecond before it makes the write data available on the system bus. The iSBC RAM Board's control logic compensates for the early arrival of the command by initiating a dummy cycle of 520 nanoseconds before executing a true write cycle. During the dummy cycle, the control logic blocks: (1) the signals that select the desired RAM bank, (2) the write enable (WE/) signal to RAM, and (3) the transfer acknowledge (XACK/) signal to the bus master. Essentially, the control logic undergoes two control cycles that appear as a single cycle to the system.

When the Write Command (MWTC/) arrives from the bus

master it forces pin 3 of refresh controller A69 low. The output at A69-4 and the T80 timing pulse toggle cross-coupled latch A52-6/8 which, in turn, starts an 80-nsec pulse moving down delay line A59, A77, A94, A106. These operations are identical to those of a normal write operation (paragraph 3-9).

Unlike a normal write operation, latch A92-5 is set at T20 of the cycle. This occurs because terminals E29 and E31 are jumpered in systems employing advance write. When set, A92-5 prevents T50 from setting RASTM latch A54-5. As a result, the RAS0/ – RAS3/ signals that select the addressed RAM banks cannot be generated. Setting advance write latch A92-5 also prevents latch A73-9 from generating the write enable (WE/) at T130. Inhibiting the generation of the RAS/ and WE/ signals prevents the writing of data into the RAM array.

As in a normal cycle, busy latch A53-6 is set at T60. Its output prevents refresh controller A69 from responding to subsequent commands from the bus master or from initiating a refresh cycle.

At T300, the second advance write latch (A92-9) is set. Its set output forces the D-input of busy latch A53-6 low, preventing the busy latch from resetting at T440. Because the busy latch output to refresh controller A69 remains low, the controller is maintained in a condition in which no bus master command or refresh cycles can be initiated.

At T520, A70-6 triggers cross-coupled latch A52-6/8. The latch responds as if it had been triggered by the refresh controller's reaction to a bus master command. That is, it causes a second timing pulse to begin moving down the delay line.

At T20 of this second cycle, advance write latch A92-5 is reset. With A92-5 reset, RASTM latch A54-5 initiates the generation of the RAS0/ through RAS3/ signals, and write enable latch A73-9 generates the WE/ signal as in a normal write cycle. Consequently, the data on the system bus is written into the addressed RAM location.

Secondary advance write latch A92-9 is reset at T300. As a result, busy latch A53-9 is permitted to reset at the trailing edge of T440 (T520), and the write cycle proceeds to its normal conclusion.

3-14. INHIBIT CIRCUIT

If the bus master issues an iSBC RAM Board address, and if there is a higher-priority device on the system bus with the same address, the higher-priority device will issue an inhibit (INH1/) signal. Essentially, INH1/ disconnects the iSBC RAM Board from the system by disabling the memory buffers and the XACK/ and AACK/ signals. When the command associated with the address is issued, the iSBC RAM Board performs the sequence of operations dictated by the command, even though the command is invalid for the board. However, the system is unaware of and unaffected by the iSBC RAM Board acitivity because of the INH1/ signal. Inhibit timing is shown in figure 3-4.

An inhibit condition is initiated at the iSBC RAM Board by the INH1/ signal. The INH1/ signal immediately activates the BUS DISABLE/ signal, disabling the board's memory buffers, and disabling the drivers that output the AACK/ and XACK/ signals.

The INH1/ signal is inverted and enables one input to gate A90-3. The other input to the gate is enabled by gate A100-11. Gate A100-11, in turn, is enabled: (1) when T50 of the current memory cycle is activated and (2) if the current cycle is not a refresh cycle (REFON inverted). Thus INH1/ is sampled 50 ns into the memory cycle, giving the INH1/ signal time to stabilize.

Enabling gate A90-3 triggers inhibit latch A99. The reset output from the latch: (1) keeps the BUS DISABLE/ signal active, (2) keeps the drivers that output the AACK/ and XACK/ signals disabled, (3) disables advance write latches A92-5 and -9, (4) prevents the setting of write enable latch A73-9, and (5) allows latch A101-5 to be reset when busy latch A53-6 is reset at the end of the invalid cycle. Condition (5) causes AACK/ of the next valid cycle to be delayed until XACK/ is generated.

Inhibit latch A99-6 is reset when gate A102-12 is enabled. This gate is enabled when: (1) the bus master command is deactivated, setting latch A103-5; (2) the busy latch resets, setting latch A101-9; and (3) the XACK and AACK latches are reset as a result of (1) and (2).

3-15. MEMORY PROTECT OPTION

The optional memory protect feature makes it possible for the bus master to prevent the iSBC 032/048/064 from responding to Read or Write Commands. The memory protect option is activated when the system controller activates the Memory Protect (MPRO/) signal.

When active, MPRO/ forces the D-input to memory protect latch A103-9 low. Consequently, the latch is reset when busy latch A53-6 is reset at T520 of the following refresh cycle. The resultant LMPRO/ signal from the set output of the memory protect latch prevents gate A41-6 from generating the card select (CDSEL) signal. Because CDSEL remains false, refresh controller A69 cannot respond to Read and Write Commands from the bus master. This condition persists as long as the MPRO/ signal is true.

When the bus master deactivates MPRO/, memory protect latch A103-9 is reset at T520 of the following refresh cycle (when busy latch A53-6 is reset). With A103-9 reset, the control logic is again able to respond to commands from the bus master.

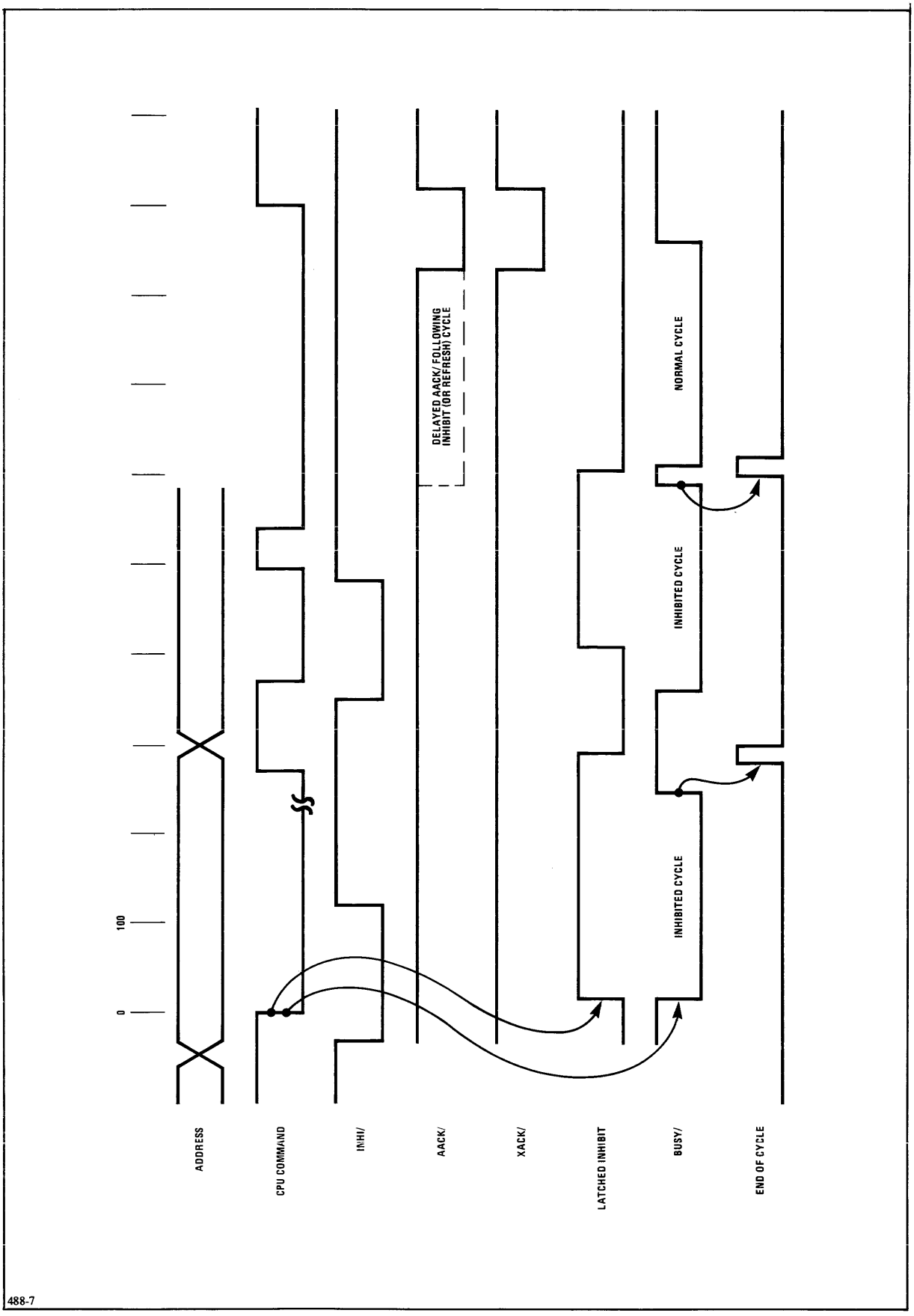


Figure 3-4. Inhibit Timing

CHAPTER 4
SERVICE INFORMATION

4-1. INTRODUCTION

This chapter provides service diagrams and service and repair assistance instructions for the iSBC 032/048/064.

4-2. SERVICE DIAGRAMS

The iSBC 032/048/064 parts location and schematic diagrams are given in figure 4-1 and 4-2, respectively. Each sheet of the schematic diagram is marked with grid coordinates. Signals that transverse from one sheet to another are assigned grid coordinates at both the signal source and destination. For example, the grid coordinates 2ZD8 locate a signal source or destination on sheet 2 in Zone D8.

Both active-high (positive-true) and active-low (ground-true) signals appear on the schematics. To avoid confusion as to the meaning of these signals, the following convention is used. The mnemonic for each active-low signal is terminated by a slash (e.g., WE/). Such references indicate that the signal level is low when the condition is true (active). A mnemonic without a slash (e.g., CASTM) refers to an active-high signal. These references indicate that the signal level is high when the condition is true (active).

4-3. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the MCD Technical Support Center in Santa Clara, California at one of the following numbers:

Telephone:

From Alaska or Hawaii call –
(408) 987-8080
From locations within California call toll free –
(800) 672-3507
From all other U.S. locations call toll free –
(800) 538-8014

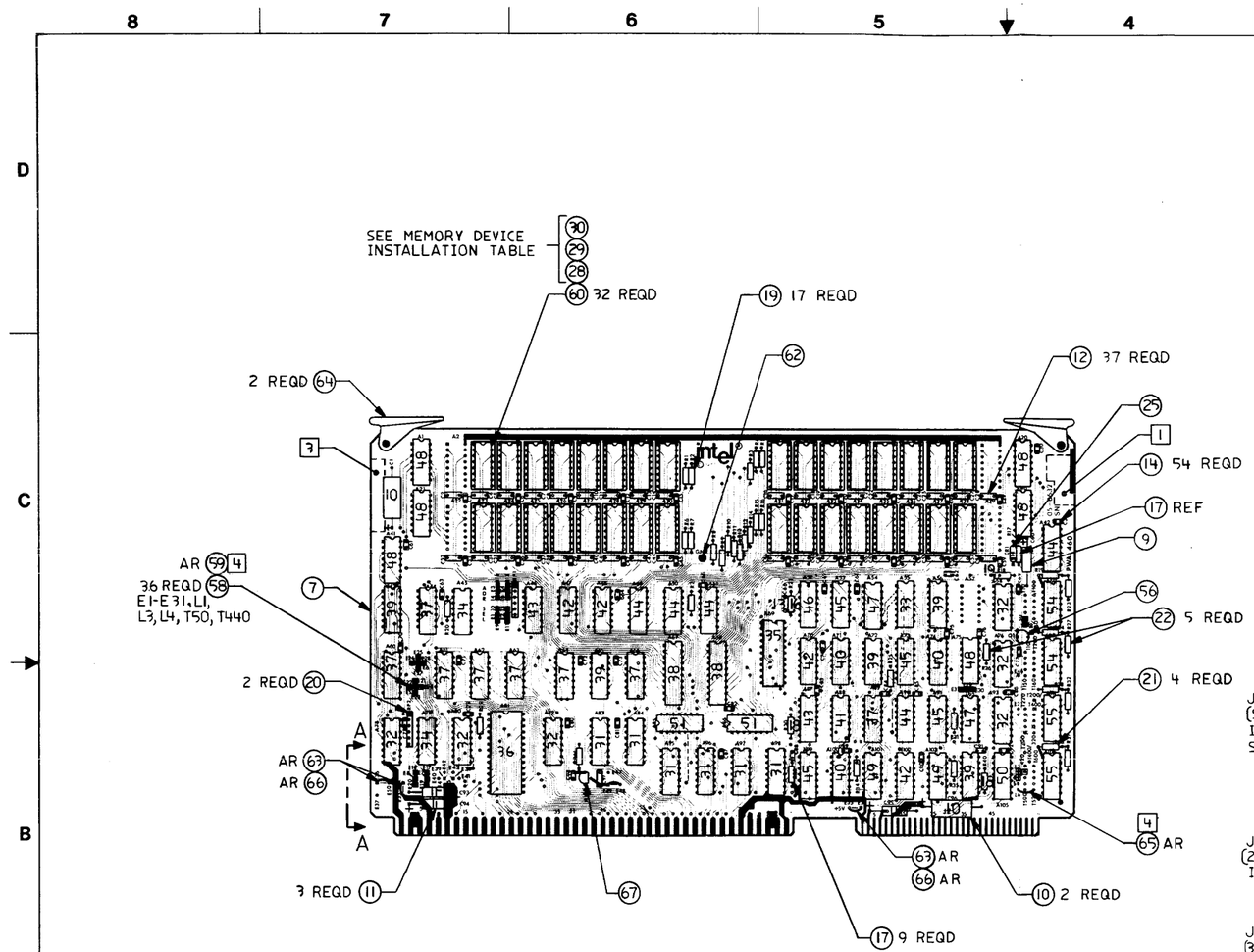
TWX: 910-338-0029
TELEX: 34-6372

Always contact the MCD Technical Support Center before returning a product to Intel for service or repair. You will be given a "Repair Authorization Number", shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment from Intel, or if the product is out of warranty, a purchase order is necessary in order for the MCD Technical Support Center to initiate the repair.

In preparing the product for shipment to the MCD Technical Support Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by MCD Technical Support Center personnel.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.



NOTES: UNLESS OTHERWISE SPECIFIED

1. STAMP ASSEMBLY DASH NO., REV LEVEL AND SERIAL NO. APPROX. WHERE SHOWN WITH CONTRASTING INDELIBLE INK
2. ASSEMBLE PER INTEL SPECIFICATION 99-0007-001.
3. STAMP MCD PART NO. APPROXIMATELY WHERE SHOWN WITH CONTRASTING INDELIBLE INK AS PER TABLE BELOW

MCD MARKING REQUIREMENTS		
MSD PART NO. DASH NO.	VERSION	MCD PART NO.
000	64K	1288-01
001	32K 2117	1293-01
002	48K 2109L	1291-01
003	48K 2109H	1291-02
004	32K 2109L	1293-02
005	32K 2109H	1293-03
006	16K 2109L	——
007	16K 2109H	——

4. INSTALL JUMPERS PER JUMPER/COMPONENT INSTALLATION TABLE.

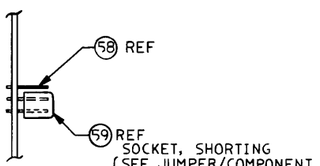
JUMPER COMPONENT/INSTALLATION TABLE											
DASH NUMBER								REF DES	FROM	TO	FUNCTION
000	001	002	003	004	005	006	007				
1	1	1	1	1	1	1	1	W1	E1	E9	0-16K
1	1	1	1	–	–	–	–	W2	E2	E12	16-32K
1	–	1	1	–	–	–	–	W3	E3	E14	32-48K
–	–	–	–	1	1	–	–	W4	E4	E16	16-32K
1	–	–	–	–	–	–	–	W4	E4	E15	48-64K
1	1	1	1	1	1	1	1	W5	E5	E21	0-64K
1	1	1	1	1	1	1	1	W6	E7	E17	0-512K
1	1	1	1	1	1	1	1	W7	E8	E18	0-512K
1	1	1	1	1	1	1	1	W8	E29	E31	ADV WRT CYCLE
1	1	1	1	1	1	1	1	W11	T50	L1	AACK
1	1	–	–	–	–	–	–	W9	E38	E41	2117
1	1	1	1	–	–	–	–	W10	E39	E40	2117
–	–	1	–	1	–	1	–	W9	E38	E45	2109 A6 LO
–	–	–	–	1	–	1	–	W10	E39	E44	2109 A6 LO
–	–	–	1	–	1	–	1	W9	E38	E43	2109 A6 HI
–	–	–	–	–	1	–	1	W10	E39	E42	2109 A6 HI
1	1	1	1	1	1	1	1	W12	T400	L2	XACK
1	1	1	1	1	1	1	1	W13	T440	L3	RAS T.E.
1	1	1	1	1	1	1	1	W14	T440	L4	BUSY T.E.
1	1	1	1	1	1	1	1	W15	T480	L5	CAS T.E.
1	1	1	1	1	1	1	1	W16	T520	L6	ADV WRT GO

JUMPER WITH (SOCKET SHORTING) ITEM 59 ONLY SEE VIEW A-A

JUMPER WITH (24 AWG WIRE) ITEM 63

JUMPER WITH (30 AWG WIRE) ITEM 65

JUMPER WITH (24 AWG WIRE) ITEM 63



VIEW A-A
SCALE: NONE

MEMORY DEVICE INSTALLATION TABLE				
ITEM NO.	DASH NO.	DEVICE DESCRIPTION	REF DES	FUNCTION
28	000	2117	A3-18,A23-38	64K BYTE RAM
28	001	2117	A3-18	32K
29	002	2109L	A23-38	48K
28		2117	A3-18	
30	003	2109H	A23-38	48K
28		2117	A3-18	
29	004	2109L	A3-18,A23-38	32K
30	005	2109H	A3-18,A23-38	32K
29	006	2109L	A3-18	16K
30	007	2109H	A3-18	16K BYTE RAM

REV	E.O. NO.	REL	DATE	DASH NO.	MODEL NO.	USED ON
04						
03	8413					
02	8409					
01	7833					
00	7732					
E	ECS 5-534		4-10-78	000 TO 007	SBC044	NONE

REVISIONS | USED ON

NOTE: UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES, TOLERANCES XX: ± XXX: ± FRACTION: ± ANGLES: ±

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APPR		
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TWX: NO. 05-0632-000-007

Figure 4-1. iSBC 032/048/064 Parts Location Diagram

ADDRESS JUMPER TABLE

JUMPER	FROM	TO	SELECTED BANKS	SELECTED ADDRESS RANGE
16K BYTE BANK PAIRS (2108)				
W1	E1	E9	0,1	0-16K SELECT ONE JUMPER AT LEFT
W1	E3	E13	2,3	
W2	E2	E12	0,1	16K-32K
W2	E4	E16	2,3	
W3	E1	E10	0,1	32K-48K
W3	E3	E14	2,3	
W4	E2	E11	0,1	48K-64K
W4	E4	E15	2,3	
32K BYTE BANK PAIRS (2116)				
W1	E1	E9	0,1	0-32K SELECT TWO JUMPERS AT LEFT
W2	E2	E12		
W1	E3	E13	2,3	
W2	E4	E16		
W3	E1	E10	0,1	32K-64K
W4	E2	E11		
W3	E3	E14	2,3	
W4	E4	E15		
W1	E1	E9	0,1	0-16K AND 48K-64K
W2	E2	E11		
W3	E3	E13	2,3	
W4	E4	E15		
W1	E1	E10	0,1	16K-48K
W2	E2	E12		
W3	E3	E14	2,3	
W4	E4	E16		

HIGH ORDER CARD SELECT ADDRESS JUMPER TABLE

JUMPER	FROM	TO	SELECTED RANGE
W5	E5	E21	0-64K
W5	E5	E22	64-128K
W5	E5	E23	128K-192K
W5	E5	E24	192K-256K
W5	E6	E25	256K-320K
W5	E6	E26	320K-384K
W5	E6	E27	384K-448K
W5	E6	E28	448K-512K
W6	E7	E17	0-512K
W7	E8	E18	
W6	E7	E19	512K-1024K
W7	E8	E20	

USER SELECTABLE OPTIONS

JUMPER	FROM	TO	FUNCTION
W8	E29	E30	DELAYED COMMAND WRT.
W8	E29	E31	ADVANCED COMMAND WRT.
W17	E32	E33	+12V BUS (CUT IF USING BATT. BACK UP)
W18	E34	E35	+5V BUS " "
W19	E36	E37	-5V BUS " "
W20	E36	E50	-5V REG
W21	E49	E47	-10V BUS INTO REG
W22	E49	E48	-12V BUS INTO REG
W23	L1	E51	ADVANCE ACK INHIBIT
W24	L1	T50	ADVANCE ACK ENABLE

RAM COMPONENT TABLE

DASH NO	DEVICE TYPE	CAPACITY	DELETE
000	2116	64K	NONE
001	2116	32K	BANKS 2,3
002	2116+2108 VOL	48K	NONE
003	2116+2108 VOH	48K	NONE
004	2108 VOL	32K	NONE
005	2108 VOH	32K	NONE
006	2108 VOL	16K	BANKS 2,3
007	2108 VOH	16K	BANKS 2,3

USER SELECTABLE COMMAND TO ADVANCE ACKNOWLEDGE DELAY

JUMPER	FROM	TO	DELAY
W12	L1	T50	50 NS
W12	L1	T100	100 NS
W12	L1	T96	130 NS
W12	L1	T200	200 NS
W12	L1	T240	240 NS
W12	L1	T300	300 NS
W12	L1	T340	340 NS
W12	L1	T400	400 NS

TIMING TAP CHART

FROM	TO	FUNCTION
T50	L1	AACK
T400	L2	XACK
T440	L3	RAS TE
T440	L4	BUSY TE
T480	L5	CAS TE
T520	L6	ADV. WR. GO

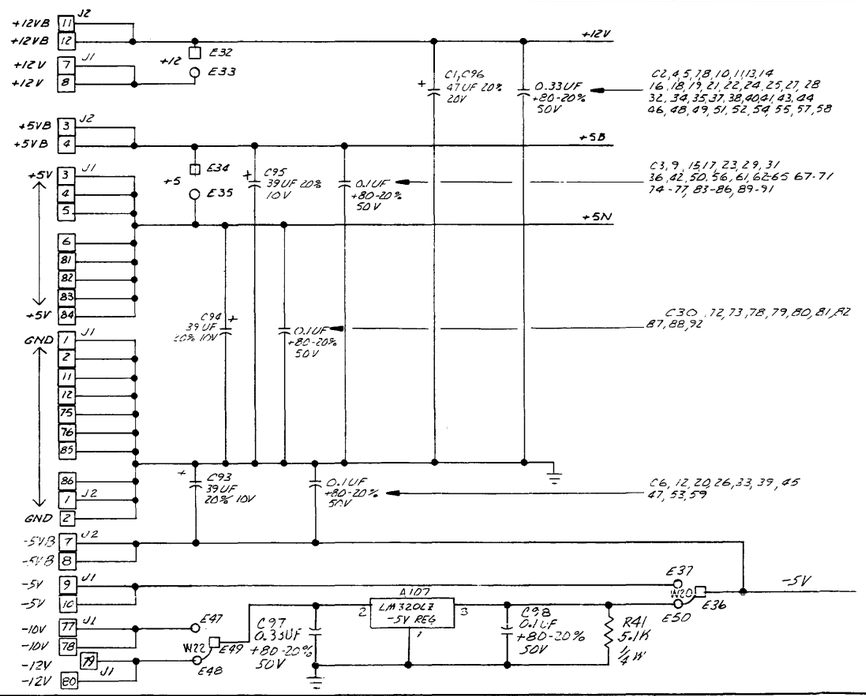
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTER VALUES IN OHMS, 1/4W.
2. ALL CAPACITORS VALUES IN U F.
3. ALL RP DESIGNATES A RESISTOR PACK.

DEVICE TABLE

TYPE	GND	+12V	+5B	+5N	-5V	REF DES	UNUSED OUTPUT PINS
74S11	7	—	14	14	—	A1, A20, A21, A90, A91, A75	A1-B, A20-B, A21-B, A90-6,8 A91-B,12, A75-6
74S20	7	—	14	14	—	A96, A87	A87-6
74S37	7	—	14	—	—	A92, A99, A50, A51, A90	A92-11, A90-6,8
74S40	7	—	14	—	—	A52	—
74S74	7	—	14	14	—	A53, A73, A91, A99	A99-B, 9
74S11A	8	—	16	—	—	A54, A92	—
74S280	7	—	—	14	—	A85, A86	—
74LS373	10	—	—	20	—	A67, A68	—
7436B	8	—	—	16	—	A105	A105-9,11
74S02	7	—	14	—	—	A55	
74S00	7	—	14	14	—	A49, A60, A61, A62 A63, A64, A66, A89	A60-B, A64-B, 11
74S04	7	—	14	14	—	A43, A56, A65, A72 A104	A43-B11, A56-9,12, A65-2,6 A72-2,12, A104-6
74LS04	7	—	14	—	—	A88	A88-6
74S08	7	—	14	—	—	A71, A74, A100	—
74S10	7	—	14	—	—	A47, A48, A70, A102	A70-8
8226	8	—	—	16	—	A83, A84, A95-A98	—
3404	8	—	16	16	—	A58, A76, A78, A80, A82 A93	A58-4, A76-2,4,9,13 A78-6,9,11,13 A80-6,9,11,13
3205	8	—	—	16	—	A45, A79	—
3222	11	—	22	—	—	A69	—
3242	14	—	28	—	—	A81	—
74LS74	7	—	14	—	—	A101, A103	—
2117	16	8	9	—	1	A2-A10, A11-A19, A22-A30 A31-A39	—
1103	16	8	9	—	1	A2-A10, A11-A19, A22-A30 A31-A39	—

REFERENCE DESIGNATIONS

HIGHEST USED	NOT USED
A107	
C98	
CR1	
E51	
L6	
Q1	
R41	R38, 39
RP2	
T600	} REFER TO TABLE
W24	



REV	E.O. NO.	REL	DATE	DASH NO.	MODEL NO.	USED ON
REVISIONS				USED ON		

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DWG NO. 01-0632-000 TO 007

98-0047-000

Figure 4-2. iSBC 032/048/064 Schematic Diagram (Sheet 1 of 6)

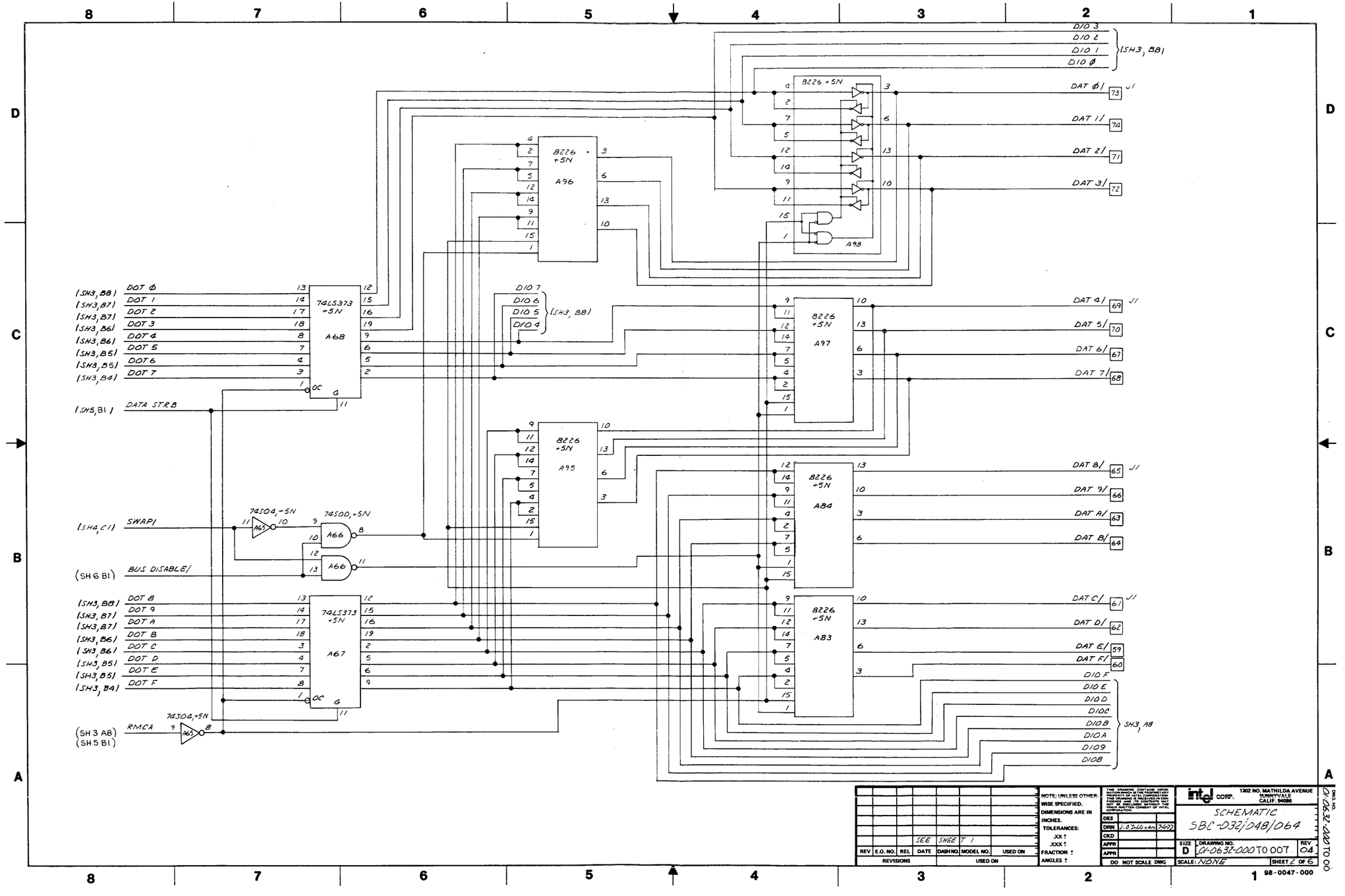

Figure 4-2. iSBC 032/048/064 Schematic Diagram (Sheet 2 of 6)

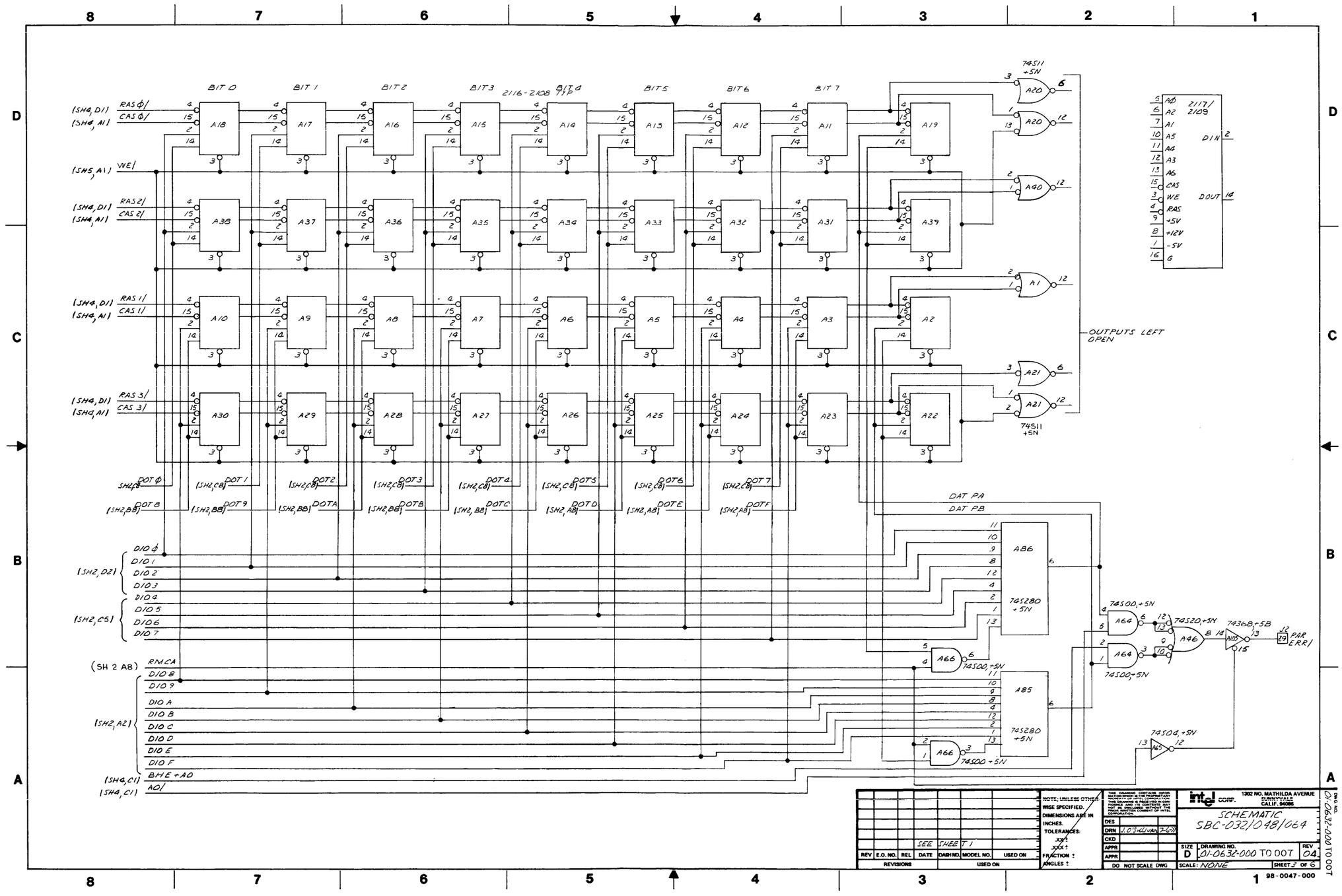

Figure 4-2. iSBC 032/048/064 Schematic Diagram (Sheet 3 of 6)

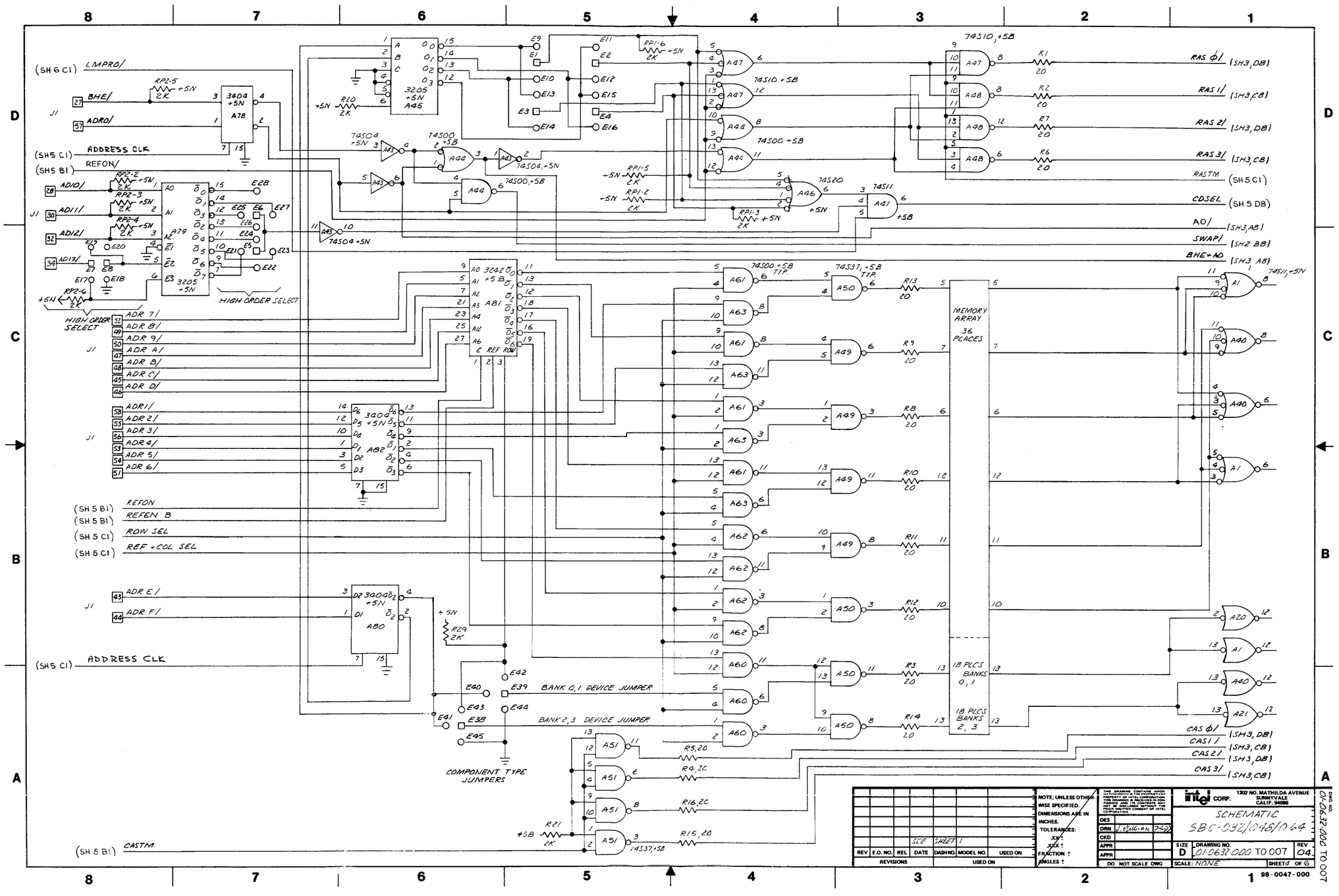

Figure 4-2. iSBC 032/048/064 Schematic Diagram (Sheet 4 of 6)

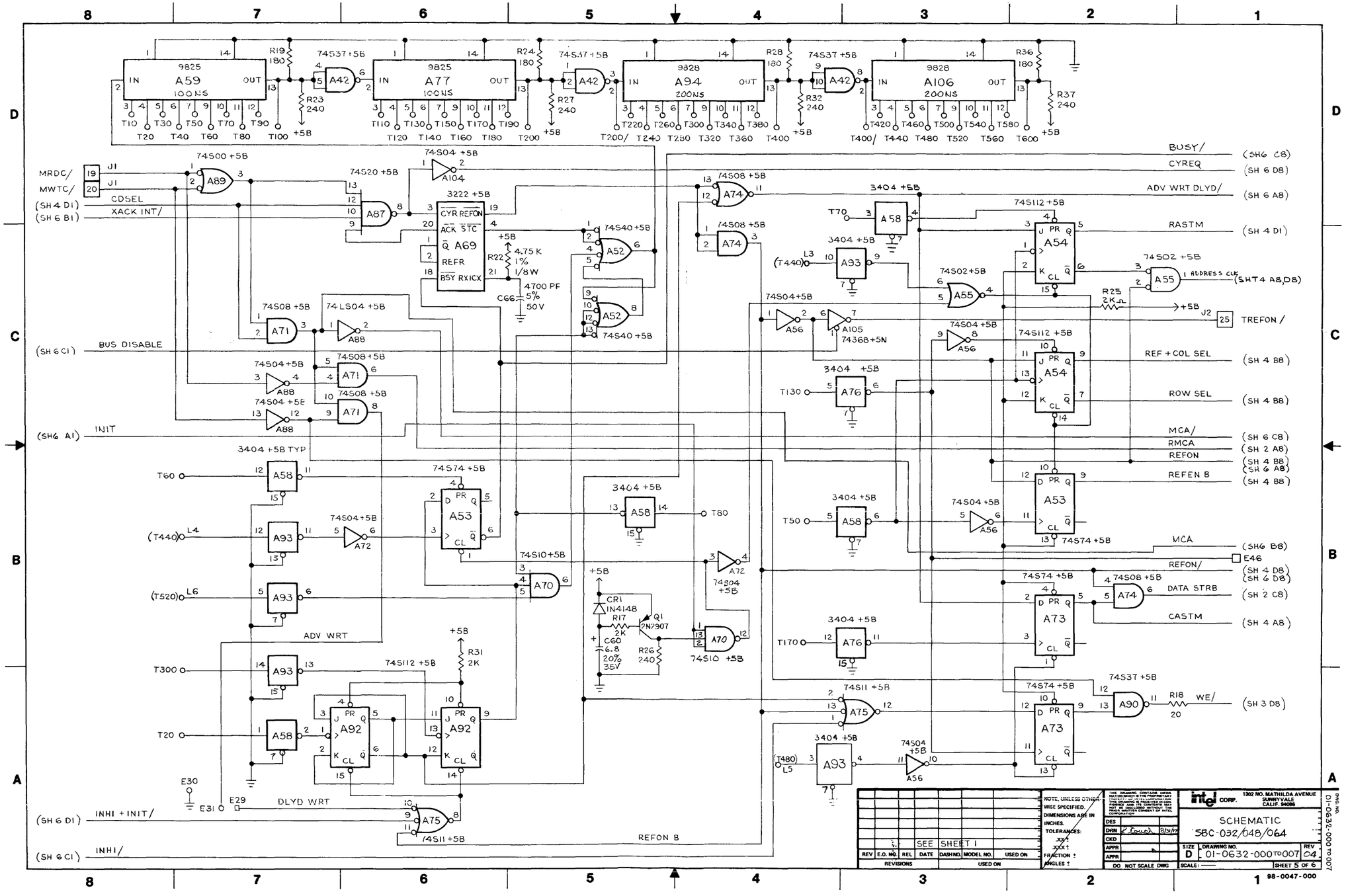

Figure 4-2. iSBC 032/048/064 Schematic Diagram (Sheet 5 of 6)

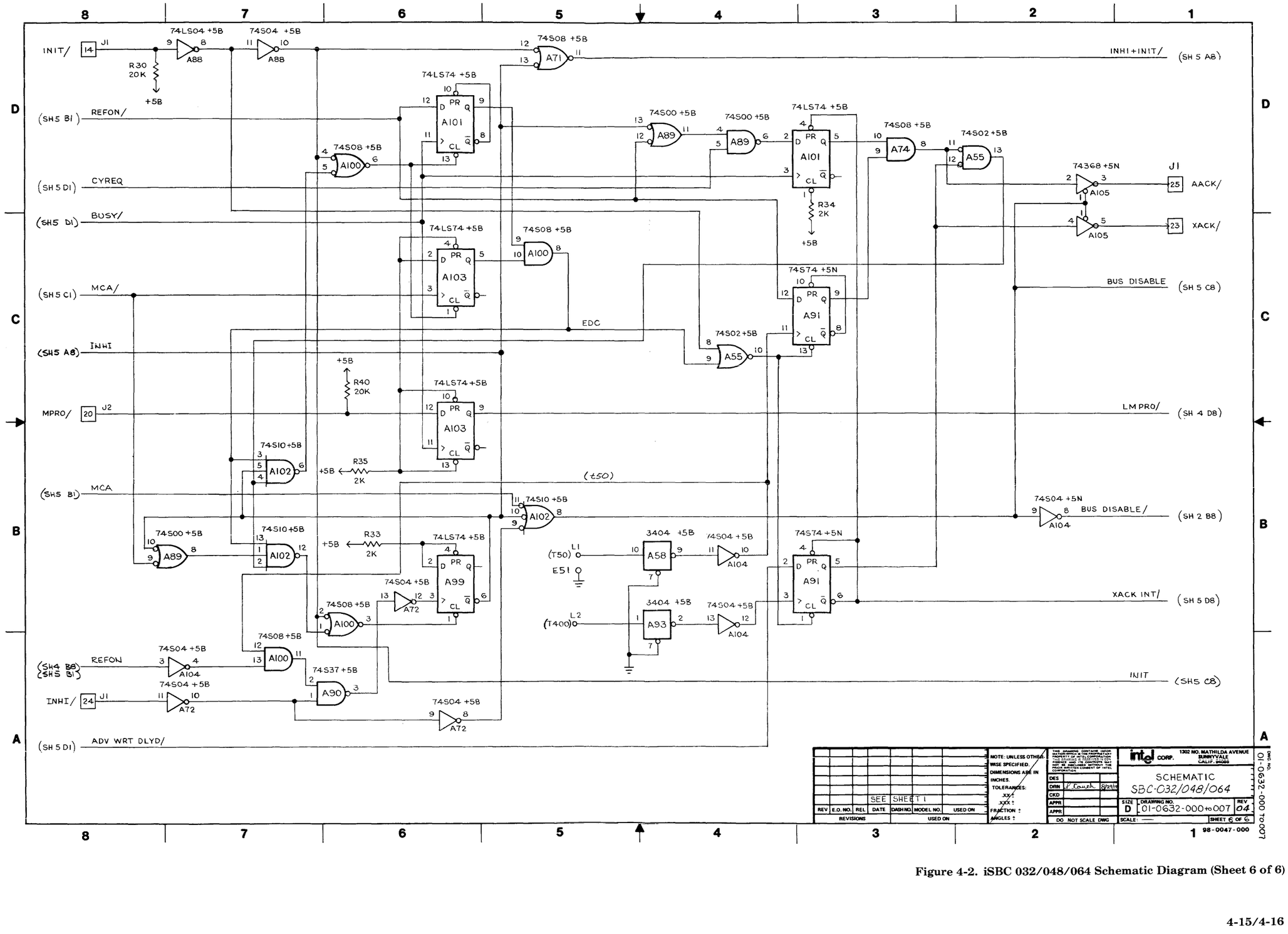

Figure 4-2. iSBC 032/048/064 Schematic Diagram (Sheet 6 of 6)

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