iSBC 80/05
SINGLE BOARD COMPUTER
HARDWARE
REFERENCE MANUAL

Manual Order Number: 9800483-03

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PREFACE

This manual provides general information, installation, programming information, principles of operation, and service information for the Intel SBC 80/05 Single Board Computer. Additional information is available in the following documents:

- *Intel MCS 85 User's Manual,* part no. 121506.
- *Intel 8080/8085 Assembly Language Programming Manual,* part no. 98-301.
- *Intel MULTIBUS Interfacing,* Application Note AP-28.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The SBC 80/05 Single Board Computer, which is a member of Intel's complete line of SBC 80 computer products, is a computer system on a single printed-circuit assembly. The SBC 80/05 includes a central processor unit (CPU), system clock, random access memory (RAM), read-only memory (ROM), one serial and three parallel I/O ports, a programmable timer, priority interrupt and Multibus control logic, and bus expansion buffers.

1-2. DESCRIPTION

The SBC 80/05 Single Board Computer (figure 1-1) is controlled by an Intel 8085A CPU, which includes six 8-bit general-purpose registers and an accumulator. The six general-purpose registers may be addressed individually or in pairs, which allows both single-precision and double-precision operations. The minimum on board execution time is 2.03 microseconds.

The 8085A CPU has a 16-bit program counter which allows direct addressing of up to 65,536 bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all six general-purpose registers. A 16-bit stack pointer controls the addressing of this external stack, which allows subroutine nesting that is bounded only by the system memory size.

Two Intel 8111-A4 RAM chips provide 256 bytes of static read/write memory; an Intel 8155 combination RAM/IO/Timer provides an additional 256 bytes of static read/write memory. Two sockets are provided for installing up to 4K bytes of nonvolatile read-only memory (ROM), which may be added in 2K byte increments using Intel 2716 Ultraviolet Erasable and Reprogrammable ROM's (EPROM's) or 8316E Masked ROM's. Optionally, if only 2K bytes are required, ROM may be added in 1K byte increments using Intel 8708 EPROM's or 8308 Masked ROM's.

Twenty-two programmable parallel I/O lines are implemented using the I/O ports of the Intel 8155 RAM/IO/Timer. The system software is used to configure the I/O lines in any combination of unidirectional input or output ports. The I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O

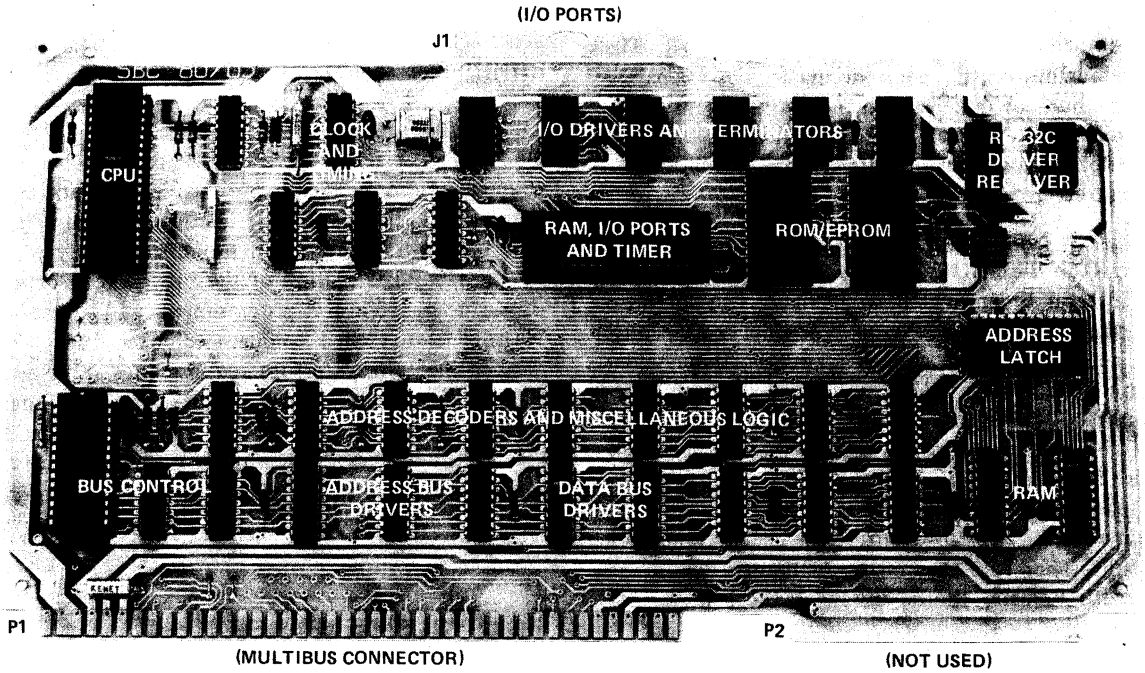

Figure 1-1. SBC 80/05 Single Board Computer

line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 22 programmable I/O lines and single ground lines are brought out to a 50-pin edge connector (J1) that mates with flat, woven, or round cable.

The SBC 80/05 includes the resources for supporting a variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPU's and/or controllers logically sharing systems tasks with communication over the Multibus), the SBC 80/05 provides full bus arbitration control logic. This control logic allows up to three bus masters (i.e., any combination of SBC 80/05. SBC 80/20, DMA controller, diskette controller, etc.) to share the Multibus in serial (daisy-chain) fashion or up to 16 bus masters to share the Multibus using an external parallel priority resolving network.

The Multibus arbitration logic operates synchronously with the bus clock, which is derived from the SBC 80/05, or can be optionally generated by some other bus master. Data, however, is transferred via a handshake between the controlling master and the addressed slave module.. This arrangement allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, the transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high-speed direct memory access (DMA) operations, and high-speed peripheral control, but are by no means limited to these three.

The Intel 8155 RAM/IO/Timer includes a programmable 14-bit interval timer, which is configured by software to meet the system requirements. Whevener a given time delay is needed, software commands to the timer select the desired operating mode. The current contents (present count) of the timer counter and the timer mode bits may be read at any time during system operation. There are four timer operating modes:

a. Timer Out goes low during the second half of count. Therefore, the count loaded in the Count Length Register should be twice the timeout desired.

b. Timer Out remains high until the first half of the count has been completed, and goes low for the second half of the count. The count length is automatically reloaded when the terminal count is reached.

c. A single low pulse is generated upon reaching the terminal count; this function is useful for generating real-time clocks.

d. A Divide-by-N Counter generates a repetitive Timer Out low pulse; a new pulse train is initiated every time the terminal count is reached.

Serial I/O capability is provided through the Serial Input Data (SID) and Serial Output Data (SOD) functions of the CPU. These functions are controlled exclusively by software through the execution of RIM and SIM instructions. The baud rate for the serial I/O interface is determined by the system time available for the execution of serial I/O support software. Hence, the maximum baud rate supported by the SBC 80/05 is solely dependent on the overall system real-time software requirements. Serial I/O signals are TTL compatible and sockets are provided on the board for optional installation of RS232C line drivers and receivers.

The SBC 80/05 provides jumper-selectable interrupts to the four interrupt request inputs of the 8085 CPU (i.e., TRAP, RST 7.5, RST 6.5, and RST 5.5), each of which generates a unique memory address. A jump (JMP) instruction at each of these addresses can provide the linkage to an interrupt handling subroutine for the appropriate interrupting device. All interrupts except TRAP may be masked by software. The TRAP interrupt should be used for conditions (such as a power-down sequence) that require the immediate attention of the CPU. Caution should be exercised when using the TRAP interrupt in conjunction with the maskable interrupts. For further details, refer to Chapter 3 of this manual.

SBC 80/05 interrupts may originate from 12 sources. One jumper-selectable interrupt request can be automatically generated by the programmable interval timer upon completion of the selected function. Two jumper-selectable interrupt requests can be automatically generated by the I/O ports section of the 8155 when Ports 01 and 02 of the 8155 are programmed to operate in the "latched and strobed" mode. (Refer to Chapter 3.) Nine jumper-selectable interrupt request lines are available to the user for direct interfaces to user-designated peripheral devices, one via the I/O edge connector and eight via the Multibus. The 12 interrupt request lines may each be selectively routed to any of four 8085A CPU interrupt inputs (i.e., TRAP, RST 7.5, RST 6.5, and RST 5.5) via jumpers.

1-3. SYSTEM EXPANSION

Processing power, memory, and I/O capacity may be increased in SBC 80/05 based systems with single +5V

power by adding standard Intel expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the SBC 310 High-Speed Mathematics Unit. Memory for these systems may be expanded using the SBC 094 4K Byte CMOS RAM board. Input/output capacity may be increased by adding SBC 80 Digital I/O boards. In addition to these expansion options, SBC 80/05 based systems equipped with multiple voltages may be expanded with many memory and I/O options. Memory may be expanded to 65,536 bytes by adding user-specified combinations of RAM boards, PROM boards, or combination boards. Input/output capacity may also be increased by adding SBC 80 Analog I/O boards. Mass storage may be added by selecting the appropriate single or double-density diskette subsystem. Modular expandable backplanes and cardcages are available to support multiboard systems.

1-4. SYSTEM SOFTWARE DEVELOPMENT

The development cycle of SBC 80/05 based products may be significantly reduced using the Intellec Microcomputer Development System. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of SBC 80/05 system software. An optional Diskette Operating System provides a relocating macroassembler, relocating loader and linkage editor, and a Library Manager. A unique In-Circuit Emulator (ICE-85) option provides the capability of developing and debugging software directly on the SBC 80/05.

Intel's high-level programming language, PL/M, is also available as a resident Intel Microcomputer Development System option. PL/M provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs for a given application.

1-5. EQUIPMENT SUPPLIED

The following is supplied with the SBC 80/05 Single Board Computer:

a. Schematic diagram, dwg no. 2001600

1-6. EQUIPMENT REQUIRED BUT NOT SUPPLIED

Because the SBC 80/05 is designed to satisfy a variety of applications, the user must purchase and install only those components required to satisfy his particular needs. A list of components required to configure all the intended applications of the SBC 80/05 is provided in table 2-1.

1-7. SPECIFICATIONS

Specifications of the SBC 80/05 Single Board Computer are listed in table 1-1.

Table 1-1. Specifications

WORD SIZE	
Instruction:	8, 16, or 24 bits.
Data:	8 bits.
CYCLE TIME:	2.03 μsec ±0.1% for fastest executable instruction; i.e., four clock cycles.
MEMORY ADDRESSING	
On-Board ROM/EPROM:	0000-0FFF.
On-Board RAM:	3E00-3FFF.
MEMORY CAPACITY	
On-Board ROM/EPROM:	4K bytes with Intel 8316E ROM's or 2716 EPROM's; 2K bytes with Intel 8308 ROM's or 8708 EPROM's.
On-Board RAM:	512 bytes.
Off-Board Expansion:	Up to 65K bytes (less on-board memory) in any combination of RAM, ROM, and EPROM.
I/O ADDRESSING:	On-board I/O addressing of parallel I/O ports are as follows:

Port	8155 Command/ Status	8155 Port 01	8155 Port 02	8155 Port 03	8155 Timer Low-Order Byte	8155 Timer High-Order Byte
Address	00	01	02	03	04	05

Table 1-1. Specifications (Continued)

PARALLEL I/O CAPACITY: 22 programmable lines (from the three 8155 I/O ports); can be expanded to 1102 programmable lines by using optional SBC 80 I/O boards.

SERIAL I/O PORT: SID and SOD functions of the 8085A CPU are used for serial I/O communication controlled by software through RIM and SIM instructions. Baud rate is determined by system time available for serial I/O handling. On-board timer may be used to greatly ease serial I/O timing requirements.

INTERRUPTS: Four-level interrupt routed to 8085A CPU interrupt inputs. Each interrupt automatically vectors the processor to a unique memory location.

Interrupt Input	Memory Address	Priority	Type
TRAP	0024	Highest	Non-Maskable
RST 7.5	003C	2nd	Maskable
RST 6.5	0034	3rd	Maskable
RST 5.5	002C	Lowest	Maskable

NOTE: Caution must be exercised in the use of the TRAP interrupt when utilized concurrently with maskable interrupts (i.e., RST 7.5, RST 6.5 and RST 5.5). For further details, refer to Chapter 3.

TIMER

Input Freq. Reference: 122.88 kHz ±0.1% (8.14 μsec period nominal).

Outputs: Operating modes vs output frequencies and timing intervals:

Function	Timer/Counter	
	Minimum	Maximum
Programmable Pulse	8.14 μsec	66.67 msec
Square Wave Rate Generator	7.50 Hz	61.44 kHz
Rate Generator	7.50 Hz	61.44 kHz
Programmable Strobe Indication	8.14 μsec	133.33 msec

INTERFACE COMPATIBILITY: All TTL compatible; sockets provided for RS232C line drivers and receivers.

MULTIBUS CLOCK: 9.8 MHz ±0.1% derived from on-board crystal; clock may be generated externally.

POWER REQUIREMENTS: DC power requirements depend on user-installed options. Refer to table 2-2.

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0° to 55°C (32° to 131°F).

Relative Humidity: To 90% without condensation.

PHYSICAL CHARACTERISTICS

Width: 30.48 cm (12.00 inches).

Height: 17.15 cm (6.75 inches).

Thickness: 1.27 cm (0.50 inch).

Weight: 340 gm (12 ounces).

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

The chapter provides instructions for preparing the SBC 80/05 Single Board Computer for use in a multiple master bus system and for use in a single board environment. It is advisable that the contents of Chapters 1 and 3 be fully understood before beginning the configuration and installation procedures contained in this chapter.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel Technical Support Center (see paragraph 5-3) to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be reshipped.

2-3. INSTALLATION CONSIDERATIONS

Important installation and interfacing criteria for fabricating an SBC 80/05 computer-based system and for using the SBC 80/05 in a single-board environment are presented in following paragraphs.

2-4. USER-FURNISHED COMPONENTS

Because the SBC 80/05 is designed to satisfy a variety of applications, the user must purchase and install only those components required to satisfy his particular needs. A list of components required to configure all the intended applications of the SBC 80/05 is provided in table 2-1. Table 2-2 lists alternative types and vendors of the connectors referenced in table 2-1.

2-5. POWER REQUIREMENTS

Power requirements for the SBC 80/05 are listed in table 2-3. Note that the power requirements not only depend on the intended application, but on the user-installed EPROM type as well. Note also that filter capacitors must be furnished and installed by the user if any power supply other than a +5V supply is required.

2-6. COOLING REQUIREMENT

The SBC 80/05 dissipates 196 gram-calories/minute (0.79 BTU/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F).

2-7. PHYSICAL DIMENSIONS

Physical dimensions of the SBC 80/05 are as follows:

a. Width:	30.48 cm (12.00 inches)
b. Height:	17.15 cm (6.75 inches)
c. Thickness:	1.27 cm (0.50 inch)

2-8. COMPONENT CONFIGURATION

Instructions for installing various components on the SBC 80/05 to satisfy a particular configuration requirement are presented in following paragraphs. The following are recommended for installing those components that must be soldered in place:

a. Ungar (or equivalent) soldering iron with a 40W heating element and pencil-shaped tip.

b. Multicore rosin flux 60/40 solder.

After the component is soldered in place, clean all traces of flux from the soldered area using Freon TF Degreaser (or equivalent).

2-9. RS232C SERIAL INPUT/OUTPUT

The SBC 80/05 can employ RS232C or TTL level serial I/O operation, but not both simultaneously. If RS232C serial I/O operation is to be used, install the line driver, line receiver, and connector as described in following paragraphs.

Table 2-1. User-Furnished and Installed Components

ITEM NO.	ITEM	DESCRIPTION	USE
1	SBC 604	Modular Backplane and Card-cage. Includes four slots with bus terminators. (See figure 5-3.)	Provides power inputs and Multibus interface between SBC 80/05 and three additional boards in a multiple board system.
2	SBC 614	Modular Backplane and Card-cage. Includes four slots without bus terminators. (See figure 5-4.)	Provides four-board extension of SBC 604.
3	Connector (mates with P1)	See Multibus connector details in table 2-2.	Power inputs and Multibus interface. Not required if (1) SBC 80/05 is installed in an SBC 604/614 or (2) if SBC 80/05 is used in a single-board configuration that needs +5V power only (see item 6).
4	Connector (mates with J1)	See parallel I/O connector details in table 2-2.	Interfaces parallel I/O devices and TTL level serial I/O device to SBC 80/05.
5	Connector J2	Male and female connector required. See table 2-2 for description.	Interfaces RS232C *or* TTL-level serial I/O device to SBC 80/05. (Either RS232C or TTL level serial I/O can be accommodated, but not both.)
6	Connector J3	Male and female connector required. See table 2-2 for description.	Provides alternative +5V power input when SBC 80/05 is used in a single-board configuration that needs +5V power only. (Refer to table 2-3.)
7	EPROM's or ROM's	One or two each of one of the following types of EPROM's or ROM's: Intel 2716 (2K x 8) or 8708 (1K x 8) EPROM	On-board UV erasable PROM's for program development
		Intel 8316E (2K x 8) or 8308 (1K x 8) ROM	On-board masked ROM's for dedicated program

Table 2-1. User-Furnished and Installed Components (Continued)

ITEM NO.	ITEM	DESCRIPTION	USE
8	RS232C line driver RS232C line receiver	Type: National DS1488 or TI SN75188 Type: National DS1489 or TI SN75189	Transmitting and receiving serial I/O data to and from RS232C device.
9	Line Driver	Type / Current: SN7403 I,OC — 16mA SN7400 I — 16mA SN7408 NI — 16mA SN7409 NI,OC — 16mA Types selected as typical; I = inverting, NI = non-inverting, and OC = open collector.	Requires two line driver IC's for each parallel output port. (Requires only one line driver IC for Port 03 if Port 03 is to be used as control signals for Ports 01 and 02.)
10	I/O Terminators	Intel SBC 901 Divider or SBC 902 Pull-Up: SBC 901: +5V, 220, 330 SBC 902: +5V, 1K	Requires two 901's or two 902's for each parallel input port. (Requires only one 901 or 902 for Port 03 if Port 03 is to be used as control signals for Ports 01 and 02.)
11	Capacitors	See table 2-3.	Required only if power supply other than +5V supply is needed.

2-10. LINE DRIVER/RECEIVER. As specified in table 2-1 (item 8), a line driver and a line receiver must be installed to accommodate RS232C serial I/O operation. Refer to figure 5-1 and install a type 1488 line driver in IC socket A11. (Orient pin 1 of 1488 adjacent to capacitor C6.) Install a type 1489 line receiver in IC socket A10. (Orient pin 1 of 1489 adjacent to capacitor C5.)

2-11. CONNECTOR. As specified in table 2-1 (item 5), connector J2 must be installed to interface the RS232C serial I/O device to the SBC 80/05. Solder this 7-pin male connector in position as shown in figure 5-1 (grid reference ZD3).

2-12. TTL LEVEL SERIAL INPUT/OUTPUT

The SBC 80/05 can employ RS232C or TTL level serial I/O operation, but not both simultaneously. Provision is made on connector J1 for interfacing the parallel I/O ports and the TTL level serial I/O device. If using connector J1 for both functions is impractical, connector J2 must be installed. Refer to table 2-1 (item 5). Solder this 7-pin male connector in position as shown in figure 5-1 (grid reference ZD3).

2-13. PARALLEL INPUT/OUTPUT PORTS

Parallel I/O Ports 01 and 02 must be individually configured as either a dedicated input port or a dedicated output port. Port 03 may also be configured as either a dedicated input port or a dedicated output port, or used as control signals for Ports 01 and 02 when these ports are to be used in the strobed input or strobed output mode. For use as a dedicated output port, line drivers (table 2-1, item 9) must be installed; for use as a dedicated input port, I/O terminators (table 2-1, item 10) must be installed. The following six IC sockets (two for

Table 2-2. User-Furnished Connector Details

Function	No. of Pairs/ Pins	Centers (Inches)	Connector Type	Vendor	Vendor Part No.	Intel Part No.
Parallel I/O Connector (J1)	25/50	0.1	Flat Crimp	3M AMP Ansley SAE	3415-0001 88083-1 609-5015 S06750 Series	102211-003
Parallel I/O Connector (J1)	25/50	0.1	Soldered	GTE Sylvania Masterite Micro Plastics Viking	6AD01-25-1A1-DD NDD8GR25-DR-H-X MP-0100-25-DP-1 3KH25/9JN5	102237-001
Parallel[1] I/O Connector (J1)	25/50	0.1	Wire Wrap	Viking TI ITT Cannon	3KH25/JND5 H421011-25 EC4A050A1A	NA
Multibus[1] Connector (P1)	43/86	0.156	Soldered PCB Mount	Elfab Viking	BS1562043PBB 2KH43/9AMK12	102247-001
Multibus[1,2] Connector (P1)	43/86	0.156	Wire Wrap No Ears	Edac Elfab	337-086-0540-201 BW1562D43PBB	102248-001
Serial I/O (J2)	0/7	0.156	Wire Crimp	Molex[3] Molex[3] AMP[4] AMP[1,4]	09-66-1071 male 09-50-7071 female 87194-6 male 3-87025-4 female	N/A
Unregulated +5V (J3)	0/2	0.156	Wire Crimp	Molex[3,5] Molex[3,5] AMP[4,5] AMP[1,4,5]	09-66-1021 male 09-50-7071 female 89194-1 male 2-87025-5 female	N/A

Notes:
[1]Connector heights are not guaranteed to conform to OEM packaging equipment.
[2]Wirewrap pin lengths are not guaranteed to conform to OEM packaging equipment.
[3]Pin Part number is 08-50-0106; key part number is 15-04-0219.
[4]Pin part number is 87023-1; key part number is 87116-2.
[5]Connector J3 does not accept key.
[6]Connector numbering convention may not agree with board connector numbers.

each port) are provided to accommodate the line drivers and I/O terminators:

Parallel I/O Port No.	IC Sockets	Figure 5-1 Grid Ref
01	A6, A7	ZD5, ZD4
02	A4, A5	ZD6, ZD5
03	A8, A9	ZD4, ZD4

If Port 03 is to be used as control signals for Ports 01 and 02, install a line driver in socket A8 and an I/O terminator in socket A9.

2-14. INPUT PORT TERMINATORS. Refer to table 2-1 (item 10) and notice that each parallel input port requires either two Intel SBC 901 Divider IC's or two SBC 902 Pull-Up IC's. Plug terminators into the appropriate IC sockets. Ensure that each IC is installed so that pin 1 is oriented toward connector J1 on the upper edge of the board.

2-15. OUTPUT PORT DRIVERS. Table 2-1 (item 9) lists four typical types of IC's which may be selected as line drivers depending on the user's application. Two driver IC's are required for each dedicated output port. Ensure that each IC is installed so that pin 1 is oriented toward connector J1 on the upper edge of the board.

2-16. READ-ONLY MEMORY

Sockets are provided to accommodate either two EPROM's or two ROM's as specified in table 2-1 (item 7). Plug EPROM's or ROM's in IC locations A16 and A17 (figure 5-1 grid coordinates C4). Ensure that each EPROM or ROM is installed so that pin 1 is oriented toward connector J1 on the upper edge of the board. Refer to paragraph 2-17 for installation of filter capacitors.

NOTE

If only one EPROM or ROM chip is being installed (i.e., a 1K or 2K configuration), install the one chip in socket A17. Socket A17 accommodates the lower addresses 0000-03FF for 1K chips and 0000-07FF for 2K chips.

2-17. POWER SUPPLY FILTERS

Filter capacitors must be installed if a power supply other than a +5V supply is required. Capacitors that must be installed by the user are specified in table 2-3. Refer to figure 5-1 and install the capacitors as follows:

Component	Supply	Capacitors	Figure 5-1 Grid Ref
RS232 Drivers	-12V	C26*	ZB5*
	+12V	C7, C24*	ZD3, ZB8*
Intel 8708 EPROM's	+12V	C11, C24*	ZC3, ZB8*
	-5V	C12, C23*	ZD3, ZB8*

* Observe polarity as shown in figure 5-1.

2-18. ALTERNATIVE +5V INPUT

Connector J3 (table 2-1, item 6) provides an alternative, economical means of inputting +5V power to the SBC 80/05. Note that connector J3 is to be installed only if the SBC 80/05 is used in a single-board configuration (i.e., the Multibus is not required) and no power other than +5V power is required. Install connector J3 as shown in figure 5-1 (grid reference B8). Pin 2 (adjacent to bus controller A19) is the +5V input; pin 1 is ground.

2-19. JUMPER CONFIGURATION

The SBC 80/05 jumper-selectable options are listed and described in table 2-4. Grid references are provided to locate each jumper on the parts location diagram (figure 5-1) and schematic diagram (figure 5-2). Grid references to figure 5-2 are four alphanumeric characters; for example, grid reference 3ZB3 signifies sheet 3 Zone B3.

Carefully study table 2-4 while making reference to figure 5-2 and configure each jumper (or jumper combination) as required. With the exception of jumper pad W5 (CPU interrupts) and jumper pad W9 (Multibus interrupts), the information presented in table 2-4 is considered adequate to properly configure the SBC 80/05 for your particular application. Clarification of jumper pads W5 and W9 is presented in paragraphs 2-20 through 2-24.

2-20. CPU INTERRUPTS

As described in table 2-4, jumper pad W5 is used for connecting selected interrupts to the CPU: TRAP, RST 7.5, RST 6.5, and RST 5.5. The TRAP interrupt (highest priority) is both edge *and* level sensitive and the RST 7.5 interrupt (second highest priority) is rising-edge sensitive. The RST 6.5 and RST 5.5 interrupts are both high-level sensitive; RST 5.5 is the lowest priority. For purpose of examples, jumper pad W5 is illustrated in figure 2-1.

2-21. TRAP INTERRUPT. The TRAP interrupt, which is not maskable, is jumpered at the factory to GND (ground) to prevent the possibility of false interrupts from being generated by noise spikes. Since this interrupt is non-maskable, cannot be disabled by the program, and has the highest interrupt, it may be used to detect catastrophic system errors such as a power failure or bus failure. The logic for detecting such catastrophic system errors must be developed by the system designer and preferably input to the SBC 80/05 CPU via the Multibus interrupt line. (Refer to paragraph 2-24.)

2-22. RST 7.5 INTERRUPT. The RST 7.5 interrupt is jumpered at the factory to the TMR (Timer) output of the 8155. It is recommended that the jumper remain in this position because the RST 7.5 interrupt is rising-edge sensitive and the 8155 outputs a single ground-true pulse when the terminal count is reached. The trailing (rising) edge of this pulse is used to trigger the RST 7.5 interrupt.

Table 2-3. Power Requirements

SUPPLY	MAXIMUM CURRENT	COMMENTS
+5V ±5%	I_{CC} = 1.8A	With no ROM/EPROM or parallel I/O ports.
	I_{CC} = 2.65A	With two Intel 2716 EPROM's (or 8316E ROM's) and six Intel SBC 901 or SBC 902 I/O terminators in the low state. See table 2-1 (items 7 and 10).
−5V ±5%	I_{BB} = 90 mA	Required only when Intel 8708 EPROM's (or 8308 ROM's) are used instead of 2716's (or 8316E's). See table 2-1 (items 7 and 11) and notes below.
+12V ±5%	I_{DD} = 137 mA	Required for Intel 8708 EPROM's (or 8308 ROM's) and RS232C line driver and receiver. See table 2-1 (items 7, 8 and 11) and notes below.
−12V ±5%	I_{AA} = 23 mA	Required only for RS232C line driver and receiver. See table 2-1 (items 8 and 11) and notes below.

Notes:

1. If power supply other than +5V supply is required, the user must furnish and install the following capacitors (refer to paragraph 2-17 for details):

   −5V supply: C12, C23
   +12V supply: C7, C11, C24
   −12V supply: C26

2. Capacitor specifications are:

   C7, C11, C12: ceramic, disc, 0.01μF +80 −20%, 25V, Sprague C092B250C1037 or equivalent.
   C23, C24, C26: tantalum, 22 μF ±20%, 15V, Sprague 150D226X9015B2 or equivalent.

3. Installation procedures are given in subsequent paragraphs.

Table 2-4. Jumper-Selectable Options

<table>
<tr><th>JUMPER</th><th>FIG. 5-1 GRID REF</th><th>FIG. 5-2 GRID REF</th><th>DESCRIPTION</th></tr>
<tr><td>W1
W6</td><td>ZC6
ZC7</td><td>3ZB3
2ZD5</td><td>W1 is used in conjunction with W6 to define four modes of resolving bus contention, three of which are for use in multiple master systems. According to the selected mode, the SBC 80/05 can gain access to the Multibus as follows:

Mode 1: Can request Multibus as needed (multiple master system).
Mode 2: Always requesting Multibus (lowest priority in a multiple master sytem).
Mode 3: Programmable override of Multibus (multiple master system). During an override condition, the SBC 80/05 will not relinquish bus control until programmed to do so.
Mode 4: Always overriding Multibus (single master system).

Jumper positions for configuring each of these four modes are as follows (for example, to configure W1 for Mode 3, remove jumpers from positions A-D and B-C and install jumper only in position A-B):
<table>
<tr><th>Jumper</th><th>Mode 1</th><th>Mode 2</th><th>Mode 3</th><th>Mode 4</th></tr>
<tr><td>W1

W6</td><td>*A-D and
*B-C
*A-B</td><td>*A-D and
*B-C
B-C</td><td>A-B
(only)
A-B</td><td>B-C
(only)
A-B</td></tr>
</table>
</td></tr>
<tr><td>W2</td><td>ZC6</td><td>1ZB7</td><td>*B-C: PC3 is used as a Port 03 input/output bit or as a Port 02 interrupt signal depending on how the 8155 is programmed. If the Port 02 strobed input or output mode is used, the INTR PORT 02 signal must be connected to the CPU interrupt input via jumper pad W5.

A-C: Connects INTR PORT 02 to interrupt an alternative system master via jumper pad W9.</td></tr>
<tr><td>W3
W4</td><td>ZC3
ZC3</td><td>3ZA7
3ZA7</td><td>* W3 loaded with jumper block accommodates Intel 2716 EPROM's or 8316E ROM's; W4 loaded with jumper block accommodates Intel 8708 EPROM's or 8308 ROM's. If 2716's or 8316E's are used, leave jumper block installed in W3; if 8708's or 8308's are used, remove jumper block from W3 and reinstall in W4 (refer to paragraphs 2-16 and 2-17).</td></tr>
<tr><td>W5</td><td>ZC8</td><td>1ZB6</td><td>Priority jumper pad for connecting selected interrupts to CPU. The CPU has three maskable interrupts (RST 5.5, RST 6.5, and RST 7.5) and one nonmaskable interrupt (TRAP). These four interrupts are characterized as follows (refer to paragraphs 2-20 through 2-24 for jumper selectable inputs):
<table>
<tr><td>TRAP</td><td>Highest Priority</td><td>Edge and level sensitive.</td></tr>
<tr><td>RST 7.5</td><td>2nd</td><td>Rising-edge sensitive.</td></tr>
<tr><td>RST 6.5</td><td>3rd</td><td>High-level sensitive.</td></tr>
<tr><td>RST 5.5</td><td>Lowest Priority</td><td>High-level sensitive.</td></tr>
</table>
</td></tr>
<tr><td>W7</td><td>ZB7</td><td>2ZC5</td><td>*A-B: Routes Bus Clock signal BCLK/ to the Multibus. Remove this jumper only if some other module is used to generate BCLK/.</td></tr>
<tr><td>W8</td><td>ZB7</td><td>2ZC5</td><td>*A-B: Routes Constant Clock signal CCLK/ to the Multibus. Remove this jumper only if some other module is used to generate CCLK/.</td></tr>
</table>

Table 2-4. Jumper Selectable Options (Continued)

JUMPER	FIG. 5-1 GRID REF	FIG. 5-2 GRID REF	DESCRIPTION
W9	ZB7	1ZC7	Interfaces 80/05 with the eight interrupt request lines (INT0/ through INT7/) on the Multibus. (Refer to paragraph 2-24 for details.)
W10	ZB8	2ZD3	*A-B: Routes Bus Priority Out signal BPRO/ to the Multibus. Remove this jumper only in a multiple master device system employing a parallel priority bus resolution scheme. Refer to paragraph 2-28.
W11	ZB5	3ZD5	*A-B: Routes ground-true Chip Enable signal to Intel 8155 chip. Do not remove jumper from this position.
W12	ZC4	3ZB3	*A-B: PC4 is used as a Port 03 input/output bit or as a Port 02 Buffer Full status bit depending on how the 8155 is programmed. A-C: PC4 used as an RS232C Reader Control output signal.
W13	ZD8	1ZC5	*A-B: Routes output of ÷5 counter to X1 (clock) input of CPU. Do not remove jumper from this position.
*Jumper installed in this position at the factory.			

2-23. RST 6.5 AND 5.5 INTERRUPTS. The RST 6.5 and RST 5.5 interrupts are level sensitive and may be driven from the following interrupt sources:

a. PORT 1 and PORT 2 (from the on-board 8155)

b. EXT 1 (from an external source via connector J1)

c. Multibus interrupt lines (refer to paragraph 2-24).

As shown in figure 2-1, two of these interrupt sources may be jumpered to the J and K inputs of an OR-gate, which in turn may be jumpered to either the RST 6.5 or RST 5.5 interrupt. When this feature is used, the interrupting source must be identified by executing a polling subroutine.

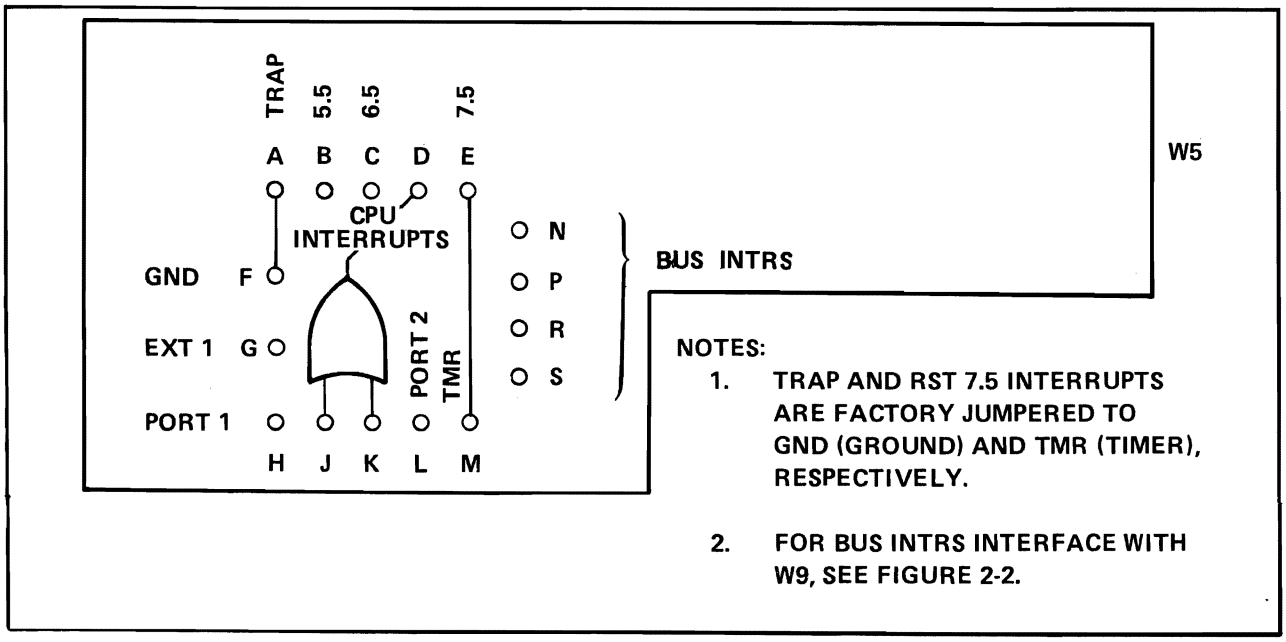

Figure 2-1. CPU Interrupt Input Jumpers

2-24. MULTIBUS INTERRUPTS

The eight Multibus interrupt lines (INT0/ through INT7/) are applied to one side of jumper block W9. (See figure 2-2.) Four of these interrupts may be jumpered and applied (via the inverters) to jumper pad W5 for distribution to the selected CPU interrupts. Refer to table 2-4 and figure 2-2 and note that W2 may be jumpered and applied to W9 through the inverter. This allows the INTR PORT 02 to be connected to an alternative system master by the selected Multibus interrupt line.

2-25. MULTIBUS CONFIGURATION

For system applications, the SBC 80/05 is designed for installation in a standard Intel SBC 604/614 Modular Backplane and Cardcage. (Refer to table 2-1, items 1 and 2.) Alternatively, the SBC 80/05 may be interfaced to a user-designed system backplane by means of an 86-pin connector. (Refer to table 2-1, item 3.) Bus signal characteristics and methods of implementing a serial or parallel priority resolution scheme for resolving bus contention in a multiple master system are described in following paragraphs.

CAUTION

Always turn off the power supply before installing the board in or removing the board from the backplane. Failure to observe this precaution can result in damage to the board.

2-26. SIGNAL CHARACTERISTICS

As shown in figure 1-1, connector P1 provides the means of interfacing the SBC 80/05 to the Multibus. Pin assignments for connector P1 are listed in table 2-5; the functions of the bus signals are described in table 2-6.

AC characteristics of the SBC 80/05 bus interface are presented in table 2-7 and figures 2-3 and 2-4. DC characteristics are specified in table 2-8.

2-27. SERIAL PRIORITY RESOLUTION

In a multiple master system, bus contention can be resolved in an SBC 604 Modular Backplane and Cardcage by implementing a serial priority resolution scheme as shown in figure 2-5. Due to the propagation delay of the BPRO/ signal path, this scheme is limited to a maximum of three devices (masters) capable of acquiring and con-

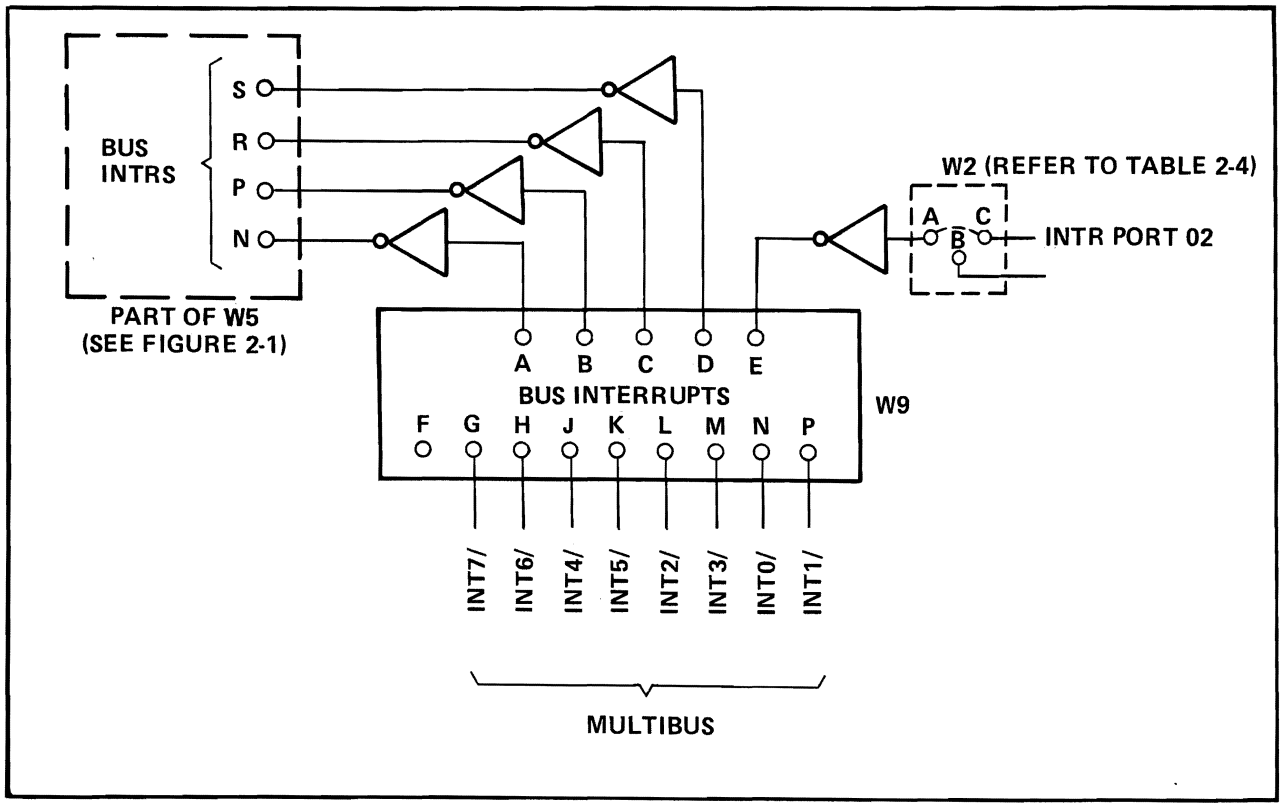

Figure 2-2. Multibus Interrupt Jumpers

trolling the Multibus. In the configuration shown in figure 2-5, the SBC 80/05 installed in slot J2 has the highest priority and is able to acquire the Multibus at any time because its BPRN/ input is enabled (tied to ground) through jumpers B and N on the SBC 604 backplane. (See figure 5-3.) If the master in slot J2 desires control of the Multibus, it drives its BPRO/ output high and inhibits the BPRN/ input to all lower-priority modules. When finished using the bus, the J2 master pulls its BPRO/ output low and passes control to the J3 master. If the J3 master does not desire to control the bus at this time, it pulls its BPRO/ output low and passes control to the J4 master.

The serial priority scheme can be implemented in a user-designed system bus if the chaining of BPRN/ and BPRO/ signals are wired as shown in figure 5-3.

Table 2-5. Connector P1 Pin Assignments

PIN*	SIGNAL	FUNCTION	PIN*	SIGNAL	FUNCTION
1	GND	Ground	44	ADRF/	Address bus
2	GND		45	ADRC/	
3	+5 VDC	Power input	46	ADRD/	
4	+5 VDC		47	ADRA/	
5	+5 VDC		48	ADRB/	
6	+5 VDC		49	ADR8/	
7	+12VDC	Power input	50	ADR9/	
8	+12VDC		51	ADR6/	
9	−5 VDC	Power input	52	ADR7/	
10	−5 VDC		53	ADR4/	
11	GND	Ground	54	ADR5/	
12	GND		55	ADR2/	
13	BCLK/	Bus Clock (9.8304 MHz)	56	ADR3/	
14	INIT/	System Initialize	57	ADR0/	
15†	BPRN/	Bus Priority In	58	ADR1/	
16	BPRO	Bus Priority Out	59		
17	BUSY/	Busy	60		
18	BREQ/	Bus Request	61		
19	MRDC/	Memory Read Command	62		
20	MWTC/	Memory Write Command	63		
21	IORC/	I/O Read Command	64		
22	IOWC/	I/O Write Command	65		
23	XACK/	Transfer Acknowledge	66		
24			67	DAT6/	Data bus
25			68	DAT7/	
26			69	DAT4/	
27			70	DAT5/	
28			71	DAT2/	
29			72	DAT3/	
30			73	DAT0/	
31	CCLK/	Constant Clock (9.8304 MHz)	74	DAT1/	
32			75	GND	Ground
33			76	GND	
34			77		
35	INT6/	Interrupt request line 6	78		
36	INT7/	Interrupt request line 7	79	−12 VDC	Power input
37	INT4/	Interrupt request line 4	80	−12 VDC	
38	INT5/	Interrupt request line 5	81	+5 VDC	Power input
39	INT2/	Interrupt request line 2	82	+5 VDC	
40	INT3/	Interrupt request line 3	83	+5 VDC	
41	INT0/	Interrupt request line 0	84	+5 VDC	
42	INT1/	Interrupt request line 1	85	GND	Ground
43	ADRE/	Address bus	86	GND	

* All unassigned pins are reserved (do not use).
† Connect BPRN/ to ground in single master systems.

Table 2-6. Multibus Signal Functions

SIGNAL	FUNCTIONAL DESCRIPTION
ADR0/-ADRF/	*Address.* These 16 address lines transmit the address of the memory location or I/O port to be accessed. ADRF/ is the most-significant bit.
BCLK/	*Bus Clock.* Used to synchronize bus control circuit on all master boards. BCLK/ from the SBC 80/05 has a period of 101.72 nanoseconds (9.8304 MHz frequency) with a 35-65 percent duty cycle.
BPRN/	*Bus Priority In.* Indicates to a particular master board that no higher priority master board is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	*Bus Priority Out.* In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the master board with the next lower bus priority.
BREQ/	*Bus Request.* Used with a parallel bus priority resolution scheme to indicate that a particular master board requires use of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	*Busy.* Indicates that the bus is in use and prevents all other master boards from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CCLK/	*Constant Clock.* Provides a clock signal of constant frequency (9.8304 MHz) for use by system boards. CCLK/ from the SBC 80/05 coincides with BCLK/ and has a period of 101.72 nanoseconds with a 35-65 percent duty cycle.
DAT0/-DAT7/	*Data.* These eight bidirectional data lines transmit and receive information to and from the addressed memory location or I/O port. DAT7/ is the most-significant bit.
INIT/	*Initialization.* Resets the entire system to a known internal state.
INT0/-INT7/	*Interrupt.* These eight lines are used for system interrupt requests.
IORC/	*I/O Read Command.* Indicates that the address of an I/O port is on the system address lines and that the output of that port is to be read (placed) onto the system data lines.
IOWC/	*I/O Write Command.* Indicates that the address of an I/O port is on the system address lines and that the contents on the system data lines are to be accepted by the addressed port.
MRDC/	*Memory Read Command.* Indicates that the address of a memory location is on the system address lines and that the contents of that location are to be read (placed) onto the system data lines.
MWTC/	*Memory Write Command.* Indicates that the address of a memory location is on the system address lines and that the contents on the system data lines are to be written onto that location.
XACK/	*Transfer Acknowledge.* Indicates that the addressed memory location or I/O port has completed the specified read or write operation. That is, data has been placed onto or accepted from the system data lines.

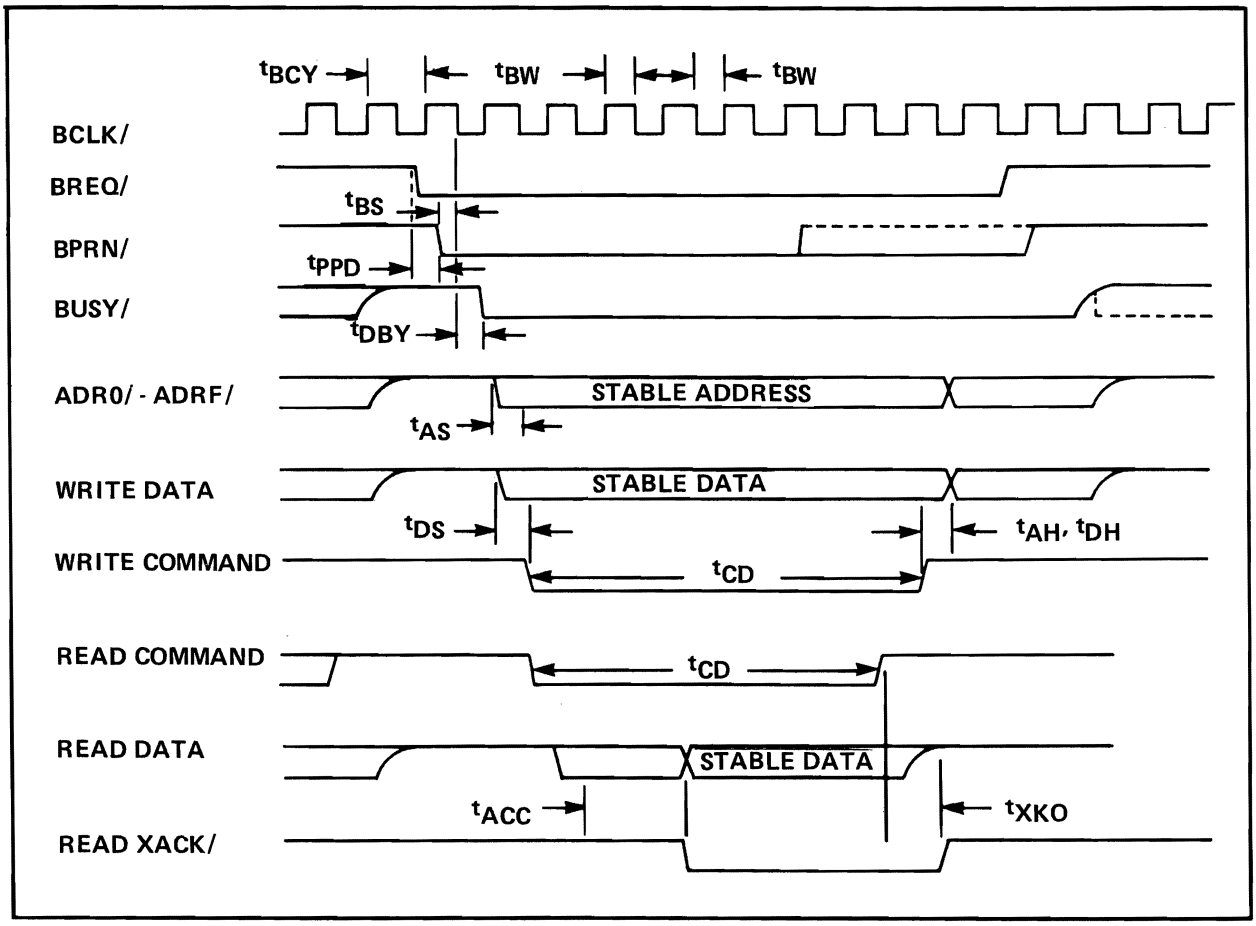

Figure 2-3. SBC 80/05 Bus Exchange Timing

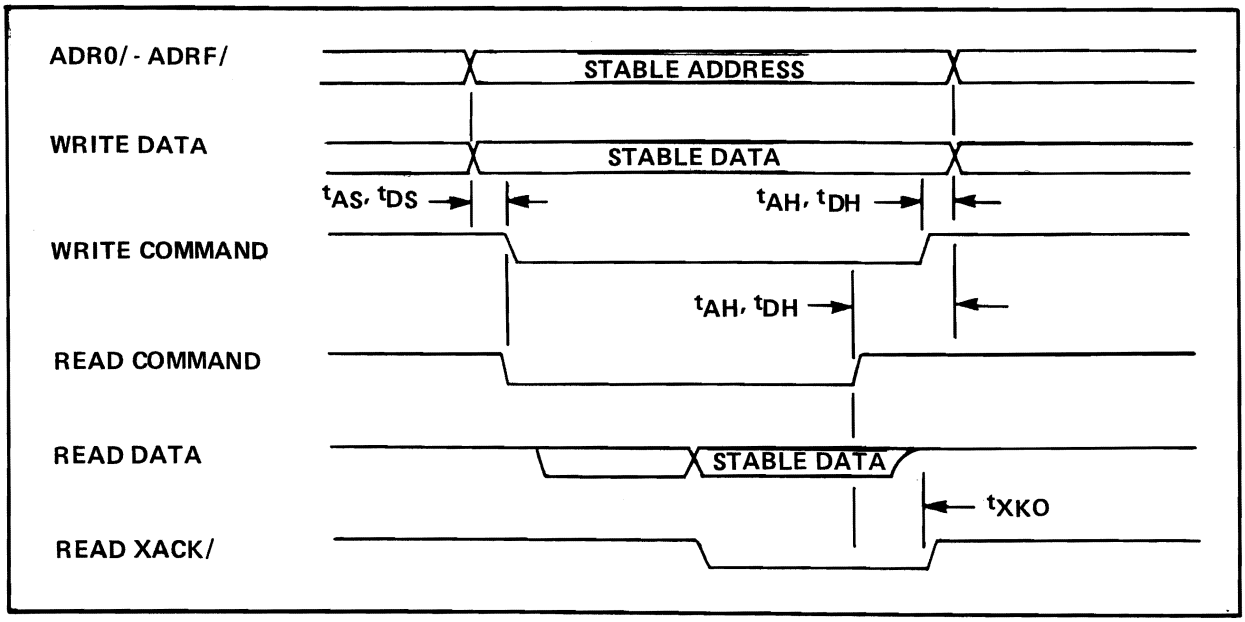

Figure 2-4. SBC 80/05 Bus Control Timing

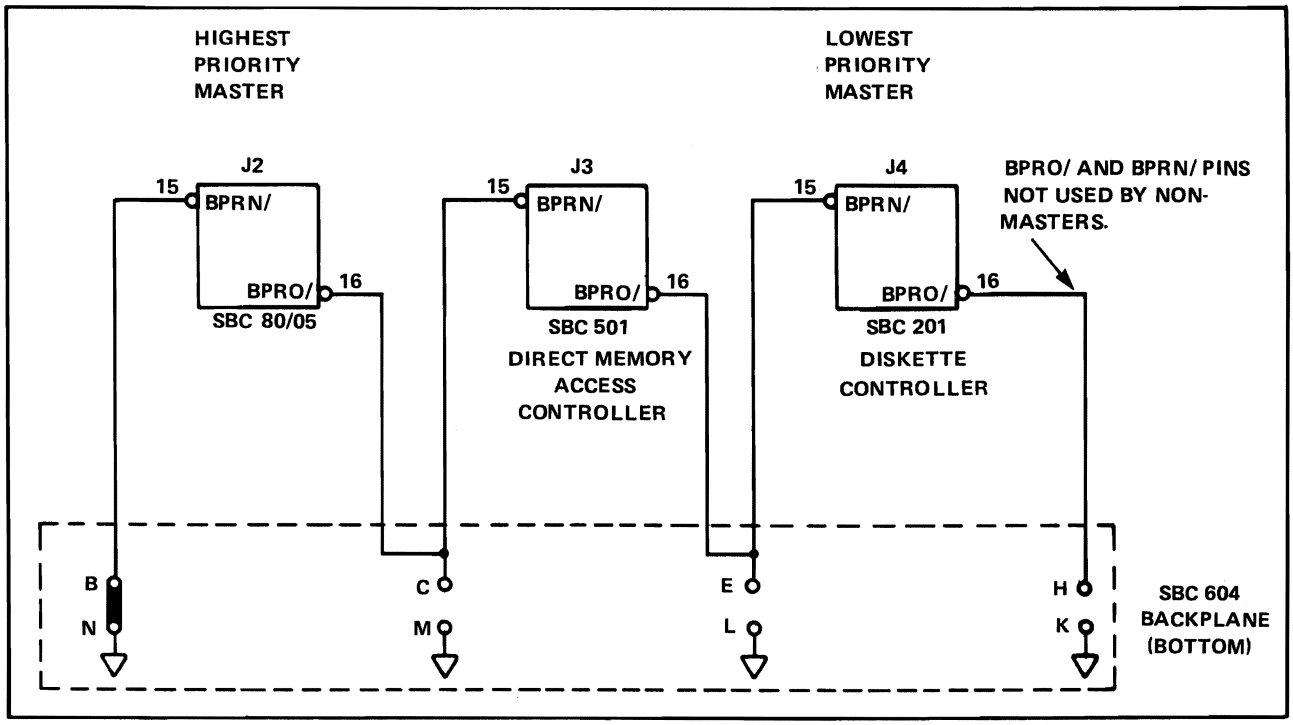

Figure 2-5. Serial Priority Resolution Scheme

Table 2-7. SBC 80/05 Bus Interface AC Characteristics

PARAMETER	OVERALL MIN. (ns)	OVERALL MAX. (ns)	READ MIN. (ns)	READ MAX. (ns)	WRITE MIN. (ns)	WRITE MAX. (ns)	DESCRIPTION*	REMARKS
t_{AS}	50		50		50		Address Setup Time to Command	
t_{AH}	50		50		50		Address Hold Time from Command	
t_{DS}	50				50		Data Setup Time to Command	
t_{DH}	50				50		Data Hold Time from Command	
t_{CY}	508	510					CPU Cycle Time	
t_{CD}			690		690		Command Width	ASSUME BUS AVAILABLE
$t_{CS1,2}$			475		475		Command Separation	Read to Read / Write to Write — Override Mode
t_{CS3}			980				Command Separation	Read to Write — Override Mode
t_{CS4}					980		Command Separation	Write to Read — Override Mode
t_{PPD}		63					Parallel Priority Resolution Delay	BREQ/ to BPRN/
t_{XKO}	0	65	0	65	0	65	XACK Turn Off Delay	
t_{BWS}	35	∞					Bus Clock Low or High Intervals	Supplied by system.
t_{BS}	15						BPRN to BCLK Setup Time	
t_{DBY}		30					BCLK to Busy Delay	
t_{PNO}		20					BPRN to BPRO Delay	
t_{BCY}	100	102					Bus Clock Period (BCLK)	From SBC 80/05 when properly terminated
t_{BW}	35	74					Bus Clock Low or High Intervals	From SBC 80/05 when properly terminated
t_{INT}	3000						Initialization Width	After all voltages have stablized.

*See figures 2-3 and 2-4 for timing diagrams.

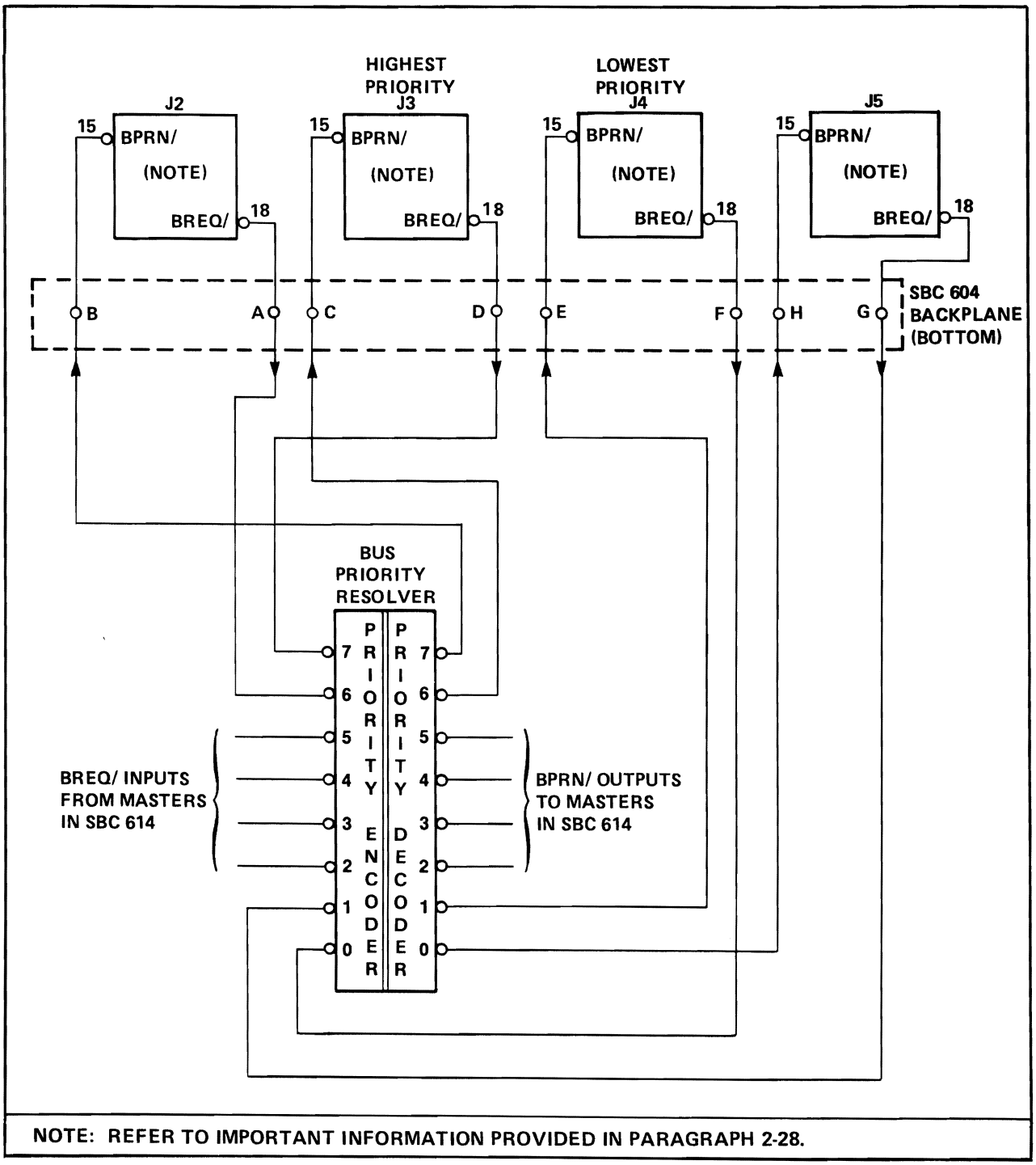

Figure 2-6. Parallel Priority Resolution Scheme

Table 2-8. SBC 80/05 Bus Interface DC Characteristics

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
ADR0/ - ADRF/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = −5.2 mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 2.4V		40	μA
	I_{LL}	Output Leakage Low	V_O= 0.4V		-40	μA
	C_L*	Capacitive Load			18	pF
BCLK/	V_{OL}	Output Low Voltage	I_{OL} = 59.5 mA		0.5	V
	V_{OH}	Out High Voltage	I_{OH} = −3 mA	2.7		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Curremt at Low V	V_{IN} = 0.45V		−0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		40	μA
	C_L*	Capacitive Load			15	pF
BPRO/	V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = −0.4 mA	2.4		V
	C_L*	Capacitive Load			10	pF
BREQ/	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = −0.4 mA	2.4		V
	C_L*	Capacitive Load			10	pF
BUSY/ (OPEN COLLECTOR)	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.45	V
	C_L	Capacitive Load			20	pF
CCLK/	V_{OL}	Output Low Voltage	I_{OL} = 60 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = −3 mA	2.7		V
	C_L*	Capacitive Load			15	pF
DAT0/ - DAT7/	V_{OL}	Output Low Voltage	I_{OL} = 50 mA		0.6	V
	V_{OH}	Output High Voltage	I_{OH} = −10 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		−0.25	mA
	I_{LH}	Output Leakage High	V_O = 5.25V		100	μA
	I_{LL}	Output Leakage Low	V_O = 0.45V		100	μA
	C_L*	Capacitive Load			18	pF
INIT/ (SYSTEM RESET)	V_{OL}	Output Low Voltage	I_{OL} = 44 mA		0.4	V
	V_{OH}	Output High Voltage	Open Collector			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		−1.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		0.7	mA
	C_L*	Capacitive Load			18	pF

Table 2-8. SBC 80/05 Bus Interface DC Characteristics (Continued)

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
INT0/-INT7/ XACK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		−0.4	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7V		20	μA
	C_L*	Capacitive Load			18	pF
MRDC/, MWTC/ IORC/, IOWC/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = −2 mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 5.25V		100	μA
	I_{LL}	Output Leakage Low	V_O = 0.45V		100	μA
	C_L*	Capacitive Load			15	pF

*Capacitive load values are approximations.

2-28. PARALLEL PRIORITY RESOLUTION

A parallel priority resolution scheme allows up to 16 masters to acquire and control the Multibus. Figure 2-6 illustrates one method of implementing such a scheme for resolving bus contention in a system containing eight master modules installed in an SBC 604/614. In this example, the priority encoder is a Texas Instruments 74148 and the priority decoder is an Intel 8205. Input connections to the priority encoder determine the bus priority, with input 7 having the highest priority and input 0 having the lowest priority. Here, the J3 master has the highest priority and the J4 master has the lowest priority.

IMPORTANT: In a parallel priority resolution scheme, the BPRO/ output signal must be disabled on all master modules. On the SBC 80/05, disable the BPRO/ output signal by removing jumper W10. If a similar jumper is not provided on the other master modules to disable the BPRO/ output signal, either clip the IC pin that supplies the BPRO/ output signal to the Multibus or cut the trace.

2-29. SINGLE-BOARD CONFIGURATION

CAUTION

Always turn off the power supply before connecting or disconnecting power leads. Failure to observe this precaution can result in damage to the board.

If the SBC 80/05 is used in a single-board configuration and power other than +5V is specified in table 2-2, an 86-pin connector must be provided to input power to the board. A description of the connector is given in table 2-1 (item 3) and power job connections are listed in table 2-5. Assuming that all the necessary components have been installed and that the jumpers have been appropriately configured, proceed with interfacing peripheral equipment to the SBC 80/05 as described in following paragraphs.

2-30. PERIPHERAL INTERFACING

An RS232C or a TTL level serial I/O device (but not both) and three TTL level parallel I/O ports may be interfaced to the SBC 80/05 as described in following paragraphs. If a Teletype Model ASR-33 is to be used as the RS232C serial I/O device, it must be modified as described in Appendix B.

2-31. SERIAL I/O WIRING

An RS232C serial I/O device must be interfaced to the SBC 80/05 via connector J2. A TTL level serial I/O device may be interfaced to the SBC 80/05 via connector J1 or J2. Pin assignments for connectors J1 and J2 are listed in tables 2-9 and 2-10, respectively.

Figure 2-7 illustrates the cabling required for interfacing connector J2 to an RS232C serial I/O device. Notice that the transmission path from J2 to the RS232C device connector should be limited to 15.25 meters (50 feet.) In an extremely noisy electrical environment, twisted-pair wires may be used in a fashion similar to that shown in figure 2-8. For interfacing with teletypewriters and other 20 mA current loop equipment, an Intel SBC 530 Teletypewriter (TTY) Adapter (or equivalent) is required. (Refer to Appendix B.)

Figure 2-8 illustrates the cabling required for interfacing connector J2 to a TTL level serial I/O device; the dc characteristics of the TTL serial I/O port are given in table 2-11. Notice in figure 2-8 that the transmission path from J2 to the TTL device connector should be

limited to 3 meters (10 feet). The TTL level serial I/O device can also be interfaced to the SBC 80/05 via connector J1. (Refer to paragraph 2-32 and table 2-9.) The individual wires connected to J1 for TTL level serial I/O should be two pair of wires of the cable used for interfacing the parallel I/O channels.

2-32. PARALLEL I/O WIRING

The SBC 80/05 interfaces to the three parallel I/O ports via connector J1. Using 50-conductor cable and a mating connector for J1 (table 2-1, item 4), interface the para-

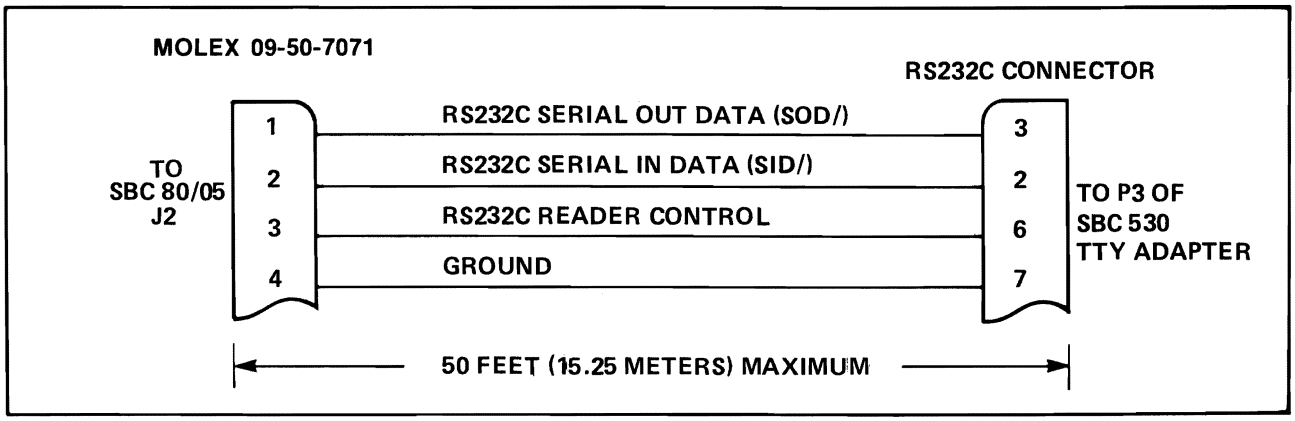

Figure 2-7. RS232C Serial I/O Device Interface Cabling

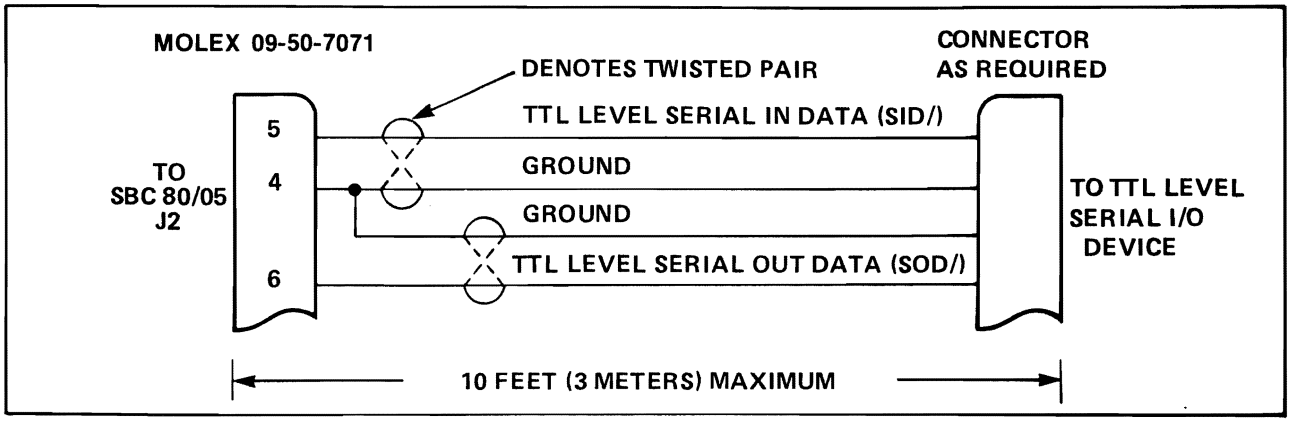

Figure 2-8. TTL Level Serial I/O Device Interface Cabling

llel I/O ports to the appropriate pins on J1 as listed in table 2-9. The transmission path from the SBC 80/05 to the parallel I/O ports should be limited to 3 meters (10 feet) maximum. The dc characteristics of the SBC 80/05 parallel I/O ports are presented in table 2-11. The following bulk cable types (or equivalent) are recommended for interfacing with the parallel I/O ports (assuming 25 line pairs are used):

a. Cable, flat, 50-conductor, 3M 3306-50.

b. Cable, flat, 50-conductor (with ground plane), 3M 3380-50.

c. Cable, woven, 25-pair, 3M 3321-25.

Table 2-9. Connector J1 Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	GND	26[1]	Port 03 bit 4 (Port 02 Buffer Full)
2	Port 02 bit 7	27	GND
3	GND	28[1]	Port 03 bit 5 (Port 02 Strobe)
4	Port 02 bit 6	29	GND
5	GND	30	TTL level SOD/ (Serial Out Data)
6	Port 02 bit 5	31	GND
7	GND	32	TTL level SID/ (Serial In Data)
8	Port 02 bit 4	33	GND
9	GND	34	Port 01 bit 7
10	Port 02 bit 3	35	GND
11	GND	36	Port 01 bit 6
12	Port 02 bit 2	37	GND
13	GND	38	Port 01 bit 5
14	Port 02 bit 1	39	GND
15	GND	40	Port 01 bit 4
16	Port 02 bit 0	41	GND
17	GND	42	Port 01 bit 3
18	Port 03 bit 3	43	GND
19	GND	44	Port 01 bit 2
20[1]	Port 03 bit 2 (Port 01 Strobe)	45	GND
21	GND	46	Port 01 bit 1
22[1]	Port 03 bit 1 (Port 01 Buffer Full)	47	GND
23	GND	48	Port 01 bit 0
24	Port 03 bit 0	49	GND
25	GND	50	EXT INTR1/ (External Interrupt 1)

1. These pins are used as control signals when Ports 01 and 02 are used in the latched and strobe mode.

2. Pin numbers refer to board connector pins only, they are not necessarily the same on the mating connectors.

Table 2-10. Connector J2 Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	Reserved	5	RS232C level RDR CTL (Reader Control)
2	TTL level SOD/ (Serial Out Data)	6	RS232C level SID/ (Serial In Data)
3	TTL level SID/ (Serial In Data)	7	RS 232C level SOD/ (Serial Out Data)
4	GND	–	

1. Pin numbers refer to board connector pins only, they are not necessarily the same on the mating connectors.

Table 2-11. Parallel I/O and TTL Level Serial I/O DC Characteristics

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNITS
8155	V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.45	V
DRIVER/	V_{OH}	Output High Voltage	I_{OH} = −400 μA	2.4		V
RECEIVER	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0	Vcc_5	V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45		10	μA
	I_{IH}	Input Current at High V	V_{IN} = 5.0		10	μA
	C_L*	Capacitive Load			18	pF
TTL SID/	V_{IL}	Input Low Voltage			0.5	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.50		−2.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7		50	μA
TTL SOD/	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = −1.0 mA	2.7		V

*Capacitive load value is approximate.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter lists the SBC 80/05 on-board memory address assignments; provides programming details for the parallel I/O section, timer section, and serial I/O port; and describes the 8085A CPU interrupt structure. The 8085A CPU instruction set is provided in Appendix A; a complete description of programming with Intel's assembly language is given in *8080/8085 Assembly Language Programming Manual,* part no. 98-310.

3-2. MEMORY ADDRESSING

Addresses for on-board read/write memory (RAM) and read-only memory (ROM or EPROM) are given in table 3-1. Note in table 3-1 that the address space listed for ROM/EPROM depends on how the SBC 80/05 is configured by the user.

When on-board memory is addressed, a Memory Advanced Acknowledge (MEM AACK/) signal is generated which allows the CPU to operate at maximum speed. When system memory is addressed, the CPU must first gain control of the Multibus and then wait for a Transfer Acknowledge (XACK/) to be received from the system memory device.

If a non-existent memory location is addressed, the CPU will hang up in a wait state until reset. It should be noted in table 3-1 that it is possible to configure ROM/EPROM such as to create *illegal* addresses. If an illegal address is used, a MEM AACK/ signal is generated as described for a legal address and the CPU will continue executing. If a read is attempted from an illegal address, erroneous data will be returned; if a write is attempted to an illegal address, the data byte is lost.

When power is initially applied to the SBC 80/05, or when a reset is otherwise initiated, the CPU program counter (PC) and instruction register are set to zero. Thus, the CPU initially fetches the instruction in location 0000. It is expected that this location in ROM/EPROM will reference a user-defined routine such as an automatic bootstrap loader for a paper tape reader, magnetic type, disc, etc.

3-3. PARALLEL I/O SECTION

The Intel 8155 includes two 8-bit parallel I/O ports (Port 01 and Port 02) and one 6-bit parallel I/O port (Port 03). Each of these three ports can be individually hardware configured as either an input port or an output port (but not both). Port 03 can be programmed to allow Port 01 and Port 02 to operate in a handshake mode with their associated input or output device. In this case, Port 03 must be specifically hardware configured to perform this function and cannot be used as an input port or as an output port.

3-4. I/O REGISTER ADDRESSING

The I/O section consists of a Command/Status (C/S) register and one register for each of the three I/O ports. Addresses for these four registers are provided in table 3-2.

Table 3-1. SBC 80/05 Memory Addresses

TYPE	CONFIG	LEGAL ADDRESSES	ILLEGAL ADDRESSES
ROM or EPROM	One 8308/8708 chip Two 8308/8716 chips	0000-03FF 0000-07FF	0400-07FF
	One 2716/8316E chip Two 2716/8316E chips	0000-07FF 0000-0FFF	0800-0FFF
RAM	N/A	3E00-3FFF	N/A

Table 3-2. I/O Register Addresses

Register	Bits	I/O Address
Command/Status	8	00
Port 01	8	01
Port 02	8	02
Port 03	6	03
LSB of Timer Count	8	04
MSB of Timer Count	8	05
Unused	—	06
Unused	—	07

3-5. PROGRAMMING THE COMMAND REGISTER (PORT 00)

The Command register consists of eight 1-bit latches. Four bits (0 - 3) define the mode of Port 01 and Port 02, two bits (4 - 5) enable or disable the Port 01 and Port 02 interrupts (in the strobed input/output mode), and two bits (6 - 7) define the programmable timer command. (Refer to paragraph 3-10.)

The Command register can be altered at any time by performing an I/O write to location 00. The specific meaning of each register command bit is shown in figure 3-1.

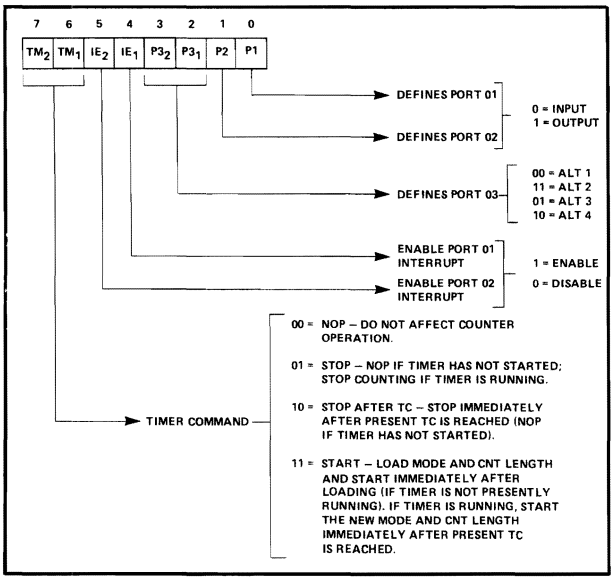

Figure 3-1. Command Register Format (Port 00)

3-6. READING THE STATUS REGISTER (PORT 00)

The Status register consists of seven 1-bit latches. Bit 0-5 define the status of the ports and bit 6 defines the status of the timer. The contents of the Status register can be obtained at any time by performing an I/O read to location 00. The format of the Status register is presented in figure 3-2.

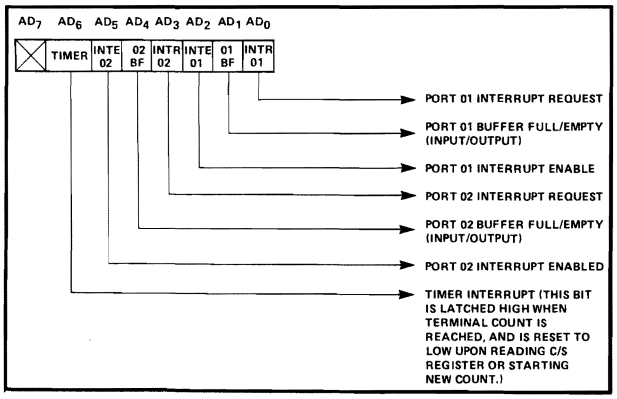

Figure 3-2. Status Register Format (Port 00)

3-7. PORT 01 REGISTER

The Port 01 register can be programmed to be either an input port or an output port depending on Command register bit 0. (See figure 3-1.) Also, depending on the Command, this port can operate in either the basic input/output mode or strobed mode depending on the alternative (ALT) mode programmed for Port 03. (Refer to paragraph 3-9.)

3-8. PORT 02 REGISTER

The Port 02 register can be programmed to be either an input port or an output port depending on Command register bit 1. (See figure 3-1.) Also, depending on the Command, this port can operate in either the basic input/output mode or strobed mode depending on the alternative (ALT) mode programmed for Port 03. (Refer to paragraph 3-9.)

3-9. PORT 03 REGISTER

The Port 03 register can be programmed as an input port, output port, or as control signals for Port 01 and Port 02 depending on the hardware configuration and Command register bits 2 and 3. Figure 3-1 shows that bits 2 and 3 specify four alternative modes for Port 03: ALT 1, ALT 2, ALT 3 and ALT 4. As noted in table 3-3 for ALT 3 mode, bits 0 - 2 are control bits for Port 01. and bits 3 - 5 depend on the user's jumper-selected options.

Table 3-3. Port 03 Programmable Modes

PORT 03 BIT	ALT 1	ALT 2	ALT 3	ALT 4
0	Input Port	Output Port	Port 01 Interrupt	Port 01 Interrupt
1	Input Port	Output Port	Port 01 Buffer Full	Port 01 Buffer Full
2	Input Port	Output Port	Port 01 Strobe	Port 01 Strobe
3	Input Port	Output Port	Note 1	Port 02 Interrupt
4	Input Port	Output Port	Note 2	Port 02 Buffer Full
5	Input Port	Output Port	Note 3	Port 02 Strobe

Notes:

1. If W2 is in position B-C, bit 3 is output bit.
2. If W12 is in position A-B, bit 4 is output bit; if W12 is in position A-C, bit 4 is RS232C Reader Control (RDR CTL) signal.
3. If W1 is in position A-B (only) and W6 is in position A-B, bit 5 is used to provide the programmable bus override mode; i.e., the SBC 80/05 will not relinquish the Multibus until Port 03 bit 5 is cleared. If the override function is not jumpered, bit 5 is not functional.

3-10. TIMER SECTION

The timer is a 14-bit down-counter that counts the 122.88-kHz timer (clock) input and outputs either a square wave or a pulse when the terminal count (TC) is reached. The timer output must be connected by the user to the selected CPU interrupt via a jumper wire.

The timer includes a 16-bit register for holding the count length (14 bits) and the operating mode (2 bits). The I/O address for the low-order byte (least-significant bits of count length) and high-order byte (most-significant bits of count length and timer mode) is 04 and 05, respectively. Figure 3-3 shows the timer format and I/O addresses.

The timer I/O addresses serve a dual purpose. During a I/O Write operation, the count length (bits 0 - 13) and mode (bit 14 - 15) are loaded into the 16-bit register; during an I/O Read operation, the *present count* (the count at the time of the I/O Read operation) and the mode bits are read. To ensure that the correct count is read, it is preferable to stop counting, read the counter, and then reload the counter and continue counting.

By connecting the counter output to the RST 7.5 input of the CPU, the CPU can be interrupt driven at the baud rate desired for serial I/O communication. The count lengths required for various baud rates are given in table 3-4. Timer interrupt routines are presented in paragraph 3-13.

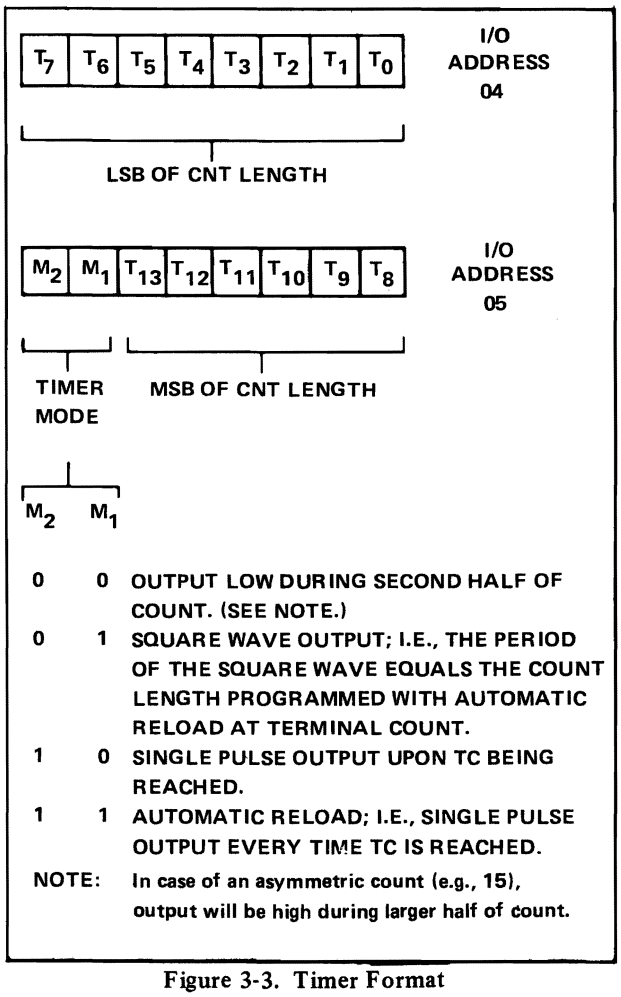

Figure 3-3. Timer Format

Table 3-4. Baud Rates Vs Count Lengths

BAUD RATE	DECIMAL COUNT	ERROR/FRAME
4800	26	1.6%
2400	51	0.4%
1200	102	0.4%
600	205	0.1%
110	1117	0.01%
75	1638	0.01%

3-11. SERIAL I/O COMMUNICATION

Tables 3-5 and 3-6, respectively, provide examples of serial input and serial output routines using the SID and SOD instructions of the 8085A CPU. Both routines, which provide programmed timing loops at 2400 baud, operate in the non-interrupt driver mode. The examples are included for illustration purposes only and are not intended to demonstrate the optimum way to program the serial I/O port.

Table 3-5. Serial Input Data Routine (Non-Interrupt Driven)

```
   FUNCTION: CIWAIT
   INPUTS: NONE
   OUTPUTS: NONE
   CALLS: WAIT
   DESCRIPTION: THIS ROUTINE WAITS FOR AN INPUT FROM THE CONSOLE BY READING
                THE SID INPUT LINE. WHEN IT DETECTS A START BIT, IT THEN READS
                THE INPUT CHARACTER AND RETURNS TO THE PLM CALLING PRO-
                GRAM WHEN THE INPUT CHARACTER IS A 'W'.

CIWAIT:
        MVI     B,00H       ; CLEAR OUT CHARACTER STORAGE REGISTER
        MVI     C,08H       ; SET COUNT REGISTER
BEGIN:  RIM
        ANI     80H         ; CHECK FOR START BIT
        JZ      BEGIN       ; CONTINUE LOOKING UNTIL FOUND
        MVI     D,1BH       ; SET-UP DELAY
        CALL    WAIT
        RIM
        ANI     80H         ; CHECK FOR VALIDITY OF START BIT
        JZ      BEGIN       ;
NEXT:   DCR     C           ; DECREMENT COUNT REGISTER
        JZ      CHKW        ; CHECK TO SEE IF INPUT CHARACTER IS A 'W'
        MVI     D,38H       ; SET-UP DELAY
        CALL    WAIT
        RIM
        ANI     80H         ; CHECK REGISTER A BIT 7
        ORA     B           ; LOAD PREVIOUS BITS INPUT INTO A
        RRC
        MOV     B,A         ; STORE DATA IN B REGISTER
        JMP     NEXT
CHKW:   MOV     A,B
        CPI     28H         ; COMPARE CI TO COMPLEMENT OF 'W'
        JNZ     CIWAIT
        RET

   FUNCTION: WAIT
   DESCRIPTION: ACCEPTS DATA IN THE D REGISTER WHICH DETERMINES THE NUMBER
                OF TIMES THE LOOP WILL BE EXECUTED. THE LOOP INVOLVES TWO
                INSTRUCTIONS OR 14 CLOCK STATES.

WAIT:
        DCR     D
        JNZ     WAIT
        RET
```

Table 3-6. Serial Output Data Routine (Non-Interrupt Driven)

```
        FUNCTION CO:
        INPUTS:  ACCEPTS A BYTE OF DATA IN THE C REGISTER OR FROM MEMORY
                 LOCATION SPECIFIED BY H&L REGISTERS.
        OUTPUTS: OUTPUTS SERIAL DATA VIA THE SOD LINE TO CONSOLE.
        CALLS:   WAIT
        DESCRIPTION: CO ACCEPTS AN ASCII BYTE FROM THE PLM SYS4 PROGRAM DIRECTLY
                     OR FROM THE MESOUT ROUTINE WHICH IS INVOKED BY THE PLM
                     SYS4 PROGRAM. IT FIRST OUTPUTS THE START BIT, THEN SEVEN
                     DATA BITS FOLLOWED BY TWO STOP BITS. THE PROPER DURATION
                     BETWEEN SOD OUTPUTS IS DETERMINED BY THE VALUE PASSED TO
                     THE WAIT ROUTINE VIA THE D REGISTER.

CO:
        MVI     A,0C0H      ; SET UP FOR START BIT INSTRUCTION
        MVI     E,07H       ; SET COUNTER FOR NUMBER OF DATA BITS
        SIM                 ; BEGIN START BIT
        MVI     A,00H
        CMP     C
        JNZ     L1          ; IF DATA IN C, DON'T LOOK IN MEMORY
        MOV     A,M         ; GET DATA FROM MEMORY
        CMA
        MOV     B,A
        JMP     L2
L1:     MOV     A,C         ; GET DATA IN C REGISTER
        CMA                 ; COMPLEMENT DATA (A 1 IN THE ACC WILL
                            ;     PUT A 0 ON THE RS232 LINE)
        MOV     B,A         ; STORE IN B REGISTER
        ANI     0FFH        ; DUMMY INSTRUCTION FOR TIMING DELAY
L2:     MVI     D,34H       ; SET-UP D REGISTER FOR TIME DELAY (2400 BAUD)
        CALL    WAIT
        JMP     L3
DELAY:  MVI     D,36H       ; SET-UP D REGISTER FOR TIME DELAY (2400 BAUD)
        CALL    WAIT
        MOV     A,B
L3:     RRC                 ; PUT LSB INTO BIT 7 FOR SIM INSTR
        MOV     B,A         ; STORE DATA IN B REGISTER
        ORI     40H         ; PUT A '1' IN BIT 6 FOR SIM INSTR
        ANI     0C0H        ; MASK ANY OTHER BITS-AFFECT RSTS
        SIM
        DCR     E           ; DECREMENT COUNT REGISTER
        JNZ     DELAY       ; CONTINUE OUTPUT FOR 7 DATA BITS
        MVI     D,38H       ; SET-UP D REGISTER FOR DELAY (2400 BAUD)
        CALL    WAIT
        MVI     A,40H       ; SET-UP A REGISTER FOR STOP BITS
        SIM
        MVI     D,76H       ; SET-UP TWO STOP BIT DELAY (2400 BAUD)
        CALL    WAIT
        RET

        FUNCTION: WAIT
        DESCRIPTION: ACCEPTS DATA IN THE D REGISTER WHICH DETERMINES THE NUMBER
                     OF TIMES THE LOOP WILL BE EXECUTED. THE LOOP INVOLVES TWO
                     INSTRUCTIONS OR 14 CLOCK STATES.
WAIT:
        DCR     D
        JNZ     WAIT
        RET
```

Table 3-6. Serial Output Data Routine (Non-Interrupt Driven) (Continued)

```
        FUNCTION: MESOUT
        INPUTS: CHARACTER STRING DATA IN MEMORY SPECIFIED BY B&C REGISTERS.
        OUTPUTS: POINTER ADDRESS IS LOADED IN H&L REGISTERS.
        CALLS: CO
        DESCRIPTION: THE PLM PROGRAM CALLS MESOUT WITH AN ADDRESS PARAMETER
                     PLACED IN THE B AND C REGISTERS. MESOUT LOADS THIS
                     ADDRESS INTO THE H AND L REGISTERS AND THEN CALLS THE
                     CO ROUTINE WHICH WILL OUTPUT THE ASCII DATA LOCATED IN
                     MEMORY SPECIFIED BY THESE REGISTERS. MESOUT WILL THEN
                     INCREMENT H&L AND CONTINUE TO CALL CO UNTIL A ZERO IS
                     FOUND IN MEMORY.

MESOUT:
        MOV     H,B
        MOV     D,C
LOOP:   MVI     C,00H       ; INDICATE TO CO THAT DATA IS IN MEMORY
        CALL    CO
        INX     H           ; GET ADDRESS OF NEXT CHARACTER IN STRING
        MOV     A,M         ; CHECK FOR END OF STRING
        ORI     00H
        JNZ     LOOP        ; CONTINUE UNTIL ZERO FOUND IN MEMORY
        RET
```

3-12. INTERRUPTS

The SBC 80/05 CPU includes four vectored interrupts: TRAP, RST 7.5, RST 6.5, and RST 5.5. Jumpers may be installed to allow interrupts from parallel I/O Ports 01 and 02, the programmable timer, one or more devices via the Multibus, or an external source. Each of the three RST inputs (7.5, 6.5, and 5.5) has a programmable mask; TRAP is not maskable. The priority and vector location for each of these restart interrupts are given in table 3-7.

3-13. TIMER INTERRUPTS

Timer interrupt routine examples are presented in table 3-8. These examples include a timer initialization, which is performed as part of the main program; a routine to service an RST 7.5 interrupt; and a subroutine to save the state of the machine upon being interrupted and to restore the state of the machine after servicing the interrupt. These examples are included for illustration purposes only and are not intended to demonstrate the optimum way of programming these functions.

Table 3-7. Interrupt Vector Memory Locations

INTERRUPT	VECTOR LOCATION	PRIORITY
TRAP	24	Highest
RST 7.5	3C	2nd
RST 6.5	34	3rd
RST 5.5	2C	Lowest

3-14. TRAP INTERRUPTS

There are special considerations that must be made when the TRAP interrupt is used. The fact that the TRAP interrupt is non-maskable can present problems in at least two areas.

Interrupt driven systems often contain parameters that must be modified only within critical regions. A critical region can be roughly defined as a section of code that once begun must complete execution before it or another critical region that corresponds to the same system parameter(s) can be executed. A TRAP interrupt handler cannot safely alter such parameters either directly or indirectly by causing the execution of procedures or tasks that may alter such parameters.

If the hardware generates a TRAP interrupt on power up or power fail, the system must be able to process the TRAP interrupt before it is completely initialized. It should also take into account that an interrupt routine that runs with interrupts disabled can still be interrupted by a TRAP.

Because of these considerations, it is recommended that the TRAP interrupt only be used for system startup and/or catastrophic error handling.

Table 3-8. Timer Interrupt Routines

```
        MAIN PROGRAM – INITIALIZES THE 8155 COUNTER AND STARTS THE
        COUNT BEFORE CONTINUING WITH ITS OTHER ROUTINES. THIS PROGRAM
        SETS THE TIME TO COUNT 122 TIMER–IN PULSES BEFORE OUT–
        PUTTING A TIMER PULSE THAT WILL GENERATE AN INTERRUPT.
        USING MODE 3, THE TIMER WILL AUTOMATICALLY RELOAD
        AND BEGIN ANOTHER COUNTDOWN.

        MVI     A,7CH
        OUT     4               ; OUTPUT LSB OF COUNT LENGTH
        MVI     A,0C0H
        OUT     5               ; OUTPUT MSB AND TIMER MODE
        MVI     A,18H
        SIM                     ; UNMASK RESTART INTERRUPTS
        EI                      ; ENABLE PROCESSOR INTERRUPTS
        MVI     A,0C0H
        OUT     0               ; START TIMER COUNTDOWN
          .
          .
          .
          .             MAIN PROGRAM CONTINUES
          .
          .

        END MAIN PROGRAM

FUNCTION: INTR75
DESCRIPTION: WHEN A RST 7.5 IS GENERATED BY THE 8155 (DETERMINED BY
             THE MAIN PROGRAM), THIS ROUTINE STORES THE STATUS WORD
             AND THEN INCREMENTS A COUNT VARIABLE. IT MAY THEN CALL
             A REAL TIME COUNT AND DISPLAY ROUTINE WHICH INCREMENTS
             VARIABLES FOR MILLISECONDS, SECONDS, ETC., AT THE PROPER TIME.
             FINALLY, THE INTERRUPT ROUTINE WILL RESET RST 7.5, RESTORE
             PROCESSOR STATUS WORD, AND ENABLE INTERRUPTS BEFORE RE-
             TURNING TO THE MAIN PROGRAM.

        ORG     003CH

        COUNT   EQU     00      ; SET TIMER DELAY

SAVE:
        PUSH    PSW             ; SAVE STATE OF MACHINE
        PUSH    B
        PUSH    D
        PUSH    H
INTR75:
        LXI     H,COUNT         ; LOAD H&L WITH LOCATION OF COUNT
        INR     M               ; INCREMENT THE COUNT
        CALL    RTC             ; CALL REAL TIME COUNT AND DISPLAY ROUTINE
        MVI     A,10H               (NOT SHOWN)
        SIM                     ; RESET RST 7.5
RSTORE:
        POP     H               ; RESTORE STATE OF MACHINE
        POP     D
        POP     B
        POP     PSW
        EI
        RET
```

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description and a circuit analysis of the SBC 80/05 Single Board Computer. The circuit analysis is presented with the assumption that the reader has access to the Intel MCS 85 *User's Manual,* part no. 98-366, which describes in detail the Intel 8085A Microprocessor (CPU) and the 8155 RAM/IO/Timer.

4-2. FUNCTIONAL DESCRIPTION

As shown in figure 4-1, the SBC 80/05 is composed of the following functional blocks:

a. Clock Generator (including power-up reset).
b. CPU (including interrupt control).
c. Bus Interface (address bus drivers, data bus drivers, and bus controller).
d. Random Access Memory (RAM).
e. Read-Only Memory (ROM/EPROM).
f. Serial I/O Interface.
g. Parallel I/O Interface (including programmable timer).

Crystal controlled *Clock Generator* A3 provides a stable time base for the SBC 80/05 as well as for the Multibus. The Clock Generator also generates a power-up reset signal to initialize the entire system to a known internal state.

The 8-bit parallel *CPU,* which is the heart of the system, performs all the system processing functions and generates the address and control signals required to access memory and I/O ports. The CPU multiplexes the 8-bit data bus and the lower eight bits of the address bus. During the first part of the machine cycle, the lower eight address bits on the address/data bus are latched into Demultiplexer A18 and RAM/IO/Timer A15. During the remainder of the machine cycle, the bus is used for memory and I/O data transfers. The CPU responds to interrupt requests originating from jumper-selectable sources. As shown in figure 4-1, these interrupt requests may be generated by the on-board timer and parallel I/O ports, by one or more devices via the Multibus, or by an external source.

The *Bus Interface* allows the SBC 80/05 to use a system bus that is common to other master devices (e.g., CPU's and DMA controllers), thus allowing system memory and I/O devices to be shared on a priority basis. The primary element of the Bus Interface is Bus Controller A19, which operates synchronously with the bus clock (BCLK/) and consists of the following functional sections:

a. Bus arbitration logic to resolve bus contention in multiple master systems.
b. Timing logic, initiated by the bus arbitration logic, to ensure adequate setup and hold times for the address and data placed on the Multibus; also generates read/write control signals.
c. Output drive logic for driving the bus memory and I/O command (control) lines.

When the SBC 80/05 gains control of the Multibus to perform a write operation, the Bus Controller gates the device address and data onto the Multibus and issues a Write command. In performing a read operation, the Bus Controller gates the device address onto the Multibus and issues a Read command. Operations between the CPU and the on-board memory and I/O ports do not require the Multibus. Notice in figure 4-1 that the data bus drivers are bidirectional and the address bus drivers are unidirectional. This allows the SBC 80/05 full control of the Multibus but prevents other modules from accessing the SBC 80/05 memory and I/O ports.

The SBC 80/05 provides 512 eight-bit words of static *Random Access Memory* (RAM). Two Intel 8111-A4 devices provide 256 words in locations 3E00-3EFF. The Intel 8155 RAM/IO/Timer provides 256 eight-bit words of static RAM in locations 3F00-3FFF. This 512 word RAM storage area requires neither refreshing nor clock inputs, thereby providing the CPU immediate access to the addressed location.

Two IC sockets are provided to allow the user to install either 2K or 4K bytes of *Read Only Memory* (ROM). The user may install two Intel 2716 (2K x 8) or 8708 (1K x 8) ultraviolet erasable and reprogrammable ROM's (EPROM's) for program development or install two Intel 8316E (2K x 8) or 8308 (1K x 8) masked ROM's containing a dedicated program. Depending on the type of ROM or EPROM installed, the address locations are 0000-07FF (two 1K x 8-bit chips) or 0000-0FFF (two 2K x 8-bit chips).

The *Serial I/O Interface* is accomplished via the Serial Input Data (SID) and Serial Output Data (SOD) pins on the CPU. Data on the SID line is loaded into the CPU by a RIM instruction; data on the SOD line is set or cleared by a SIM instruction. Data buffers are provided for TTL level interface. Sockets are provided for the installation of level converters for RS232C interface.

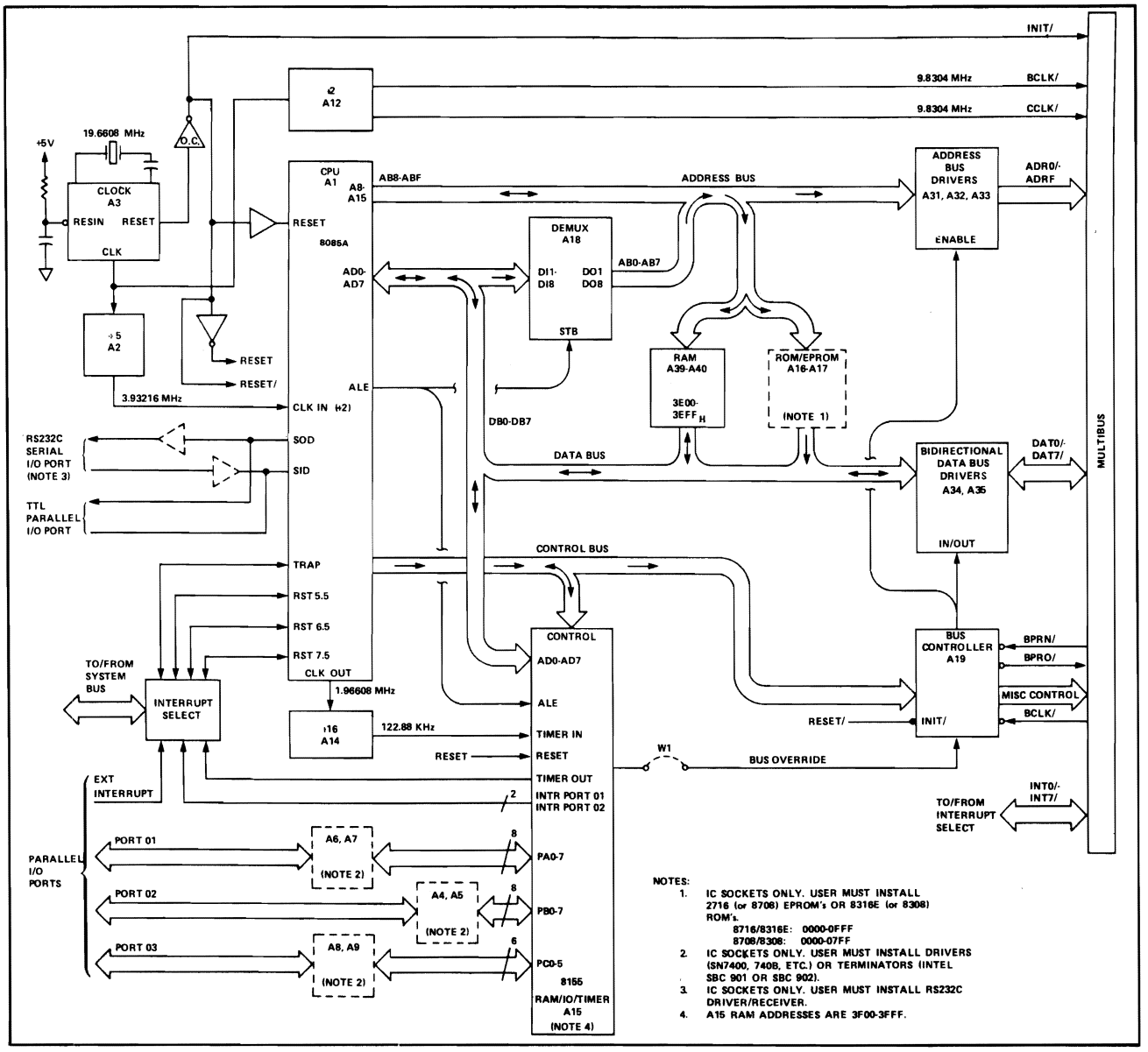

Figure 4-1. SBC 80/05 Block Diagram

The *Parallel I/O Interface* consists of three general purpose ports provided by the Intel 8155 RAM/IO/Timer. Each of the three ports can be programmed to be either an input port or an output port. One of the three ports (Port 03) can be programmed to be status pins, thus allowing the other two ports (Ports 01 and 02) to operate in a handshake mode. The I/O portion of the 8155 contains four internal registers – one register for command and status and one data register for each of the three ports. Sockets are provided for the installation of input terminators or output drivers as required by the user's configuration.

The 8155 timer is a programmable 14-bit binary down-counter that counts the input pulses and outputs either a square wave or a pulse when the "terminal-count" is reached. The count length and the timer output mode are loaded under program control. The four selectable timer modes are as follows:

a. Timer Out goes low during the second half of count. Therefore, the count loaded in the Count Length Register should be twice the timeout desired.

b. Timer Out remains high until the first half of the count has been completed and goes low for the second half of the count. The count length is automatically reloaded when the terminal count is reached.

c. A single low pulse is generated upon reaching the terminal count; this function is useful for generating real-time clocks.

d. A Divide-by-N Counter generates a repetitive Timer Out low pulse; a new pulse train is initiated every time the terminal count is reached.

4-3. CIRCUIT ANALYSIS

The schematic diagram for the SBC 80/05 is given in figure 5-2. The schematic diagram consists of three sheets, each of which includes grid coordinates. Signals that transverse from one sheet to another are assigned grid coordinates at both the signal source and signal destination. For example, the grid coordinates 2ZB1 locate a signal source (or signal destination as the case may be) on sheet 2 Zone B1.

Both active-high and active-low signals are used. A signal mnemonic that ends with a virgule (e.g., DAT7/) denotes that the signal is active low ($\leq$0.4V). Conversely, a signal mnemonic without a virgule (e.g., ALE) denotes that the signal is active high ($\geq$2.0V).

4-4. INITIALIZATION

When power is applied in a start-up sequence, the contents of the CPU program counter, instruction register, and interrupt enable flip-flop are subject to random factors and cannot be predicted. For this reason, a power-up sequence is used to set the CPU (as well as Bus Controller A19 and the I/O ports of A15) to a known internal state.

When power is initially applied to the SBC 80/05, capacitor C1 (1ZC7) begins to charge through resistor R4. The charge developed across C1 is sensed by a Schmitt trigger, which is internal to Clock Generator A3. The Schmitt trigger converts the slow transition appearing at pin 2 into a clear, fast-rising synchronized RESET output signal at pin 1. The RESET signal is inverted by open-collector gate A24-3 to produce Initialize signal INIT/, which is distributed as shown in figure 4-1. The INIT/ signal clears the CPU program counter, instruction register, and interrupt enable flip-flop; initializes the three I/O ports of A15 to the input mode; and sets Bus Controller A19 to a known internal state.

4-5. CLOCK CIRCUITS

The time base for the SBC 80/05 is provided by Clock Generator A3 (1ZC7) and crystal Y1. The 19.6608-MHz output of A3 is divided by A12 (2ZC6) to produce a 9.8304-MHz signal, which is driven through gate A30 to produce Multibus clocks BCLK/ and CCLK/. Jumpers W7 and W8 are provided so that, when removed, some other master module can be used to generate one or both of these clocks if desired.

The 19.6608-MHz output of A3 is divided by A2 (1ZD6) to produce a 3.93216-MHz clock input to CPU A1, which internally divides this into a 1.96608-MHz clock output. This output is further divided by A14 (2ZB6) to produce the 122.88-kHz timer input to A15 (3ZD4).

4-6. INSTRUCTION TIMING

The execution of any program consists of read and write operations, where each operation transfers one byte of data between the CPU and a particular memory or I/O address. Although the CPU can vary the address, data, type, and sequence of operations, it is capable of performing only a basic read or write operation. With the exception of a few control lines, such as Address Latch Enable (ALE), these read and write operations are the only communication necessary between the processor and the other components to execute any instruction.

An *instruction cycle* is the time required to fetch and execute an instruction. During the fetch phase, the selected instruction (consisting of up to three bytes) is read from memory and stored in the operating registers of the CPU. During the execution phase, the instruction is decoded by the CPU and translated into specific processing activities.

Each instruction cycle consists of up to five machine cycles. A *machine cycle* is required each time the CPU accesses memory or an I/O port. The fetch phase requires one machine cycle for each byte to be fetched. Some instructions do not require any machine cycles other than those necessary to fetch the instructions from memory; other instructions, however, require an additional machine cycle(s) to write or read data to or from memory or I/O devices.

Every instruction cycle has at least one reference to memory during which time the instruction is fetched. An instruction cycle must always have a fetch, even if the execution of that instruction requires no reference to memory. The first machine cycle in every instruction cycle is therefore a fetch, and beyond that there are no specific rules. For instance, the IN (input) and OUT (output) instructions each require three machine cycles: fetch (to obtain the instruction), memory read (to obtain the I/O address of the peripheral), and an input or output machine cycle (to complete the transfer).

Each machine cycle consists of a minimum of three and a maximum of six states designated T_1 through T_6. A *state* is the smallest unit of processing activity and is defined as the interval between two successive falling edges of the CPU clock. Each state (or CPU clock cycle) has a duration of 508 nanoseconds (derived by dividing the crystal frequency by 10).

Every machine cycle normally consists of three T-states with the exception of an opcode fetch, which consists of either four or six T-states. The actual number of states required to execute any instruction depends on the instruction being executed, the particular machine cycle within the instruction cycle, and the number of *wait* states inserted into the machine cycle. The wait state is initiated when the READY input to the CPU is pulsed low.

There is no wait state imposed when the CPU is addressing on-board I/O or memory. As discussed later in this chapter, the wait state occurs only while waiting for XACK/ to be pulled low in response to an off-board I/O or memory read or write operation. Thus, the wait state depends on how quickly the Multibus can be accessed and the speed of the addressed memory or I/O device.

Figure 4-2 is presented to show the relationship between an instruction cycle, machine cycle, and T-state. This example shows the execution of a Store Accumulator Direct (STA) instruction involving on-board memory. Notice that for this instruction the opcode fetch (machine cycle M_1) requires four T-states and the remaining three cycles each require three T-states.

The opcode fetch is the only machine cycle that requires more than three T-states. This is because the CPU must interpret the requirements of the opcode fetched during T_1 through T_3 before it can decide what must be done in the remaining T-state(s).

4-7. OPCODE FETCH TIMING

Figure 4-3 shows the timing relationship of a typical opcode fetch machine cycle. At the beginning of T_1 of *every* machine cycle, the CPU performs the following:

a. Pulls IO/$\overline{M}$ low to signify that the machine cycle is a memory reference operation. (The CPU also drives status lines S0 and S1; however, these lines are not used by the SBC 80/05.)

b. Places high-order bits (PCH) of program counter onto address lines A8-A15. These address bits will remain true until at least T_4.

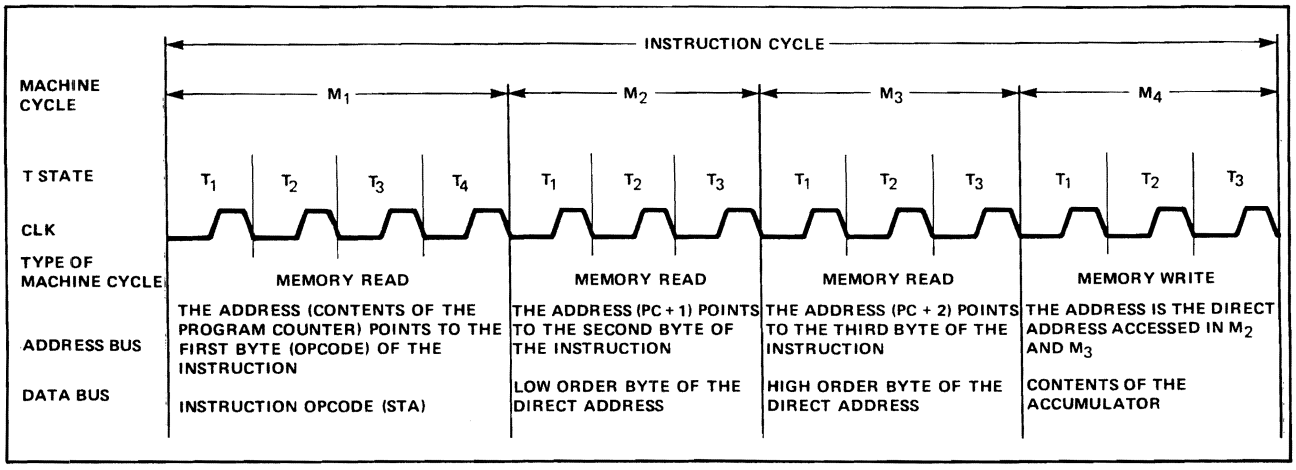

Figure 4-2. Typical CPU Instruction Cycle

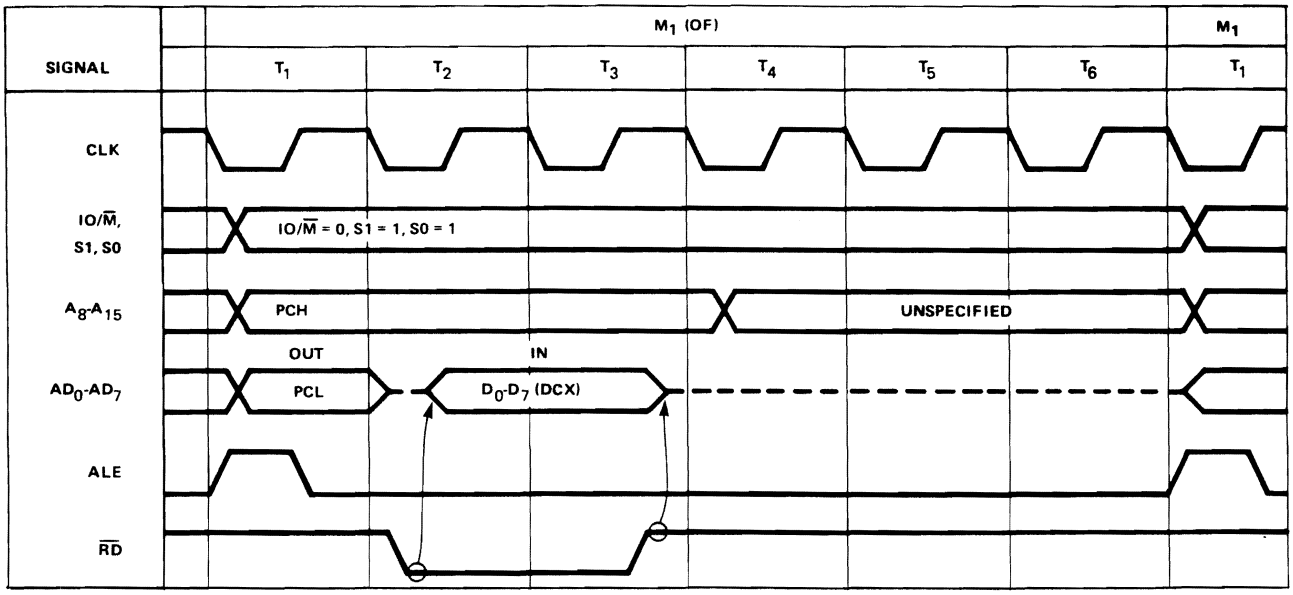

Figure 4-3. Opcode Fetch Machine Cycle

c. Places low-order bits (PCL) of program counter onto address/data lines AD0-AD7. These address bits will remain true for only one clock cycle, after which AD0-AD7 go to their high-impedance state as indicated by the dashed line in figure 4-3.

d. Activates the Address Latch Enable (ALE) signal.

At the beginning of T_2, the CPU pulls the RD/ line low to enable the addressed memory device. The device will then drive the AD0-AD7 lines. After a period of time, as determined by the access time of the addressed memory device, valid data (the DCX instruction in this example) will be present on the AD0-AD7 lines. During T_3 the CPU loads the data on DC0-DC7 into its instruction register and drives RD/ high, disabling the addressed memory device. During T_4 the CPU decodes the opcode and decides whether or not to enter T_5 on the next clock cycle or start a new machine cycle and enter T_1. In the case of the DCX instruction, the CPU will enter T_5 and then T_6 before beginning a new machine cycle.

Figure 4-4 is identical to figure 4-3 with one exception, which is the use of the READY input to the CPU. As shown in figure 4-4, the CPU examines the state of the READY input during T_2. If the READY input is high, the CPU will proceed to T_3 as shown in figure 4-3. If the READY input is low, however, the CPU will enter the T_{wait} state and stay there until READY goes high. When READY goes high, the CPU will exit the T_{wait} state and enter T_3. The external effect of using the READY input is to preserve the exact state of the CPU signals at the end of T_3 for an integral number of clock periods before finishing the machine cycle. This 'stretching' of the system timing, in effect, increases the allowable access time for memory or I/O devices. By inserting T_{wait} states, the CPU can accommodate slower memory or slower I/O devices. A common use of the READY input is to single-step the CPU using a manual switch. It should be noted, however, that access to the on-board memory and I/O ports does not impose a T_{wait} state.

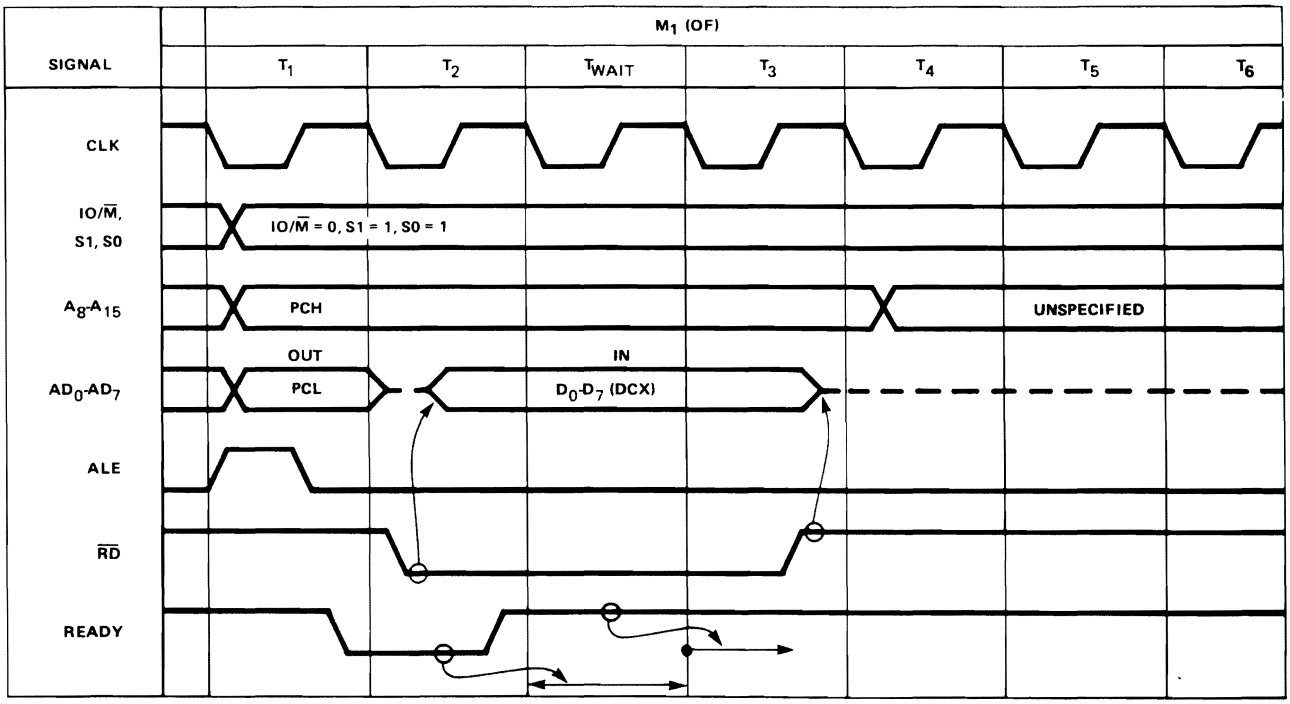

Figure 4-4. Opcode Fetch Machine Cycle (With Wait)

4-8. MEMORY READ TIMING

Figure 4-5 shows the timing of two successive memory read machine cycles, the first without a T_{wait} state and the second with one T_{wait} state. Disregarding the states of the S0 and S1 lines, the timing during T_1 through T_3 is identical with the opcode fetch machine cycle shown in figure 4-3. The major difference between the opcode fetch and memory read cycles is that an opcode fetch machine cycle requires four or six T-states whereas the memory read machine cycle requires only three T-states. One minor difference between the two cycles is that the memory address used for the opcode fetch cycle is always the contents of the program counter (PC), which points to the current instruction; the address used for a memory read cycle can be one of several origins. Also, the data read from memory is placed into the appropriate register instead of the instruction register. Note that a T_{wait} can be imposed by slower memory devices as previously described.

4-9. I/O READ TIMING

Figure 4-5 also illustrates the timing of two successive I/O read machine cycles, the first without a T_{wait} state and the second with one T_{wait} state. With the exception of the IO/$\overline{M}$ status signal, the timing of a memory read cycle and an I/O read cycle is identical. For an I/O read, IO/$\overline{M}$ is driven high to identify that the current machine cycle is referencing an I/O port. One other minor exception is that the address used for an I/O read cycle is derived from the second byte of an IN instruction; this address is duplicated onto both the A8-A15 and AD0-AD7 lines. The data read from the I/O port is always placed in the accumulator specified by the IN instruction. Note that a T_{wait} may be imposed by slower I/O devices as described for slower memory devices.

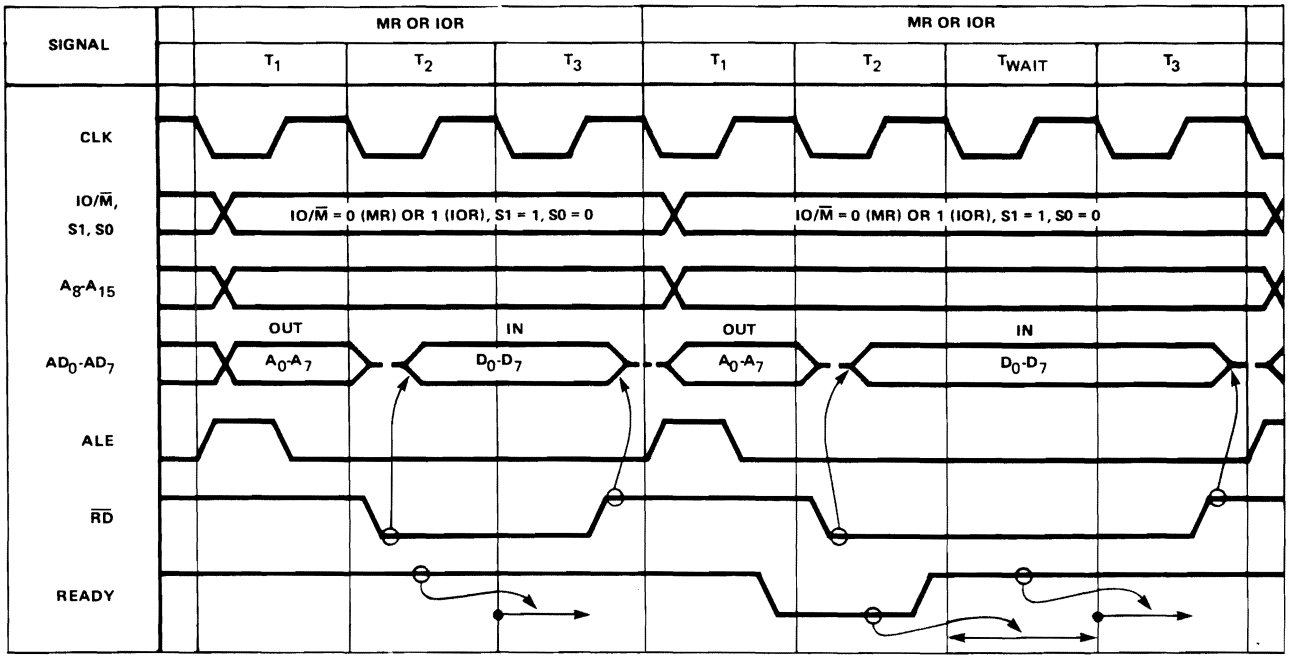

Figure 4-5. Memory Read (or I/O Read) Machine Cycles

4-10. MEMORY WRITE TIMING

Figure 4-6 shows the timing of two successive memory write machine cycles, the first without a T_{wait} state. Again, disregarding the states of the S0 and S1 lines, the timing during T_1 is identical to the timing of an opcode fetch, memory read, and I/O read cycles. The difference occurs, however, at the end of T_1. For instance, in a memory read cycle the AD0-AD7 lines are disabled (high impedance) at the beginning of T_2 in anticipation of the returned data. In a memory write cycle, the AD0-AD7 lines are not disabled and the data to be written into memory is placed on these lines at the beginning of T_2. The Write (WR/) line is driven low at this time to enable the addressed memory device. During T_2 the READY input is checked to determine if a T_{wait} state is required. If the READY input is low, T_{wait} states are inserted until READY goes high. During T_3, the WR/ line is driven high to disable the addressed memory device and terminate the memory write operation. Note that the contents on the address and data lines do not change until the next T_1 state.

4-11. I/O WRITE TIMING

Figure 4-6 also illustrates the timing of two successive I/O write machine cycles, the first without a T_{wait} state and the second with one T_{wait} state. With the exception of the IO/$\overline{M}$ status signal, the timing of a memory write cycle and an I/O write cycle are identical.

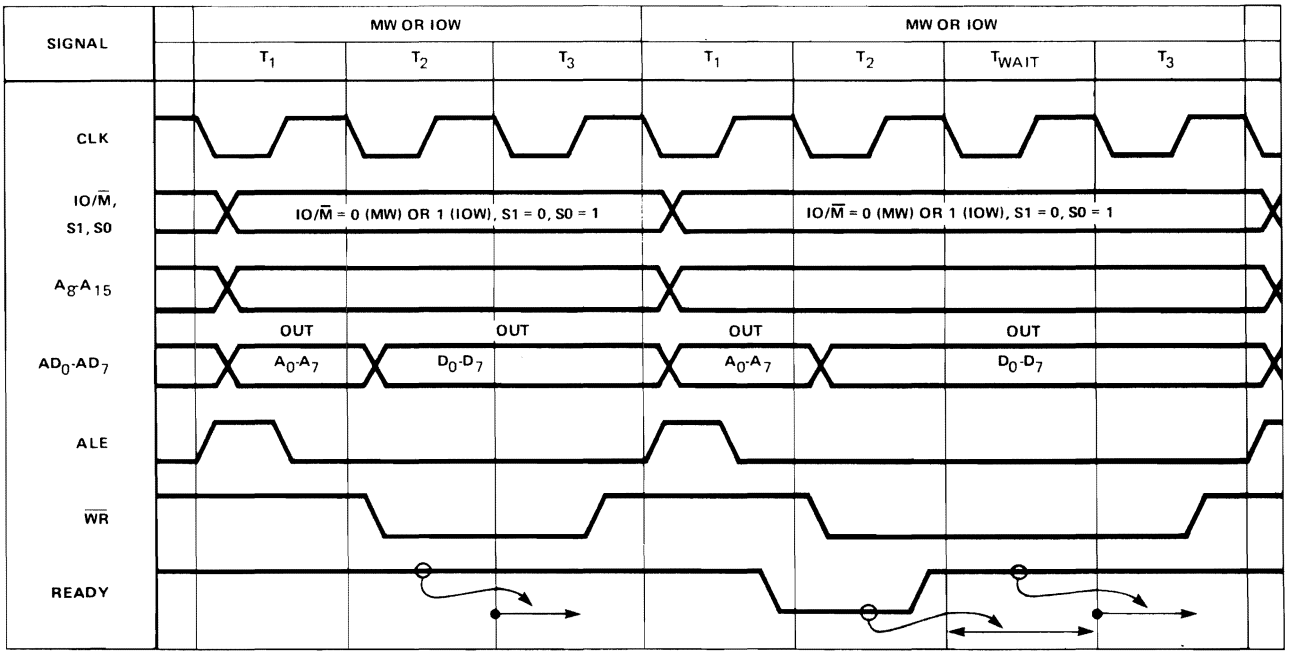

Figure 4-6. Memory Write (or I/O Write) Machine Cycles

4-12. MULTIPLEXED ADDRESS/DATA BUS

The lower eight bits (AD0-AD7) of the memory address or I/O address (depending on whether a memory reference machine cycle or an I/O reference machine cycle is in progress) are output by the CPU during the first clock cycle (T_1). The AD0-AD7 lines become the data bus during the second and third cycles (T_2 and T_3). The trailing edge of the Address Latch Enable (ALE) signal issued by the CPU during T_1 strobes these eight address bits into Demultiplexer A18 (1ZC3) and into RAM/IO/Timer A15 (3ZB6). The low-order address bits (AB0-AB7) from A18 are placed on the SBC 80/05 address bus together with the high-order address bits (AB0-AB7). This 16-bit address bus (AB0-ABF) is distributed to Address Bus Drivers A31-A33 (2ZA2), ROM/EPROM A16-A17 (3ZA5), and RAM A39-A40 (3ZB6).

4-13. MULTIBUS INTERFACE

The Multibus interface consists of unidirectional Address Bus Drivers A31-A33 (2ZA2), bidirectional Data Bus Drivers A34-A35 (2ZB4), and Bus Controller A19 (2ZD4).

Bus Controller A19 arbitrates all requests for control of the Multibus. When the SBC 80/05 acquires control of the Multibus, the Bus Controller generates the appropriate memory or I/O command and enables the address onto the Multibus by enabling the Address Bus Drivers. The Bus Controller also enables the Data Bus Drivers which, depending on whether the operation is a read or write, transfers data from or to the Multibus. The RC network (R8 and C13) connected to the DLYADJ input of the Bus Controller provides a 70-nanosecond delay to ensure an adequate setup and hold relationship between the address/data lines and the appropriate control signals.

The falling edge of the BCLK/ signal provides a timing reference for the bus arbitration logic. Bus arbitration begins when the CPU needs access to an external memory or I/O port. When this requirement occurs, the Command (CMD) and Off-Board Request (OFF BD REQ) are both high at the Transfer Start Request (XSTR) input to the Bus Controller. The Bus Controller drives Bus Request (BREQ/) low and forces Bus Priority Out (BPRO/) high. The BREQ/ output from the master modules is used by the Multibus when the bus priority is resolved by a parallel priority scheme as described in paragraph 2-28. BPRO/ is used by the Multibus when the bus priority is resolved in a serial priority scheme as described in paragraph 2-27.

The SBC 80/05 gains control of the Multibus when the BPRN/ input to the Bus Controller is driven low which, on the next falling edge of BCLK/, drives its BUSY/ and ADEN/ outputs low. The BUSY/ output indicates to all master devices that the bus is in use and prohibits any other master from acquiring control of the bus; the ADEN/ output enables the Address Bus Drivers and Data Bus Drivers. The ADEN/ output also activates the Bus Control (BUS CTL/) signal, which is applied to the input of gate A23-8 (1ZB6). As discussed later, the BUS CTL/ signal is used in conjunction with Transfer Acknowledge (XACK/) to activate the READY input to the CPU.

The Bus Controller now examines the IO/$\overline{M}$, RD/, and WT/ inputs and then outputs the appropriate command signal as follows:

IO/$\overline{M}$	RD/	WT/	BUS COMMAND
0	0	1	Memory Read Command MRDC/
0	1	0	Memory Write Command MWTC/
1	0	1	I/O Read Command IORC/
1	1	0	I/O Write Command IOWC/

If the bus command is either an IORC/ or a MRDC/, the Bus Controller drives its Read Data (RDD) signal high to the Direction Input Enable (DIEN) input of bidirectional Data Bus Drivers A34-A35. When DIEN is driven high, data is transferred from the Multibus to the SBC 80/05. If the bus command is either an IOWC/ or a MWTC/, RDD is driven low and data is transferred from the SBC 80/05 to the Multibus.

The SBC 80/05 can lose control of the Multibus if its BPRN/ input goes high or when the CMD is completed. This causes the Bus Controller Transfer Complete (XCP) input to go low. In no case, however, will the SBC 80/05 lose control of the bus if the transfer is not complete or if the override function is invoked. The override function is discussed under paragraph 4-22. The timing of the bus signals is presented in figures 2-3 and 2-4.

4-14. ON-BOARD MEMORY

The on-board RAM and ROM/EPROM are discussed in following paragraphs. During a machine cycle involving on-board memory, a Memory Advanced Acknowledge (MEM AACK/) signal is generated to maintain the CPU READY input high and prevent the CPU from entering a T_{wait} state. During a matching cycle involving system memory, the CPU must acquire bus control and enter a T_{wait} state until a Transfer Acknowledge (XACK/) signal is received from the addressed memory device via the Multibus.

4-15. READ-ONLY MEMORY. The SBC 80/05 includes two sockets (A16-A17) to accommodate either two 1K by 8-bit or two 2K by 8-bit masked read-only memory (ROM) or programmable ROM (EPROM) chips. A jumper block is installed in position W3 or W4 as required to accommodate the address decoding and power requirements of the particular ROM/EPROM type installed. The address block for 2K of ROM/EPROM (using two 1K chips) is 0000-07FF; the address block for 4K of ROM/EPROM (using two 2K chips) is 0000-0FFF.

If 4K of ROM/EPROM is installed in sockets A16-A17 (3Z5A), the address jumper block is installed in position W3. Socket A17 contains the lower 2K address block (0000-07FF) and socket A16 contains the upper 2K address block (0800-0FFF). The upper and lower address blocks are selected by decoding address bits ABB-ABF. To select either block of ROM/EPROM, ABC-ABF must be false (low). When address bit ABB is low, the lower 2K block is selected; otherwise, the upper 2K block is selected. The target address within the selected 2K block is selected by address bits AB0-ABA.

If 2K of ROM/EPROM is installed in sockets A16-A17, the address jumper block is installed in position W4. Socket A17 contains the lower 1K address block (0000-03FF) and socket A16 contains the upper 1K address block (0400-07FF). The upper and lower address blocks are selected by decoding address bits ABA-ABF. To select either block of ROM/EPROM, ABB-ABF must be false. When address bit ABA is low, the lower 1K block is selected; otherwise, the upper 1K block is selected. The specific address within the selected 1K block is selected by address bits and AB0-AB9.

The actual read operation is initiated during T_2 when the CPU pulls the RD/ line low. The RD/ and IO/$\overline{M}$ signals and ANDed by A23-3 (1ZB2) to produce the Memory Read (MEM RD/) signal, which is driven through A27-8 or A27-12 to the chip select (C/S) input of the appropriate ROM/EPROM chip.

When either type of ROM/EPROM is installed and addressed, NAND-gate A38-3 (3ZA6) is enabled and generates a Memory Advanced Acknowledge (MEM AACK/) signal, which drives the CPU READY input high.

4-16. RANDOM ACCESS MEMORY. The SBC 80/05 includes 512 bytes of static read/write memory: 256 bytes in A39-A40 (3ZB6) and 256 bytes in A15 (3ZC4). Memory address block 3E00-3EFF is contained in A39-A40 and memory address block 3F00-3FFF is contained in A15.

Memory address block 3E00-3EFF is selected when the CE1 and CE2 chip enable inputs to A39-A40 are driven low. The CE1 inputs are driven low when IO/$\overline{M}$ is low, address bits AB9-ABD are high, and address bits ABE-ABF are low. The CE2 inputs are low when address bit AB8 is low.

Memory address block 3F00-3FFF is selected when the IO/$\overline{M}$ input (signifying a memory operation) and the CE chip enable input to A15 are driven low. The CE input to A15 is driven low when IO/$\overline{M}$ is low, address bits AB8-ABD are high, and address bits ABE-ABF are low.

When either of the two blocks of RAM memory is addressed, NAND-gate A38-6 is enabled and generates MEM AACK/, which drives the CPU READY input high.

When A39-A40 is enabled, the target address is specified by address bits AB0-AB7. A memory read or write operation is specified by the R/W input. During a read operation, the CPU Write (WRT/) output is false (high) and a read occurs by default. During a write operation, the CPU WRT/ output is true and a write occurs. The data output of A39-A40 is disabled during a write operation by the false MEM RD/ signal applied to the OD inputs.

When A15 is enabled for a memory operation, the trailing edge of the Address Latch Enable (ALE) signal latches in the target address bits specified by data bus bits DB0-DB7. During a write operation, the CPU WRT/ output is true and a write occurs; during a read operation, the CPU RD/ output is true and a read occurs. Data is read from and written into A15 via its address/data pins AD0-AD7.

4-17. ON-BOARD I/O PORTS AND TIMER

The SBC 80/05 includes three parallel I/O ports, each of which can be hardware configured as an input port or an output port (but not both). One of the three ports (Port 03) can be programmed to provide status information to allow Port 01 and Port 02 to operate in a handshake mode. Whether these three ports are used as input ports or output ports depends on whether the user installs input terminators or output drivers in sockets A4 through A9. (See figure 5-2, sheet 3.)

These three I/O ports, 256 bytes of RAM, and a 14-bit binary down-counter (timer) are contained in A15 (3ZC4). The I/O section of A15 consists of four registers – a Command/Status (C/S) register and one register for each of the three I/O ports.

The timer is a 14-bit down-counter that counts the 122.88-kHz timer (clock) input and outputs either a square wave or a pulse when the Terminal Count (TC) is reached. The three I/O ports and the timer can each be programmed to operate in one of four modes; details of how these modes are used are presented in Chapter 3.

During a machine cycle in which the on-board I/O section or timer is accessed, an I/O Advanced Acknowledge

(I/O AACK) signal is generated to prevent the CPU from entering a T_{wait} state. During a machine cycle involving system I/O, the CPU must acquire bus control and enter a T_{wait} state until a Transfer Acknowledge (XACK/) signal is received from the addressed I/O device via the Multibus.

4-18. **REGISTER ADDRESSING.** The address assignments of the four registers are as follows:

Address	Function
00	Command/Status (C/S)
00	Port 01
02	Port 02
03	Port 03

The CPU timing for I/O read and write machine cycles are described in paragraphs 4-9 and 4-11, respectively. During T_1 the Chip Enable (CE) input to A15 is driven low via NAND-gate A28-3 (3ZC6) when IO/$\overline{M}$ is high and address bits AB3 and ABC-ABF are low. When NAND-gate A28-3 is enabled, the I/O AACK/ signal is enabled and drives the CPU READY input high. When A15 is thus enabled for an I/O operation, the trailing edge of the Address Latch Enable (ALE) signal latches in the register address specified by data bus bits DB0-DB7.

During a read operation, the CPU drives the RD/ output low during T_2 and waits for the addressed register to output data onto the data bus. When the data is valid during T_3, the CPU accepts the data and drives the RD/ output high. During a write operation, the CPU drives the WRT/ output low during T_2 and outputs the data byte on the data bus. The addressed register latches in the data during T_3 when the CPU drives the WRT/ output high.

4-19. *Command/Status Register.* A command is written into the C/S register during a write operation. A command is used to specify either an input or output operation for Ports 01 and 02, define the input/output or control assignment for Port 03, enable or disable the Port 01 and Port 02 interrupts, and output the timer command. The status of Ports 01 and 02 and the timer are read from the C/S register during a read operation. The contents of the C/S register are *not* accessible *except* through software.

4-20. *Port 01 Register.* This eight-bit register can be programmed to be either an input port or an output port depending on the command contents of the C/S register. Also, depending on the contents of the C/S register, this register can operate either in the basic mode or strobed and latched mode as described in Chapter 3.

4-21. *Port 02 Register.* This eight-bit register functions the same as described for Port 01.

4-22. *Port 03 Register.* This six-bit register can be programmed to be an input port, an output port, or as control signals for Ports 01 and 02. (Refer to Chapter 3.) When used as a control port, three bits (PC0-PC2) are assigned for Port 01 and three bits (PC3-PC5) are assigned for Port 02. PC0 and PC3 are interrupts, PC1 and PC4 are buffer status (buffer full), and PC2 and PC5 are port strobe inputs.

When it is desired to use Port 01 in the strobed input mode, Port 03 is programmed as control signals in the ALT 3 or ALT 4 mode. (Refer to Chapter 3.) Thus, the device inputs data to the PA0 through PA7 inputs and then drives the Strobe ($\overline{STB}$) signal low at PC2. Port 01 then drives the Buffer Full (BF) signal high at PC1 to acknowledge receipt of the data. Next, Port 01 drives PC0 high to generate an interrupt request (INTR PORT 01). After the CPU services the interrupt, Port 01 pulls the BF signal low at PC1 to signify that it is ready to accept data.

When it is desired to use Port 02 in the strobed output mode, Port 03 is programmed as control signals in the ALT 4 mode. (Refer to Chapter 3.) Thus, the CPU first performs an I/O write to Port 02 and, when data is accepted by Port 02, it drives the BF signal high at PC4. The output device then drives the $\overline{STB}$ input low to PC5 and accepts the data. After accepting the data, the output device drives $\overline{STB}$ high and then Port 02 drives PC3 to generate an interrupt request (INTR PORT 02).

If jumper W1 is installed in position A-B, Port 03 can be used to invoke the override function to prevent losing control of the Multibus at a critical time. (Refer to paragraph 4-13.) The override function is invoked by first defining Port 03 as an output port, and then performing a write operation to Port 03 with data bit 5 set. The override function will remain in effect (PC5 set) until cleared by the program. This function is also useful where the SBC 80/05 is the only master module in the system. In this application, the SBC 80/05 can save the time it would otherwise take to gain control of the bus. It should be noted that W6 (2ZD5) must be installed in position B-C along with W1 in position A-B when it is desired to have the SBC 80/05 always requesting the bus.

4-23. **TIMER ADDRESSING.** The timer section requires two address bytes: address 04 for the low-order byte and address 05 for the high-order byte. During a write operation, the Count Length Register (bits 13-0) and the timer mode (bits 15-14) are loaded. During a read operation, the contents of the counter (the present count) and the mode bits are read. There are four modes selectable by bits 15-14:

a. Timer Out goes low during the second half of count. Therefore, the count loaded in the Count Length Rerister should be twice the timeout desired.

b. Timer Out remains high until the first half of the count has been completed and goes low for the second half of the count. The count length is automatically reloaded when the terminal count is reached.

c. A single low pulse is generated upon reaching the terminal count; this function is useful for generating real-time clocks.

d. A Divide-by-N Counter generates a repetitive Timer Out low pulse; a new pulse train is initiated every time the terminal count is reached.

Bits 7-6 of the Command/Status (C/S) register are used to start and stop the timer. Details concerning programming the timer section are given in Chpater 3.

4-24. INTERRUPTS. As mentioned in paragraph 4-22, when Port 03 is used as control bits, PC0 and PC3 are used for Port 01 and Port 02 interrupts. These interrupts, plus the TIMER out signal, are routed to interrupt select jumper pad W5. From W5 these interrupts may be connected to the CPU interrupt inputs or to the Multibus via jumper pad W9. (See paragraphs 2-20 through 2-24.)

4-25. SERIAL I/O COMMUNICATION

Serial in and serial out communication is implemented by software RIM and SIM instructions, respectively. For TTL level serial I/O, input data is received at the SID input of the CPU via inverter A22-2 (1ZD6); data from the SOD output of the CPU is transmitted via inverter A22-4.

For RS232C serial I/O, serial input data is inverted and converted to TTL level by A10-3; the output of A10-3 is applied to the SID/ input of the CPU via inverter A22-2. For RS232C serial output, the output of A22-4 is inverted and converted to RS232C level by A11-3.

It is possible to transmit data simultaneously to both a TTL and an RS232C device; however, it is not possible to receive data simultaneously from the two different sources.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides service diagrams and reshipment instructions for the SBC 80/05.

5-2. SERVICE DIAGRAMS

The SBC 80/05 parts location diagram and schematic diagram are given in figures 5-1 and 5-2, respectively. The schematic diagram consists of three sheets, each of which includes grid coordinates. Signals that transverse from one sheet to another are assigned grid coordinates at both the signal source and signal destination. For example, the grid coordinates 2ZD8 locate a signal source (or signal destination) on sheet 2 in Zone D8.

A signal mnemonic that ends with a virgule (slash, slant, solidus) denotes that the signal is active low ($\leq$ 0.4V). Conversely, a signal mnemonic without a virgule denotes that the signal is active high ($\leq$ 2.0V).

Included for reference are schematic diagrams of the SBC 604 termination backplane (figure 5-3) and the SBC 614 expansion backplane (figure 5-4).

5-4. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the MCSD Technical Support Center in Santa Clara, California at one of the following numbers:

Telephone:

From Alaska or Hawaii —
(408) 987-8080

From locations within California call toll free —
(800) 672-3507

From all other U.S. locations call toll free —
(800) 538-8014

TWX: 910-338-0029 or 910-338-0255

TELEX: 34-6372

Always contact the MCSD Technical Support Center before returning a product to Intel for service or repair. You will be given a "Repair Authorization Number", shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment from Intel, or if the product is out of warranty, a purchase order is necessary in order for the MCSD Technical Support Center to initiate the repair.

In preparing the product for shipment to the MCSD Technical Support Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by MCSD Technical Support Center personnel.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

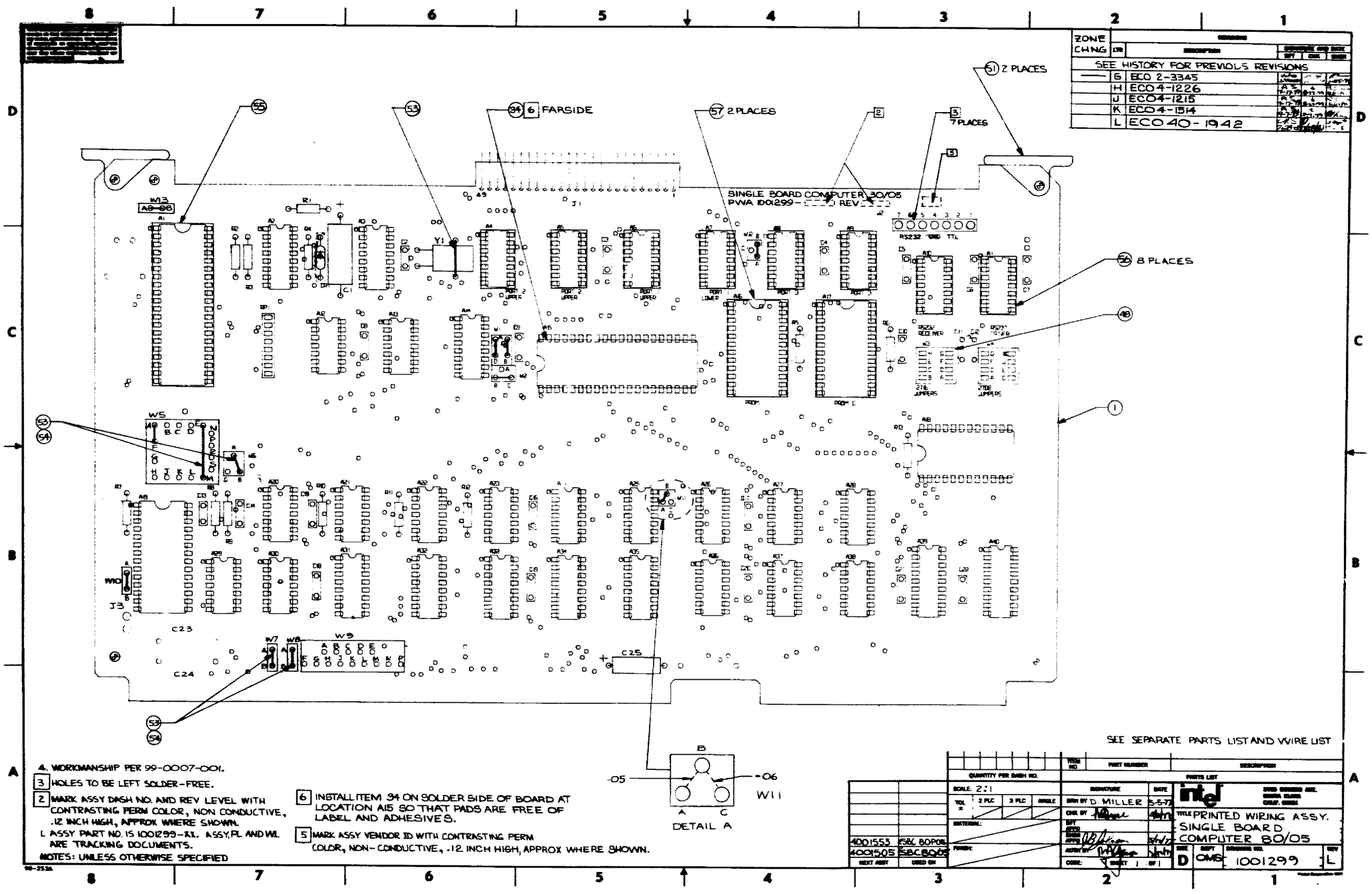

Figure 5-1. SBC 80/05 Parts Location Diagram

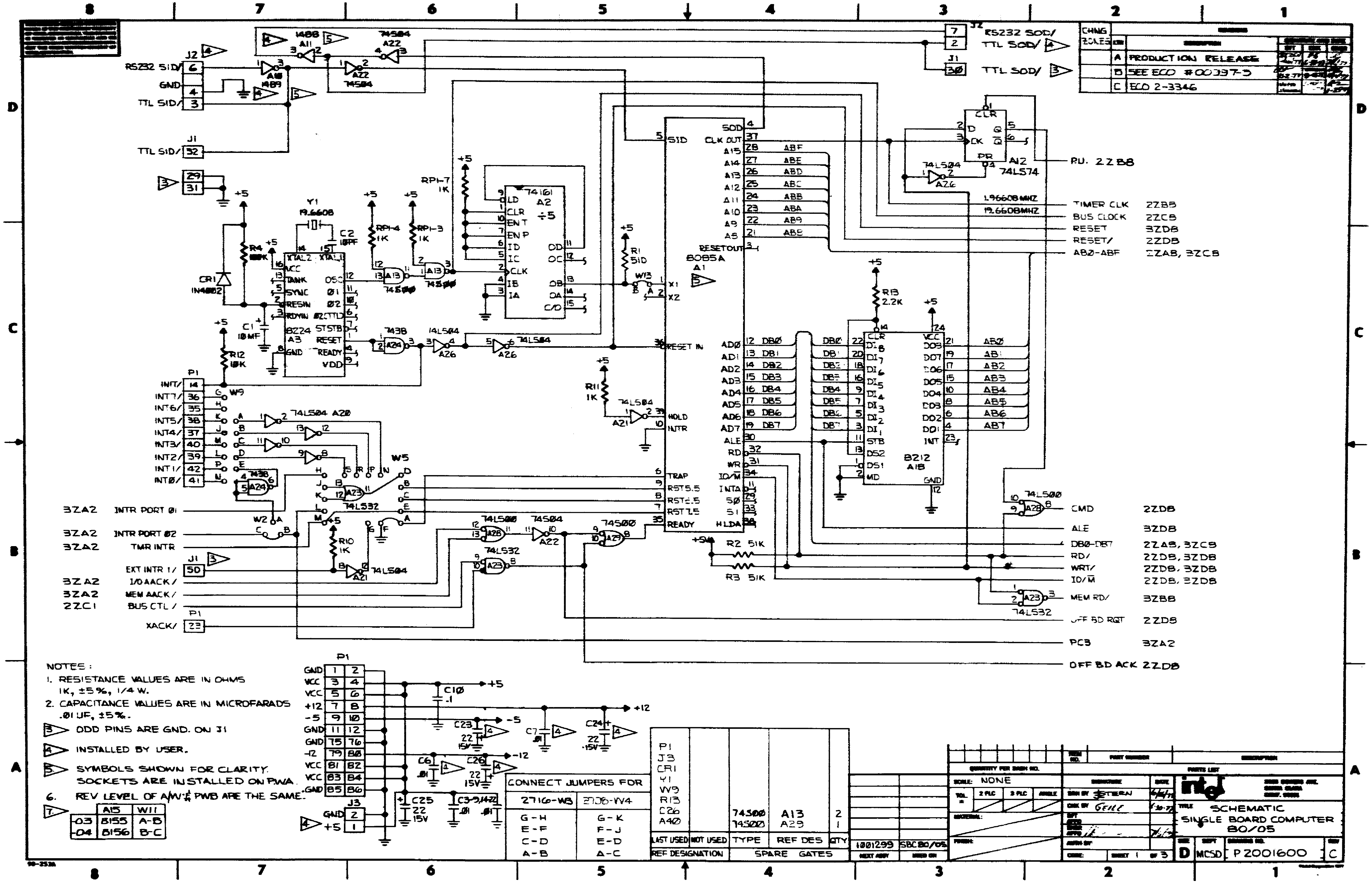

Figure 5-2. SBC 80/05 Schematic Diagram (Sheet 1 of 3)

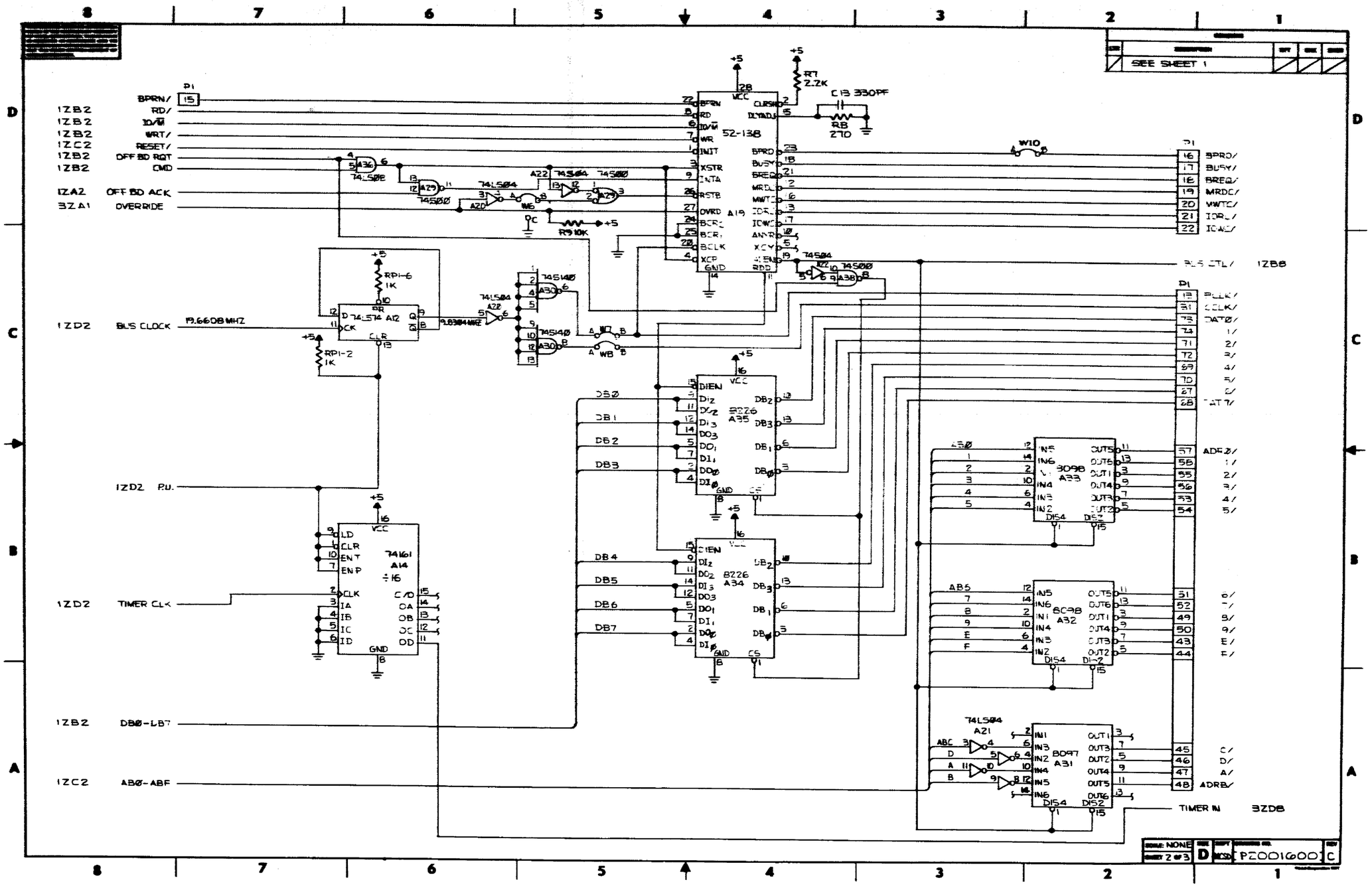

Figure 5-2. SBC 80/05 Schematic Diagram (Sheet 2 of 3)

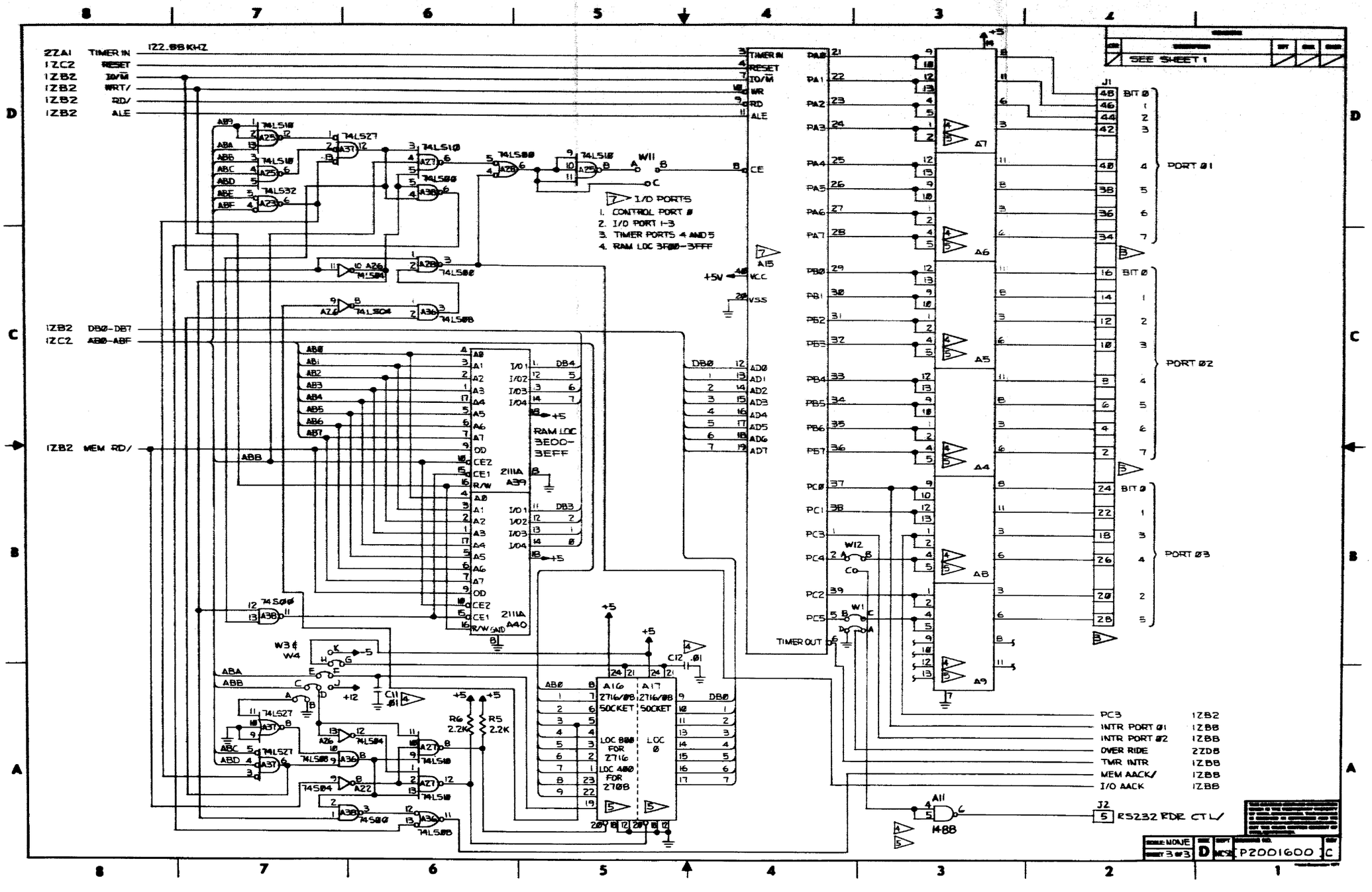

Figure 5-2. SBC 80/05 Schematic Diagram (Sheet 3 of 3)

APPENDIX A
TELETYPEWRITER MODIFICATIONS

A-1. INTRODUCTION

This appendix provides information required to modify a Model ASR-33 Teletypewriter for use with certain Intel iSBC 80 computer systems.

A-2. INTERNAL MODIFICATIONS

WARNING

Hazardous voltages are exposed when the top cover of the teletypewriter is removed. To prevent accidental shock, disconnect the teleprinter power cord before proceeding beyond this point.

Remove the top cover and modify the teletypewriter as follows:

a. Remove blue lead from 750-ohm tap on current source resistor, reconnect this lead to 1450-ohm tap. (Refer to figures A-1 and A-2.)

b. On terminal block, change two wires as follows to create an internal full-duplex loop (refer to figures A-1 and A-3):

   1. Remove brown/yellow lead from terminal 3; reconnect this lead to terminal 5.
   2. Remove white/blue lead from terminal 4; reconnect this lead to terminal 5.

c. On terminal block, remove violet lead from terminal 8; reconnect this lead to terminal 9. This changes the receiver current level from 60 mA to 20 mA.

A relay circuit card must be fabricated and connected to the paper tape reader drive circuit. The relay circuit card to be fabricated requires a relay, a diode, a thyractor, a small 'vector' board for mounting the components, and suitable hardware for mounting the assembled relay card.

A circuit diagram of the relay circuit card is included in figure A-4; this diagram also includes the part numbers of the relay, diode, and thyractor. (Note that a 470-ohm resistor and a 0.1 F capacitor may be substituted for the thyractor.) After the relay circuit card has been assembled, mount it in position as shown in figure A-5. Secure the card to the base plate using two self-tapping screws. Connect the relay circuit to the distributor trip magnet and mode switch as follows:

a. Refer to figure A-4 and connect a wire (Wire 'A') from relay circuit card to terminal L2 on mode switch. (See figure A-6.)

b. Disconnect brown wire shown in figure A-7 from plastic connector. Connect this brown wire to terminal L2 on mode switch. (Brown wire will have to be extended.)

c. Refer to figure A-4 and connect a wire (Wire 'B') from relay circuit board to terminal L1 on mode switch.

A-3. EXTERNAL CONNECTIONS

Connect a two-wire receive loop, a two-wire send loop, and a two-wire tape reader control loop to the external device as shown in figure A-4. The external connector pin numbers shown in figure A-4 are for interface with an RS232C device.

A-4. iSBC 530 TTY ADAPTER

The iSBC 530 TTY adapter, which converts RS232C signal levels to an optically isolated 20 mA current loop interface, provides signal translation for transmitted data, received data, and a paper tape reader relay. The iSBC 530 TTY adapter interfaces an Intel iSBC 80 computer system to a teletypewriter as shown in figure A-8.

The iSBC 530 TTY adapter requires +12V at 98 mA and -12V at 98 mA. An auxiliary supply must be used if the iSBC 80 system does not supply this power. A schematic diagram of the iSBC 530 TTY adapter is supplied with the unit. The following auxiliary power connector (or equivalent) must be procured by the user:

Connector, Molex 09-50-7071
Pins, Molex 08-50-0106
Polarizing Key, Molex 15-04-0219

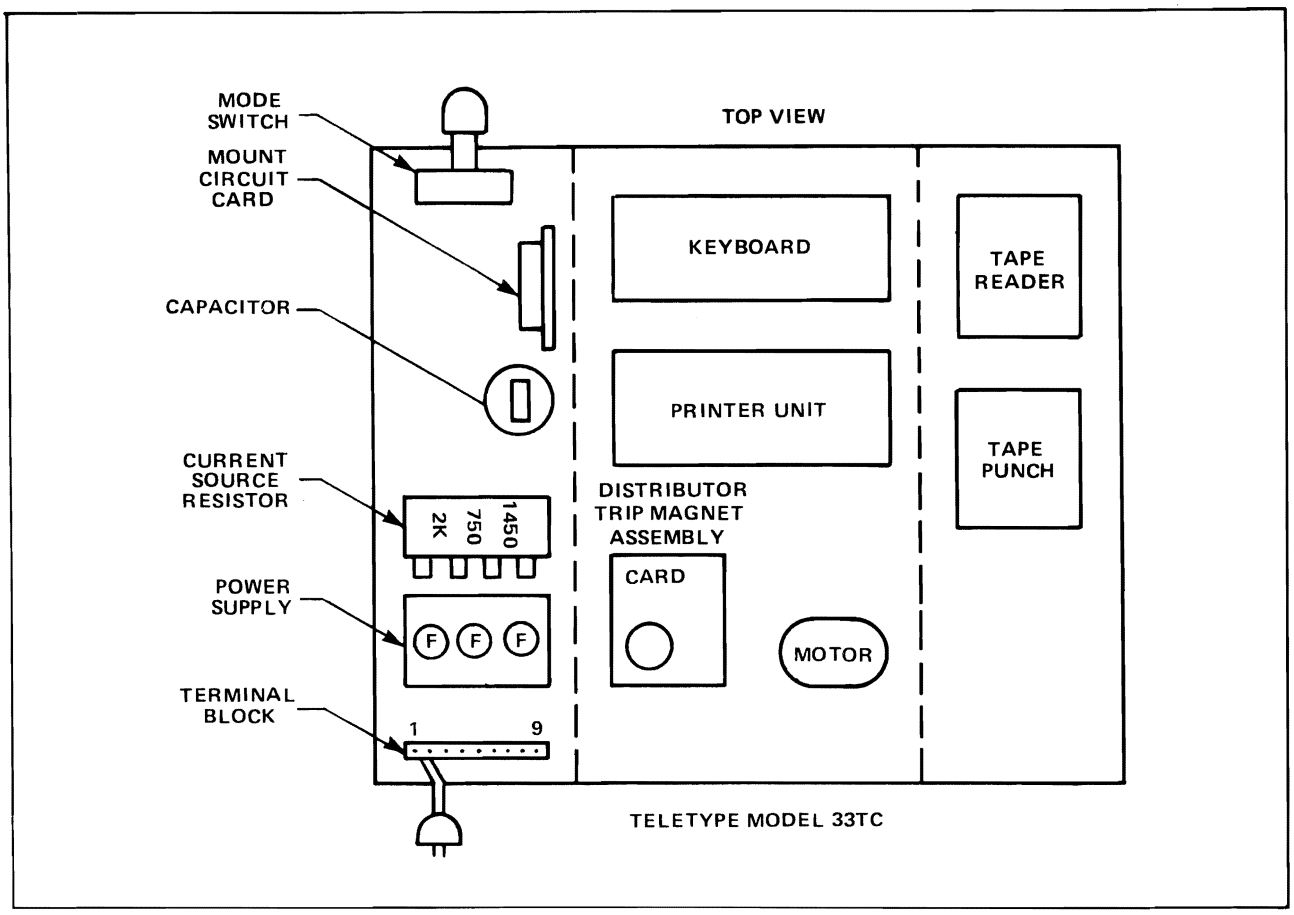

Figure A-1. Teletype Component Layout

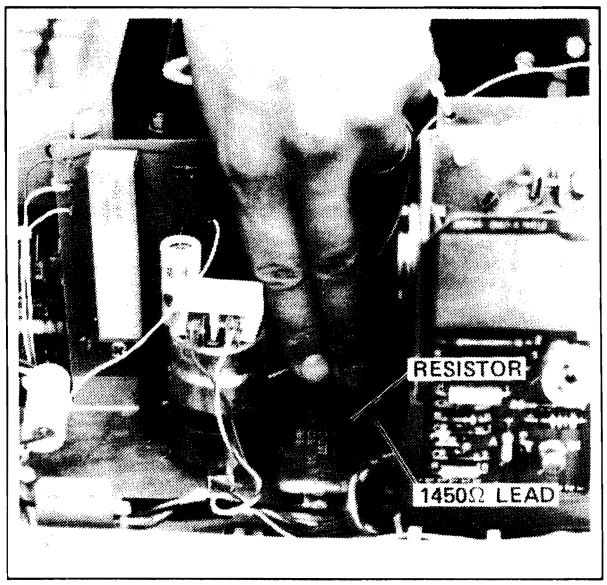

Figure A-2. Current Source Resistor

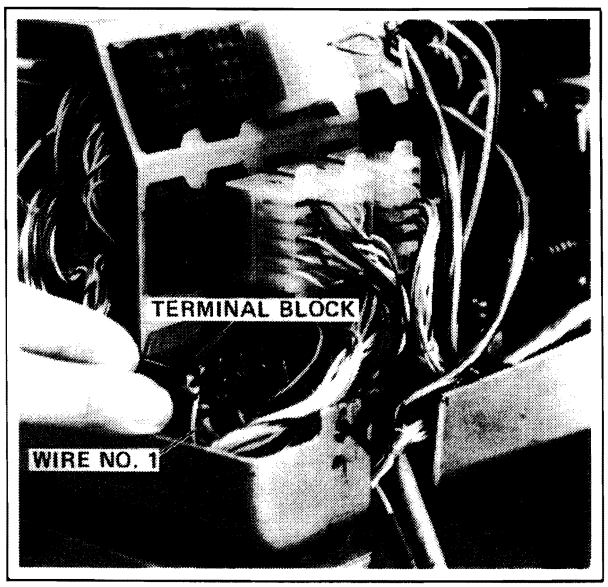

Figure A-3. Terminal Block

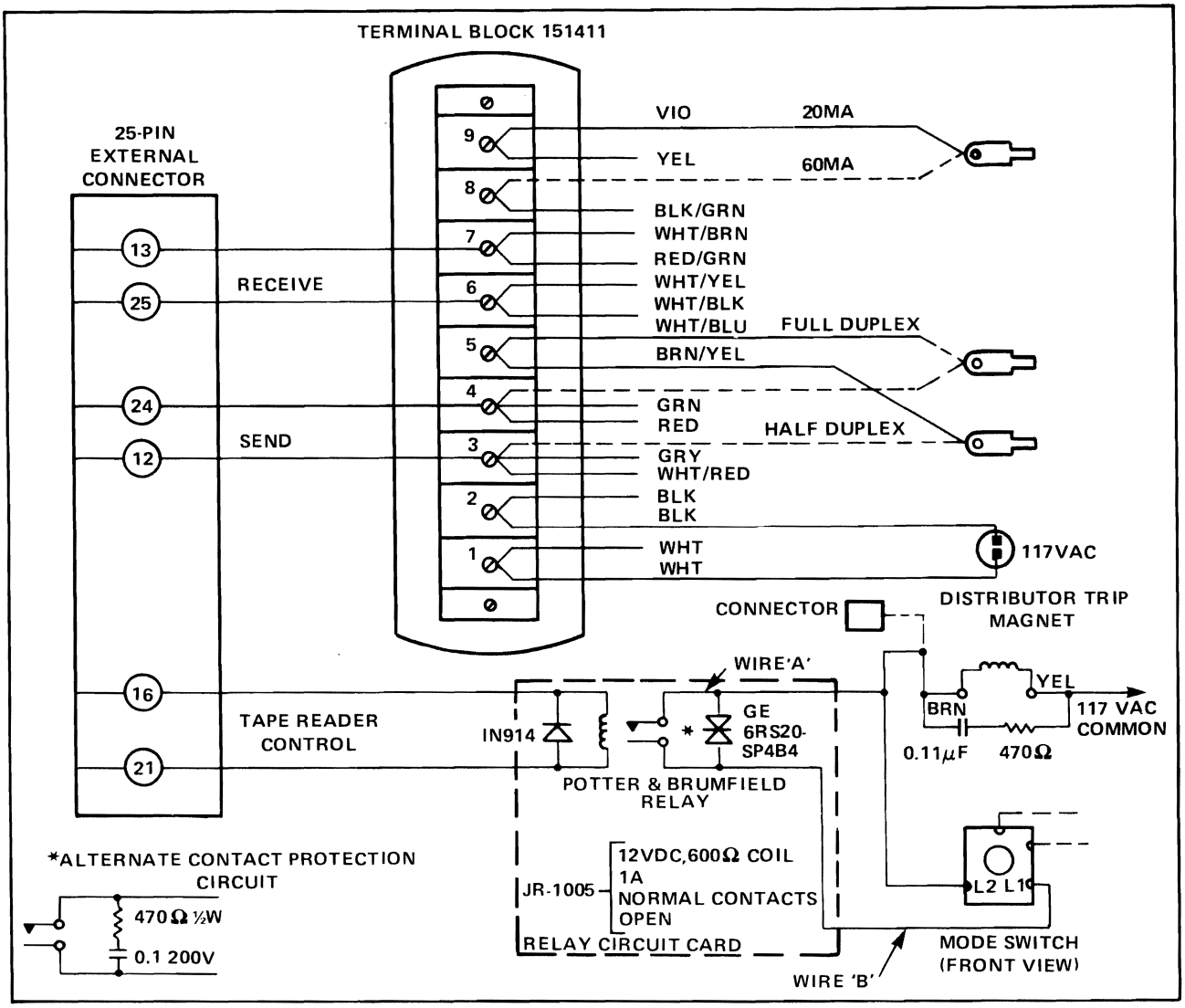

Figure A-4. Teletypewriter Modifications

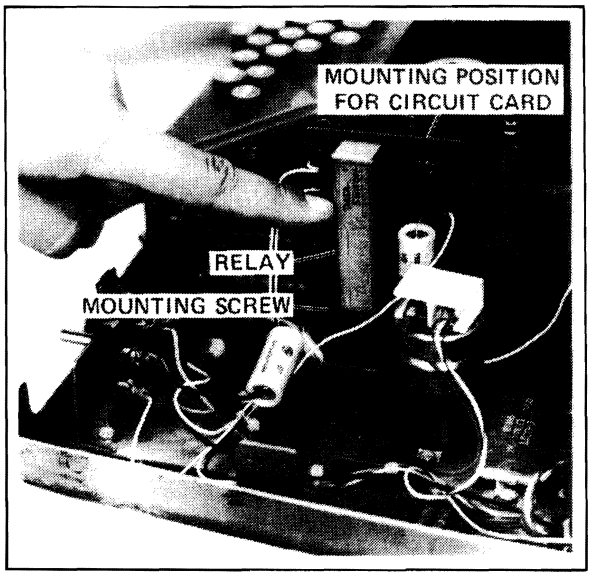

Figure A-5. Relay Circuit

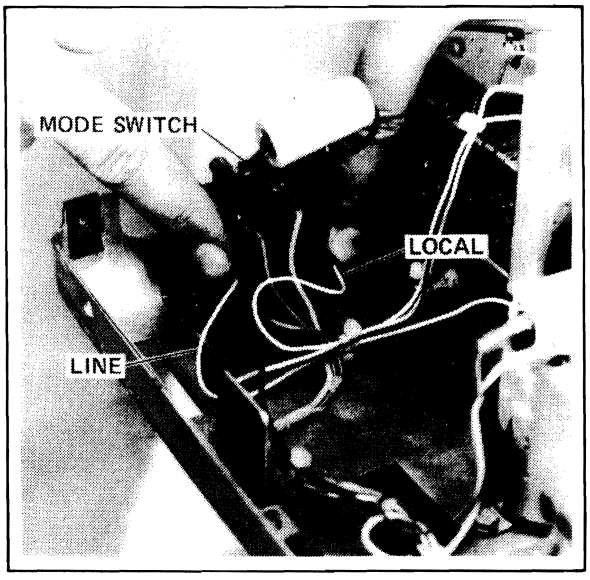

Figure A-6. Mode Switch

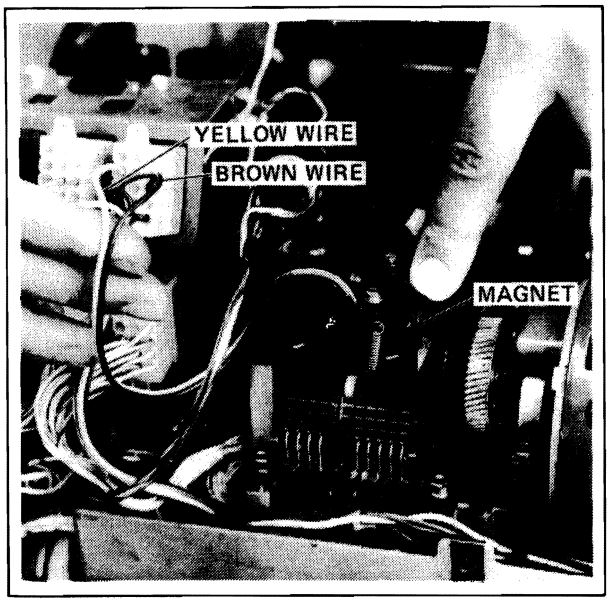

Figure A-7. Distributor Trip Magnet

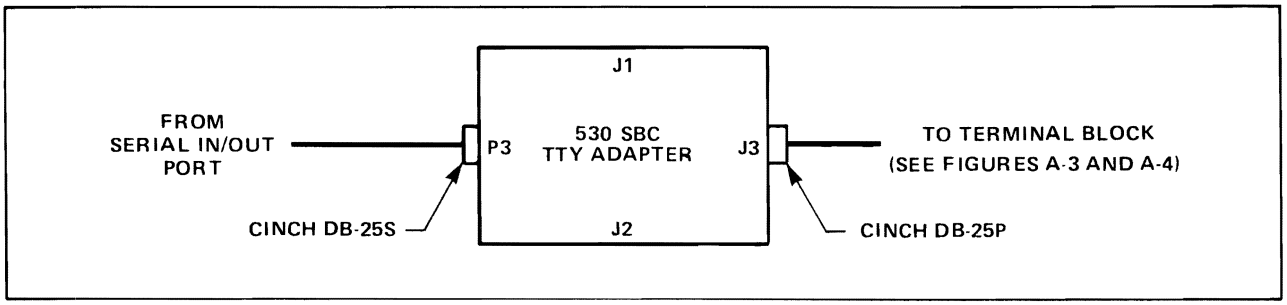

Figure A-8. TTY Adapter Cabling