SBC 202
DOUBLE DENSITY DISKETTE CONTROLLER HARDWARE REFERENCE MANUAL

Order Number: 9800420A

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PREFACE

This manual provides general information, preparation for use, principles of operation, and service information for the Intel SBC 202 Double Density Diskette Controller. The information presented herein is adequate to support normal installation and programming needs. Additional system information is available in the following documents.

- Intel SBC 80 Single Board Computer Hardware Reference Manual.
- Intel System 80 Microcomputer Hardware Reference Manual.
- Intel Series 3000 Microprogramming Manual, Part No. 98-210A.
- Intel Series 3000 Reference Manual, Part No. 98-221A.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The Intel SBC 202 Double Density Diskette Controller provides control for interfacing up to four flexible diskette drives to any Intel SBC 80 Single Board Computer or System 80. The controller has been implemented with Intel's Series 3000 Bipolar Computing Elements. The SBC 202 provides a high-speed, efficient, and easy to use high capacity random access bulk storage interface. All DMA logic is provided so that no additional board or circuitry are required. Figure 1-1 is a block diagram of a typical system with an SB 202.

The SBC 202 has been designed to be compatible with most double density specified flexible diskette drives. The controller facilitates recording all data in soft-sector format. The microprogrammed track format consists of 52 records with 128 bytes/record. The Shugart SA 800-1 Drive is fully compatible with this dense track format due to its "straddle-erase" magnetic head. Use of other manufacturers' flexible disk drives is also accommodated, with the limitation that after any "write data" operation, the CPV must delay 500 microseconds before issuing another read or write command. Therefore, use of multi-sector "write data" commands is only possible with the SA 800-1.

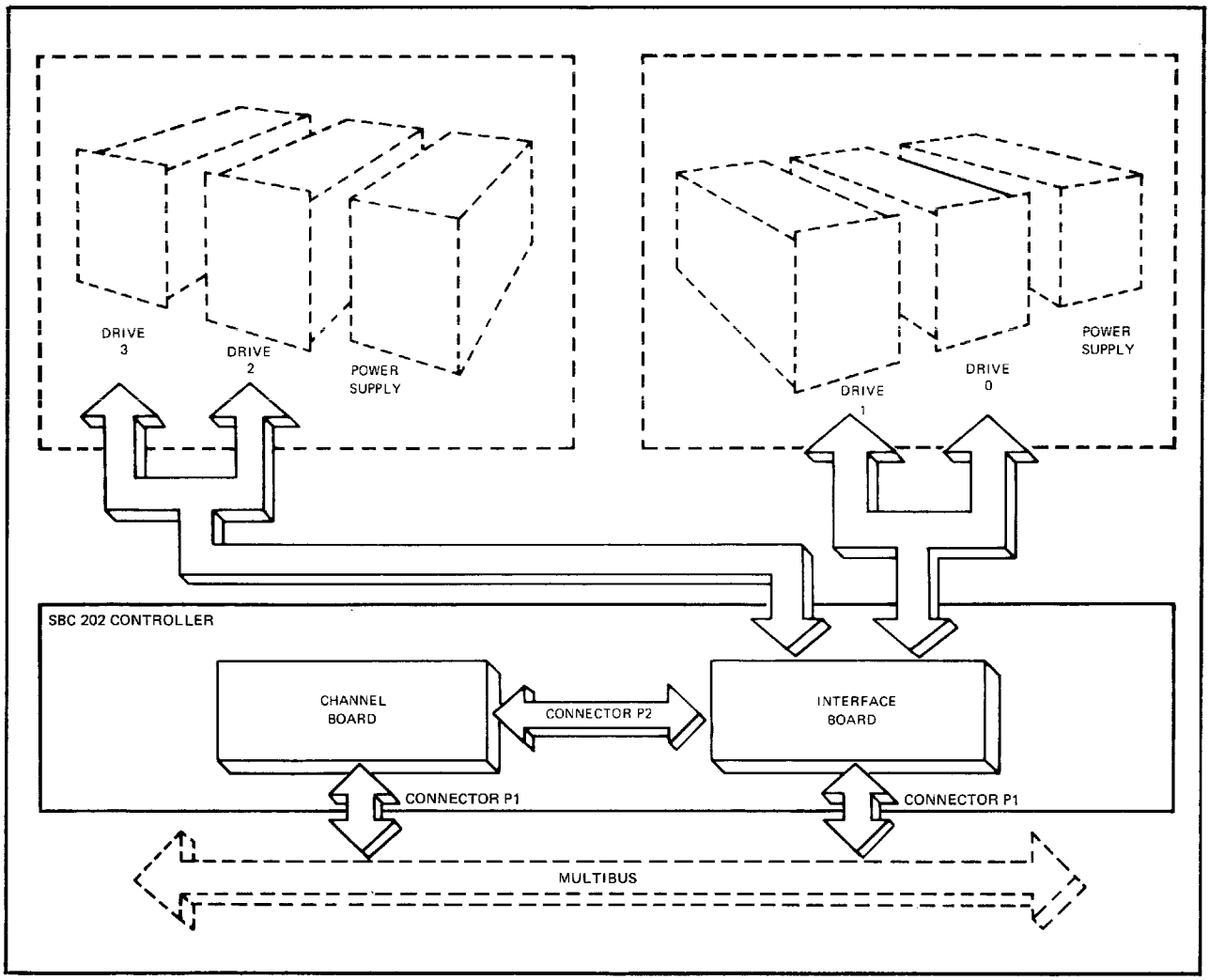


Figure 1-1. Typical System Block Diagram

1-2. DESCRIPTION

The SBC 202 Controller consist of two boards—the Channel Board and Interface Board. These boards may reside in the System 80 chassis, the SBC 604 or 614 Module Cardcage, or in the customer's own custom designed SBC 80 bus-compatible backplane. The Channel Board and the Interface Board are discussed in detail below.

1-3. CHANNEL BOARD

The Channel Board is the primary control module within the diskette controller. It receives, decodes, and responds to channel commands from the Central Processor Unit (CPU) on the Intel SBC 80 Single Board Computer. The Channel Board can access a block of system memory to determine the particular diskette operations to be performed and fetch the parameters required for the successful completion of the specified operation.

The control functions of the Channel Board have been achieved with an 8-bit microprogrammed processor, designed with Intel's Series 3000 Bipolar Microcomputer Set. This 8-bit processor includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit, and 512 × 32 bits of 3604 programmable read-only memory (PROM) which stores the microprogram. It is the execution of the microprogram by the microcomputer set which actually effects the control capability of the Channel Board.

1-4. INTERFACE BOARD

The Interface Board provides the SBC 202 Double Density Diskette Controller with a means of communication with the diskette drives, as well as with the Intel SBC 80 Multibus.

Under control of the mieroprogram being executed on the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), cause the head to move to the proper track, and verify successful operation. The Interface Board accepts the data being read off the diskette, interprets synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and then transfers the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times, and generates the CRC characters which are then appended to the data.

When the diskette controller requires access to the system memory, the Interface Board requests and maintains DMA transfer control of the system bus, and generates the appropriate memory command. The Interface Board also acknowledges I/O commands as required by the Intel SBC 80 Multibus.

The diskette controller is capable of performing seven different operations: recalibrate, seek, format track, write data, write deleted data, read data, and verify CRC.

1-5. SPECIFICATIONS

Table 1-1 lists the physical and performance characteristics of the SBC 202.

1-6. TERMINOLOGY

Whenever a signal is active-low, its mnemonic is followed by a slash; for example MRDC/ means that the level on that line will be low when the memory read command is true (active). If the signal is subsequently inverted, thus making it active-high, the slash is omitted; for example, MRDC means that the level on that line will be high when the memory command is true.

Table 1-1. Specifications

MEDIA (Flexible Diskette)	
Recording Surface:	One
Tracks/Diskette:	77
Sectors/Track:	52
Bytes/Sector:	128
PHYSICAL CHARACTERISTICS	
Mounting:	Occupies two slots of System 80 Chassis or SBC 604/614 Cardcage.
Dimensions (each board);	
Height:	6.75 in. (17.15 mm)
Width:	12.00 in. (30.48 mm)
Depth:	0.50 in. (1.27 mm)
ELECTRICAL CHARACTERISTICS	
DC Power Requirements:	
Channel Board:	5V @ 3.75A (typ), 5A (max)
Interface Board:	5V @ 1.5A (typ), 2.5A (max) -5V @ 0.1A (typ), 0.2A (max)
ENVIRONMENTAL CHARACTERISTICS	
Temperature	
Operating:	0°C to 55°C
Non-Operating:	-55°C to +85°C
Humidity:	
Operating:	Up to 90% relative humidity without condensation.
Non-Operating:	All conditions without condensation of water or frost.

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the SBC 202 Double Density Diskette Controller. The instructions include unpacking and inspection; installation considerations such as power and cooling requirements, physical dimensions, bus interface requirements, ac and dc signal characteristics, and switch and jumper configurations.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel Technical Support Center (see paragraph 5-3) to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The Diskette Controller is designed to interface an Intel SBC 80 Single Board Computer System 80 based product with a Double Density Diskette such as the Shugart SA 800-1 Drive. Important interfacing criteria are presented in the following paragraphs.

2-4. POWER REQUIREMENTS

The Diskette Controller requires +5V (±0.25V) at 7.5A maximum and -5V (±0.25V) at 0.2A maximum. For installation in an SBC 80 Single Board Computer based system ensure that the system power supply has sufficient current overhead to accommodate the additional requirements.

2-5. COOLING REQUIREMENT

The Diskette Controller dissipates 522 kilogram-calories/hour (131.5 BTU/hour) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F).

Exercise caution in locating the Diskette Drives. The SA 800-1 dissipates 1046 kilogram-calories/hour (314 BTU/hour) for each drive. Provide adequate ventilation to permit the convective dissipation of heat from the system components.

2-6. PHYSICAL DIMENSIONS

Physical dimensions of the Diskette Controller are specified in table 1-1.

2-7. INTERFACE REQUIREMENTS

The Channel and Interface Boards each communicate with the Multibus through a standard 86-pin double-sided PC edge connector (P1), 0.156" contact centers (see figure 2-1). CONTROL DATA CORPORATION'S VPB01E43A00A1 is one suitable type of connector for P1. The two controller boards communicate with each other via a 60-pin, double-sided PC edge connector, 0.1" contact centers (see figure 2-1). CDC97169001 is one suitable type of connector for P2. Both boards also include a 100-pin, double-sided PC edge connector (J1), 0.1" contact centers (see figure 2-1). VIKING 3VH50/1JN5 is one suitable type of connector for J1. The Channel Board only uses its J1 connector as a means of accessing various test points on the board. The Interface Board, however, communicates with the diskette drives(s) via its J1 connector. The Interface Board's J1 connector also allows access to various test points. Pin allocations for each of the connectors on the Channel Board are provided in tables 2-1 and 2-2. The same information for the Interface Board is provided in tables 2-3 thru 2-5.

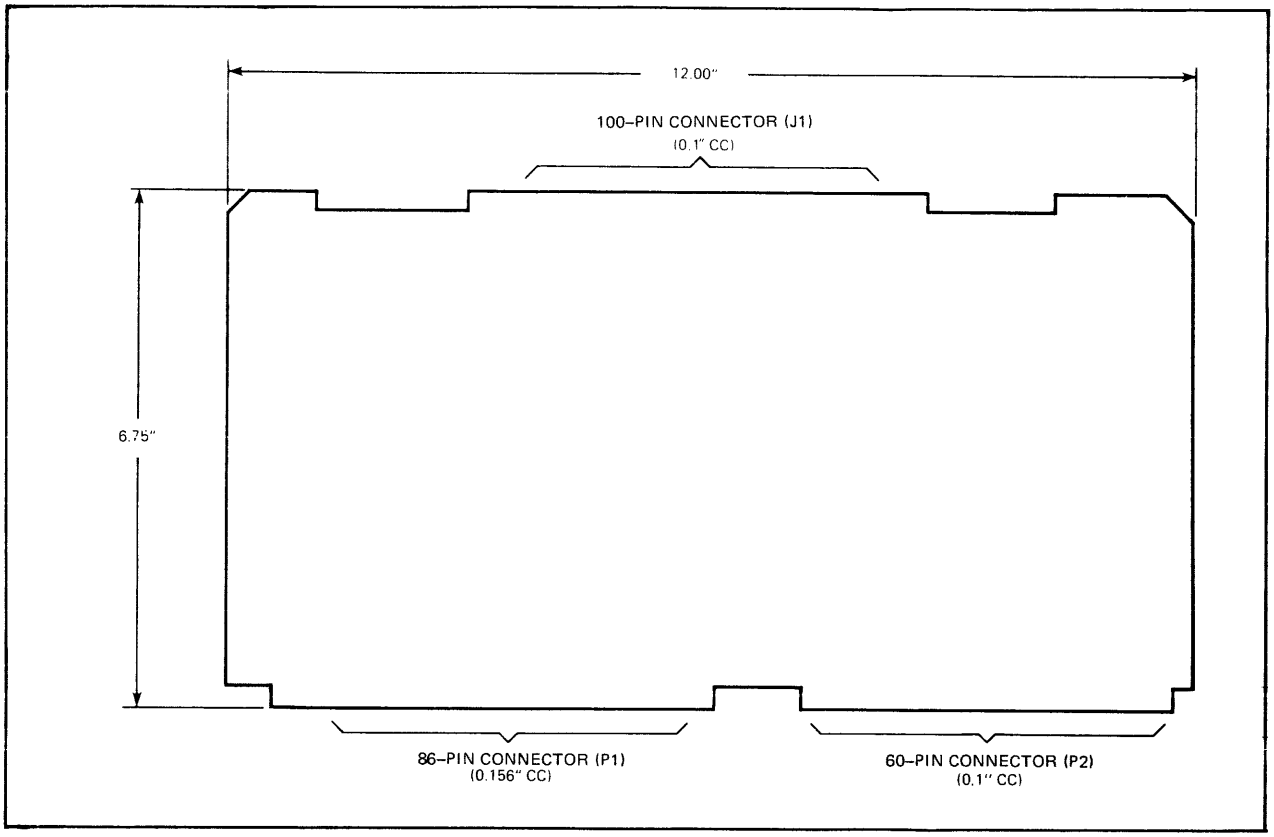


Figure 2-1. Channel and Interface Board Connectors

Table 2-1. Channel Board P1 Connector Pin Assignments

PIN	SIGNAL	FUNCTION
1 2	GND	Power
3 4 5 6	+5V	
7 8 9 10	NO CONNECTION	
11 12	GND	
13 THRU 42	NO CONNECTION	

Table 2-1. Channel Board P1 Connector Pin Assignments (Continued)

PIN	SIGNAL	FUNCTION
43	ADRE/	ADDRESS lines
44	ADRF/	
45	ADRC/	
46	ADRD/	
47	ADRA/	
48	ADRB/	
49	ADR8/	
50	ADR9/	
51	ADR6/	
52	ADR7/	
53	ADR4/	
54	ADR5/	
55	ADR2/	
56	ADR3/	
57	ADR0/	
58	ADR1/	
59	DATE/	DATA lines
60	DATF/	
61	DATC/	
62	DATD/	
63	DATA/	
64	DATB/	
65	DAT8/	
66	DAT9/	
67	DAT6/	
68	DAT7/	
69	DAT4/	
70	DAT5/	
71	DAT2/	
72	DAT3/	
73	DAT0/	
74	DAT1/	
75	GND	Power
76		
77	NO CONNECTION	
78		
79		
80		
81	+5V	
82		
83		
84		
85	GND	
86		

Table 2-2. Channel Board P2 Connector Pin Assignments

PIN	SIGNAL	FUNCTION
1	–	–
2	MK4	Mask bit 4
3	CLK1/	Diskette controller clock 1
4	MK1	Mask bit 1
5	–	–
6	SR CLK IN 1	Serial clock input line
7	–	–
8	CLK SR STB	Serial clock strobe
9	USA	Unit select bit A
10	SR CLK OUT	Serial clock out line
11	TRACK 00/	Track 00 detected
12	USB	Unit select bit B
13	MKØ	Mask bit 0
14	DSK WRT PROT/	Disk write protected
15	DR0/	Drive 0 ready
16	DOR/	Data overrun error
17	DR1/	Drive 1 ready
18	WRT ERR/	Write error
19	SR OUT	Write data multiplexer control level
20	SEL DR NRDY/	Selected drive not ready
21	DEC OUT 0/	Control decoder output 0
22	SR DATA IN/	Serial data in line
23	ID1/	Input data bit 1
24	DATA SR STB	Serial data strobe
25	SR DATA OUT	Serial data out line
26	ID0/	Input data bit 0
27	DEC OUT 5/	Control decoder 5 output
28	DEC OUT 4/	Control decoder 4 output
29	STB MEM IN	Strobe memory data in
30	CLK2/	Diskette controller clock 2
31	SET STOP/	'Stop diskette' channel command
32	ENABLE	Diskette controller addressed
33	DEC OUT 7	Control decoder output 7
34	MK3	Mask bit 3
35	DEC OUT 6	Control decoder output 6
36	MK6	Mask bit 6
37	RD RI/	'Read result type' channel command
38	TIME OUT	10 msec. timing pulse
39	XFER REQ/	Controller requests Multibus
40	INT/	Interrupt line
41	AZ	All zeros, valid CRC check
42	INDEX	Index mark detected

Table 2-2. Channel Board P2 Channel Pin Assignments (Continued)

PIN	SIGNAL	FUNCTION
43	SELECTED	Controller has control of Multibus
44	GATE LOWER	Input low-order data byte
45	BUSY START	Microprogram responding to channel command
46	MR/	Master reset
47	WSUB2/	Not used at present
48	WSUB1/	Not used at present
49	RESET/	'Reset' channel command
50	MK2	Mask bit 2
51	MEM WRT	Write data to Multibus memory
52	DEC OUT 1/	Control decoder output 1
53	WRT CMD	I/O write command
54	MK5	Mask bit 5
55	WRT GT	Write gate control level
56	MR	Master reset
57	RD INT/	'Read subsystem status' command
58	F	Shift registers are full or empty
59	–	–
60	RD CMD	I/O read command

Table 2-3. Interface Board P1 Connector Pin Assignments

PIN	SIGNAL	FUNCTION
1	GND	Power
2		
3	+5 V	
4		
5		
6		
7	NO CONNECTION	
8		
9	-5V	
10		
11	GND	
12		
13	BCLK/	Bus clock (9.803 MHz)
14	INIT/	System initialization
15	BPRN/	Bus priority in
16	BPRO/	Bus priority out
17	BUSY/	Bus busy
18	BREQ/	Bus request
19	MRDC/	Memory read command
20	MWTC/	Memory write command
21	IORC/	I/O read command
22	IOWC/	I/O write command
23	XACK/	Transfer acknowledge
24	NO CONNECTION	
25		
26		
27		
28		
29		
30		
31	CCLK/	Common clock (9.803 MHz)
32	NO CONNECTION	
33		
34		
35	INT6/	Priority interrupt request lines
36	INT7/	
37	INT4/	
38	INT5/	
39	INT2/	
40	INT3/	
41	INT0/	
42	INT1/	
43	NO CONNECTION	
44		
45		
46		
47		
48		

Table 2-3. Interface Board P1 Connector Pin Assignments (Continued)

PIN	SIGNAL	FUNCTION
49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74	NO CONNECTION	
75 76	GND	Power
77 78 79	NO CONNECTION	
80 81 82 83 84	+5 V	
85 86	GND	

Table 2-4. Interface Board P2 Connector Pin Assignments

PIN	SIGNAL	FUNCTION
1	—	—
2	MK4	Mask bit 4
3	CLK1/	Diskette controller clock 1
4	MK1	Mask bit 1
5	TP	Test point
6	SR CLK IN/	Serial clock in line
7	TP	Test point
8	CLK SR STB	Serial clock strobe
9	USA	Unit select bit A
10	—	—
11	TRACK00/	Track 00 detected
12	USB	Unit select bit B
13	MK0	Mask bit 0
14	DISK WPROT/	Disk write protected
15	DR0/ (DR2/)	Drive 0 ready or Drive 2 ready
16	DOR/	Data overrun error
17	DR1/ (DR3/)	Drive 1 ready or drive 3 ready
18	WRT ERR/	Write error
19	SR OUT	Shift register out control level
20	SEL DR NRDY/	Selected drive not ready
21	DEC OUT 0/	Control decoder output 0
22	SR DATA IN/	Serial data in line
23	—	—
24	DATA SR STB/	Serial data strobe
25	SR DATA OUT	Serial data out line
26	—	—
27	DEC OUT 5/	Control decoder 5 output
28	DEC OUT 4/	Control decoder 4 output
29	STB MEM IN	Strobe memory data in
30	CLK2/	Diskette controller clock 2
31	—	—
32	—	—
33	DEC OUT 7	Control decoder output 7
34	MK3	Mask bit 3
35	DEC OUT 6	Control decoder output 6
36	MK6	Mask bit 6
37	RD RI/	'Read result type' channel command
38	TIME OUT	10 msec. timing pulse
39	XFER REQ/	Controller requests Multibus
40	INT/	Interrupt line
41	AZ	All zeros, valid CRC check
42	INDEX	Index mark detected
43	SELECTED	Controller has control of Multibus
44	GATE LOWER	Input low order data byte
45	—	—
46	MR/	Master reset
47	—	—
48	—	—

Table 2-4. Interface Board P2 Connector Pin Assignments (Continued)

PIN	SIGNAL	FUNCTION
49	RESET/	'Reset' channel command
50	MK2	Mask bit 2
51	MEM WRT	Write data to System memory
52	DEC OUT 1/	Control decoder output 1
53	WRT CMD	I/O write command
54	MK5	Mask bit 5
55	WRTGT	Write gate control level
56	MR	Master reset
57	RD INT/	'Read subsystem status' channel command
58	F	Shift registers full or empty
59	TP	Test point
60	RD CMD	I/O read command

Table 2-5. Interface Board J1 Connector Pin Assignments

PIN	SIGNAL	FUNCTION
1	GND	Ground
2	STEP 0, 1/	Steps head one track (drive 0, 1)
3	GND	Ground
4	STEP 2, 3/	Steps head one track (drive 2, 3)
5	GND	Ground
6	DIR 0, 1/	Step direction indicator (drive 0, 1)
7	GND	Ground
8	DIR 2, 3/	Step direction indicator (drive 2, 3)
9	GND	Ground
10	WRT DAT 0, 1/	Write data (drive 0, 1)
11	GND	Ground
12	WRT DAT 2, 3/	Write data (drive 2, 3)
13	GND	Ground
14	WRT GT 0, 1/	Write gate (drive 0, 1)
15	GND	Ground
16	WRT GT 2, 3/	Write gate (drive 2, 3)
17	GND	Ground
18	WPROT 2, 3/	Diskette write protected indicator (drive 0, 1)
19	GND	Ground
20	WPROT 0, 1/	Diskette write protected indicator (drive 2, 3)
21	GND	Ground
22	READY 3/	Ready indicator from drive 3
23	GND	Ground
24	READY 1/	Ready indicator from drive 1
25	GND	Ground
26	READY 2/	Ready indicator from drive 2
27	GND	Ground
28	READ DATA 2, 3/	Read data, unseparated (drive 2, 3)

Table 2-5. Interface Board J1 Connector Pin Assignments (Continued)

PIN	SIGNAL	FUNCTION
29	GND	Ground
30	READY 0/	Ready indicator from drive 0
31	GND	Ground
32	FILE INOP 0, 1/	Drive inoperable, write fault (drive 0, 1)
33	GND	Ground
34	FILE INOP 2, 3/	Drive inoperable, write fault (drive 2, 3)
35	GND	Ground
36	READ DATA 0, 1/	Read data, unseparated (drive 0, 1)
37	GND	Ground
38	TRACK00 – 0, 1/	Track 0 indicator (drive 0, 1)
39	GND	Ground
40	INDEX 2, 3/	Index indicator (drive 2, 3)
41	GND	Ground
42	INDEX 0, 1/	Index indicator (drive 0, 1)
43	GND	Ground
44	TRACK00 – 2, 3/	Track Ø indicator (drive 2, 3)
45	GND	Ground
46	DRV SEL 0/	Select/load head drive Ø
47	GND	Ground
48	DRV SEL 1/	Select/load head drive 1
49	GND	Ground
50	DRV SEL 2/	Select/load head drive 2
51	GND	Ground
52	DRV SEL 3/	Select/load head drive 3
53	GND	Ground
54	LED 0/	Drive 0 selected indicator
55	GND	Ground
56	TRACK > 43 – 0, 1/	Track greater than 43, low write current (drive 0, 1)
57	GND	Ground
58	TRACK > 43 – 2, 3/	Track greater than 43, low write current (drive 2, 3)
59	GND	Ground
60	INOP RESET 0, 1/	File inoperable reset (drive 0, 1)
61	GND	Ground
62	INOP RESET 2, 3/	File inoperable reset (drive 2, 3)
63	GND	Ground
64	LED 2/	Drive 2 selected indicator
65	GND	Ground
66	LED 1/	Drive 1 selected indicator
67	GND	Ground
68	LED 3/	Drive 3 selected indicator
69	TP	Test Point
70	TP	
71	TP	
72	TP	
73	TP	
74	TP	
75	TP	
76	TP	Test Point

Table 2-5. Interface Board J1 Connector Pin Assignment (Continued)

PIN	SIGNAL	FUNCTION
77	TP	Test Point
78	TP	
79	TP	
80	TP	
81	TP	
82	TP	
83	TP	
84	TP	
85	TP	
86	TP	
87	TP	
88	TP	
89	TP	
90	TP	
91	TP	
92	TP	
93	TP	
94	TP	
95	TP	
96	TP	
97	TP	
98	TP	
99	TP	
100	TP	Test Point

2-8. OPERATING CHARACTERISTICS

AC characteristics of the Diskette Controller are presented in tables 2-6 and 2-7, and figures 2-2 through 2-9. DC characteristics are specified in tables 2-8 and 2-9.

Table 2-6. Diskette Controller/Multibus AC Characteristics

PARAMETER	MINIMUM (nsec)	MAXIMUM (nsec)	DESCRIPTION	REMARKS
t_{SAS}	50		Address Setup Time to I/O Command	Provided by Host CPU
t_{SDS}	0		Data Setup Time to I/O Command	Provided by Host CPU
t_{SAH}	0		Address Hold Time from I/O Command	Provided by Host CPU
t_{SDHW}	0		Data Hold Time from I/O Command	Provided by Host CPU
t_{SDHR}	25		Read Data Hold Time from I/O Command	Provided by Flexible Disc Controller (FDC)
t_{ACC}	Bus Timeout		I/O Access Time	Provided by FDC
t_{XKD}	7		XACK Delay from Read Data	Provided by FDC
t_{XKO}	30		XACK Hold Time from I/O Command	Provided by FDC
t_{BCY}	100		Bus Clock Cycle Time	Provided by CPU
t_{BW}	25		Bus Clock Low and High Periods	Provided by CPU
T_{CCY}	100		Common Clock Cycle Time	Provided by CPU
t_{CW}	25		Common Clock Low and High Periods	Provided by CPU
t_{DRQ}		35	Bus Request Delay	
t_{DBY}		65	Bus Busy Turn on Delay	
t_{DBYF}		40	Bus Busy Turn off Delay	
t_{DBPN}	30		Priority Input Setup Time	
t_{DBPO}		20	BPRO/ Serial Delay from BPRN/	
t_{DB}	50		Busy to Address/Data Delay	

Table 2-6. Diskette Controller/Multibus AC Characteristics (Continued)

PARAMETER	MINIMUM (nsec)	MAXIMUM (nsec)	DESCRIPTION	REMARKS
$t_{AS, DS}$	60		Address/Data Setup to Command	
t_{XKCO}	35	125	XACK to Command Turn Off	
t_{AH}	115		Address Hold Time	
t_{DHW}	125		Data Hold Time	
t_{DHR}	0		Read Data Hold Time	Provided by Memory Module (Slave)
t_{BS}	200		Bus Sample Delay Time	

Table 2-7. Diskette Controller/Drive Interface AC Characteristics

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	DESCRIPTION
t_{SCYS}	8 msec	10 msec	12 msec	Step Cycle Time
t_{SPW}		10 usec		Step Pulse Width
t_{LSET}		60 msec		Settling Time – Select to Data
t_{SSET}		20 msec		Settling Time – Step to Data
t_{RDPW}	200 nsec	250 nsec	300 nsec	Read Data Pulse Width (Rd)
t_{CELL}		2 usec		Bit Cell Time
t_{WDPW}		250 nsec		Write Data Pulse Width (Wt)
t_{NXPW}		1.5 msec		Multibus Pulse Width
t_{NXCY}		166.7 msec		Index Cycle Time
t_{WFPW}	2 usec		2.8 usec	Write Fault Reset Pulse Width

Table 2-8. Diskette Controller/Multibus DC Characteristics

SIGNAL	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITION	PARAMETER		
				MIN	MAX	UNITS
ADRF/–ADR8/	V_{OL}	Output Low Voltage	I_{OL}=10mA		.45	V
	V_{OH}	Output High Voltage	I_{OH}=–1mA	2.4		V
	*C	Capacitive Load			15	pf
ADR7/ – ADRØ/	V_{OL}	Output Low Voltage	I_{OL}=15mA		.45	V
	V_{OH}	Output High Voltage	I_{OH}=–1mA	3.65		V
	V_{IL}	Input Low Voltage			.8	V
	V_{IH}	Input High Voltage		2		V
	I_{IL}	Input Current at V_{IL}	V_{IL}= .4V		–1.6	mA
	I_{IH}	Input Current at V_{IH}	V_{IH}=2.4V		40	uA
	*C	Capacitive Load			15	pf
DATF/ – DAT4/	V_{OL}	Output Low Voltage	I_{OL}=15mA		.45	V
	V_{OH}	Output High Voltage	I_{OH}=–1mA	3.65		V
	V_{IL}	Input Low Voltage			.85	V
	V_{IH}	Input High Voltage		2		V
	I_{IL}	Input Current at V_{IL}	V_{IL}= .45V		–.25	mA
	I_{IH}	Input Current at V_{IH}	V_{IH}=5.25V		10	uA
	*C	Capacitive Load			15	pf
DAT3/ – DATØ/	V_{OL}	Output Low Voltage	I_{OL}=15mA		.45	V
	V_{OH}	Output High Voltage	I_{OH}=–1mA	3.65		V
	V_{IL}	Input Low Voltage			.85	V
	V_{IH}	Input High Voltage		2		V
	I_{IL}	Input Current at V_{IL}	V_{IL}= .45V		–.25	mA
	I_{IH}	Input Current at V_{IH}	V_{IH}=5.25V		10	uA
	*C	Capacitive Load			15	pf
BCLK/	V_{IL}	Input Low Voltage			.8	V
CCLK/	V_{IH}	Input High Voltage		2		V
	I_{IL}	Input Current at V_{IL}	V_{IL}= .4V		–2	mA
	I_{IH}	Input Current at V_{IH}	V_{IH}=2.4V		50	uA
	*C	Capacitive Load			15	pf
BPRN/	V_{IL}	Input Low Voltage			.8	V
	V_{IH}	Input High Voltage		2		V
	I_{IL}	Input Current at V_{IL}	V_{IL}= .4V		–3.2	mA
	I_{IH}	Input Current at V_{IH}	V_{IH}=2.4V		80	uA
	*C	Capacitive Load			15	pf
IORC/, IOWC/	V_{IL}	Input Low Voltage			.8	V
INIT/	V_{IH}	Input High Voltage		2		V
	I_{IL}	Input Current at V_{IL}	V_{IL}= .4V		–1.6	mA
	I_{IH}	Input Current at V_{IH}	V_{IH}=2.4V		40	uA

Table 2-8. Diskette Controller/Multibus DC Characteristics (Continued)

SIGNAL	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITION	PARAMETER		
				MIN	MAX	UNITS
	*C	Capacitive Load			15	pf
XACK/	V_{OL}	Output Low Voltage	I_{OL}=16mA		.4	V
	V_{OH}	Output High Voltage	I_{OH}=−5.2mA	2.4		V
	V_{IL}	Input Low Voltage			.8	V
	V_{IH}	Input High Voltage		2		V
	I_{IL}	Input Current at V_{IL}	V_{IL}= .4V		−1.6	mA
	I_{IH}	Input Current at V_{IH}	V_{IH}=2.4V		40	uA
	I_{LL}	Input Leakage Low	High Z V_o=2.4V		−40	uA
	I_{LH}	Input Leakage High	High Z V_0= .4V		40	uA
	*C	Capacitive Load			15	pf
BPRO/	V_{OL}	Output Low Voltage	I_{OL}=3.2mA		.45	V
	V_{OH}	Output High Voltage	I_{OH}=400uA	2.4		V
	*C	Capacitive Load			15	pf
BREQ	V_{OL}	Output Low Voltage	I_{OL} =20mA		.45	V
	V_{OH}	Output High Voltage	I_{OH}=400uA	2.4		V
	*C	Capacitive Load			15	pf
MRDC/, MWTC/	V_{OL}	Output Low Voltage	I_{OL}=32mA		.4	V
	V_{OH}	Output High Voltage	I_{OH}=−2mA	2.4		V
	*C	Capacitive Load			15	pf
BUSY/	V_{OL}	Output Low Voltage	I_{OL}=20mA		45	V
	V_{OH}	Output High Voltage	Open Collector			
	*C	Capacitive Load			15	pf
INT7/ – INTØ/	V_{OL}	Output Low Voltage	I_{OL}=16mA		.4	V
	I_{OH}	Output High Leakage	Open Collector Off		250	uA
	*C	Capacitive Load	V_{OH}=5.5V		15	pf

* Capacitance values are approximations.

Table 2-9. Diskette Controller/Drive Interface DC Characteristics

SIGNAL	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITION	PARAMETER		
				MIN	MAX	UNITS
SELØ/, SEL1/ SEL2/, SEL3/	V_{OL} I_{OH}	Output Low Voltage Output High Leakage	I_{OL}=48mA Open Collector Off V_{OH}=5.5V		.4 250	V uA
WRT DAT/ WRT GT/ STEP/ DIR/ WRT FLT RESET/ TRACK GT 43/	*C	Capacitive Load			15	pf
READY Ø/	V_{IL}	Input Low Voltage			.8	V
READY 1/	V_{IH}	Input High Voltage		3.0		V
SEP DATA/	I_{IL}	Input Current at V_{IL}	V_{IL}= .8		–26	mA (2)
SEP CLOCK/	I_{IH}	Input Current at V_{IH}	V_{IH}=3.0		10	mA (1)
TRACK Ø/ INDEX/ WRT FLT/ WPROT/	*C	Capacitive Load			15	pf
LEDØ/ LED1/	V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL}=16mA I_{OH}=400ua	 2.4	.4 	V V
	*C	Capacitive Load			15	pf

(1) Includes 9.1mA due to 220/330Ω pull-up/pull-down.
(2) Includes 25mA due to 220/330Ω pull-up/pull-down.
* Capacitance values are approximations.

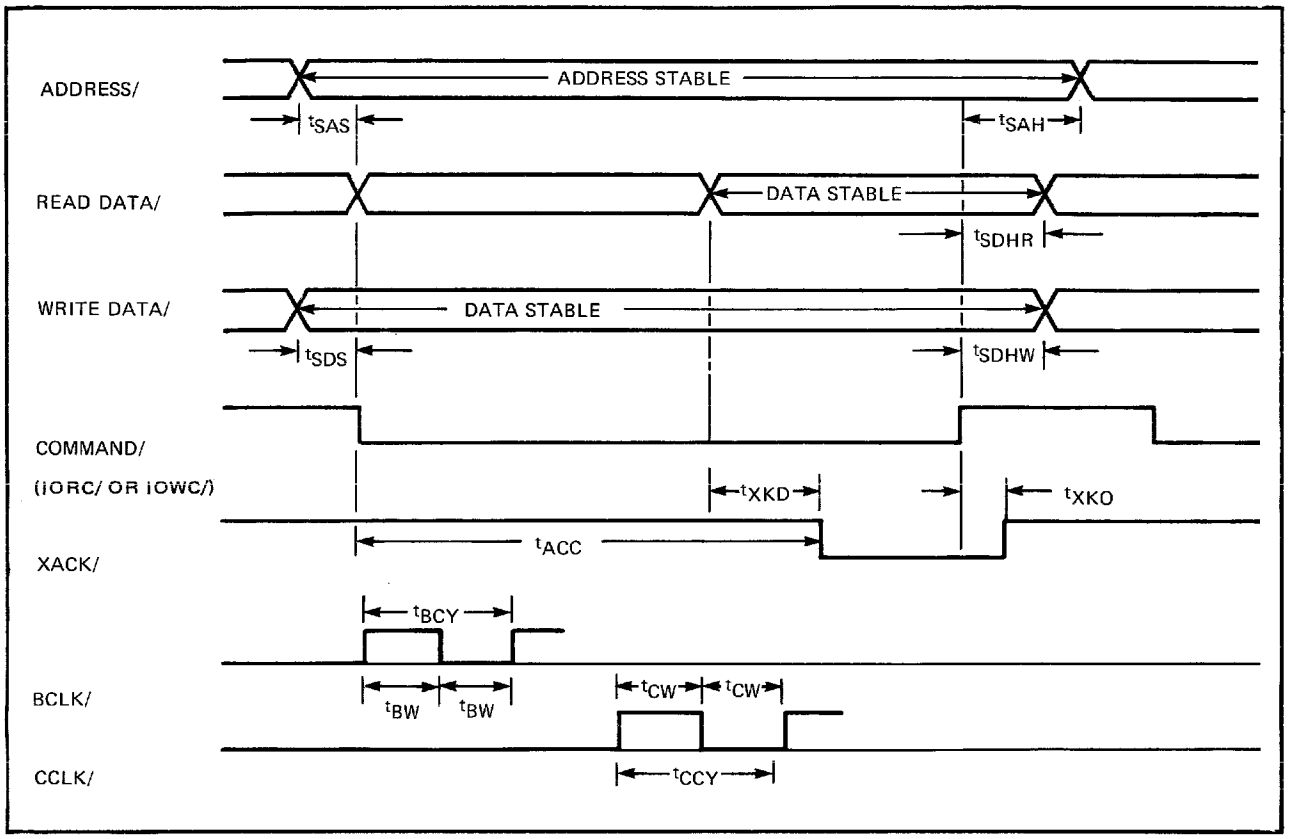


Figure 2-2. Slave Command Timing

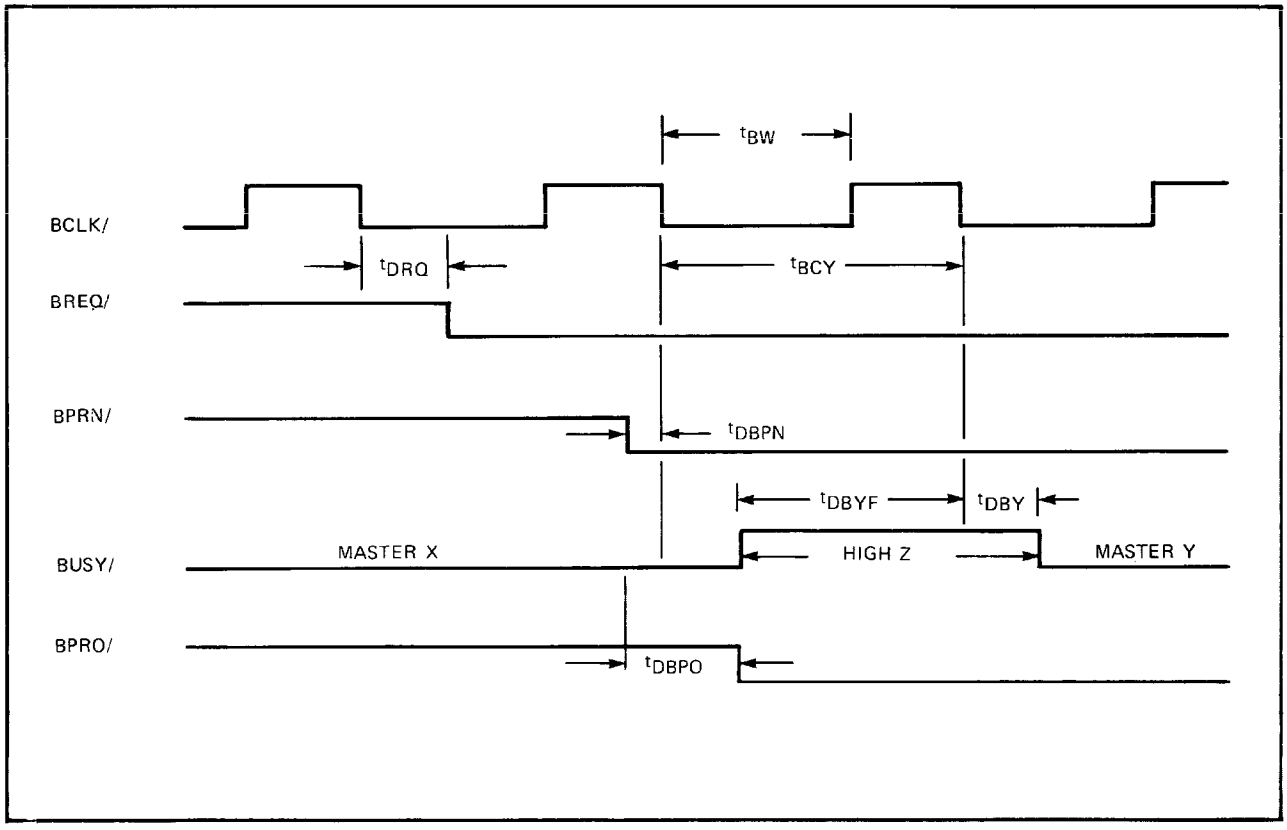


Figure 2-3. Bus Exchange Timing

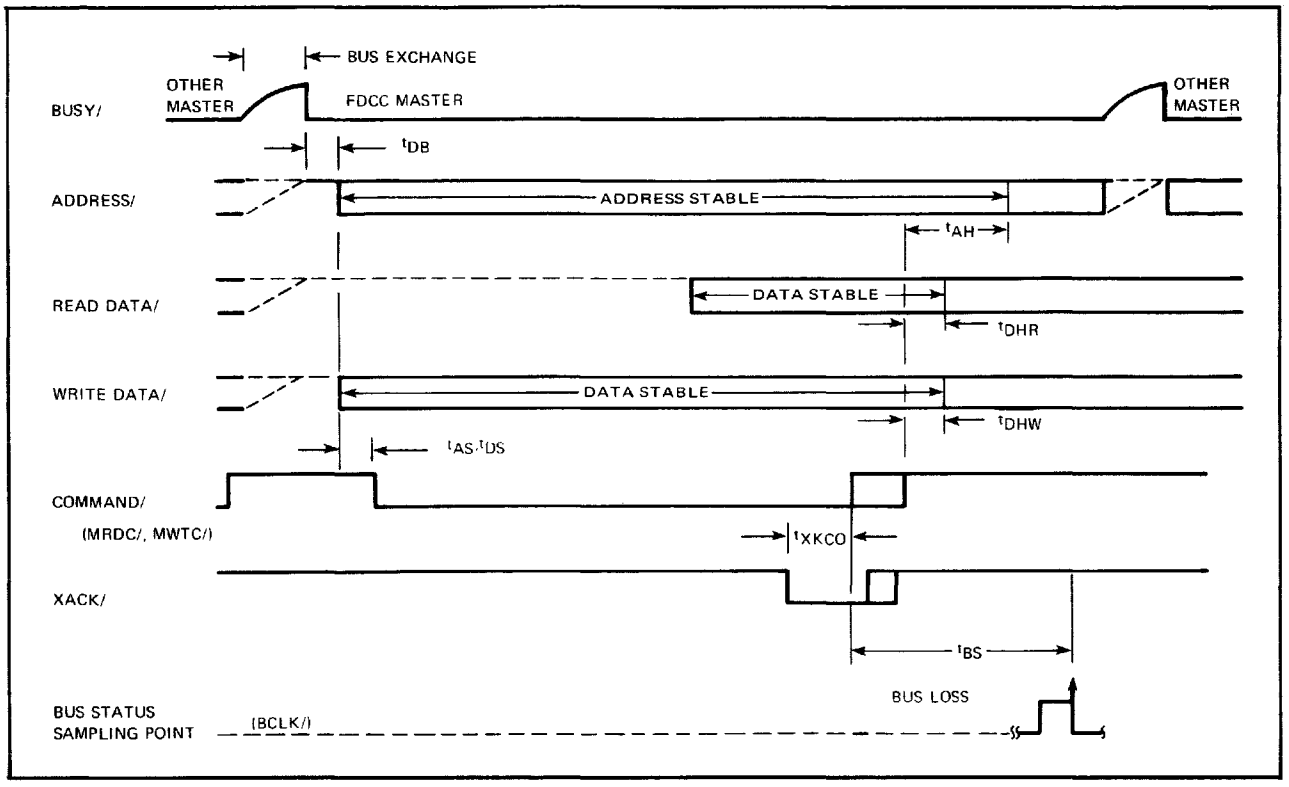


Figure 2-4. Master Command Timing

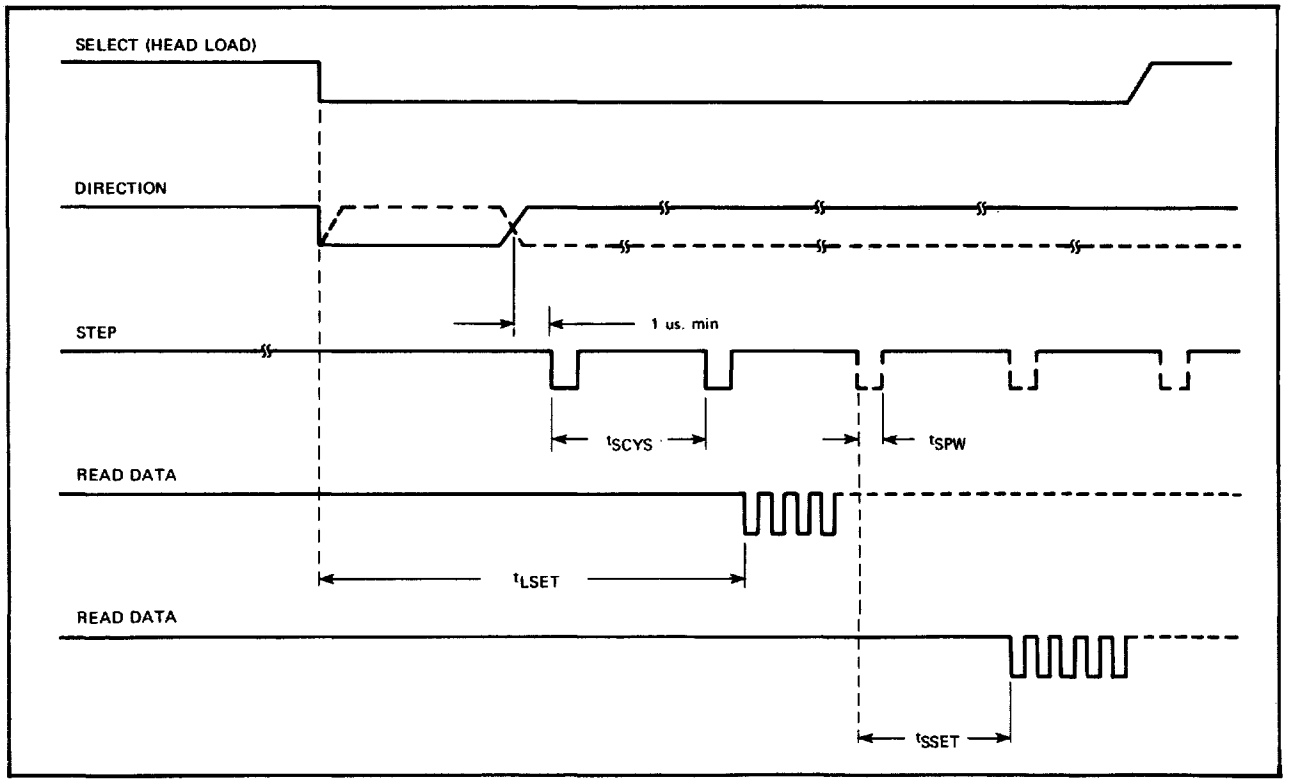


Figure 2-5. Step/Settling Timings

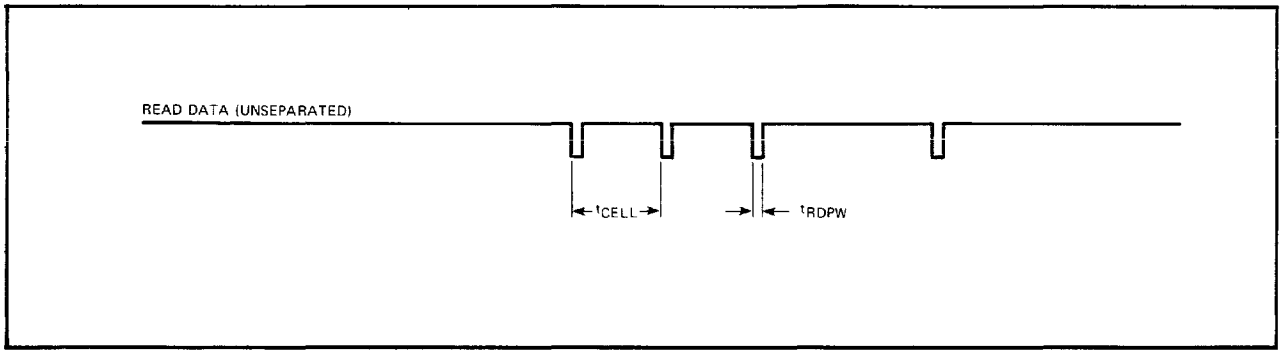


Figure 2-6. Read Timing

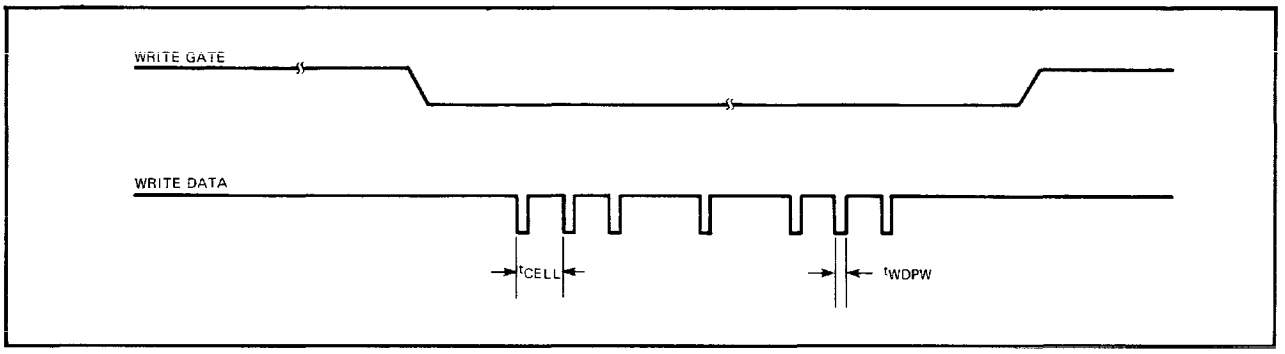


Figure 2-7. Write Timing

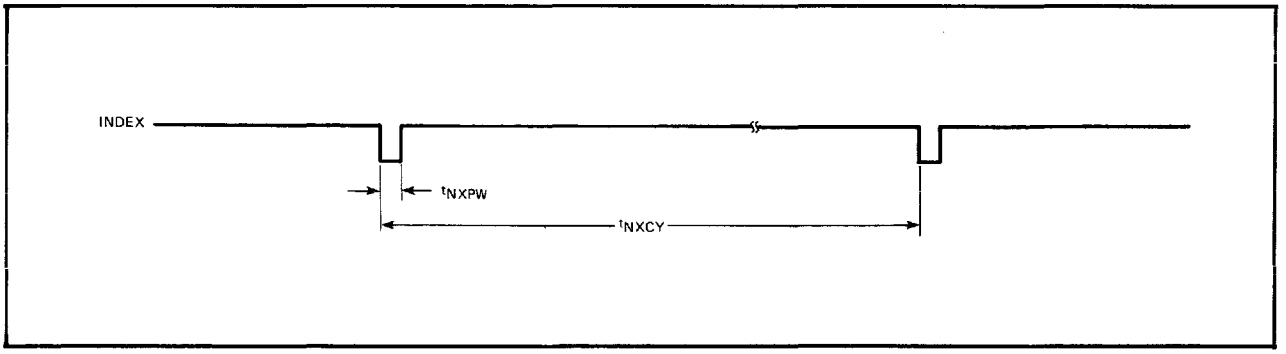


Figure 2-8. Index Timing

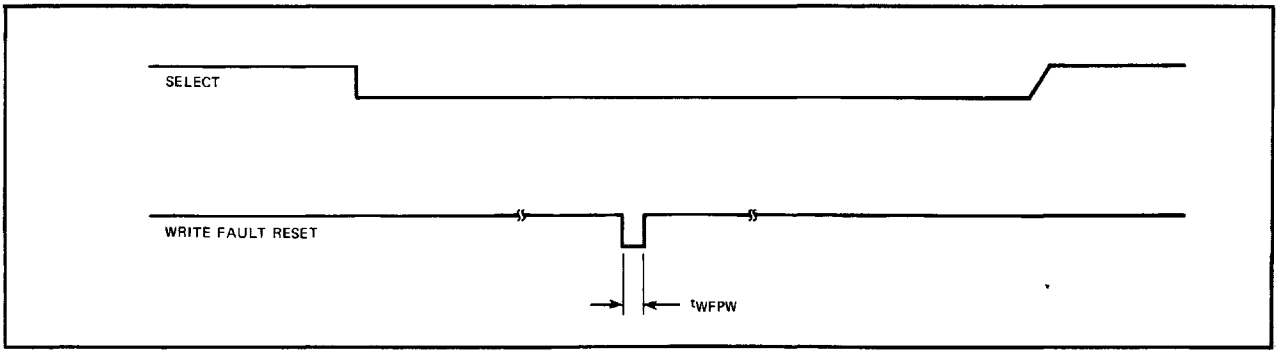


Figure 2-9. Write Fault Reset Timing

2-9. SWITCH AND JUMPER CONFIGURATIONS

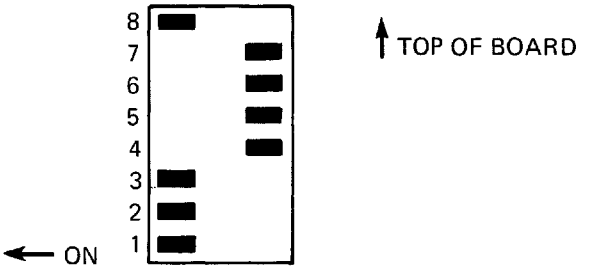
The following paragraphs provide instructions for configuring the I/O Base Address switch and the Interrupt Level Select switch. The memory base address, which is under program control, is described in paragraph 4-4.

2-10. I/O BASE ADDRESS SELECTION

The user must assign a base address to the Diskette Channel. The base address is defined by the five most significant bits of the eight-bit I/O port address. The three least significant bits, then, can be used to differentiate between eight input or eight output channel commands. When the CPU accesses the Diskette Channel by executing an I/O instruction the base address (BASE) is used to select the Diskette Channel, while the three low-order address bits select one of the channel commands, as described in Chapter 3.

A base address is assigned by opening or closing the five most significant switch positions of the S1 switch (S1 -4, 5, 6, 7, 8) on the Channel Board (see sheet 1 of the Channel Board schematic in Chapter 5). When a switch position is closed (on) (tied to ground) it represents the assignment of a logical 0 address bit. When a position is open (off) (+5V), it represents a logical 1 selection.

The following sketch represents a base address selection of 78_{16}.

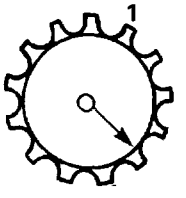


2-11. INTERRUPT LEVEL SELECTION

The user can assign the Diskette Channel's interrupt request line to any one of eight interrupt priority levels (INT0/-INT7/) by moving the interrupt level select switch (S1) on the Interface Board to the desired position. This eight position rotary switch is shown on sheet 3 of the Interface Board schematic in Chapter 5. The eight switch positions are associated with the following priority levels:

SWITCH POSITION	INTERRUPT PRIORITY LINE	RELATIVE PRIORITY (INTELLEC MDS SYSTEM)
1	INT0/	HIGHEST
2	INT1/	
3	INT2/	
4	INT3/	
5	INT4/	
6	INT5/	
7	INT6/	
8	INT7/	LOWEST

The following sketch shows the switch settting 3 corresponding to priority line INT2/.



CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

All operations must be initiated by the Central Processor Unit (CPU). Once initiated the controller completes the specified operation without further intervention on the part of the CPU. From the CPU's point of view, there are only three general steps required to complete any diskette operation.

- The CPU must prepare and store in system memory an I/O Parameter Block (IOPB) for each operation to be performed. An IOPB (seven bytes) specifies a particular diskette operation and provides all of the parameters required for execution of that operation.
- The CPU must then pass the memory address of the IOPB to the Controller Channel.
- The CPU must process the result information from the Controller Channel upon completion of the operation(s).

The following paragraphs define the system operation.

The 7-byte parameter block (IDPB) must adapt the following format:

Byte 1 Channel Command
2 Diskette Instruction
3 Number of Records
4 Track Address
5 Sector Address
6 Buffer Address (Lower)
7 Buffer Address (Upper)

The preparation of the IOPB by the CPU, in itself, requires no interaction with the Controller Diskette Channel. The passing of the memory address for the IOPB and the result processing, however, do require interaction. Six channel commands have been defined to allow the CPU to perform these interactive steps. Three of the channel commands are the result of the CPU executing an output instruction to a dedicated I/O port address, while the other three commands are the result of input instructions to dedicated ports. The six channel commands are:

(1) Write memory address lower (output)
(2) Write memory address upper and start the diskette operation (output)
(3) Reset the channel (output)
(4) Read subsystem status (input)
(5) Read result type (input)
(6) Read result byte (input)

The channel command provides the Controller with information which:

(1) Determines the method of assigning logical sector addresses.
(2) Enables or disables a series of possible diskette interrupts.
(3) Determines the length of the data word to be transferred.

The CPU outputs the memory address of the IOPB by executing channel commands 1 and 2. Upon execution of channel command 2, the Controller Channel will request master control of the Multibus, fetch the diskette instruction and associated parameters from the IOPB, and proceed to perform the specified diskette operation. The diskette instruction byte in the IOPB can specify any one of seven diskette operations:

(1) Recalibrate (seek track 00)
(2) Seek
(3) Format a track
(4) Write data (with data address marks)
(5) Write data (with deleted address marks)
(6) Read data
(7) Verify CRC

The Controller Channel can interrupt the CPU when the operation is completed or when the diskette ready status changes. The host system software can implement its CPU interrupt mechanism via this direct interrupt feature or it can "poll" the Controller Channel by executing channel command 4 (read subsystem status). When the CPU determines that the operation sequence has been completed (either by receiving an interrupt request or by reading the interrupt status), the CPU should execute channel commands 5 and 6 (read result type and read result byte) to determine whether the diskette operations were successfully completed, and if not which type of error occurred.

Thus, in summary, we see that certain channel commands are executed by the CPU to point the Controller Channel to an IOPB in system memory, and initiate the operation sequence. The Controller Channel, then, accesses the IOPB to perform the diskette operation specified by the instruction byte of the IOPB. The Controller Channel will, if enabled by the IOPB, generate an I/O complete interrupt request upon completion of each diskette operation or detection of an error. The CPU, then, executes other channel commands to determine the result of the diskette operation.

3-2. CHANNEL COMMANDS

There are six channel commands to which the Controller Channel will respond. Three of the channel commands are issued when a CPU in the system executes output (I/O write) instructions with the appropriate eight-bit I/O addresses. The other three commands are issued when the CPU executes input (I/O read) instructions with the appropriate I/O addresses.

When the CPU executes one of the output channel commands, it activates the I/O write (IOWC/) line and duplicates the appropriate 8-bit I/O address on address lines ADR0/-ADR7/ and ADR8/ - ADRF/ of the System bus. Depending on the particular channel command, the CPU may also place relevant data on data lines DAT0/-DAT7/ of the System bus. The CPU maintains the data lines until the Controller Channel returns the transfer acknowledge (XACK/) signal.

When the CPU executes one of the input channel commands, it activates the I/O read (IORC/) line and duplicates the appropriate I/O address on both halves of the System bus. The CPU expects the Controller Channel to activate the transfer knowledge (XACK/) line when it has placed the requested data on data lines DAT0/-DAT7/.

The Controller Channel differentiates between the different channel commands by interrogating the I/O read (IOCR/) and I/O write (IOWC/) lines and the three least significant address lines (ADR0/ - ADR2/). The five most significant I/O address lines (ADR3/ - ADR7/) define the switch-selectable BASE address for the Controller Channel.

If the Controller Channel is not busy, it will respond to an output channel command within 3 microseconds. It is is busy, the "write MA lower" and "write MA upper" commands are ignored; no acknowledge is returned. (Note: Because no acknowledge is returned in this case, it could be possible to "hang up" the host system if the system does not include a Fail Safe time-out provision, as is provided on the Front Panel Control Module in the system). The "reset" command, however, is acknowledged even if the Controller Channel is busy. "Reset" is executed immediately (if issued during a data write operation, garbled data will be written).

The Diskette Controller responds to "read subsystem status" and "read result type" input channel commands within 1 microsecond. The information returned in response to a "read subsystem status" command is always valid. The eight bits of data returned in response to a "read result type" command, however, are only valid if the Controller Channel had previously issued an interrupt request to the CPU. The Controller Channel will, if not busy, respond to a "read result byte" input command within 3 microseconds. If the Controller Channel is busy, however, it ignores the "read result byte" command (i.e., no acknowledge is returned). The "read result type" and "read result byte" commands must be executed sequentially ("read result type" first), and should be executed only in response to an interrupt request from the Controller Channel; execution at other times could produce erroneous result data.

The use and format of each of the six channel commands is described below:

WRITE MEMORY ADDRESS LOWER (OUTPUT)

This channel command outputs the low order byte of the 16-bit memory address that points to byte 1 ("channel word") of the IOPB.

System address bus: BASE + 1

System data bus: Eight least significant bits of the 16-bit memory address that points to the first IOPB.

WRITE MEMORY ADDRESS UPPER AND START THE DISKETTE OPERATION (OUTPUT)

This channel command outputs the high order byte of the 16-bit memory address that points to byte 1 of the IOPB. This command also causes the Controller Channel to begin executing the diskette operation specified in byte 2 (instruction byte) of the addressed IOPB.

System address bus BASE + 2

System data bus: Eight most significant bits of the 16-bit memory address

RESET DISKETTE SYSTEM (OUTPUT)

This output channel command causes all control logic in the Controller Channel to be reset in an initialized state. If this command is issued while a "write data" diskette operation is in progress, the data in the sector currently being written will be garbled. This command is intended to clear a "hang up" in the Controller Channel.

System address bus: BASE + 7

System data bus: Not used.

READ SUBSYSTEM STATUS (INPUT)

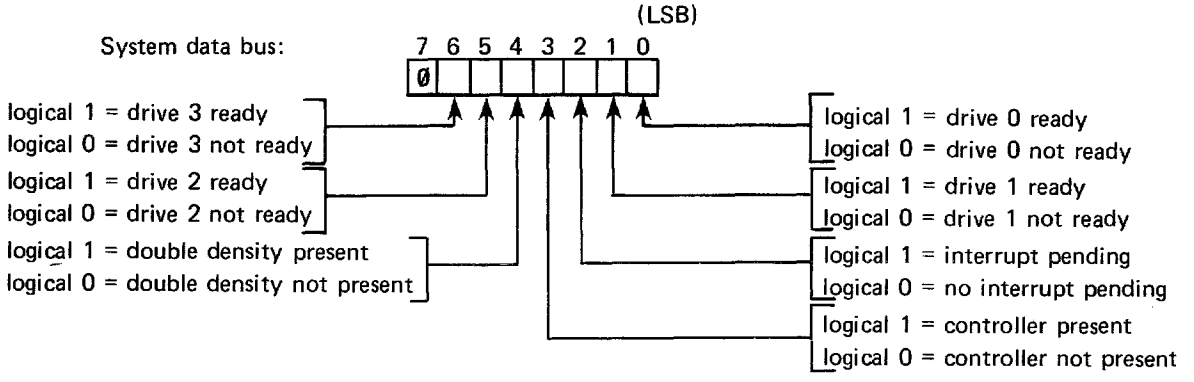
This input channel command causes the Controller Channel to return.

bit 0 — ready status of drive 0
bit 1 — ready status of drive 1
bit 2 — state of the channel's interrupt flip-flop
bit 3 — controller presence indicator
bit 4 — double density controller presence indicator
bit 5 — ready status of drive 2
bit 6 — ready status of drive 3

These indications allow the operating system to monitor the operation of the Controller Channel.

System address bus: BASE + 0

System data bus: (LSB)

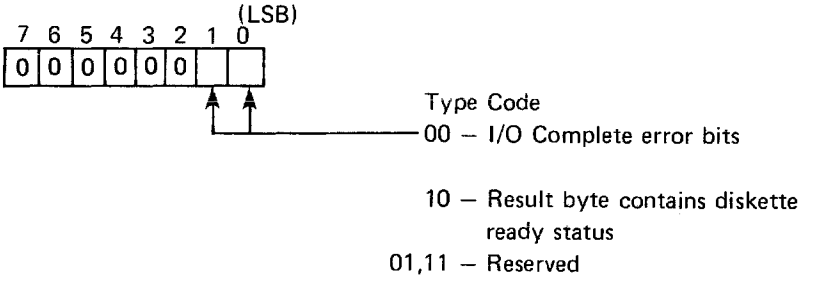


READ RESULT TYPE (INPUT)

This input channel command causes the Controller Channel to return eight bits of information to the CPU. The two least significant bits specify one of four different types of result byte (see next paragraph) associated with diskette operations.

System address bus: BASE + 1

System data bus: (LSB)



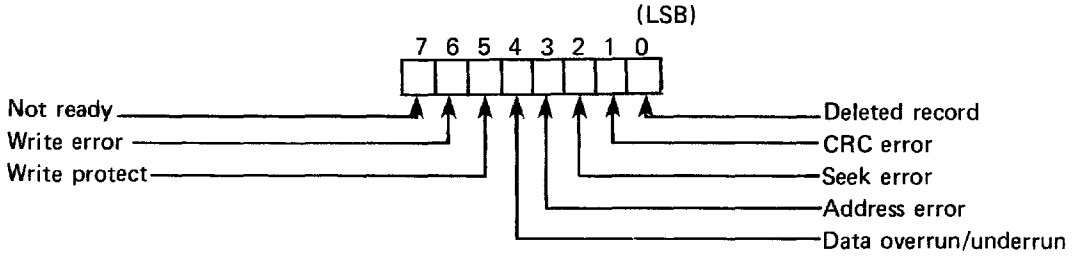
READ RESULT BYTE (INPUT)

This input channel command causes the Controller Channel to return eight bits of information to the CPU. The interpretation of these bits is dependent upon the type code returned in the result type word (see previous paragraph). The "read result byte" channel command should only be executed after a "read result type" command has been executed.

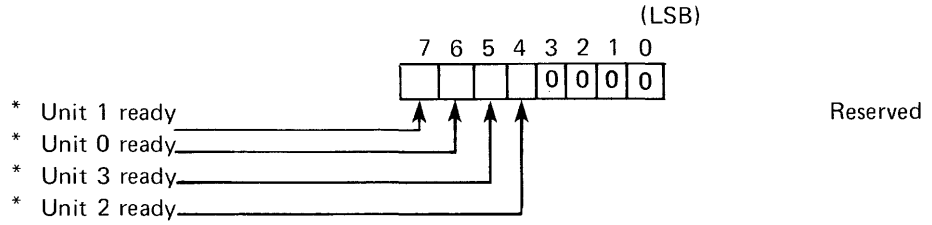
System address bus: BASE + 3

System data bus: If the type code in the result type word = 00, the result byte, input on the data bus, will contain error bits (see Paragraph 3-5 for error explanations) and will be formatted as follows:

(LSB)



If the type code = 10, the controller has detected a change in the ready status of a drive and the contents of the result byte will indicate the current ready status of the diskette drives:



*NOTE: A logical 1 means that the drive is currently ready; a logical 0 means the drive is not ready. It is the responsibility of the host system software to maintain appropriate tables to track these status changes. There is one instance in which a drive can appear "not ready" to the host system, when in fact it is ready. For example, assume that while drive 0 is selected, drive 1 just goes not ready then returns to the ready state (perhaps the diskette platter was changed). When the drive 0 operation is completed, the diskette controller will return two consecutive status change interrupts, the first showing drive 1 not ready, the second showing drive 1 ready. The first interrupt, indicating drive 1 to be not ready, is returned even though the drive is now actually ready because it is important that the operator know that the ready status of the drive changed while the other drive was selected. For instance, this would protect against inadvertently accessing an "unknown" disk, if the drive went not ready then ready again because someone changed disk platters.

3-3. DISKETTE OPERATIONS

The Diskette System is capable of performing seven different operations: recalibrate, seek, format track, write data (with data marks), write data (with deleted data marks), read data, and verify CRC. To initiate any diskette operation, the CPU will output both bytes of the 16-bit memory address that points to the first byte of an I/O Parameter Block (IOPB). The second byte in the IOPB specifies one of the seven diskette operations (see Paragraph 3-4 for IOPB format). After the Diskette Controller receives the upper byte of the 16-bit memory address, it accesses the IOPB to determine the operation to be performed and to acquire the various parameters that are necessary for execution of the diskette instruction. The Diskette System will perform the specified operation, then set its interrupt flip-flop.

NOTE: The Diskette Channel automatically unloads the read/write head after a fixed length of time following a diskette operation. This feature is meant to reduce head wear. The feature is implemented by counting index pulses after a "read result byte" channel command is executed. When the specified count is achieved, the head is unloaded, and the count is reinitialized. At present, the count is set for 6; that is, the head will remain loaded for at least five complete revolutions following each diskette operation or group of linked diskette operations.

The seven diskette operations are defined in the following paragraphs:

RECALIBRATE

This operation causes the head of the selected diskette unit to be moved over track 00. The diskette drive's track 0 sensor is sampled to determine successful completion of this operation. This is often the first instruction executed after a diskette is loaded, or when a seek error occurs (see Paragraph 3-5).

SEEK

This operation causes the head of the selected diskette unit to be moved over the track specified in byte 4 of the IOPB. The Diskette Channel will verify the head position by reading the track address from the diskette platter before completing the operation. If at the completion of the head movement, the head is not over the expected track, a "seek error" will be indicated (see Paragraph 3-5).

FORMAT TRACK

This operation initializes the track specified in byte 4 of the IOPB, by writing all address marks, gaps, address fields and data fields, as shown in Figure 3-1.

The method of assigning logical sector addresses, which are written into the sector address fields, is specified by bit 6 of the first IOPB byte (the channel word). If this bit is equal to logical 0 the sequence of logical sector addresses will match the physical sequence on the diskette (i.e., sector address "01" is written into the first physical sector after the index mark, sector address "02" is written into the second physical sector, and so on). In addition, the data byte stored in the memory location specified by the 16-bit buffer address contained in bytes 6 and 7 of the IOPB will be written into the 128-byte locations of each sector's data field. No other data bytes need to be stored in this buffer.

If, on the other hand, the sequence of logical addresses being assigned to the sectors is "random" (that is, do not match the physical sequence of sectors), bit 6 of the channel word will be equal to logical 1, and 104 bytes (52 pairs) of data will be stored in memory beginning at the 16-bit buffer address contained in bytes 6 and 7 of the IOPB. Each of the 52 pairs of

data bytes will specify the logical sector address to be written into the sector address field of the corresponding physical sector, and the data character which will be written (128 times) into the data field portion of that sector. For example, if the first four bytes of the buffer are:

Byte	Contents (hex)
1	01
2	FF
3	0E
4	00
.	.
.	.

Then, sector address "01" will be written into the sector address field of the first physical sector after the index mark, and "FF_{16}" (all ones) will be written into each of the 128 byte locations in the data field portion of this sector. The sector address "$0E_{16}$" (14_{10}) will be written into the sector address field of the second physical sector (i.e., the sector which is physically next to the first sector), and "00_{16}" (all zeros) will be written into each of the 128 byte locations in the data field portion of this sector. And so on, until a logical sector address has been written into the sector address field of each of the 52 physical sectors on the track, and a data byte is written into each of the 128 byte locations in the data field portion of each of the 52 sectors.

The firmware implementation of the format command is such that in order to format track n ($n \neq 0$), track n-1 must already be formatted (i.e., already have readable address information written into it). Track 0 can always be formatted even if no valid address information is written on the disk.

During formatting, a "data mark" (i.e., a character which has a clock pattern equal to 70_{16} and a data pattern equal to $0B_{16}$; see Figure 3-2) is written into the "data/deleted data address mark" character position of each sector (i.e., the character position immediately preceding the 128 byte data field.

If, when the format track operation is initiated, the head is not already positioned over the track specified in byte 4 of the IOPB, the format track instruction will cause the head to move (seek) to the proper track before the actual formatting begins.

WRITE DATA

This operation transfers N x 128 bytes of contiguous data from memory to the diskette. N represents the number of sectors to be written. N is specified by the contents of byte 3 of the IOPB. The 16-bit buffer address stored in bytes 6 and 7 of the IOPB specifies the memory location containing the first data byte to be transferred. The contents of bytes 4 and 5 of the IOPB (track and sector addresses, respectively) specify the logical address of the first sector to be written into.

Each 128 byte data field will be preceded by a "data" address mark (see Figure 3-2) that is used for synchronization. Two bytes (16 bits) of CRC check bits will be generated and written after each data field; the CRC bytes are generated from the address mark, as well as the 128 data bytes.

A multi-sector operation (i.e., $N \geq 2$) may begin at any sector, but must not go beyond the last logical sector on a track (sector 52).

If the head is not already positioned over the track specified in byte 4 of the IOPB, the write data instruction will cause the head to move (seek) to the proper track before the actual writing begins.

WRITE "DELETED" DATA

This operation is identical to the WRITE DATA operation, described above, except that each 128 byte data field is preceded by a "deleted data" address mark, shown in Figure 3-3.

READ DATA

This operation transfers N sectors of data (128 bytes per sector) from diskette to memory. N is specified by the contents of byte 3 of the IOPB. The contents of bytes 4 and 5 of the IOPB (track and sector addresses, respectively) specify the logical address of the first sector to be read. The 16-bit buffer address stored in bytes 6 and 7 of the IOPB specifies the memory location into which the first data byte will be written.

Two bytes of CRC check bits will be generated as each sector is being read. When the "data" address marks and all 128 data bytes of a sector have been read, the generated CRC bits are compared with the 16 CRC bits previously written. If there is a mismatch, a CRC error is indicated (see Paragraph 3-5).

A multi-sector operation (i.e., $N \geq 2$) may begin at any sector, but must not go beyond the last logical sector on a track (sector 52).

If the head is not already positioned over the track specified in byte 4 of the IOPB, the read data instruction will cause the head to move (seek) to the proper track before the actual data reading begins.

VERIFY CRC

This operation is identical to the READ DATA operation, described above, except that no data is transferred to memory.

3-4. I/O PARAMETER BLOCK

The CPU in the system initiates a diskette operation by outputting a 16-bit address that points to the beginning (the channel word) of the I/O Parameter Block (IOPB) in system memory. The Diskette Channel then accesses the IOPB. An IOPB specifies one of the diskette operations (see Paragraph 3-3) and provides all of the parameters required for the completion of that operation. An IOPB consists of seven bytes, as shown in Table 3-1.

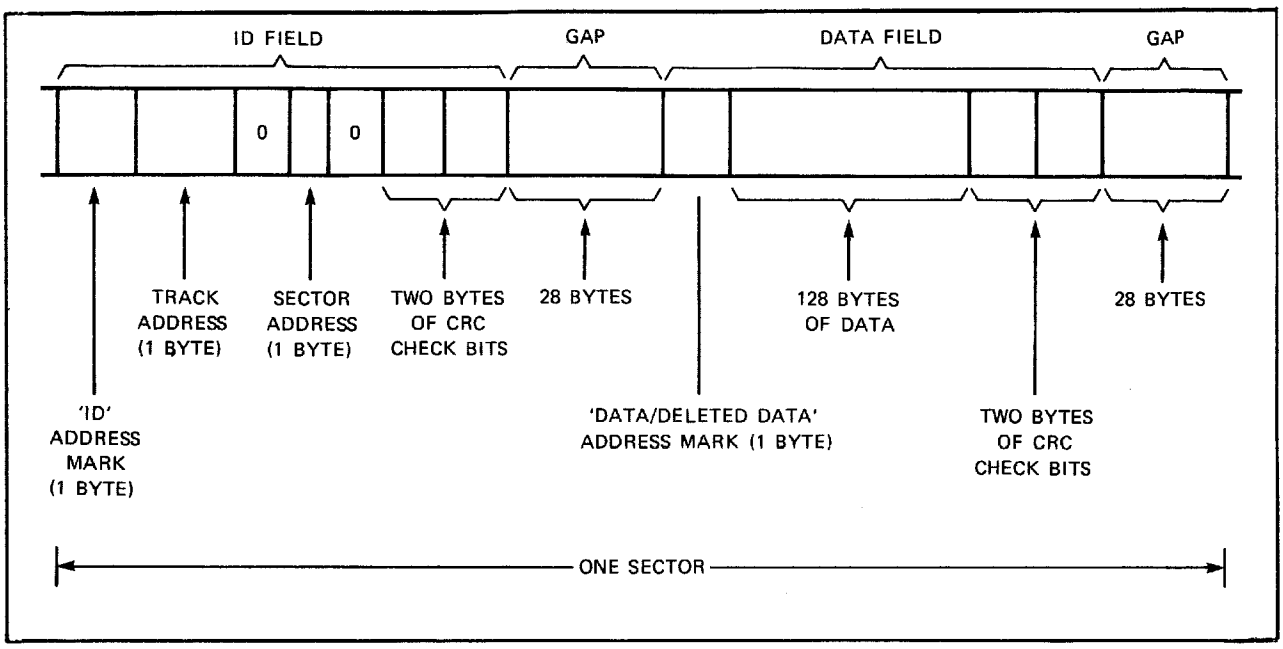


Figure 3-1. Sector Format

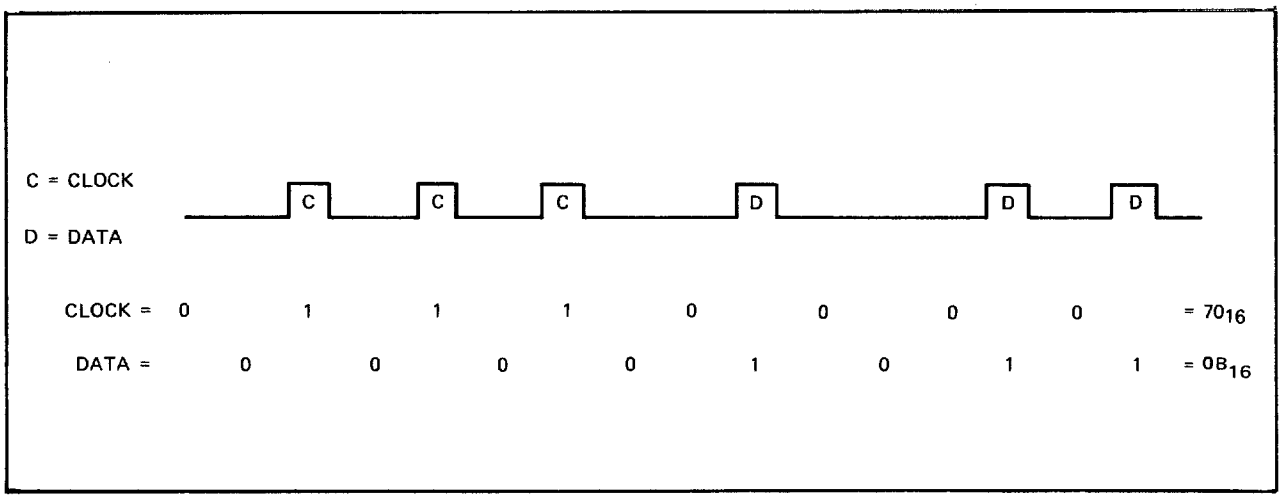


Figure 3-2. 'DATA' Address Mark

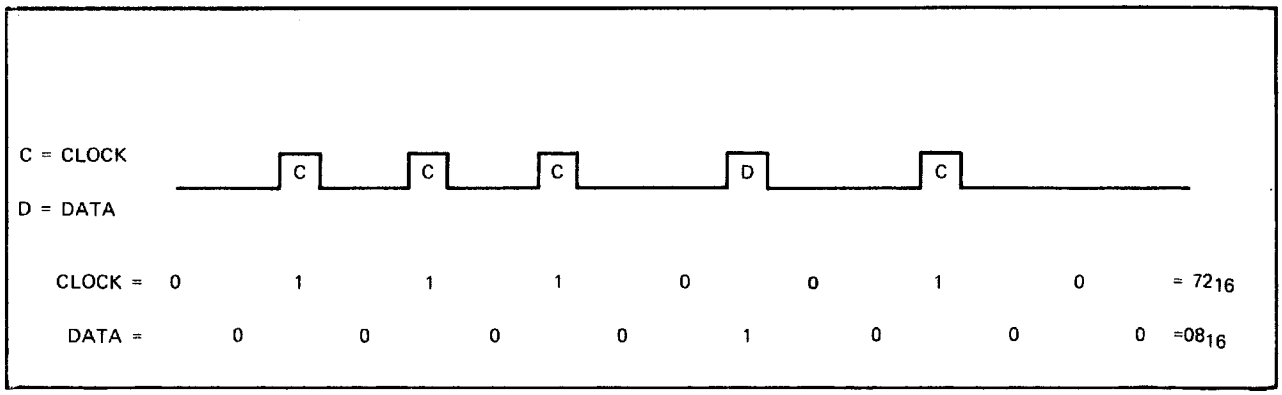
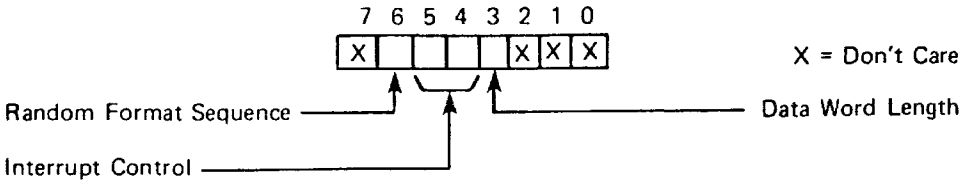


Figure 3-3. 'DELETED DATA' Address Mark

Byte 1. Channel Word

This byte contains channel control information to be used by the Diskette System. Bit assignments in this byte are as follows:



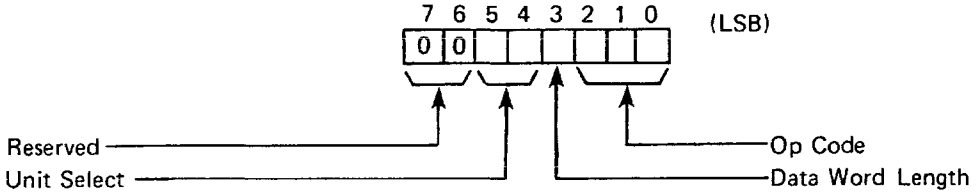
The "random format sequence" bit (6) specifies the method of assigning logical sector addresses when formatting a track. If this bit is reset (logical 0), sector addresses are assigned in sequential order. If this bit is set (logical 1), sector addresses are assigned in random order according to the pattern listed in the 52 byte memory buffer, which begins at the location addressed by the contents of IOPB bytes 6 and 7. (Refer to the description of the FORMAT TRACK operation in Paragraph 3-3.)

The "interrupt control" bits (4 and 5) enable or disable Controller Channel interrupts according to the scheme shown in Table 3-2.

The "data word length" bit (3) must be reset (logical 0) when the Diskette Controller is being used with 8-bit systems, or set (logical 1) when being used with 16-bit systems. This bit must be logical 0 when being used with the SBC 80 system (an 8-bit system).

Byte 2. Diskette Instruction

This byte specifies the diskette operation to be performed and identifies the diskette unit to be used:



The "unit select" bits (4-5) specify the drive address as follows:

00 = drive 0
01 = drive 1
10 = drive 2
11 = drive 3

The "data word length" must contain the same value as the corresponding bit in the channel word (byte 1).

The "op code" bits (0-2) specify one of the seven diskette operations (refer to Section 3-3):

BIT: 3	2	1	OPERATION
0	0	0	No operation
0	0	1	Seek
0	1	0	Format Track
0	1	1	Recalibrate
1	0	0	Read data
1	0	1	Verify CRC
1	1	0	Write data
1	1	1	Write 'Deleted' Data

Table 3-1. I/O Parameter Block (IOPB) Format

BYTE	IOPB FORMAT
*1	Channel Word
2	Diskette Instruction
3	Number of Records
4	Track Address
5	Sector Address
6	Buffer Address (Lower)
7	Buffer Address (Upper)

*The 16-bit address output to the Controller Channel by the two 'Write MA' channel Commands points to the first byte of an IOPB.

Table 3-2. Interrupt Control Bits

BIT: 5	4	FUNCTION
0	0	I/O complete interrupt request to be issued (a) upon completion of diskette operation, (b) upon detection of an error in any operation.
0	1	All I/O complete interrupts are disabled.
1	1	Illegal code
1	0	
NOTE:		The interrupt control bits do not affect interrupt requests which are issued as the result of a change in diskette ready status.

Byte 3. Number of Records

This binary number specifies the number of sectors to be transferred. Multi-sector operations are allowed, but they must not go beyond the last sector on a track (sector 52); that is, an address error (see Paragraph 3-5) will be indicated if (starting sector address) + (number of records) × 52_{10}. Therefore, the maximum block transfer is 52 sectors (from sector 1 to sector 52).

Byte 4. Track Address

This binary number identifies the track. Acceptable values are 0 to $4C_{16}$ (76_{10}), inclusive.

Byte 5. Sector Address

Bits 5 through 0 of this byte contain a binary number which specifies the first sector to be accessed during transfer operations. Acceptable values are 1 to 34_{16} (52_{10}), inclusive. Bits 6 and 7 are not used.

Byte 6. Buffer Address (Lower)

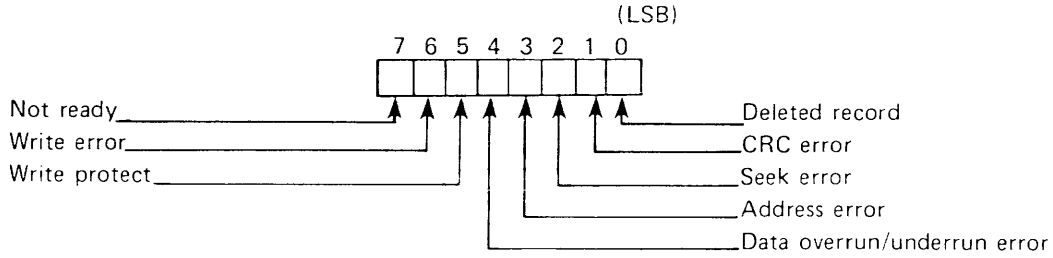
This byte contains the eight least significant bits of the 16-bit buffer memory address.

Byte 7. Buffer Address (Upper)

This byte contains the eight most significant bits of the 16-bit buffer memory address. Bytes 6 and 7 together contain the 16-bit address of the first word of the buffer in system memory. During read data operations, the data from the diskette is transferred to the buffer. During write operations, data from the buffer is written to diskette. During format track operations, the address assignment pattern and/or the data field "format characters" are stored in the buffer.

3-5. ERROR INDICATIONS

If the CPU executes a "read result byte" channel command (in response to a "read result type" channel command which returned a code of 00), the Diskette Channel will return the following result word on the system data bus:



The bits are defined as follows:

NOT READY. This bit (7) indicates that the selected unit was not ready or that the selected unit changed to a not ready state during an operation.

WRITE ERROR. This bit (6) indicates that, during a write operation, a condition existed which precluded data integrity. This error is detected by the drive and monitored by the Controller Channel. An example of a condition that could cause this error is an attempt to write through an unloaded head.

WRITE PROTECT. This bit (5) indicates that the selected drive contains a diskette platter which is in the "read only" mode. This condition is checked on format track, write data (with data address marks) and write data (with deleted data address marks) operations.

DATA OVERRUN/UNDERRUN ERROR. This bit (4) indicates that the Diskette Controller was not able to service a byte transfer request from the drive before the next request occurred. The data byte is "lost".

ADDRESS ERROR. This bit (3) indicates that the disk address received from the CPU is invalid; that is:

- track address > 76_{10},
- sector address = 00,
- sector address > 52_{10}, or
- sector address + number of records > 52_{10}

SEEK ERROR. This bit (2) indicates that, at the completion of a head movement sequence, the head is not positioned over the expected track. This bit indicates the Diskette System Controller and/or drive are malfunctioning, and a recalibrate diskette operation (see Paragraph 3-3) should be performed. Because all of the diskette operations may implicitly cause the head to move, a seek error can occur during any diskette operation.

CRC ERROR. This bit (1) indicates that the two CRC characters generated during a read data or verify CRC operation were not the same as the two CRC characters appended to the data field when it was written on diskette.

DELETED RECORD. This bit (0) indicates that a sector addressed during a read data or verify CRC operation was preceded by a deleted data address mark.

Three other error conditions are indicated when more than one error bit is true:

ID CRC ERROR. If the address error (3) and CRC error (1) bits are true, it indicates that the CRC characters generated during the reading of an ID field were not the same as the CRC characters appended to the field when it was written by a format track operation.

NO ADDRESS MARK. If the address error (3), seek error (2) and CRC error (1) bits are true, it indicates that no address mark was encountered for a full revolution of the diskette. This usually indicates that the track has not been formatted.

DATA MARK ERROR. If the address error (3), seek error (2), CRC error (1), and deleted record (0) bits are true, it indicates that the data field of a particular sector was not preceded by either a data mark or a deleted data mark.

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description with a circuit analysis of the SBC 202 Double Density Diskette Controller. The circuit analysis is presented with the assumption that the reader is familiar with the architecture of the SBC 80 Single Board Computer and has access to literature describing in detail the Intel Series 3000 components.

4-2. FUNCTIONAL DESCRIPTION

The control functions of the channel and Interface Board are provided by an 8-bit microprogrammed processor, implemented with Intel's Series 3000 Bipolar Microcomputer Set. The 8-bit controller includes four 3002 Central Processing Elements (2-bit slices per CPE), a 3001 Microprogram Control Unit, and 512 × 32 bits of 3604 programmable-read-only-memory (PROM) which stores the microprogram. The processing and control capabilities of the Diskette Controller are achieved by execution of the microprogram.

The Channel Board and Interface plug into the system backplane. The Channel Board, together with the Interface Board, constitute the Diskette Controller.

4-3. CHANNEL BOARD

The Channel Board is the primary control module within the Diskette Controller. The Channel Board receives, decodes, and responds to channel commands from the Central Processor Unit (CPU) in the host system. The Channel Board can access the host system memory to determine the particular diskette operations to be performed and to fetch the parameters required for the successful completion of the specified operations. The Channel Board also monitors drive status and error conditions, and organizes these indications into "result type" and "result byte" words that can be read by the CPU in the host system.

For description purposes, the circuitry on the Channel Board can be divided into six functional blocks: (see Figure 4-1)

- Channel command block
- Micro control unit (MCU) block
- Microprogram memory block
- Central processing element (CPE) block
- Data/clock shift register (SR) block
- Data flow control block

The CHANNEL COMMAND BLOCK is responsible for recognizing and decoding channel commands being executed by a CPU in the host system. When the channel command block recognizes the switch-selectable BASE address of the Diskette Channel on the Multibus address lines, it decodes the three least significant address bits (ADR0/ - ADR2/) to determine which of the seven channel commands is being executed. The three address bits are also latched and made available to the MCU block, which is ultimately responsible for controlling the diskette controller's response to a channel command. The channel command block also includes the interrupt latch which stores the fact that an interrupt request has been issued to the CPU by the microprogram.

The MICRO CONTROL UNIT (MCU) BLOCK accepts and decodes the three address bits from the channel command block (ADR0/ - ADR2/) specifying a channel command or the three least significant data outputs from the CPE block (D0-D2) specifying one of the seven diskette operations. The two groups of 3 bits select one of the ten routines which implement the channel commands and I/O operations. Having determined the microprogram routine to be executed, the MCU block then generates and outputs the appropriate nine-bit memory address from the microprogram memory. The MCU continuously examines the two flag control lines and the seven address control lines (AC0 - AC6) from the microprogram memory block to determine the address of the next microinstruction to be fetched and executed.

The MICROPROGRAM MEMORY BLOCK stores the microprogram. The microprogram memory is organized into 512 words of 32 bits each. The nine address bits from the MCU block determine which 32-bit microinstruction will be output from the microprogram memory. Nine bits of the microinstruction (the address control and flag control bits) are applied to the MCU block, as mentioned above, while the seven function bits (F0-F6) are applied to the CPE block and specify the operation to be performed by the processing elements. The other sixteen bits of the microinstruction words perform a variety of control functions, that are described in the following paragraphs.

The CENTRAL PROCESSING ELEMENT (CPE) BLOCK includes four Intel 3002 Central Processing Elements, which form an 8-bit processor. The CPE block receives data from the data flow control block and the data/clock shift register block and receives status information from the Interface Board. The CPE can operate on these various types of input data under the direction of the function and mask control bits from the microprogram memory. The results of these arithmetic/logical operations can then be output onto the eight most significant

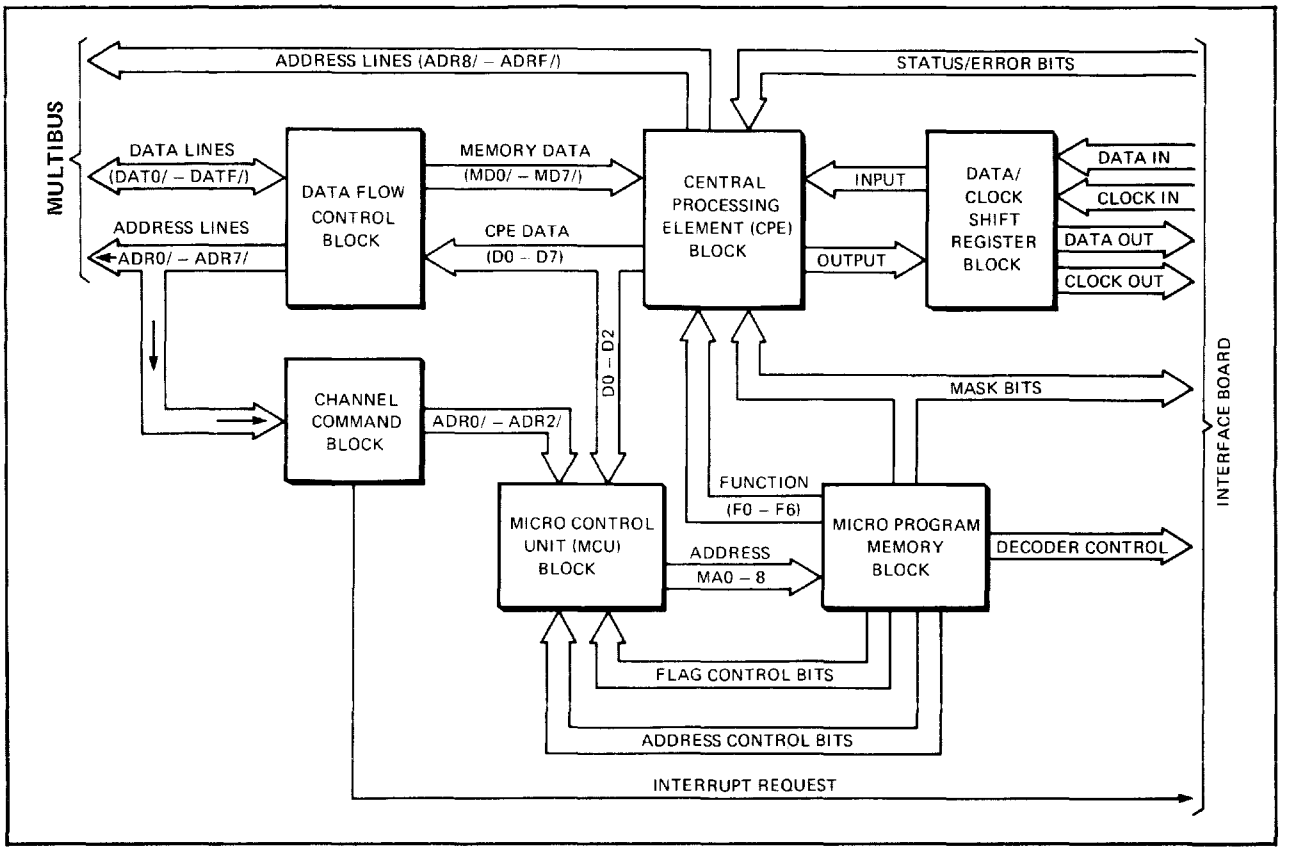


Figure 4-1. Channel Board Functional Block Diagram

system address lines (ADR8/ - ADRF/) or the eight CPE data lines (D0 - D7). D0 - D7 are, in turn, made available to the MCU block, the data/clock shift register block and the data flow control block.

The DATA/CLOCK SHIFT REGISTER BLOCK includes the shift registers that accept the serial data bits and the serial clock bits and input them, in parallel, to the CPE block during read operations. During write operations, the data and clock bytes are (parallel) loaded into the shift registers from the CPE block and shifted out (serially) to the Interface Board.

The DATA FLOW CONTROL BLOCK routes data from the CPE data lines (D0 - D7) to the eight least significant System address lines (ADR0/ - ADR7/) or to either the lower or upper eight lines of the System data bus (DATA0/ - DATA7/ or DATA8/-DATAF/). This block also routes data from either half of the System data bus onto the memory data input lines (MD0/-MD7/) that feed the CPE block.

4-4. CHANNEL COMMAND BLOCK. The channel command block recognizes and decodes all channel commands directed to the diskette controller. This block includes an eight position (S1) for BASE address assignment, eight 74LS86 EXCLUSIVE-OR gates for address recognition, two 3205 three-to-eight decoders, two 7474 D-type flip-flops, a 74175 quad latch, and other assorted gating circuits.

The CPU specifies channel operations for the Diskette system by executing one of the seven channel commands. A channel command may be the result of either an input or output instruction to a dedicated I/O port address on the Channel Board:

1) Write MA Lower (output to "BASE+1")
2) Write MA Upper and Start I/O (output to "BASE+2")
3) Stop Diskette Operation (output to "BASE + 3")
4) Reset Channel (output to "BASE+7")
5) Read Subsystem Status (input to "BASE+0")
6) Read Result Type (input to "BASE+1")
7) Read Result Byte (input to "BASE+3")

The three least significant bits (ADR0/-ADR2/) of the 8-bit I/O address (received at pins P1-51 through P1-58) differentiate between the various input or output channel commands. The five most significant address bits (ADR3/-ADR7/) select the Channel Board if they match the BASE address that is assigned by setting five positions of switch S1. These five switch positions each feed one input on five EXCLUSIVE-OR gates. If ADR3/-ADR7/ match the switch-selected BASE address, the 7410 NAND gate (A31-8) is activated and, in turn, enables one of the two 3205 decoders.

If an input channel command is being received, the RD CMD line (pin P2-60) will be true, and the 3205 decoder at A20 will be enabled. Address bits ADR0-ADR2 (once inverted) are applied to the three data inputs on the 3205 section (A0-A2), and activate one of three inverted outputs (O_0, O_1 or O_3), depending on the channel command. If it is "read subsystem status" command, output 0 goes true and READ INT/ is asserted at pin P2-57. (On the Interface Board, READ INT/ is used to gate the device 0 and device 1 ready indicators onto system data bus lines 0 and 1, DAT0/ and DAT1/). The low level on READ INT/ also enables two 8093 circuits, one of which transmits the output of the interrupt latch (INT/) to the data bit 2 line (DAT2/) of the system data bus. The other 8093 circuit transmits a low-level to the data bit 3 line (DAT3/), indicating that the diskette controller is present. INT/ is also passed to the Interface Board via pin P2-40.

If a "read result type" command is being received, the output 1 from the decoder goes true, and the RD RI/ signal is generated (pin P2-37) The low level on RD RI/ pre-sets the interrupt latch (A37-10), thus removing the active-low system interrupt request (INT).

The interrupt latch can subsequently be clocked reset (i.e., reset to the active-low state) by a pulse on the CLK line, when the central processing element block determines that an "I/O complete" or "ready status change" interrupt should be issued.

If a "read result byte" command is being received, output 3 from the decoder will go true, and the 74175 quad latches are clocked, latching up address bits ADR0-ADR2. The three most significant quad latch outputs are made available to the micro control unit block, which responds to this command via a routine stored in microprogram memory. Either read result command will generate the RD RES/ signal which is used by the data flow control block to gate the appropriate status word onto the Multibus data lines.

If an output channel command is being received, the WRT CMD line (pin P2-53) will be true, and the other 3205 decoder will be enabled. Address bits ADR0-ADR2 are applied to inputs A0-A2, causing one of the eight inverted decoder outputs to go true. If outputs 0, 1 or 2 go true, the WSUB1/ line (pin P2-48) is activated. If outputs 4, 5 or 6 from the decoder go true, the WSUB2/ line (pin P2-47) is activated. Either WSUB1/ or WSUB2/ will cause the 74175 quad latches to be clocked and latch up address bits ADR0 - ADR2, just as a "read result byte" command did. The three most significant outputs of the quad latches are made available to the micro control unit block which responds to the "write MA lower", the "write MA upper and start I/O" and the "read result byte" channel commands, using routines stored in microprogram memory. The response mechanisms for the other channel commands are implemented in hardware, not micro code.

If a "stop diskette operation" command is being received, output 3 from the decoder goes true, asserting a low level on the SET STOP/ line (pin P2-31). The subsequent low-to-high transition on SET STOP/ clocks the stop latch reset (i.e., the active-low state). After the stop latch is sampled, the microprogram presets (i.e., clears to the non-active-high state) the latch.

If a "reset channel" command is being received, output 7 from the decoder goes true, asserting a low level on the RESET/ line to the Interface Board (pin P2-49).

4-5. MICROPROGRAM CONTROL UNIT (MPU). The Microprogram Control Unit (Figure 4-2) is the primary source of control for the Diskette Controller. The MPU controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

- Maintenance of the microprogram address register
- Selection of the next microinstruction based on the contents of the microprogram address register
- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence
- Saving and testing of carry output data from the central processor (CPE) array
- Control of carry/shift input data to the CPE array
- Control of microprogram interrupts

Address control information is supplied to the 3001 at inputs AC0-AC6. AC1-AC6 are provided directly from bits 27-32 of the microinstruction currently being fetched from microprogram memory. The AC0 input, however, is supplied by the output of the 74151 eight-to-one multiplexer.

Five control lines from the Interface Board (AZ, INDEX, XFER REQ, TIME OUT and F), one line from the CPE block (CO) and one line from the channel command block (BUSY START) are applied to the 74151 inputs along with the AC0 bit (bit 26) from the microinstruction currently being fetched. The three select lines applied to the A, B and C inputs on the 74151 section specify which of the eight lines are actually multiplexed through to the AC0 input on the 3001 device. The three select lines are supplied by bits 14, 15 and 16 (IN0, IN1 and IN2) of the current microinstruction. Table 4-1 correlates the values in bit positions 14, 15 and 16 of the current microinstruction with the control line which is multiplexed into the AC0 input on the 3001 section.

The "flag logic" input (F1) to the 3001 device (pin 17) is also provided by CO. The level on the CO line will reflect the "Carry out" output from the 3002 Central Processing Element (CPE) at A21 or the "shift right" output from the 3002 CPE at A23.

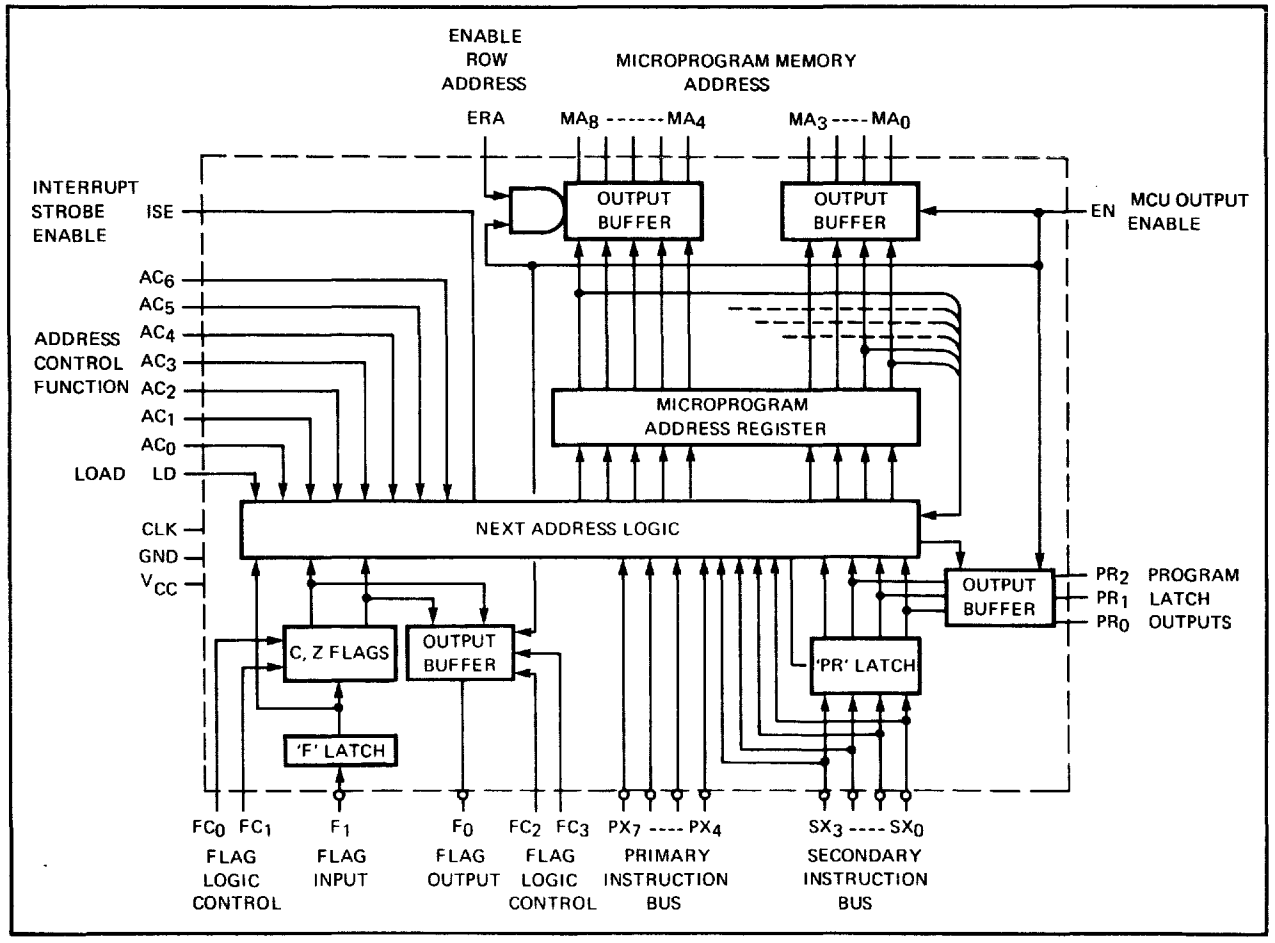


Figure 4-2. Microprogram Control Unit Functional Block Diagram

Table 4-1. ACO Input Selection

Select Lines			ACO Input At 3001 MCU
(Bit 14)	(Bit 15)	(Bit 16)	(Pin 39)
0	0	0	Bit 26 of current microinstruction (ACO)
0	0	1	CO: The carry out output from the 3002 CPE at A21 or the shift right output from the 3002 CPE at A23.
0	1	0	BUSY START: Indicates that a 'write MA lower', 'write MA upper' or 'read result byte' channel command has been received.
0	1	1	F (pin P2-58): Indicates that data/clock shift registers are full during read or empty during write.
1	0	0	AZ (pin P2-41): Indicates a valid CRC check (all zeros).
1	0	1	INDEX (pin P2-42): Indicates that an index mark has been detected (i.e., the beginning of a track).
1	1	0	XFER REQ (pin P2-39): Indicates that Interface Board has requested use of the Multibus.
1	1	1	TIMEOUT (pin P2-38): Ten millisecond pulse that is used by the microprogram for general timeouts.

The "clock" input (CLK) to the 3001 device (pin 19) is supplied by CLK1/ (pin P2-3) which is one of the two clock pulses generated on the Interface Board (see Figure 4-13).

The load input (LD) to the 3001 (pin 36) is fed by the master reset (MR) signal from the Interface Board (pin P2-56).

The four "flag logic control" inputs (FC0-FC3) to the 3001 device are provided by bits 17 and 18 of the current microinstruction. Bit 17 is applied to both FC0 (pin 15) and FC1 (pin 16) while bit 18 is applied to FC2 (pin 13) and FC3 (pin 12).

The "enable" (EN) and "enable row address" (ERA) inputs to the 3001 (pins 25 and 35, respectively) are held high.

Unless the active-low master reset (MR/) signal from the Interface Board is true (low), the "secondary instruction bus" inputs (SX0-SX3) to the 3001 device (pins 10, 8, 6 and 5, respectively) will reflect the complement of the level on the four least significant memory address outputs (MA0-MA3). That is, SX0 = MA0, SX1 = MA1, SX2 = MA2 and SX3 = MA3 if MR/ is false (high). If MR/ is true (low), the four SXn inputs will be all high, regardless of the state of the MAn outputs.

The four "primary instruction bus" inputs (PX4-PX7) to the 3001 device are fed by the four inverting outputs of the 8234 eight-to-four multiplexer (A5). The multiplexer outputs are controlled by the levels on the S0 and S1 inputs.

The A1, A2 and A3 inputs to the 8234 section are the three least significant data outputs from the central processing element (CPE) block that have been buffered and inverted; the A0 input is always high. After having fetched the diskette instruction byte from the I/O Parameter Block in system memory (see Paragraph 3-3) the CPE block will output the three bits that specify one of the seven diskette operations onto its three least significant data outputs (D0-D2).

At this time, the mask and output bits of the current microinstruction being output from the microprogram memory block will produce a high level on the S0 input to the 8234 section and a low level on the S1 input, multiplexing the inverted levels of the 8234's A inputs (specifying a particular diskette operation) into the PX4-PX7 inputs on the 3001 MCU. This allows the 3001 MCU to subsequently access those microinstructions which will effect the appropriate diskette operation.

The B1, B2 and B3 inputs to the 8234 multiplexer are the three least significant system address bits that were buffered and inverted in the channel command block; the B0 input is always held low. Recall that these three address bits specify one of the seven channel commands. At this time, the mask and output bits of the current microinstruction being output from the microprogram memory block will produce a low level on the S0 input to the 8234 section, multiplexing the inverted levels of the 8234's B inputs (specifying a particular channel command) into the PX4-PX7 inputs on the 3001 MCU. This allows the 3001 MCU to subsequently access those microinstructions which will produce the proper Diskette System response to the channel command received.

The MCU outputs the 9-bit address of the next microinstruction to be fetched on MA0-MA8. MA0-MA8 are applied to the nine address inputs on each of the 3604 PROM's that constitute the microprogram memory.

4-6. MICROPROGRAM MEMORY BLOCK. The microprogram memory block stores the microinstructions which direct the operation of the diskette controller. The microprogram memory block consists of four 3604 programmable-read-only-memory devices (512 × 8 bits each), which store 32 bit microinstructions; a 3205 three-to-eight decoder, which generates eight timing control pulses (DEC OUT0-DEC OUT7) based on bits 11, 12 and 13 (OUT0-OUT2) of the current microinstruction; and a 3404 six-bit high speed latch, which provides various control signal levels based on the decoder outputs mentioned above and the mask bit field of the current microinstruction.

The 9-bit memory address (MA0-MA8) for the four 3604 PROM's is provided by the 3001 Microprogram Control Unit. MA0-MA8 cause the addressed microinstruction to appear on the 32 output lines from the four PROM's.

Table 4-2 summarizes bit definitions for the 32-bit microinstructions. The address control bits, AC0-AC6 (bits 26-32), the flag control bits (bits 17 and 18), and the input control bits used for AC0 select (bits 14-16) are fed to the micro control unit block. The function field bits, F0-F6 (bits 19-25), the mask bits M0-M7 (bits 1-8) and the K-bus select bits S0 and S1 (bits 9-10) are applied to the central processing element (CPE) block. The output bits OUT0-OUT2 (bits 11-13) are applied to the three address inputs on a 3205 decoder. The enable inputs to this 3205 section are provided by the CLK2/ pulse from the Interface Board (pin P2-30), the seventh mask bit M7 (bit 8 of the current microinstruction) and S0, one of the two K-bus select bits mentioned above (bit 9 of the current microinstruction). The eight decoder outputs, DEC OUT0-DEC OUT7, provide timing control pulses that, when used with the mask bits, provide overall control for the Diskette Controller (see Table 4-3).

The mask field bits M0-M7 (bits 1-8 of the current microinstruction) are actually used for three disjoint functions in the Diskette System:

1) Generating control signals for the hardware. These control signals are pulses (positive or negative and of 50-75 nsec. duration) or levels. The pulses are generated by gating the appropriate mask bit with one of the 3205 decoder outputs (DEC OUTn). The levels are derived by using the DEC OUTn outputs to strobe 3404 six-bit latches. The DEC OUTn outputs provide the write enable strobes to the 3404 latches, while the mask bits provide the data inputs and, consequently, the actual controls. Refer to Table 4-3 for a summary of the control pulses and levels generated by the DEC OUTn strobes and mask field bits. The control function definitions are given in Table 4-4.

2) Driving the input multiplexers to the 3002 Central Processing Element (CPE) array. Four fields (data shift register, clock shift register, errors and status) are multiplexed through 8234 and 8233 multiplexer devices and into the I-bus inputs of the CPE array. The selection bits for the multiplexers are provided by the mask field bits, as listed in Table 4-5.

3) Providing generalized inputs to the K-bus inputs of the 3002 CPE array. The mask bits are multiplexed through two 8234 multiplexer devices and into K-bus inputs of the CPE array. The selection bits are provided by S0 and S1 (bits 9-10 of the current microinstruction). Table 4-6 correlates the levels on the S0 and S1 lines with the K-bus inputs.

4-7. CENTRAL PROCESSING ELEMENT (CPE). The central processing element (CPE) block executes the function indicated by each microinstruction output from the microprogram memory. The CPE block includes an array of four Intel 3002 Central Processing Elements, as well as four 8234 and one 8233 eight-to-four multiplexers that provide various inputs to the CPE array.

An Intel 3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. When wired together in an array, a set of CPE's provide the following capabilities:

- Two's complement arithmetic
- Logical AND, OR, NOT and EXCLUSIVE-OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

A functional block diagram of a 3002 CPE is shown in Figure 4-3.

Table 4-2. Microinstruction Bit Assignment

MICROINSTRUCTION BIT	SIGNAL	DEFINITION	PROM LOCATION – PIN
01	MASK0 (M0)	Mask field	A13- 9
02	MASK1 (M1)		A13-10
03	MASK2 (M2)		A13-11
04	MASK3 (M3)		A13-13
05	MASK4 (M4)		A13-14
06	MASK5 (M5)		A13-15
07	MASK6 (M6)		A13-16
08	MASK7 (M7)		A13-17
09	SLK0 (S0)	K-bus select	A12- 9
10	SLK1 (S1)		A12-10
11	OUT0	Decoder output select	A12-11
12	OUT1		A12-13
13	OUT2		A12-14
14	IN0	AC0 Select	A12-15
15	IN1		A12-16
16	IN2		A12-17
*17	FC0	Flag control	A11- 9
*17	FC1		A11- 9
*18	FC2		A11-10
*18	FC3		A11-10
19	F0	Function field	A11-11
20	F1		A11-13
21	F2		A11-14
22	F3		A11-15
23	F4		A11-16
24	F5		A11-17
25	F6		A10- 9
26	AC0	Address control	A10-10
27	AC1		A10-11
28	AC2		A10-13
29	AC3		A10-14
30	AC4		A10-15
31	AC5		A10-16
32	AC6		A10-17

*Bit 17 drives FC0 and FC1; bit 18 drives FC2 and FC3

Table 4-3. Control Pulses and Levels Generated by Microprogram

OUT CODE (DEC OUT n) MASK BIT	000 (0)	001 (1)	010 (2)	011 (3)	100 (4)	101 (5)	110 (6)	111 (7)
M0	CSTEP		NSUB0			AMWRT	SMREQ	CSYNC
M1	SSCLK	RDYRS	NSUB1			WFLRS	STBDU	RSAMD
M2	LDHD			LDNXM			STBDL	UNLHD
M3		RINH				LOWEN	LDADD	RSTST
M4		SINH		WTGTN		MEMWT	GTR43	NGT43
M5		SACK		SR OUT	CRC MD		SINTR	RNDX
M6		RDOR		LDADM	DIREC		CINBS	LDOPC

Table 4-4. Control Function Definitions

– – CONTROL FUNCTION DEFINITIONS – –		
CSTEP	–	This pulse triggers the one-shot which drives the STEP/ line to the diskette drives. STEP/ causes the selected drive to move its head one track.
SSCLK	–	This pulse triggers the TIMEOUT one-shot. TIMEOUT provides a 10 msec. pulse for use by the microprogram.
LDHD	–	This pulse sets the LOAD latch on the Interface Board which causes the read/write head on the selected unit to be loaded.
RINH	–	This pulse resets the inhibit memory write latch (A48–1).
SINH	–	This pulse sets the inhibit memory write latch (A48–4).
SACK	–	This pulse sets the transfer acknowledge (XACK/) latch on the Interface Board.
RDOR	–	This pulse resets the data overrun latch on the Interface Board.
NSUB0 and NSUB1	–	These levels select 'primary instruction bus' inputs to 3001 MCU.
LDNXM	–	This level is used to load the clock shift register with the bit patterns required to write the different address marks onto a diskette.
WTGTN	–	When the data and clock shift registers are empty, this level allows both shift registers to be parallel loaded with information that will be serially shifted out to the Interface Board and then to the diskette. Used to generate PE/ and WRT GT/ signals.

Table 4-4. Control Function Definitions (Continued)

– – CONTROL FUNCTION DEFINITIONS (CONTINUED) – –		
SROUT	–	This level enables data bits from data register (when high) or from 9401 CRC device (when low) to be sent to the selected diskette.
LDADM	–	This level is used to load clock shift register with the bit patterns required to write the different address marks onto a diskette.
CRCMD	–	This level indicates the operating mode for the 9401 CRC device on the Interface Board.
DIREC	–	This level indicates the direction of head movement for the selected diskette drive.
AMWRT	–	This level enables writing of an extra clock pulse and is activated during writing of an address mark.
LOWEN	–	This level drives the GATE LOWER line that enables data onto the memory data inputs (M0/ – M7/) to the CPE array.
MEMWT	–	This level indicates when the Diskette System wishes to write data to memory.
SMREQ	–	This pulse initiates the bus request sequence intended to gain master control of the Multibus.
STBDU	–	This pulse loads CPE data outputs (D0 – D7) into the latch which drives the system data lines, DATA8/ – DATAF/.
STBDL	–	This pulse loads CPE data outputs (D0 – D7) into the latch which drives the system data bus lines, DATA0/ – DATA7/.
LDADD	–	This pulse loads CPE data outputs (D0 – D7) into the latch which drives the system address bus lines, ADR0/ – ARD7/.
SINTR	–	This pulse is used to generate a signal which clocks the interrupt latch on the Channel Board.
CINBS	–	This pulse is used to latch data from the system data bus into the latches which drive MØ – M7/ of the CPE array.
CSYNC	–	This pulse initializes the synchronization logic prior to detecting an address mark.
RSAMD	–	This pulse resets the synchronization logic prior to initializing the logic with the CSYNC pulse.
UNLHD	–	This pulse clears the LOAD latch on the Interface Board, and ultimately causes the read/write head on the selected drive to be unloaded.
RSTST	–	This pulse is used to generate CLR START STOP signal which resets the STOP latch and the 74145 latch at A8–1 on the Channel Board.
RNDX	–	This pulse resets the INDEX latch on the Interface Board.
LDOPC	–	This pulse latches diskette operation code (D0–D5) and makes latched code available to 'primary instruction bus' multiplexer.

Table 4-4. Control Function Definitions (Continued)

– – CONTROL FUNCTION DEFINITIONS (CONTINUED) – –		
RDYRS	–	This pulse reset the Drive Ready flip-flops on the Interface Board.
WFLRS	–	This level generates the write fault reset pulse to the selected drive.
GTR43	–	This pulse sets the low current mode for writes on tracks greater than 43_{10}.
NGT43	–	This pulse resets the low current mode for writes on tracks equal to or less than 43_{10}.

Table 4-5. I–BUS Selection by Mask Field Bits

	INPUT FIELDS*			
MASK BITS	DATA SHIFT REGISTER (A36 and A29) OUTPUTS	CLOCK SHIFT REGISTER (A34 and A27) OUTPUTS	ERROR LINES (DOR, WRT PROT, WRT ERR, SEL DR NRDY)	STATUS LINES (DRO, DR1, STOP, TRACK00)
M7 =	1	1	1	1
M6 =	0	0	1	1
M5 =	0	0	0	1
M4 =	1	1	0	0
M3 =	0	1	0	0

* An input field will be multiplexed into the I inputs of 3002 CPE array if the mask bits reflect the values listed for that field and if the K-Bus select line, S0 (bit 9 of the current microinstruction) is high (logical 1). Refer to Paragraph 4-7 for a more complete description of the 3002 CPE array inputs.

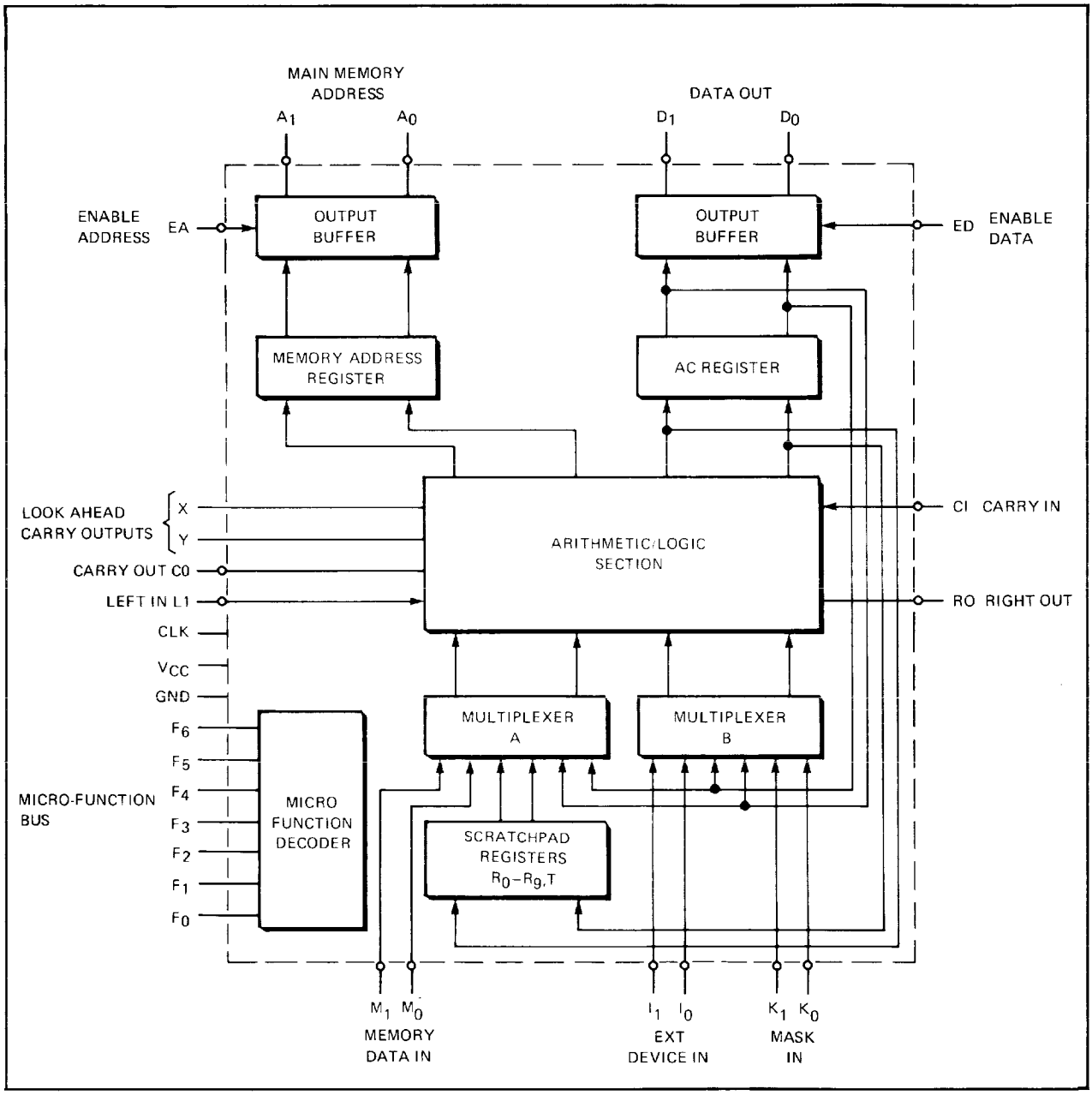


Figure 4-3. Central Processing Element Functional Block Diagram

During each micro-cycle, the function field of the current microinstruction is applied to the F-bus inputs (F0-F6) of each 3002 CPE. The function bits are decoded, the operands are selected by the internal multiplexers, and the specified operation is performed. Within each CPE, data is stored in eleven scratchpad registers or the accumulator.

Data being output from the CPE array is carried on the address bus (A0-A7) or the data out bus (D0-D7). The address outputs drive the eight most significant lines of the system address bus, ADR8-ADRF. The data outputs are made available to the data flow control block (Paragraph 4-9) and the micro control unit block (Paragraph 4-5).

Data is brought into the CPE array on three separate input buses, the memory data bus (M0-M7), the I-bus (I0-I7) and the K-bus (K0-K7). The memory data inputs are supplied by the data flow control block (Section 3.2.6) which routes data from the system data bus to the CPE array. The latter two buses are driven by five multiplexers.

The K-bus inputs (K0-K7) are driven by two 8234 eight-to-four multiplexers (located at A33 and A26). The S0 and S1 outputs from the microprogram memory (bits 9 and 10 of the current microinstruction) determine the four outputs on each of the two 8234 sections. If S0 = 1 and S1 = 0, all eight inverted outputs will be low. If S0 = 1 and S1 = 1, all eight outputs will be high. If S0 = 0, however, the eight mask bits, M0-M7, from the microprogram memory (bits 01-08 of the current microinstruction) will be inverted and applied to the K-bus inputs of the CPE array (see Table 4-6).

The I-bus inputs (I0-I7) are driven by two 8234 (inverting outputs) and one 8233 (non-inverting outputs) eight-to-four multiplexers (located at A28, A45 and A35). Mask bits M3-M7 from the microprogram memory (bits 04-08 of the current microinstruction) determine the I-bus inputs as listed in Table 3-4. These mask bits will enable the eight outputs from the two 4-bit data shift registers (at A36 and A29), or the eight outputs from the two clock shift registers (at A34 and A27) through the 8233 section and one of the 8234 sections and into the I0-I7 inputs on the CPE array. The mask bits can also enable the four error lines (DOR, WRT PROT, WRT ERR and SEL DR NRDY) or the four status lines (DR0, DR1, STOP and TRACK 00) from the Interface Board through the other 8234 section (at A45) and into the I4-I7 inputs on the CPE array.

The clock input to the 3002 CPE's is provided by the CLK1/ pulse generated on the Interface Board. The enable address inputs (EA), which enable the address outputs (A0-A7), are fed by the SELECTED line from the Interface Board (pin P2-43). When true, SELECTED indicates that the Diskette Controller has master control of the Multibus. The enable data input (ED) to each 3002 CPE is permanently held low (active).

The carry output (CO) from each 3002 CPE feeds the carry input (CI) of the adjacent 3002 CPE. Likewise, the shift right output (RO) feeds the shift right input (LI) of the adjacent 3002 CPE. The carry output (CO) from the most significant CPE (A21-7) feeds its own shift right input (LI) and is wire—ORed with the shift right output (RO) from the least significant CPE (A23-8) to form the CO line, which is applied to the flag control input (FI) on the 3001 Microprogram Control Unit. CO is also inverted and applied to the D1 input on the 74151 multiplexer (A30-3) which provides the least significant address control bit, AC0, to the 3001 MCU. The carry input (CI) to the least significant 3002 CPE (A23-10) is provided by the flag control output (FO) from the 3001 MCU.

4-8. DATA/CLOCK SHIFT REGISTER. During read operations, the data/clock shift register (SR) block accepts serial data and clock bits that the Interface Board has received from the selected diskette drive and converts them into eight bit bytes that are input, in parallel, to the CPE array. During write operations, the shift registers are parallel loaded with data and clock bytes which are then shifted out to the Interface Board. This block includes four 9300 four-bit shift registers.

The data and clock bits are interspersed when information is written on disk. When that information is later read, the dis-

Table 4-6. K–BUS Input Selection

K–BUS SELECT LINES		K–BUS INPUTS TO 3002 CPE ARRAY							
S1 (Bit 10)	S0 (Bit 9)	K0	K1	K2	K3	K4	K5	K6	K7
0	0	M0	M1	M2	M3	M4	M5	M6	M7
0	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0	0

Note that only when S0 and S1 equal zero will the K-bus inputs be supplied by the mask bits; otherwise, the K-bus inputs will be all ones or all zeros.

kette drive separates the data and clock pulses before passing them to the Interface Board.

The Interface Board, in turn, sends the data bits to the Channel Board via the SR DATA IN/ line (pin P2-22) along with the data strobe SR DATA STB/ (pin P2-24). SR DATA IN/ feeds the J and K/ inputs on the first data shift register at A36. The Q3 output from this first shift register then feeds the J and K/ inputs on the shift register at A29. When the data shift registers are full, the eight data bits are transferred in parallel to the CPE array. The four outputs from the first data shift register (A36) are applied to the "A" inputs on the 8233 multiplexer that feeds the four least significant I-bus inputs to the CPE array. The first two outputs are also made available to the Interface Board via the ID0/ (pin P2-26) and ID1/ (pin P2-23) lines. The four outputs from the second data shift register (A29) are applied to the 8234 multiplexer (A28) that feeds the four most significant bits of the I-bus inputs to the CPE array. Both data shift registers are clocked by SR DATA STB.

During write operations, both data shift registers can be parallel loaded when the PE/ input is low. PE/ will go low when the shift register is empty and the WTGTN signal is true (see Table 4-3).

The parallel inputs to the first data shift register (A36) are supplied by the four least significant data outputs from the CPE array, as follows:

D0 → P0
D1 → P1
D2 → P2
D3 → P3

The parallel inputs to the second data shift register (A29) are supplied by the four most significant CPE array data outputs:

D4 → P0
D5 → P1
D6 → P2
D7 → P3

The data bits can then be shifted out, in serial, to the Interface Board via the SR DATA OUT line (pin P2-25) which is driven by the Q3 output on the second data shift register.

During read operations, the Interface Board sends the clock bits (that were interleaved with the data bits on the diskette) to the Channel Board via the SR CLK IN/line (pin P2-6) along with the clock strobe, CLK SR STB (pin P2-8). SR CLK IN/ feeds the J and K/ inputs on the first clock shift register at A34. The Q3 output of this first clock shift register then feeds the J and K/ inputs on the shift register at A27. When the clock shift registers are full, the eight clock bits can be transferred in parallel to the CPE array. The four outputs from the first clock shift register (A34) are applied to the "B" inputs on the 8233 multiplexer that feeds the four least significant bits of the I-bus to the CPE array. The four outputs from the second clock shift register (A27) are applied to the 8234 multiplexer that feeds the four most significant bits of the I-bus. Both clock shift registers are clocked by CLK SR STB.

During write operations, both clock shift registers can be parallel loaded when the PE/ signal (described above) is low. The P0, P1 and P2 inputs to the first clock shift register and the P2 and P3 inputs to the second clock shift register are tied to ground. The P3 input to the first shift register and the P1 input to the second are both fed by the output of a 7408 AND gate (A7-6). The inputs to this gate are the LDNXM and LDADM control levels which have been set in the 3404 latches at A16 by the microprogram (refer to Table 4-3). The P0 input to the second clock shift register is fed by the LDADM control output. LDNXM and LDADM allow the microprogram to produce the varied patterns of clock bits that are required to write the different types of address marks onto a diskette.

4-9. DATA FLOW CONTROL. The data flow control block routes data to/from the various other functional blocks within the Channel Board. This block consists of five 8212 bidirectional latching bus drivers, a 3404 six-bit latch and various gating circuits.

The six least significant data outputs (D0-D5) from the CPE array are applied to the inputs of the 3404 six-bit latch. When the microprogram generates the LDOPC control pulse (see Table 4-3), D0-D5 are latched and inverted. D0/-D2/ are made available to the "primary instruction bus" multiplexer (A5) in the MCU block. D3/ is used for 16-bit data flow control as described below. D4/ and D5/ are sent to the Interface Board as the unit select signals, USA (pin P2-9) and USB (pin P2-12), respectively.

All eight CPE data outputs, D0-D7, are also applied to three of the 8212 latching bus drivers. D0-D7 are loaded into the 8212 device at A41 when the microprogram generates the LDADD control pulse (see Table 4-3). The 8212 device at A41 drives the eight least significant lines of the system address bus, ADR0/-ADR7/. When the microprogram generates the STBDL control pulse (see Table 4-3), D0-D7 are latched into the 8212 device at A43 which drives the eight least significant lines of the system data bus, DAT0/-DAT7/ (pins P1-67 through P1-74). STBDL is generated when the microprogram is setting a result word or preparing write data. When the microprogram generates the STBDU control pulse (see Table 4-3), D0-D7 are latched into the 8212 device at 42, which drives the eight most significant system data bus lines, DAT8/-DATF/ (pins P1-59 through P1-66). STBDU would only be generated if the Diskette System were operating in the 16 bit mode. The address latch (A41) is gated onto the MDS system bus whenever the SELECTED signal is true. The high-order data latch (A42) is gated onto the bus whenever the SELECTED, MEMORY WRITE and 16-BIT MODE signals are true. The low-order data latch (A43) is gated onto the bus during memory write operations or "read result" operations.

When a master bus module is in the System outputs data to the Diskette Controller, the data from lines DAT0/ - DAT7/ is

applied to the 8212 bus driver at A25. DAT8/ - DATF/ is applied to the 8212 at A24. The data on those lines are strobed into the input latches at A24 and A25 by the microprogram control pulse CINBS (see Table 4-3). "Slave" memory modules also drive the data lines, DAT0/ - DAT7/ and possibly DAT8/-DATF/. Memory data are strobed into the latches when the STB MEM IN signal is generated by the Interface Board. The outputs from the devices at A24 and A25 are "OR-ed" into lines M0/-M7/. Depending on the state of the GATE LOWER signal, data from only one of the two latches will actually be gated onto the M input lines (M0/-M7/) to the CPE array.

4-10. INTERFACE BOARD

The Interface Board provides the Diskette Channel with a means of communicating with the Diskette Drives, as well as with the system bus. Under control of the microprogram being executed on the Channel Board, the Interface Board generates those signals which cause the read/write heads to move to the proper track. The Interface Board accepts the data being read off the diskette, interprets certain synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and passes the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times. It also generates CRC characters which are appended to the data; this allows the data to be verified when it is subsequently read.

When the CPU in the system issues a Channel Command to the Controller the Interface Board acknowledges the command as required by system bus protocol.

When the Controller requires access to the system memory, the Interface Board requests and maintains master control of the system bus, and generates the appropriate memory commands.

For descriptive purposes, the circuitry on the Interface Board can be divided into five functional blocks (see Figure 4-4):

- Disk drive control block
- Serial data/clock synchronization block
- Write clock generator block
- Cyclic Redundancy Check (CRC) block
- Bus control block

The DISK DRIVE CONTROL BLOCK provides the unit selection/head loading (SELn/) signal, the direction indicator (DIR/) and the step pulse (STEP/) that moves the read/write head on the selected unit one track in the specified direction. The disk drive control block also monitors the READY status, the INDEX indicator and the TRACK0 indicator from the drives.

The SERIAL DATA/CLOCK SYNCHRONIZATION BLOCK receives the unseparated data, separates the data and clock bits with a phase locked loop, and examines the bit patterns looking for specific patterns which indicate an address mark. Address marks precede address and data fields and are used to synchronize the controller with the drive. The synchronization block then generates data and clock strobes (DATA SR STB and CLK SR STB) which shift the data and clock bits into the shift registers on the Channel Board. The synchronization block also includes a bit counter that determines when a byte (8-bits) has been shifted to/from the selected drive.

The WRITE CLOCK GENERATOR BLOCK provides double density encoding and timing references for the writing of data and clock bits. Data and clock bits are both output to the drive via the WRT DAT/ line. This write clock generator includes timing precompensation circuitry to anticipate bit shifting which occurs upon readback of the double density bit patterns.

The CRC BLOCK generates two CRC characters (16 bits) which are appended to the end of each address field and data field during format and write data operations. During read operations, the CRC block generates two CRC characters for each data field (includes address mark and 128 bytes of data) read, then compares these with the two CRC characters that were appended to the data field, to verify the validity of the data.

The BUS CONTROL BLOCK provides the interface with the Multibus. The bus control block requests and maintains master control of the system bus, and generates the memory read (MRDC/) and memory write (MWTC/) commands that allow the diskette controller to access system memory. In addition, the bus control block acknowledges (XACK/) the I/O read (IORC/) or I/O write (IOWC/) command that is issued when the CPU in the system executes a channel command to the Diskette Controller.

4-11. DISK DRIVE CONTROL. The disk drive control block interfaces with all drive input/output signals except read data, write data and write gate. The main function of this block is to cause the read/write head on the diskette drive to move to the next track (in either direction). The circuitry in this block includes inop reset, track >43, drive selection, drive ready write protect, step, direction, track 0, index and file inop.

The drive READY/ lines (pins J1-30, J1-24, J1-26, and J1-22 are driven by each drive to indicate that a diskette is ready to be accessed in that drive. The disk drive control block receives the READY/ signals (I.C. A30) which are then passed to the Channel Board via the 7400 gates (A45) and the 74367 multiplexing gates at signal lines DR0/ (pin P2-15) and DR1/ (pin P2-17). The GATE LOWER signal (A58-9) is controlled by the microprogram (see Table 4-3) to multiplex the ready signals of either drives 0 and 1 or drives 2 and 3 to these pins. The ready lines for each drive are gated by a flip-flop which retains the "drive not ready" status for that drive (I.C.s A43 and A44). These flip-flops are cleared by the RDY RS/ pulse

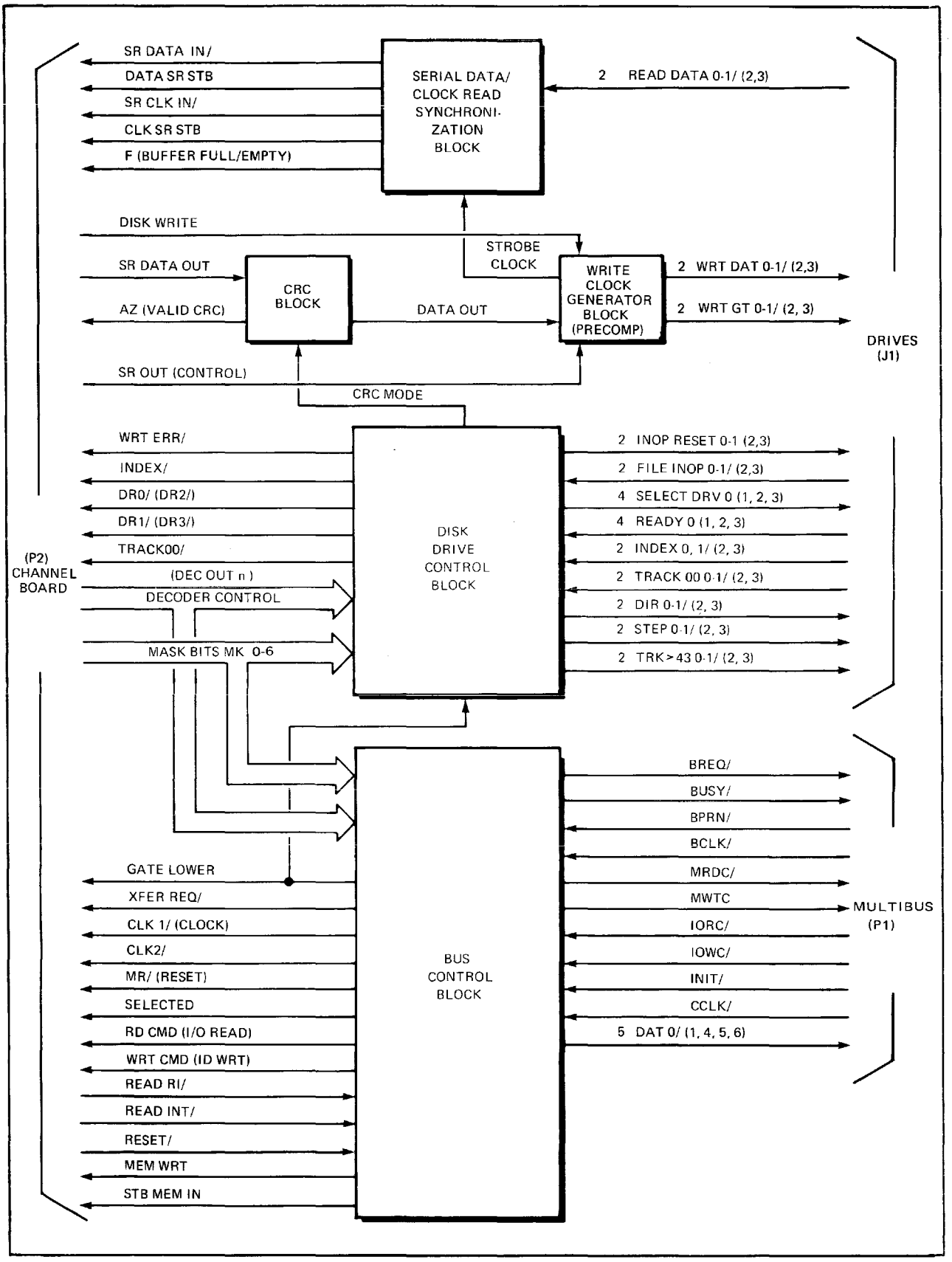


Figure 4-4. Interface Board Functional Block Diagram

(A38-11) which is generated by the microprogram (see Table 4-3). In essence these flip-flops are used to insure that the Channel Board sees a "drive not ready" status whenever a diskette is changed on a non-selected drive. The DAT0/, DAT1/, DAT5/ and DAT6/ MDS Multibus lines are driven at the P1 connector whenever the READ INT/ signal is activated by the Channel Board, indicating the drive ready status to the Channel. The non-gated ready status of the selected drive is multiplexed and passed directly to the Channel Board as the SEL DR NRDY/ signal (pin P2-20) by the 74153 multiplexer (A31) under control of the unit select lines from the Channel Board (USA at Pin P2-9, USB at pin P2-12).

The unit select lines, USA and USB, are decoded by the 74S139 decoder (A56) to generate the drive select signals. The decoder outputs are inverted and driven by 7438 gates (A17) at the DRV SEL lines to the drives (J1-46, J1-48, J1-50, J1-52). The HEAD LOAD/ signal (I.C. A46-4) gates the DRV SEL signals. The decoder outputs are also used as inputs to the drivers for the drive select LED indicators (LED/ lines at J1-54, 66, 64, 68). These lines are also gated by the HEAD LOAD/ signal.

The HEAD LOAD latch is set by the LDHD/ control pulse (A47-3) which is generated by the microprogram being executed on the Channel Board (see Table 4-3). The LOAD latch is cleared by the UNLHD/ pulse (A47-11) which is also generated by the microprogram.

After loading the read/write head on the selected drive, the head must be positioned over the proper track. Any of the seven diskette operations will cause the Diskette Controller to seek the track specified in the I/O Parameter Block (IOPB), prior to actually performing the operation (refer to Chapter 3).

The direction of head movement is defined by the level on the DIR/ lines (pins J1-6, J1-8). The DIREC control level (I.C. A58-11), maintained by the microprogram (see Table 4-3), is applied to the 7438 NAND gates in the disk drive control block. The outputs from these 7438 gates (A11-3, A11-6) drive the DIR/ lines.

Each pulse on the STEP/ lines (pins J1-2, J1-4) will cause the read/write head on the selected unit to move one track either in or out depending on the level on the DIR/ lines. When DIR/ is high, the head will move one track away from the center of the diskette. When DIR/ is low, the head will move one track closer to the center.

The STEP/ pulse is defined by the output of a 9602 one-shot (at A61-10). This one-shot is triggered by the CSTEP control pulse, generated by the microprogram (see Table 4-3), unless the read/write head at the selected unit is already over track 0 (the outermost track) while the DIR/ line indicates outward movement. If the head on the selected unit is loaded, the output from the one-shot will produce a 10 usec. pulse on the STEP/ line, as shown in Figure 4-5.

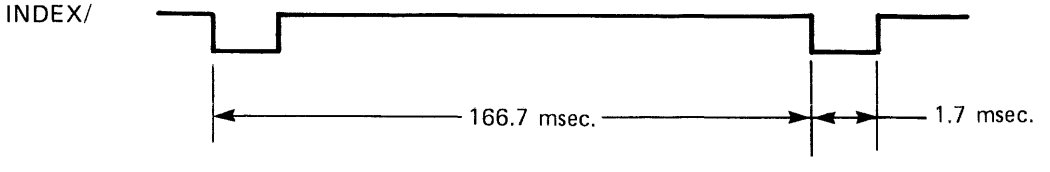
After the head has been positioned over the proper track (by pulsing STEP/ the required number of times), the Diskette Controller must wait at least 20 msec. before it begins examining the read data in an attempt to detect the ID address mark which precedes an address field. Reading the address field will verify that the seek operation placed the head over the proper track. Read initiate timing is illustrated in Figure 4-6.

The disk drive control block also includes a 9602 one-shot (at A61-7) which produces a 10 msec. TIMEOUT pulse, which is made available to the Channel Board (pin P2-38) for use by the microprogram. The microprogram triggers this one-shot by generating the SSCLK control pulse (see Table 4-3). Ten milliseconds after SSCLK triggers the one-shot, a low-to-high transition from the O/ output of the one-shot will appear on the TIMEOUT line.

The disk drive control block drives the INOP RESET/ lines (pins J1-60 and J1-62) and the TRACK > 43/ lines (pin J1-56 and J1-58) to the diskette drives under control of the microprogram. The TRACK > 43 latch (I.C. A46-7) is set by the GTR43/ pulse (A59-3) which is generated by the microprogram (see Table 4-3).

The latch is reset by the NGTR43/ pulse (A59-6). The WFLRS level (I.C. A58-2) is maintained by the microprogram and drives the 7438 gates which in turn drive in INOP RESET/ lines to the drives. INOP RESET/ resets the FILE INOP/ lines driven by the selected drive. TRACK > 43/ forces the selected drive to reduce the write current on inner tracks of the diskette.

The disk drive control block accepts the TRACK0/, INDEX/, FILE INOP/, and WPROT/ lines from the diskette drives and passes them to the Channel Board for use of the microprogram. TRACK0/ (pin J1-38 or J1-44 depending on which drive is selected) is merely inverted twice and output as TRACK00/ at pin P2-11. INDEX/ (pin J1-42 or J1-40) is inverted and clocks a 7474 latch to the set state. The Q output of this latch drives the INDEX line (pin P2-42) to the Channel Board. The microprogram can reset the INDEX latch by generating the RNDX/ control pulse (see Table 4-3). An INDEX pulse will be received once every 166.7 msec. and will be approximately 1.7 msec. wide:



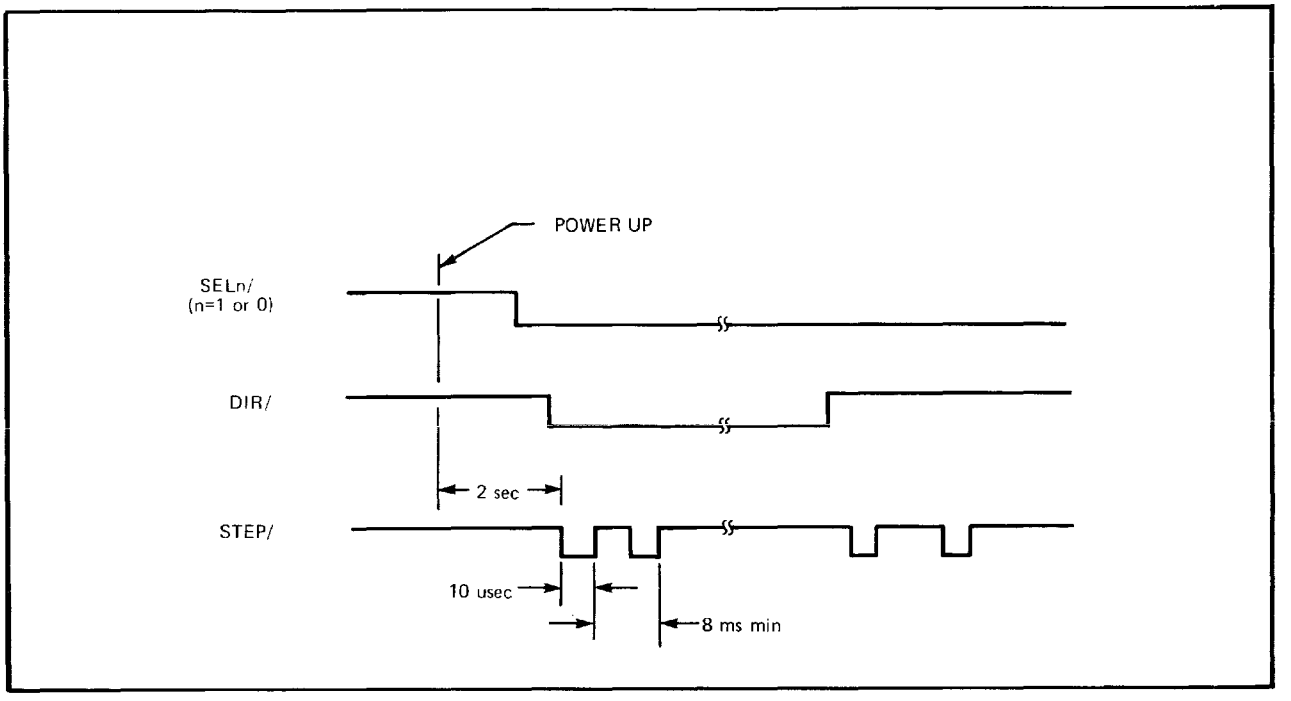


Figure 4-5. Head Movement Control Timing

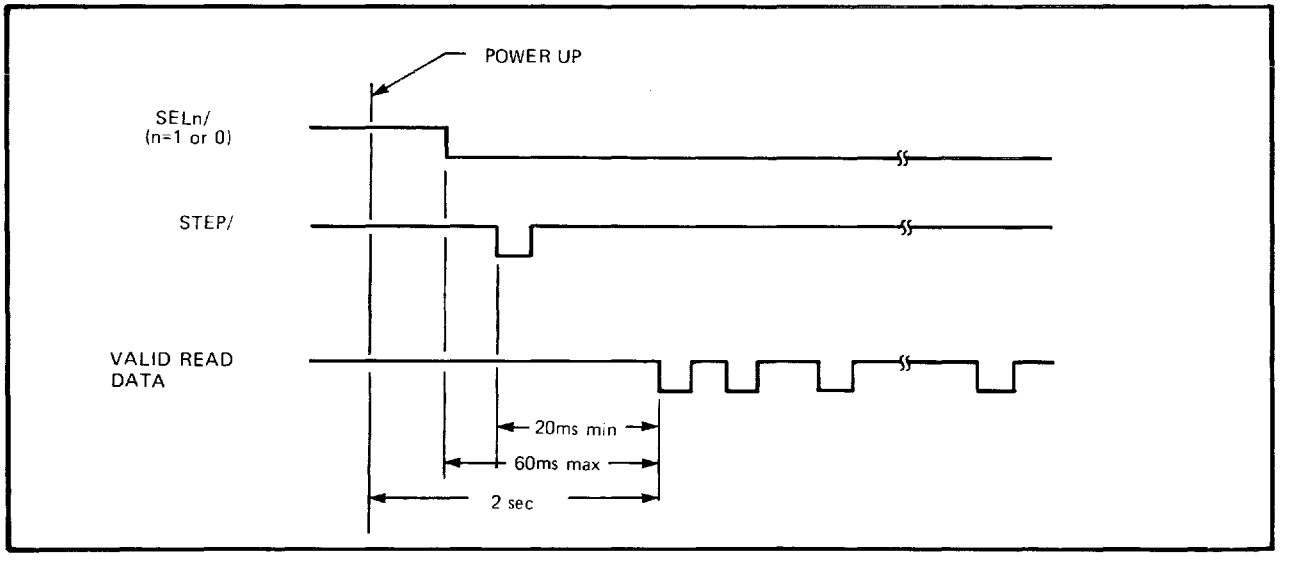


Figure 4-6. Read Initiate Timing

FILE INOP/ (pin J1-32 or J1-34) is inverted twice and passed to the channel board as the WRT ERR/ signal at pin P2-18. WPROT/ lines (pin J1-20 or J1-18) are multiplexed by the 74153 multiplexer (I.C. A31) and passed on to the channel board at pin P2-14 to indicate the presence of a write protected diskette in the selected drive.

4-12. WRITE DATA GENERATOR. The write data generator block develops the pulse stream which is driven to the drives as the WRT DAT/ lines (J1-10 and J1-12). For each negative pulse on the WRT DAT/ line, the selected drive will change the direction of write current in the magnetic head, resulting in a flux reversal on the diskette media. The selected drive supplies write current to the media (that is, "writes") only if the WRT GT/ signal is activated. The microprogram controls the WRT GT/ lines (pins J1-14 and J1-16) by the DISK WRITE signal which is sent to the Interface Board at P2-55.

The write data is double-density encoded using the Modified-Modified Frequency Modulation (M^2FM) algorithm. Figure 4-7 illustrates the double density encoding and provides a comparison with single-density (FM) encoding to show that the bit cell time can be halved from 4 us to 2 us since the minimum time between pulses is 2 us. in both cases. Note that clock bits are only written to aid read-back synchronization and data recovery.

Since the bit cell is halved with double-density encoding, data recovery is more susceptible to errors associated with magnetic bit shift. To minimize the effects of read-back bit shift, the write data block includes precompensation circuitry. This circuitry anticipates magnetic shifts by writing bits earlier or later than nominal bit times in an opposite direction to the magnetic shifts that will occur upon readback. For example, the third data bit from the left (M^2FM) in Figure 4-7 will tend to shift upon readback towards the "0" bit cell (to the right). This shift is "precompensated" by writing the bit closer to the preceding data bit (more to the left).

The precompensation and encoding circuitry are shown on sheet 2 and 3 of the schematic. The write oscillator, Y1, outputs an 8 MHz clock signal which drives a 74164 (A8-8) 8-bit shift register which has been connected as a bit-ring. The outputs of the bit ring are connected to "AND" gates (7402, 7411 and 7408) which generate active high pulses relating to the specific clock bit times and data bit times which, in turn, are selected as WRT DAT/ pulses by the 74150 multiplexer (A34).

Figure 4-8 illustrates the timing of the precompensation circuitry which generates the pulses used by the encoding circuitry. Note that there are two possible times to write a clock bit: on-time (C), or 125 ns. early (CE). There are three possible times to write a data bit: on-time (D), 250 ns. early (DE) or 250 ns. late (DL).

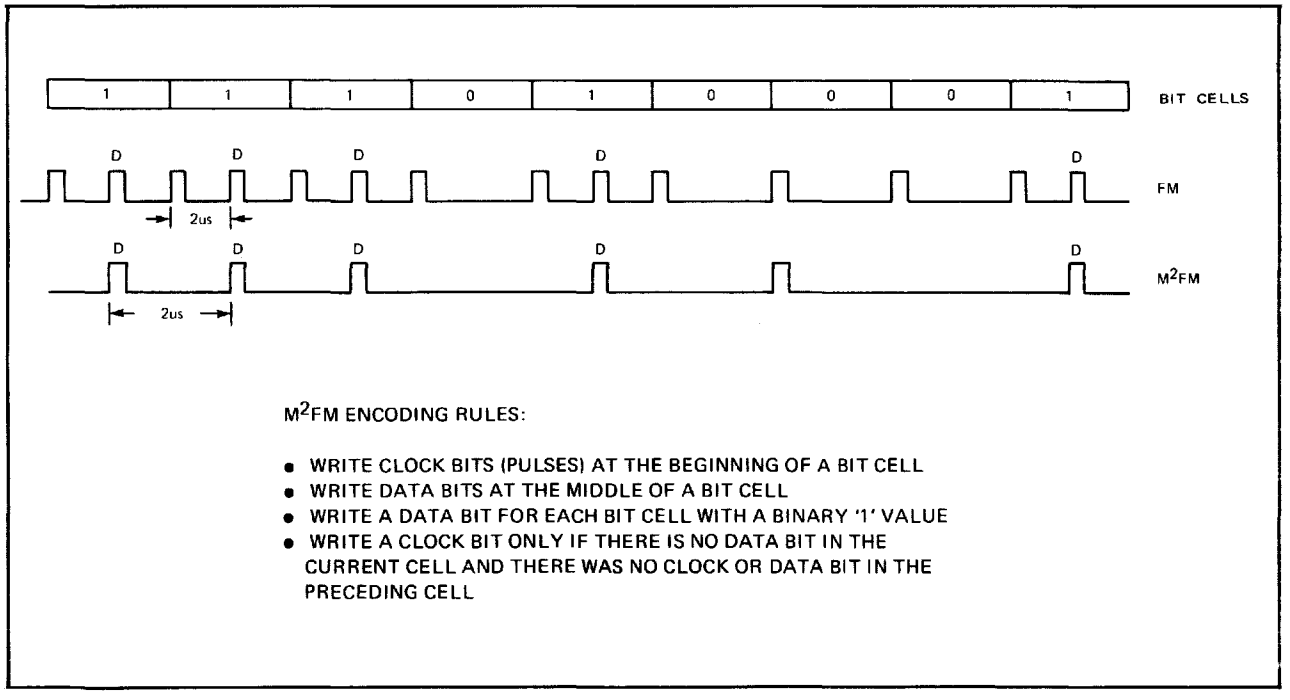


Figure 4-7. M^2FM Data Encoding

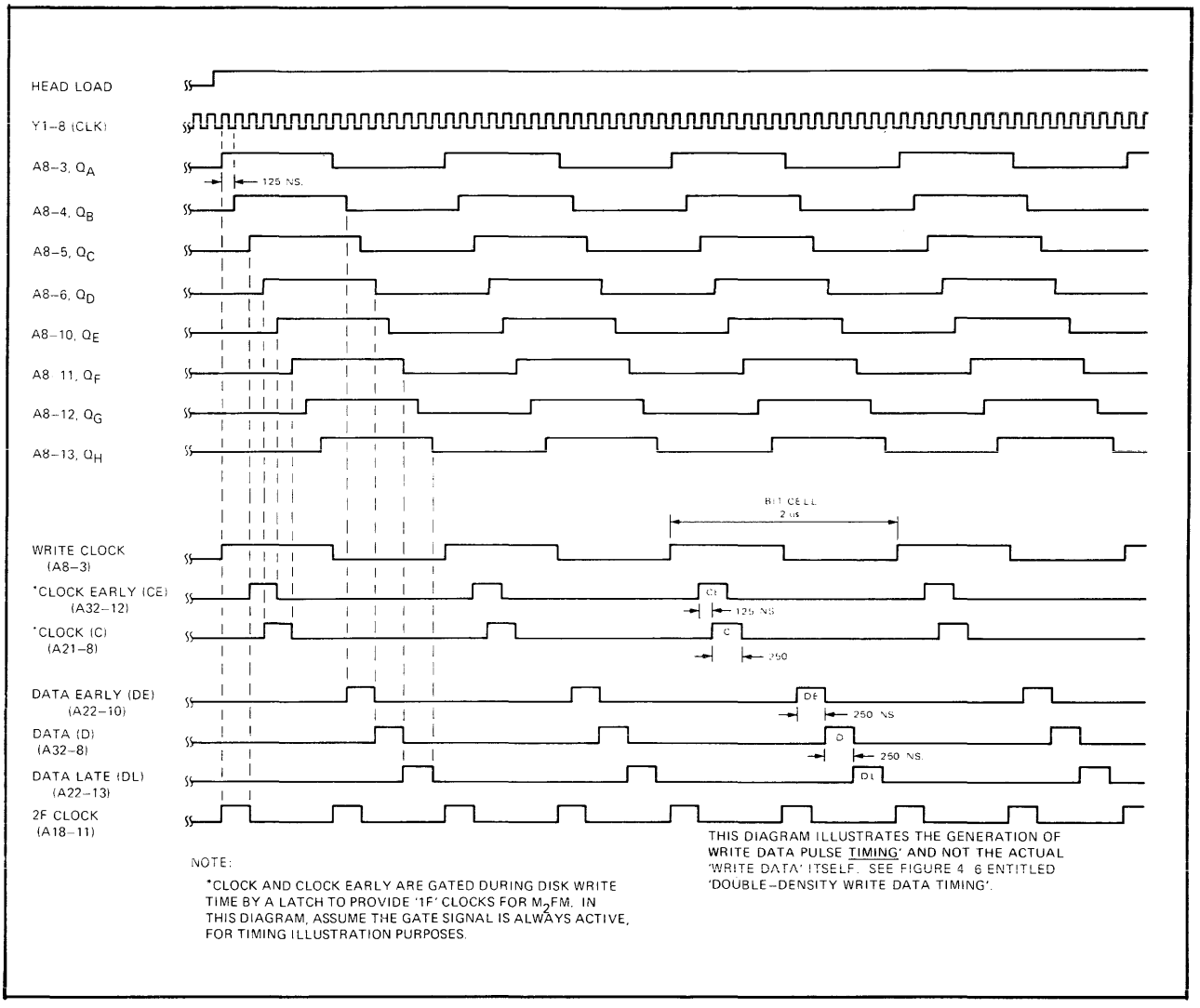


Figure 4-8. Precompensation Timing

The WRITE CLOCK signal (A8-3) is used to shift the serial data in the precomp selection and encoding shift register (A48). In addition, the WRITE CLOCK signal is multiplexed with the read clock by the DISK WRITE signal to generate the CLOCK SR STB and DATA SR STB signals (P2-8 and P2-48). These signals are used by the Channel Board to shift the data byte being written or read by the drive.

The encoding and precompensation selection for the write data is performed by the data shift register (A48) and the 74150 multiplexer (A34). The outputs of the register (SDA, SDB, SDC, SDD) drive the select inputs of the 74150 multiplexer. Depending upon the data pattern presented at the select inputs, the 74150 selects one of the five timing pulses during each bit cell (i.e., C, CE, D, DE or DL). For a "zero-data" bit cell which was preceded by a bit cell which generated a pulse, no pulse is selected. The pair of flip-flops (A10 on sheet 3) which are clocked by WRITE CLOCK generate the CLOCK GATE signal (A10-8). This signal gates the C and CE pulses so that only every other clock bit is written in a string of "zero" bit cells. Figure 4-9 illustrates the signal timing of the circuitry which generates WRT DAT/ pulses.

The AMWRT/ latch (A58-6) is controlled by the microprogram on the Channel Board and is used to set the CLOCK GATE active during the writing of an address mark, resulting in a unique clock pattern (three clock bits in sequential bit cells) which aids in read-back synchronization. In addition, the AMWRT/ level controls the 74157 multiplexer (A7-5) by selecting the appropriate precompensation times during an address mark. Note that all of the switches shown on sheet 2 and 3 of the schematic are only manufacturing options for an alternate type of data encoding and are not field selectable.

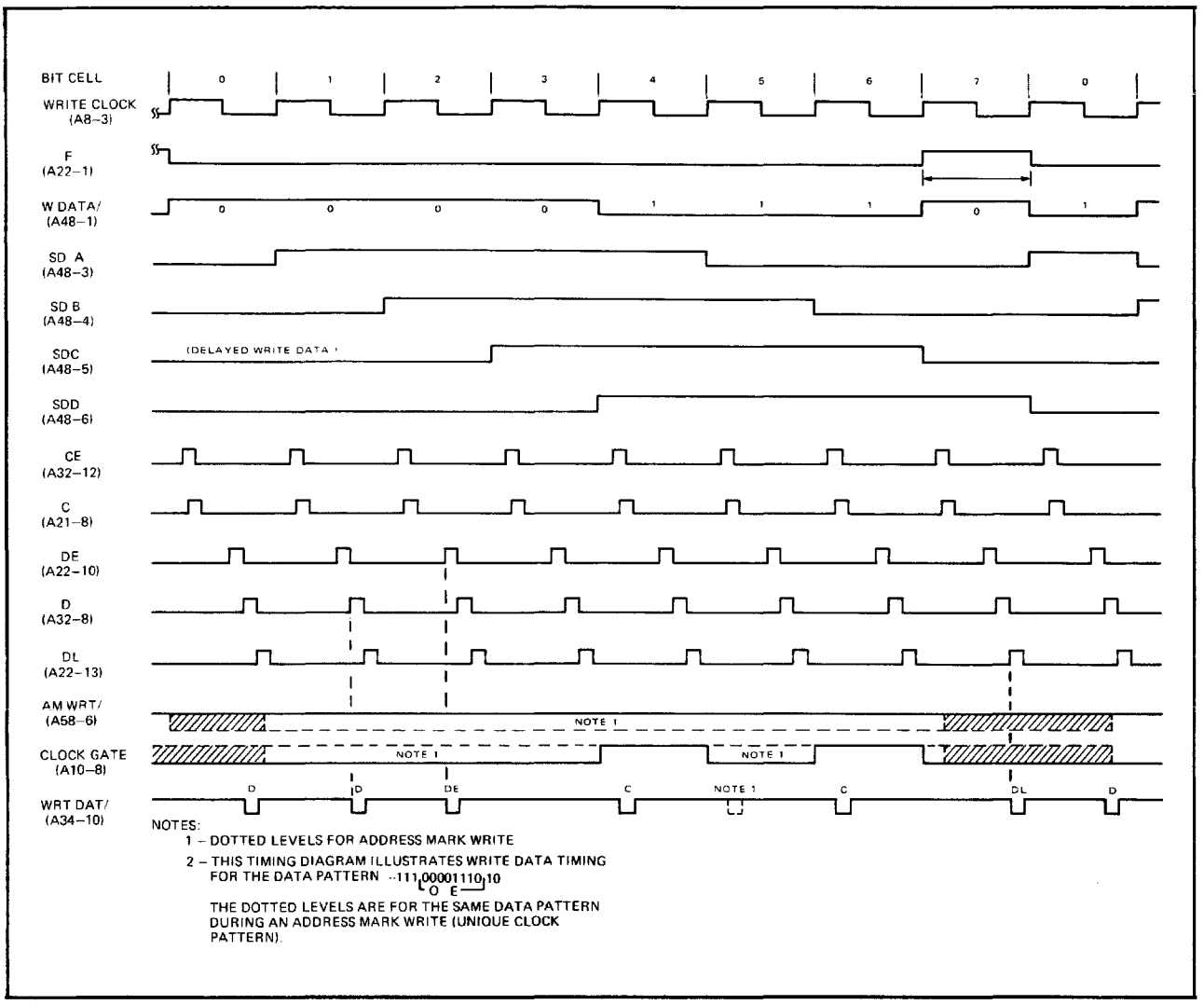


Figure 4-9. Write Data Timing

4-13. SERIAL DATA/CLOCK SYNCHRONIZATION.

The serial data/clock synchronization block contains circuitry which separates the serial READ DATA pulses from the drive into data and clock bits for serial transfer to the Channel Board. The circuitry can be subdivided into the following segments: phase locked oscillator (PLO), PLO start-up logic and byte-synchronization counter (A19).

The PLO consists of linear circuitry which "locks" onto the recorded information and generates separate "windows" for data bits and clock bits. Staying in synchronization with small, slow variations in disk speed, it averages quick variations caused by bit shift. Figure 4-10 provides a block diagram of the PLO with startup logic and data separator.

When not reading, the RESET READ/ level (A46-9), maintained by the microprogram on the Channel Board, is active (low) and the PLO is locked to the write oscillator. The 2F CLOCK signal is multiplexed to fire the SAMPLE one-shot (A37-5) which provides the input pulse train feeding the PLO. When the microprogram initiates a read operation by inactivating the RESET READ/ signal, the PLO startup logic is activated. The startup logic monitors the drives' READ DATA/ signals (pins J1-36 and J1-28) until the all 1's area in an address mark preamble is detected. Then the PLO input pulse stream is switched from the write oscillator to read data. As soon as the PLO is locked to the read data, the startup logic starts waiting for the first bit of the address mark, that is, the first "0" bit cell. When this bit cell is detected, the ENABLE BR signal (A15-5) is activated, enabling the 74195 bit ring to start counting the bits. On every eighth bit cell count, the "F" signal (pin P2-58) is activated to notify the Channel Board that a valid data byte has been read. When the Channel Board receives the first "F" signal, it compares the data and clock bytes with the known address mark patterns. If there is a match, the Channel Board continues to accept data bytes and the PLO stays locked to the read data. If there is not a match, the Channel Board resets the read circuitry by activating the RESET READ/ level and later enabling the read circuitry to continue searching for the desired address mark. Figure 4-11 illustrates the detailed timing for the serial data/clock synchronization block during the address mark synchronization process.

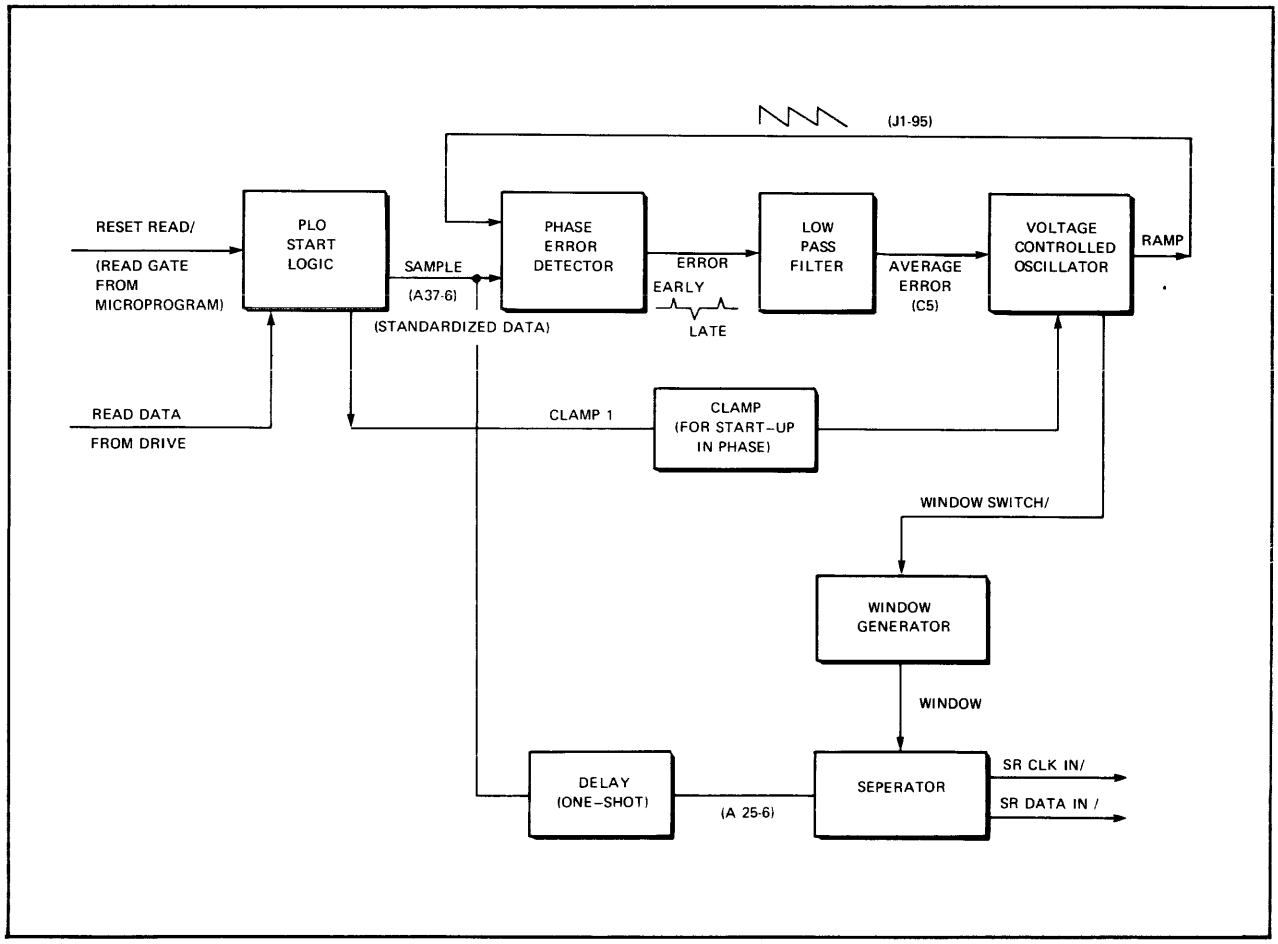


Figure 4-10. Phase Locked Oscillator

4-14. CYCLIC REDUNDANCY CHECK (CRC). Two cyclic redundancy check (CRC) characters (16-bits) are generated for each data field (i.e., the address mark and 128 bytes of data) and are then appended to the data field as it is written to diskette. During all read operations, 16 CRC bits are generated as data is read; these CRC bits are then compared with the CRC bits that were appended to the field when it was written. CRC generation and checking are performed by the CRC block which consists of a 9401 Universal Polynomial Generator (UPG), a 7451 multiplexer, a control latch, and several inverting circuits.

During write operations, data bits from the data shift register (on the Channel Board) are input to the 9401 UPG device (pin 11, D), as well as the 7451 multiplexer via the SR DATA OUT line. The SR OUT control level (maintained by the microprogram on the Channel Board — see Table 4-3) allows the data bits through the multiplexer and onto the WRT DAT/ line. The data bits, which are also being input to the 9401 device, cause the 9401 to generate the CRC characters (16 bits) for the 128 data bytes by "dividing" the data by the encoding polynomial ($x^{16} + x^{12} + x^5 + 1$). When the entire 129 bytes (1 address mark byte and 128 data bytes) have been written to disk, the microprogram lowers the SR OUT level, which allows the 16 CRC bits being output by the 9401 device (pin 12, SDO) to pass through the 7451 multiplexer and be written onto the diskette immediately after the data.

During read operations, each data byte is shifted into the 9401 UPG device as the succeeding data byte is being shifted into the data shift register (on the Channel Board). The data bits are carried on the SR DATA OUT line, just as during a write operation. The absence of the SR OUT control level (from the microprogram), however, prevents the data bits from being gated out onto the WRT DAT/ line. The 129 bytes are "divided" by the encoding polynomial to generate 16 CRC bits. After all 129 bytes have been read, the 16 CRC bits which were appended to the data when it was written are also shifted into the 9401 device where they are compared with the CRC bits just generated. If the two sets of CRC bits match, the all zeroes output (ER, pin 13) goes true (low), and is applied to the D-input on a 7474 latch at A60-12. When the bit counter in address mark detection logic determines that all data has been shifted out of the data register (i.e., when the F signal goes true), the low level from the ER output is clocked into the 7474 latch. The high O/ output from this latch drives the AZ line (pin P2-41) to the Channel Board.

The microprogram controls the various operating modes of the 9401 UPG by maintaining the appropriate levels on the CRCMD control line (see Table 4-3). CRCMD, which feeds the shift right (CWE) input to the UPG, is usually low, causing logical zeroes to be shifted through the UPG. It is only when CRC characters are being generated or checked that CRCMD presents a false (high) level to the active-low CWE input. The 9401 device is clocked by the data shift register strobe signal.

4-15. BUS CONTROL. The bus control block maintains the Diskette Controller interface with the Multibus. This block consists of a 52-104 Bus Control I.C., six flip-flops, a 9602 one-shot multivibrator and assorted gating and inverting circuits.

Before the diskette controller can transfer data to or from system memory, the bus control block must request and be granted master control of the system bus. When the Diskette Channel requires access to memory, the microprogram (being executed on the Channel Board) will initiate the bus request sequence by generating the SMREQ/ control pulse (see Table 4-3). SMREQ/ will cause the 74LS112 latch at A51-4 to be pre-set unless the inhibit memory write latch (A46-13) is set.

The inhibit memory write latch will be set during VERIFY CRC diskette operations, in which data is read and verified but is not transferred to memory. The inhibit memory write latch is set and reset by the SINH/ and RINH/ control pulses, respectively (both are generated by the microprogram, see Table 4-3).

The Q output from the 7474 latch which is pre-set by SMREQ/ (A51-5) is applied to the transfer request inputs of the 52-104 Bus Control I.C. (A50-25, 3, 4). The next bus clock pulse (BCLK/ at P1-13) will clock this input into the 52-104. The low Q/ output drives the XFER REQ/ line (pin P2-39) which informs the Channel Board that the memory transfer is not yet complete. The Q output from the transfer request latch feeds the J-input of the data overrun (DOR/) latch.

If the microprogram requests a memory access again (i.e., if SMREQ is generated again) before the current access is completed, the data overrun latch will be clocked to the set state, and its Q output will drive a true (low) level on the DOR/ error line to the Channel Board (pin P2-16).

When the 52-104 Bus Control I.C. receives the XFER REQ input, it initiates a memory transfer bus cycle, causing BREQ/ (pin P1-18) to go true (low). BREQ/ requests use of the Multibus.

If no other master module is using the bus (i.e., if BUSY/ is false), and if no higher priority module is requesting the bus (i.e., the bus priority in line, BPRN/, is true), the next bus clock pulse (BCLK/) after BREQ/ will cause the 52-104 to activate BUSY/ (pin P1-17). BUSY/ informs the system that the Diskette Controller has master control of the bus. In addition the 52-104 activates the ADEN/ output which is inverted to generate the SELECTED signal (pin P2-43). On the next BCLK/ pulse after BUSY/ goes true, the 52-104 will drive the memory read (MRDC/) or memory write (MWTC/) command at pins P1-19 and P1-20, respectively, depending upon whether a read or write cycle was requested by the microprogram controlled MEMWRT level (A58-4).

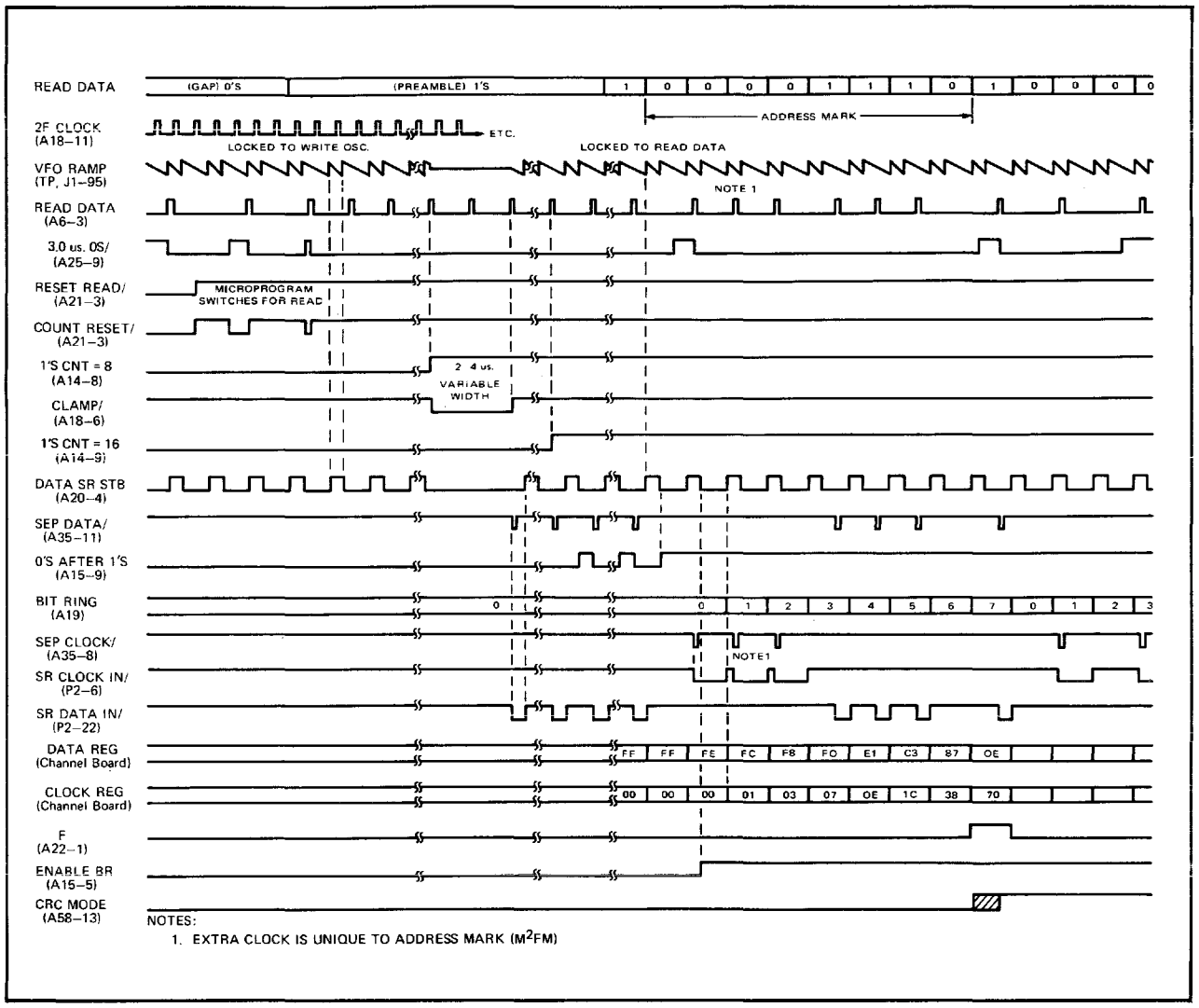


Figure 4-11. Read Synchronization Timing

Recall that while logic on the Interface Board requests control of the bus, then generates the memory read or write command, it is the Channel Board which actually drives the system data and address buses as gated by the SELECTED signal.

When the memory has accepted the data to be written or output the data which was read, it generates a transfer acknowledge signal (XACK/) which is received at pin P1-23 on the Interface Board. XACK/ triggers a 9602 one-shot (A37-11). The high pulse (~70 nsec. wide) at the Q output of the one-shot drives the STB MEM IN line (pin P2-29) which allows the Channel Board to accept data read from memory.

The Q/ output from the one-shot clocks the XFER REQ 7474 latch at A51-1 to the reset state. As a result, succeeding bus clock pulses (BCLK/) can reset the bus control logic, and cause the Interface Board to relinquish master bus control to another module.

Bus control timing is illustrated in Figure 4-12.

In addition to being the master module during memory access operations, the Diskette Controller also acts as the "slave" module during I/O operations in which the CPU executes a channel command for the Diskette Controller. The bus control block accepts the I/O read (IORC/) or I/O write (IOWC/) command from the CPU (at pins P1-21, P1-22), inverts it and passes it to the Channel Board on the READ CMD line (pin P2-60) or the WRT CMD line (pin P2-53).

The "slave" module must acknowledge all commands from the master. The bus control block performs this function in response to channel commands. Receipt of a "reset", "read subsystem status" or "read result type" channel command (see Chapter 3) will clock the acknowledge latch (at A39-3) to the set state. The acknowledge latch is set at the proper time by the SACK/ control pulse (A57-11) from the microprogram for each of the other channel commands. The Q output from the acknowledge latch feeds a 74125 tri-state driver. The output from the 74125 circuit (XACK/) is driven through pin P1-23. XACK/ is reset when IORC/ or IOWC/ go false via the 7432 gate (A38-8).

The bus control block also has an 8 position rotary switch which connects the interrupt line (INT/) from the Channel Board (pin P2-40) with one of the eight system priority interrupt request lines, INT0/-INT7/ (via a 74125 tri-state gate which provides the required electrical characteristics for the Multibus).

In addition, the two phase clock pulses (CLK1/ and CLK2/) are generated in the bus control block. CLK1/ and CLK2/ are derived from the system common clock, CCLK/ (9.8 MHz). CCLK/ is divided by the two 74LS74 flip-flops at A54 to produce CLK1/ and CLK2/ (400 nsec. period, 12% duty cycle) at the outputs of the 74S139 decoder as shown in Figure 4-13.

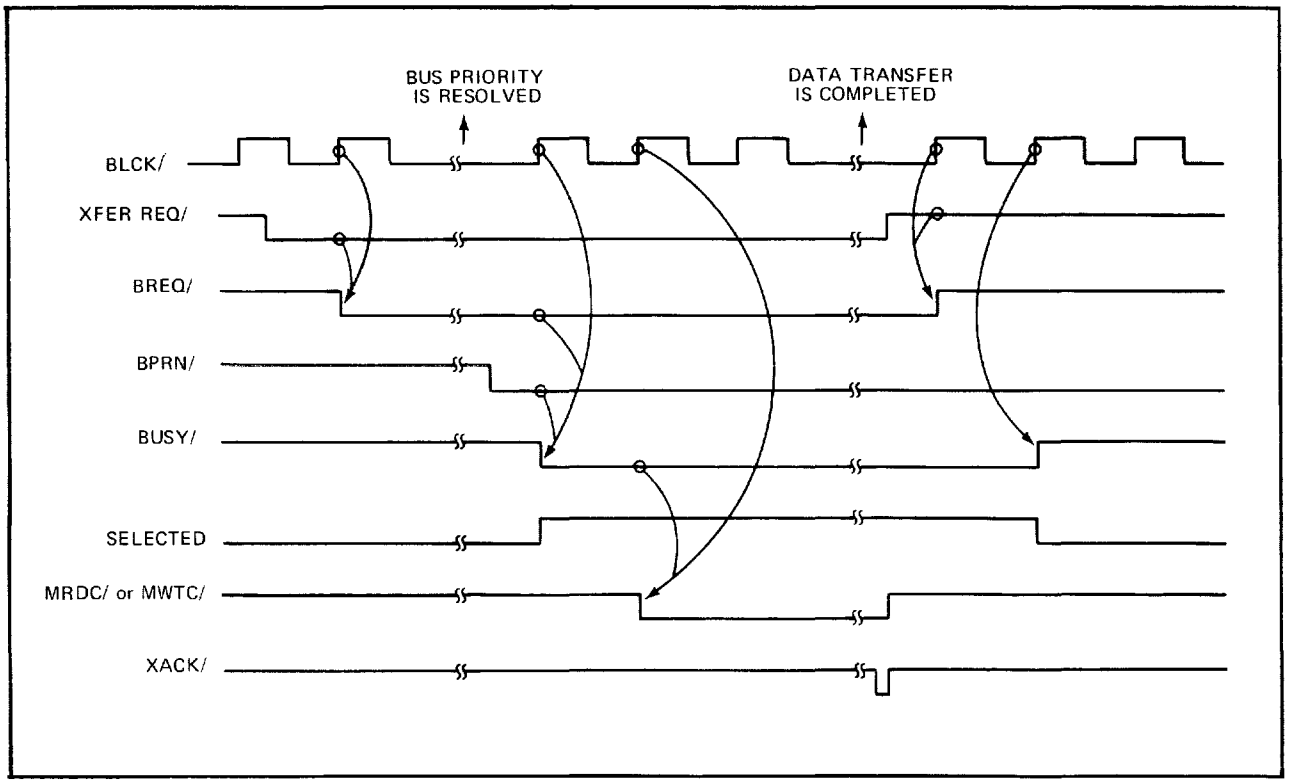


Figure 4-12. Bus Control Timing

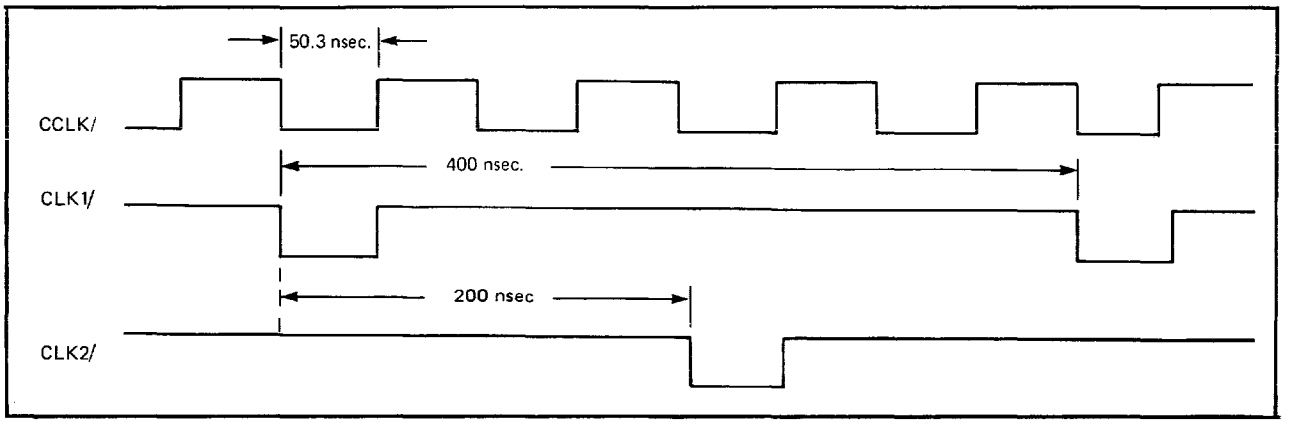


Figure 4-13. CLK1/ and CLK2/ Timing

4-16. RECORDING FORMAT

The following paragraphs summarize the specifications for the soft-sectored recording format the controller is designed to interact with.

4-17. PHYSICAL DATA FORMAT

The physical data format is the format that the Diskette Controller circuitry must interact with. The elements of the physical data format are the hard index hole, index mark, sector address marks, sector headers, and data sectors. The index mark and sector address marks are recorded with unique clock patterns requiring the controller circuitry to accumulate the unique clock patterns for index and sector address mark identification. Figure 4-14 illustrates the general physical data format.

A "byte", when referring to serial data (being written to or read from the diskette drive), is defined as eight (8) consecutive bit cells. The most significant bit cell is defined as bit cell 0 and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation bit cell 0 of each byte is transferred to the drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the diskette first and the least significant byte is transferred last.

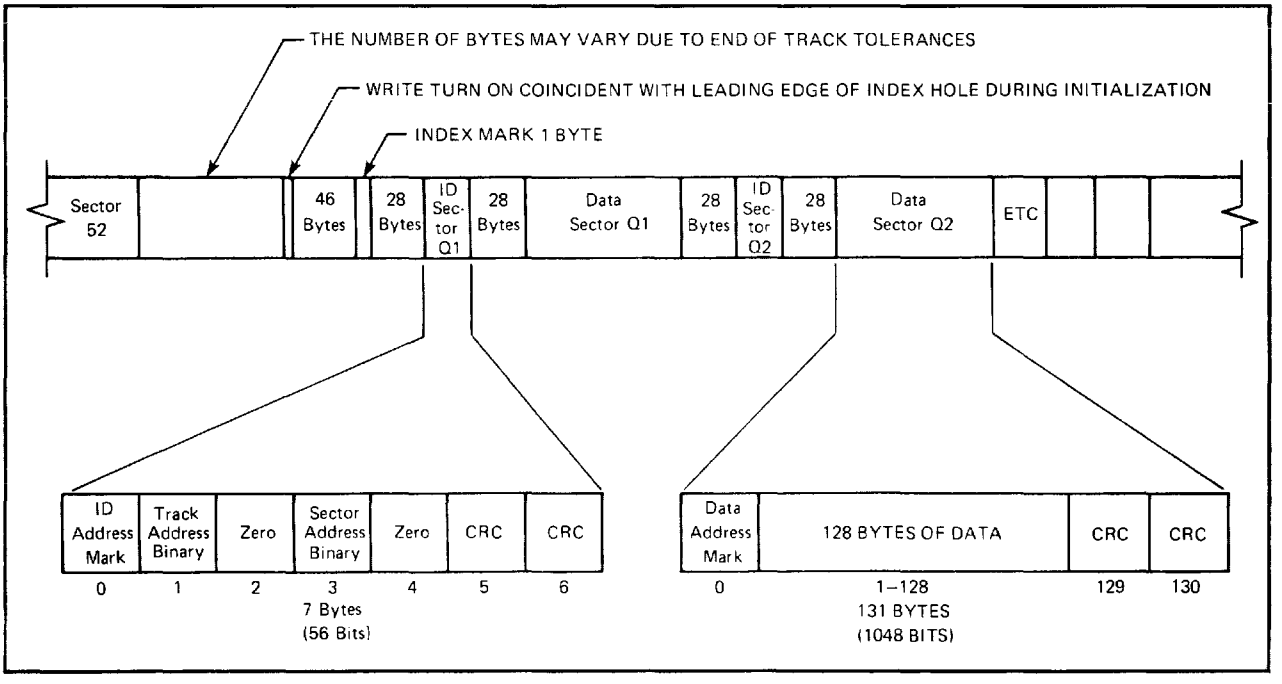


Figure 4-14. Physical Data Format

When data is being read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with reading, the most significant byte will be transferred first from the drive to the user.

Figure 4-15 illustrates the relationship of the bits within a byte and Figure 4-16 illustrates the relationship of the bytes for read and write data.

Data is recorded on the diskette using modified modified (M^2) frequency modulation as the recording mode. Data written on and read back from the disc takes the form shown in Figure 4-17. Clock bits are written only if there is no data bit in the bit cell and there was no data bit or clock bit written in the previous bit cell. By definition, a Bit Cell is the period (2 us) consisting of a clock bit time (1 us) and a data bit time (1 us). Figure 4-18 illustrates a Bit Cell.

4-18. TRACK FORMAT

Each track recorded on a diskette consists of 52 fixed length records along with necessary gaps for record updating. Figure 1-19 illustrates the format of one complete track.

Each field on a track is separated from adjacent fields by a number of bytes containing no data. These areas are referred to as gaps and are provided to allow the updating of one field without affecting adjacent fields. As can be seen from Figure 1-19, there are four different types of gaps on each track:

Gap 1 — Post-Index Gap

This gap is defined as the 28 bytes between Index Address Mark and the ID Address Mark for Sector one (excluding the address mark bytes). This gap is always 28 bytes in length and is not affected by any updating process.

Gap 2 — ID Gap

The 28 bytes between the ID Field and the Data Field are defined as Gap 2 (ID Gap). This gap does not vary in size.

Gap 3 — Data Gap

The 28 bytes between the Data field and the next ID field are defined as Gap 3 (Data Gap). The Data Gap may vary slightly in length after the adjacent Data field has been updated, due to differences in disk rotational speed between formatting and updating of individual data fields.

Gap 4 — Pre-Index Gap

The 338 bytes between the last Data field on a track and the Index Address Mark are defined as Gap 4 (Pre-Index Gap). Initially, this gap is nominally 338 bytes in length; however, due to write frequency tolerances and diskette speed tolerances this gap may vary slightly in length. Also, after the data field of record 52 has been updated this gap may again change slightly in length.

4-19. ADDRESS MARKS

Address Marks are unique bit patterns one byte in length which are used to identify the beginning of ID and Data fields and to synchronize the deserializing circuitry with the first byte of each field. Address Mark bytes are unique from all other data bytes in that each Address Mark contains an extra clock bit in bit cell 2. There are four different types of Address Marks used. Each of these is used to identify different types of fields:

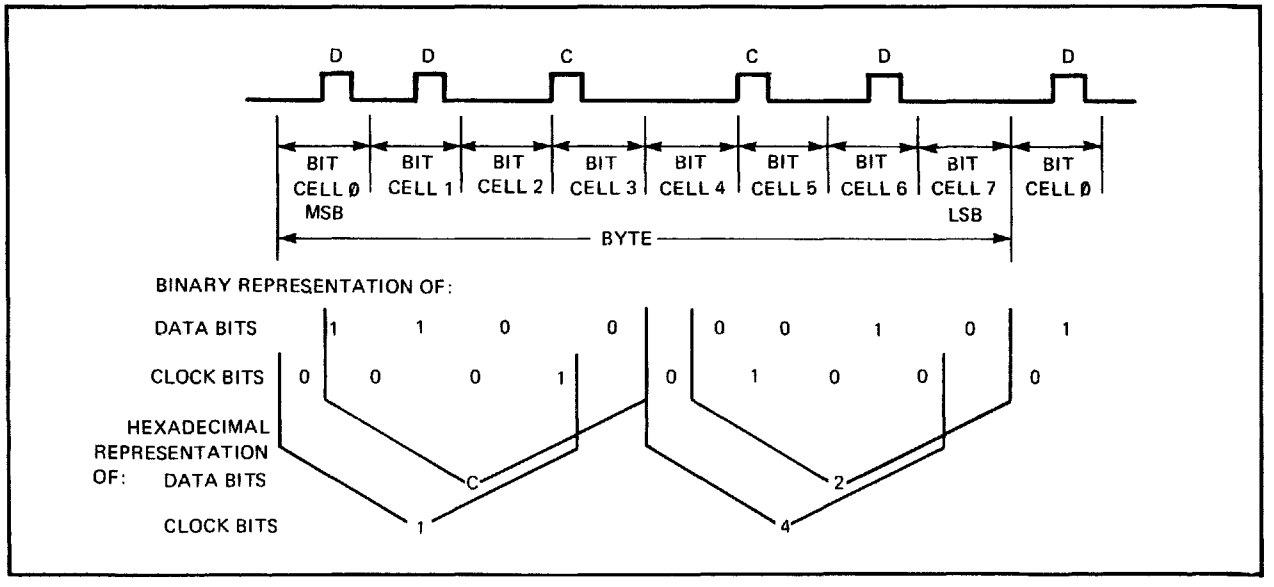


Figure 4-15. Byte Representation

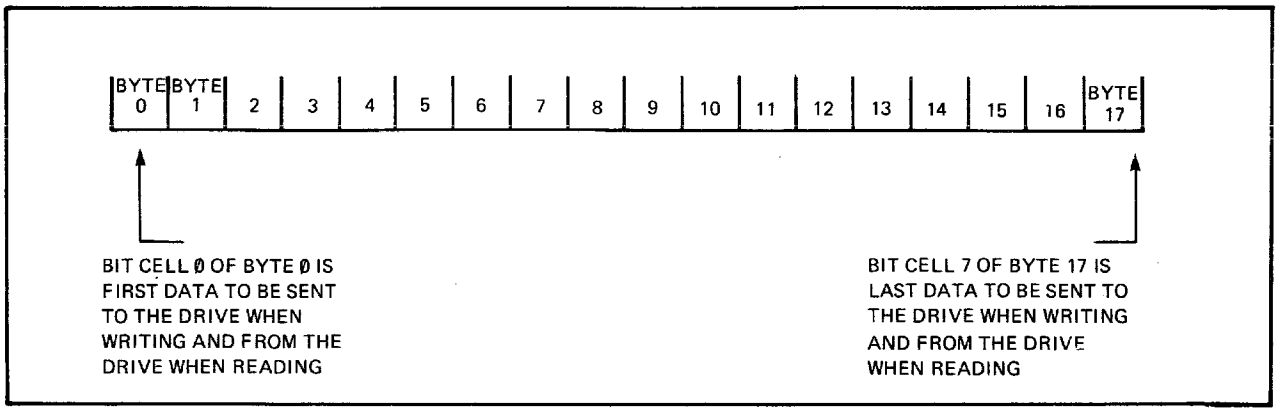


Figure 4-16. Data Bytes

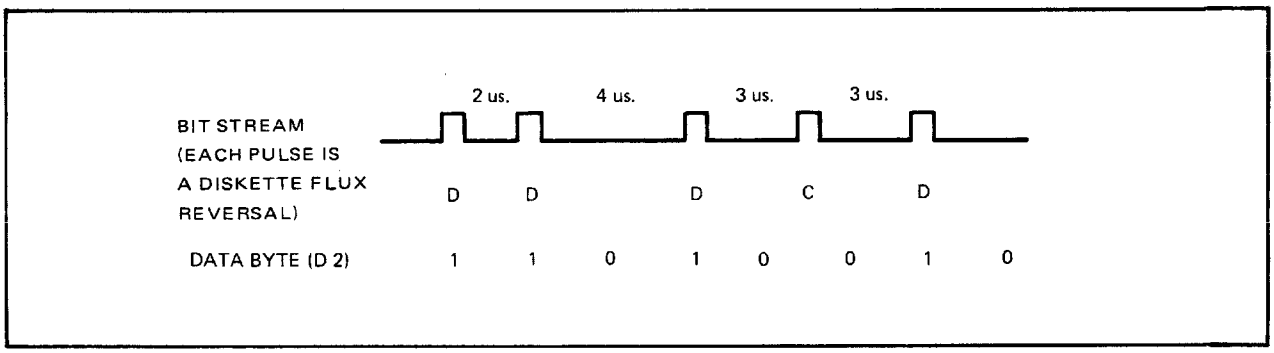


Figure 4-17. Data Bit

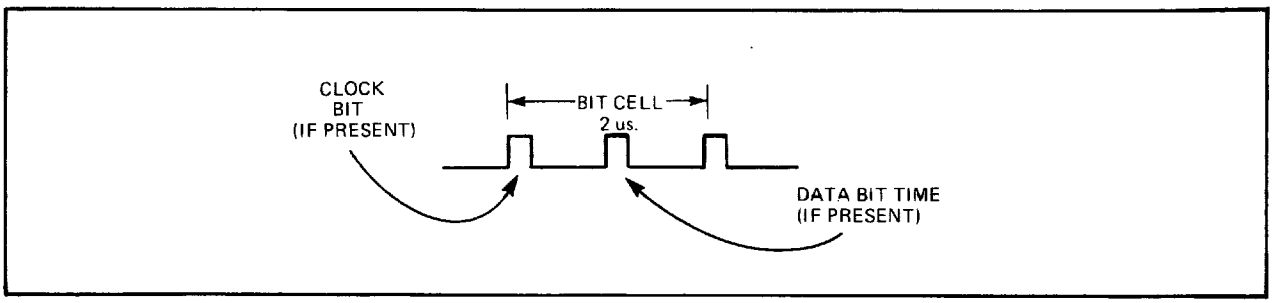


Figure 4-18. Bit Cell

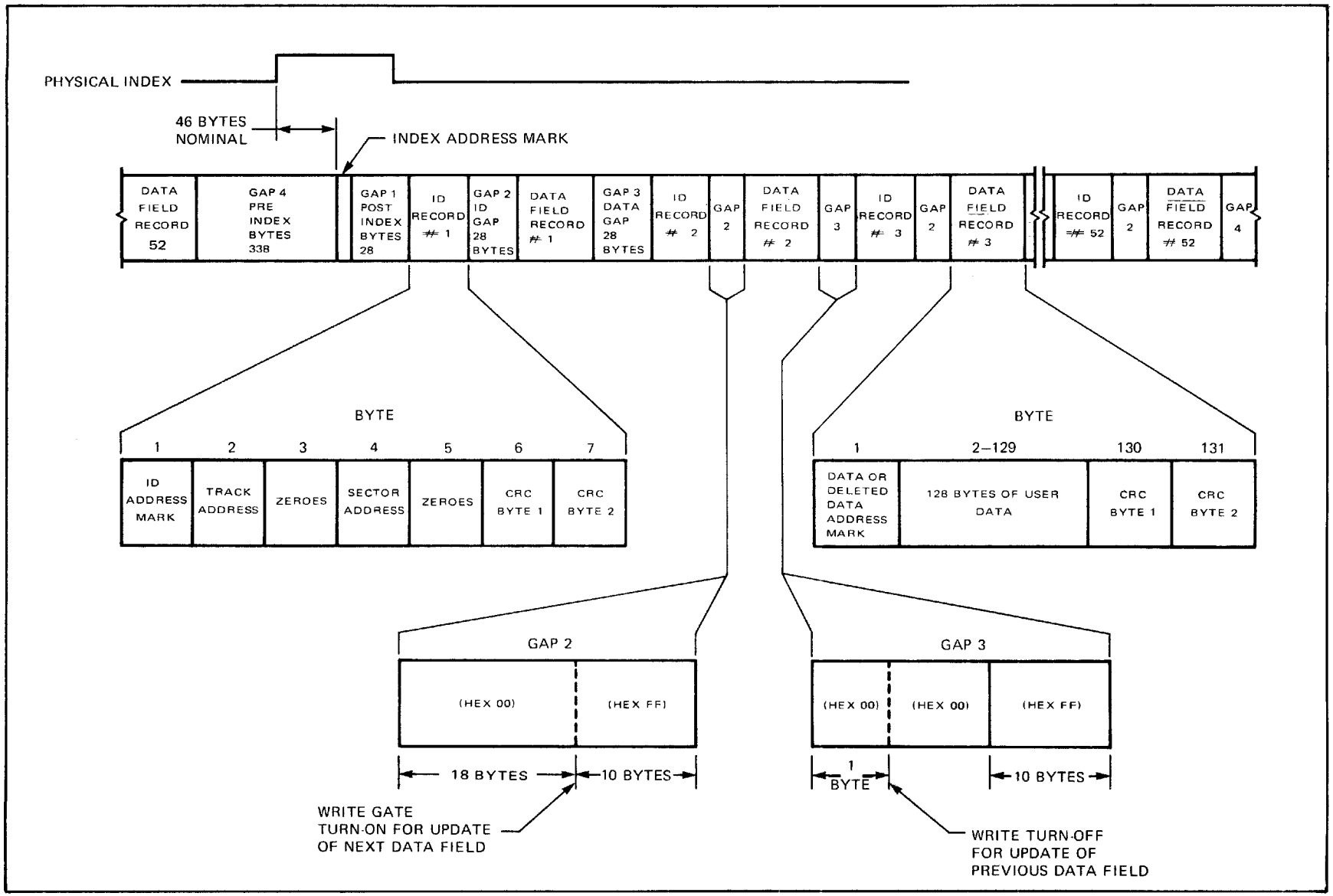


Figure 4-19. Track Format

Index Address Mark

The Index Address Mark is located at the beginning of each track and is a fixed number of bytes in front of the first record. The bit configuration for the Index Address Mark is shown in Figure 4-20.

ID Address Mark

The ID Address Mark byte is located at the beginning of each ID field on the diskette. The bit configuration for this Address Mark is shown in Figure 4-21.

Data Address Mark

The Data Address Mark byte is located at the beginning of each non-deleted Data Field on the diskette. The bit configuration for this Address Mark is shown in Figure 4-22.

Deleted Data Address Mark

The Deleted Data Address Mark byte is located at the beginning of each deleted Data field on the diskette. The bit configuration for this Address Mark is shown in Figure 4-23.

4-20. CRC BYTES

Each field written on the diskette is appended with two Cyclic Redundancy Check (CRC) bytes. These two CRC bytes are generated from a cyclic permutation of the data bits starting with bit zero of the address mark and ending with bit seven of the last byte within a field (excluding the CRC bytes). This cyclic permutation is the remainder from the division of the data bits in the field (represented as an algebraic polynomial) by a generator polynomial G(X). For all fields recorded on a diskette, this generator polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

When a field is read back from a diskette, the data bits (from bit zero of the address mark to bit seven of the second CRC byte) are divided by the same generator polynomial G(X) and a non-zero remainder indicates an error within the data read back from the drive while a remainder of zero indicates the data has been read back correctly from the diskette or an undetectable error has been read back.

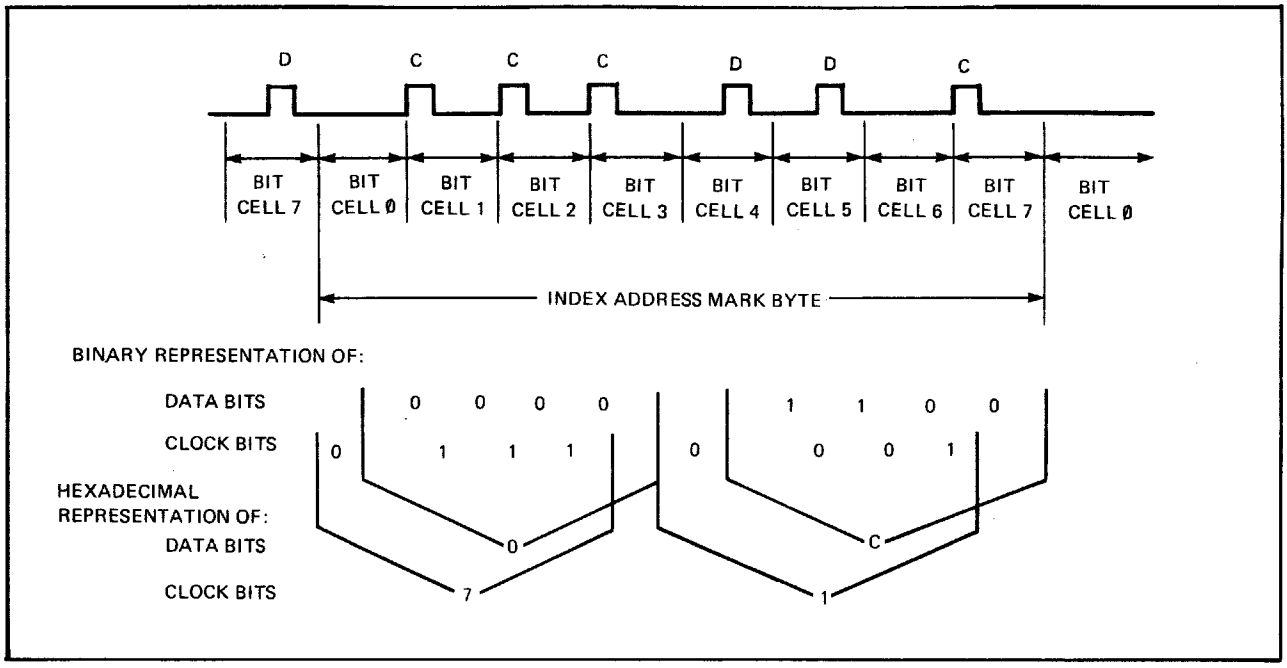


Figure 4-20. Index Address Mark

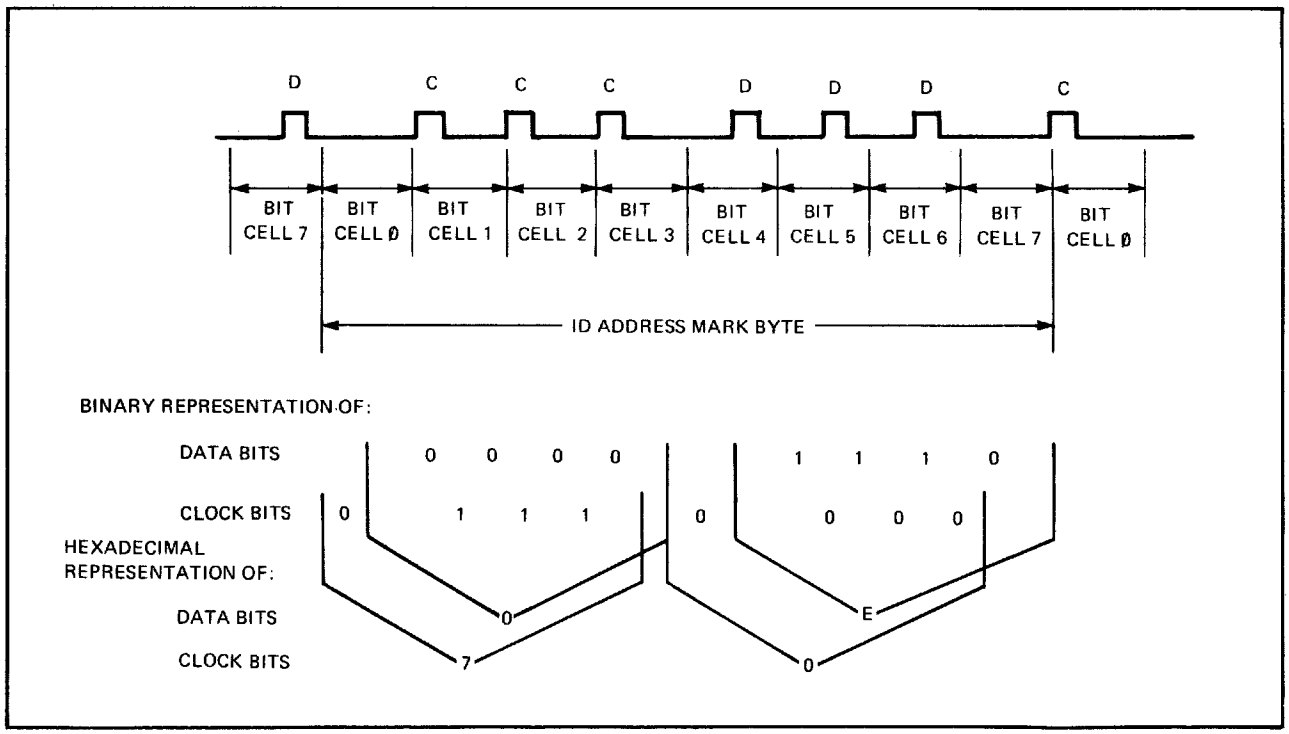


Figure 4-21. ID Address Mark

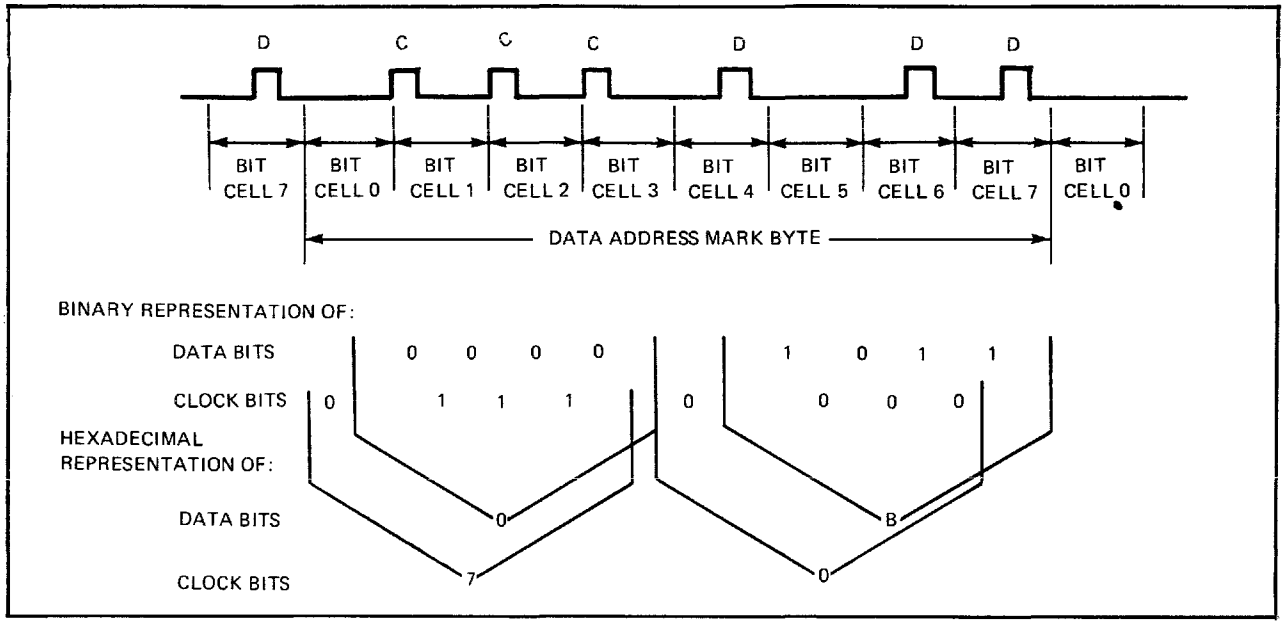


Figure 4-22. Data Address Mark

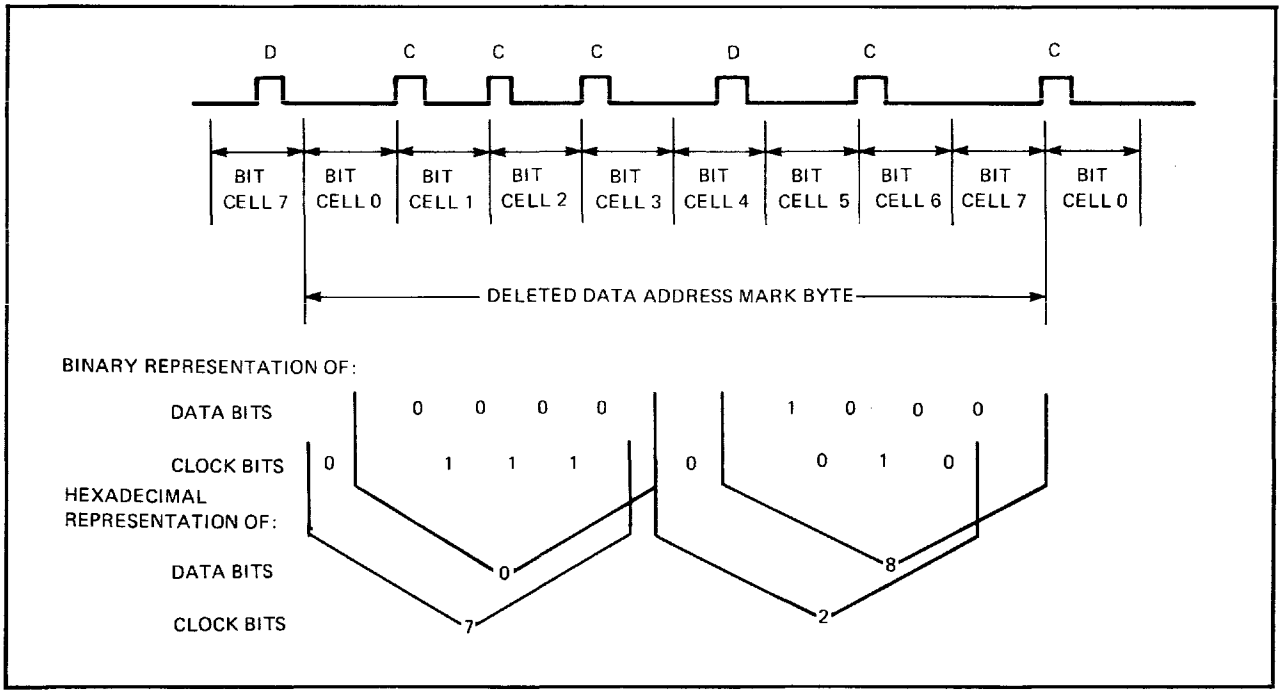


Figure 4-23. Deleted Data Address Mark

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This section provides parts location diagrams, and schematic diagrams for the SBC 202 Double Density Diskette Controller.

5-2. SERVICE DIAGRAMS

The Diskette Controller parts location diagrams and schematic diagrams are given in figures 5-1 through 5-4. The Channel Board Schematic (Figure 5-3) consists of four sheets and the Interface Board (Figure 5-4) consists of six sheets. Each of the sheets contains grid coordinates. Signals that transverse from one sheet to another are assigned grid coordinates at both the signal source and signal destination. For example, the grid coordinates 2ZD8 locate a signal source (or destination) on sheet 2 zone D8.

Whenever a signal is active-low, its mnemonic is followed by a slash; for example MRDC/ means that the level on that line will be low when the memory read command is true (active). If the signal is subsequently inverted, thus making it active-high, the slash is omitted; for example, MRDC means that the level on that line will be high when the memory command is true.

5-3. RESHIPMENT

If the product is to be shipped to Intel for service or repair, contact the Technical Support Center at the telephone number listed below to obtain a Return Authorization Number and further instructions. If the product was damaged during shipment from Intel, or if the product is out of warranty, a purchase order will be required to complete the repair.

The original factory packaging material, if available, to ship the product to the Technical Support Center. If original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a corrugated carton suitable for shipping. Seal the shipping carton securely, mark it "FRAGILE" to ensure careful handling, and address it to:

Intel Corporation
Technical Support Center
3065 Bowers Avenue
Santa Clara, California 95051
Telephone: (408) 246-7501
TWX: 910-338-0026
TELEX: 34-6372

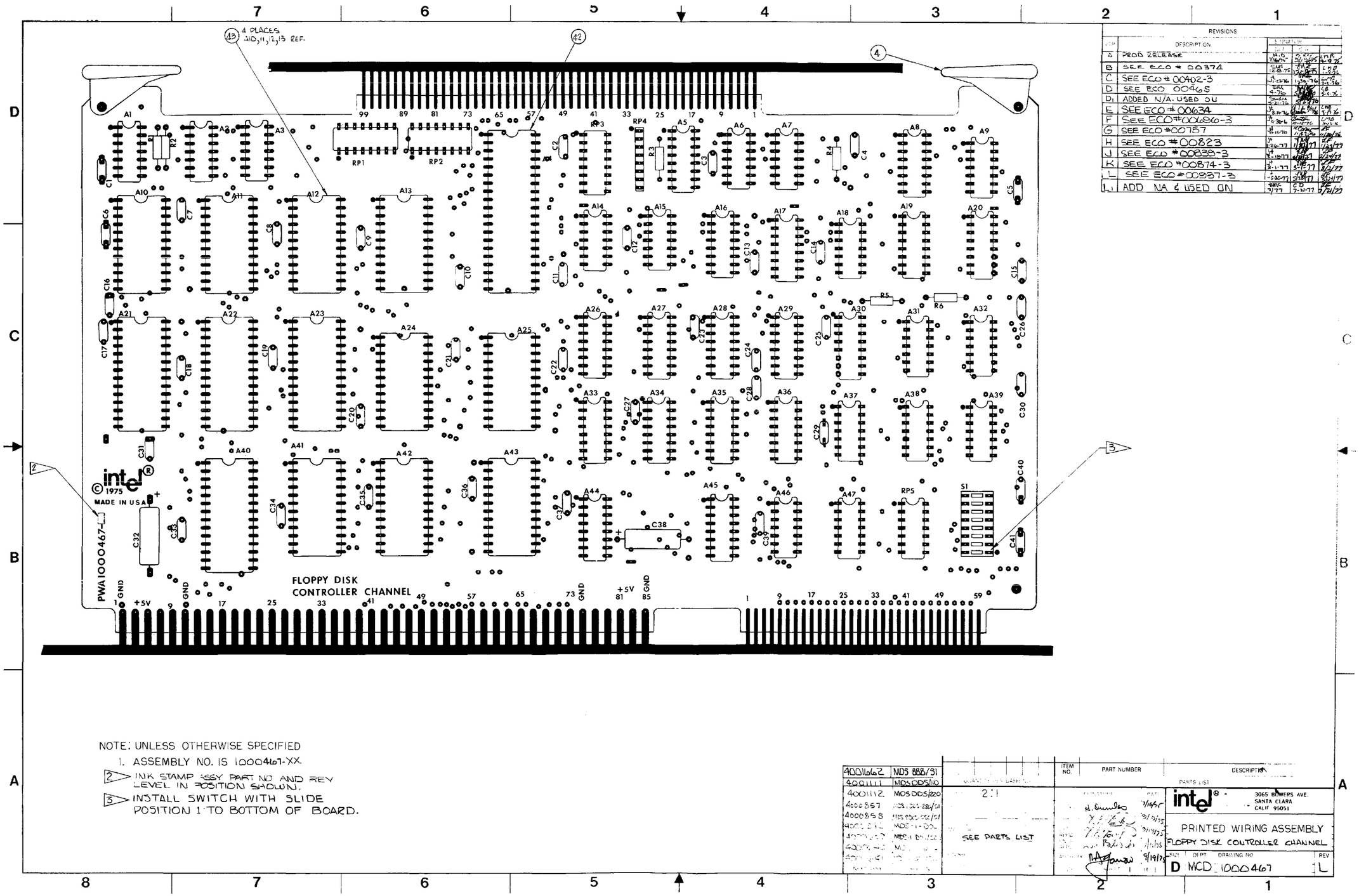


Figure 5-1. Parts Location: Channel Board

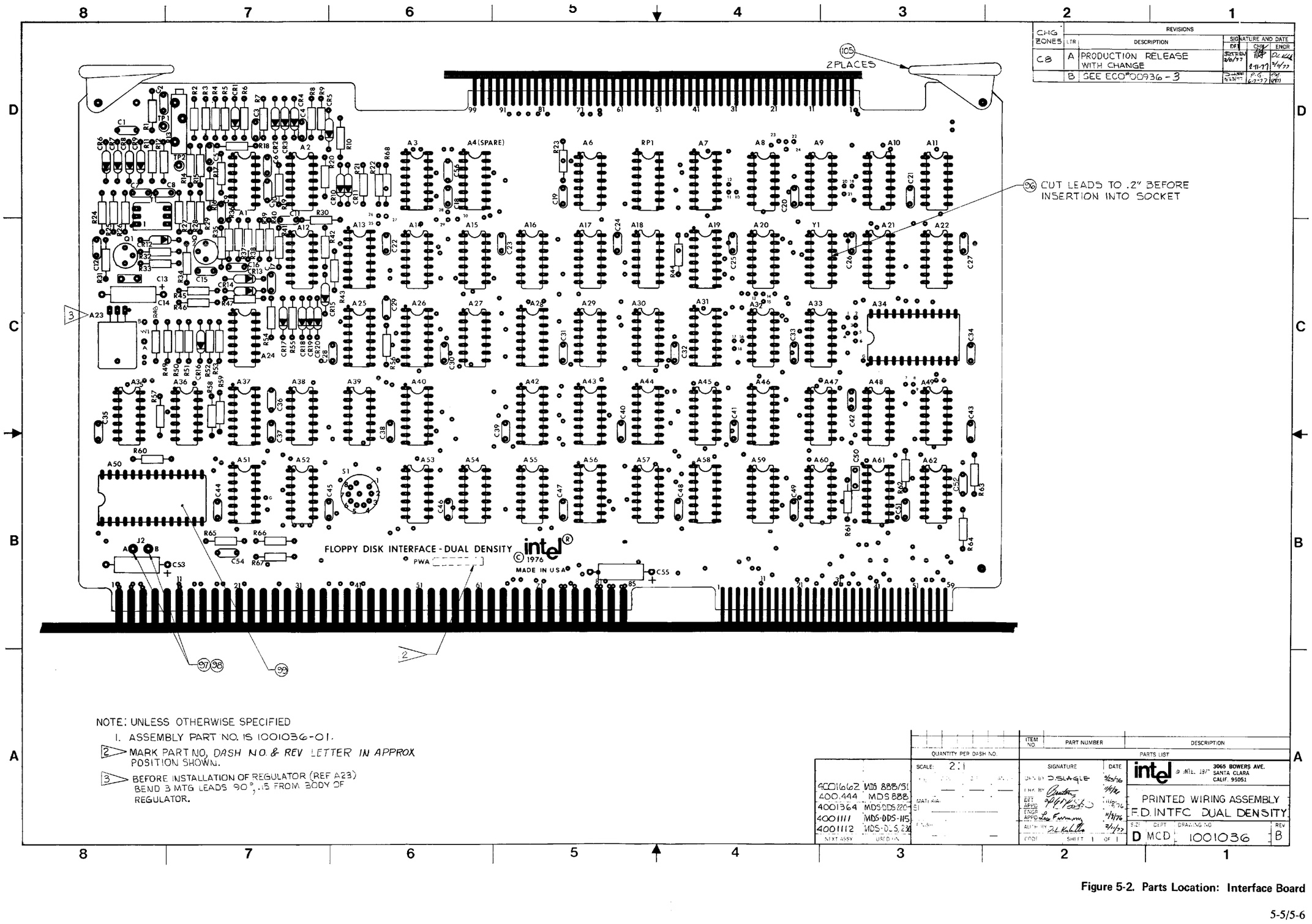
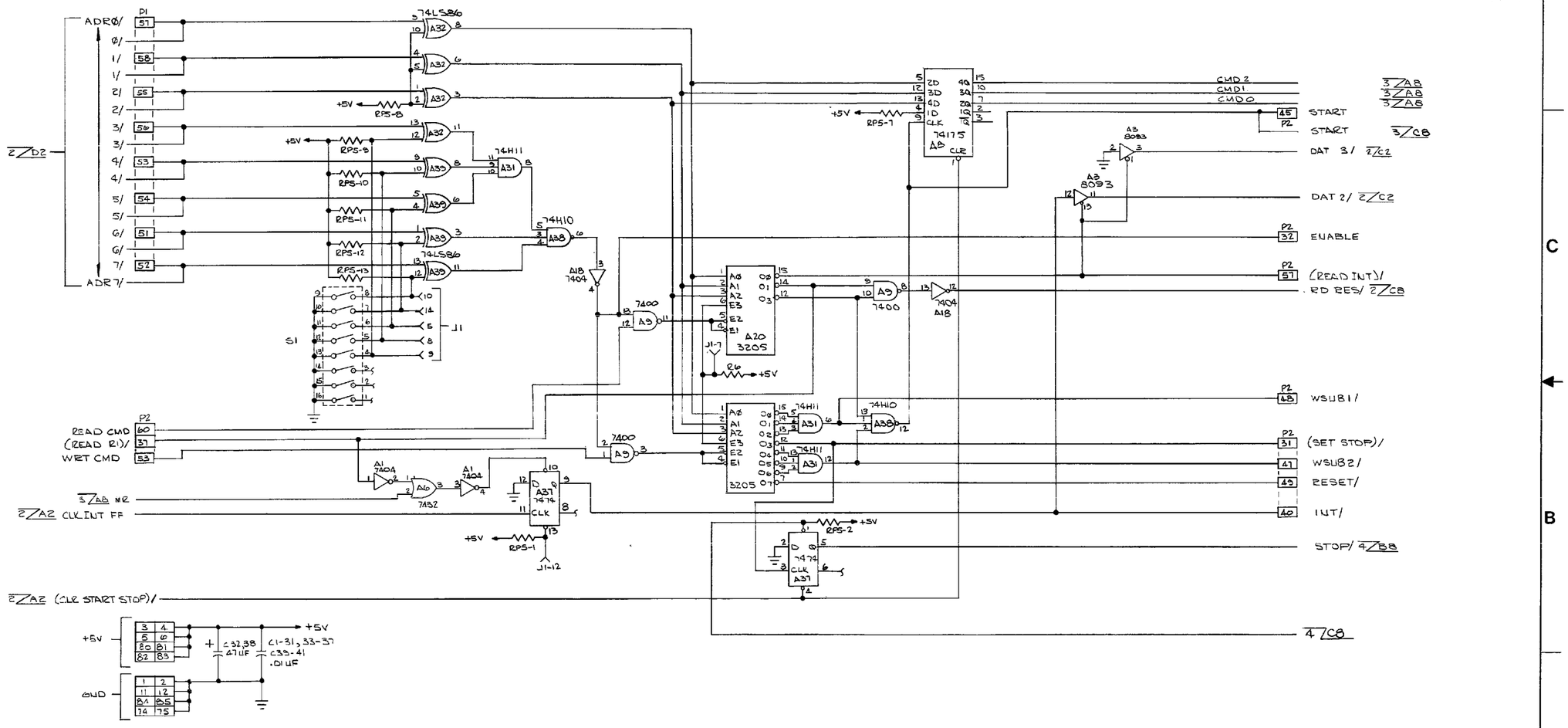


Figure 5-2. Parts Location: Interface Board

REVISIONS				
LTR	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGR
9	ENG'G RELEASE			
A	PROD RELEASE			
B	SEE ECO # 00402-1			
C	SEE ECO # 00696-2			
D	SEE ECO # 00816			
E	SEE ECO # 00839-1			
F	SEE ECO # 00874-1			
G	SEE ECO # 00937-1			



NOTES: UNLESS OTHERWISE SPECIFIED.

1. THIS DOCUMENT REFLECTS ARTWORK NO. 1000468, REV 'F'.
2. RESISTOR VALUES ARE IN OHMS 1K, 1/4W, 5%.
3. CONNECTOR J1 IS USED FOR TEST POINT ONLY.

J1,P2				
RP5				
S1				
R6				
C41		A6	7432	1
A37		A3	8093	1
LAST USED	WDT USED	A1	7404	4
REF DESIG.		REF. DESIG	TYPE	QTY
	SPARE GATE			

1000467	MDS-003
NEXT ASSY	USED ON

QUANTITY PER DASH NO.			
SCALE: NONE			
TOL ±	2 PLC —	3 PLC —	ANGLE —
MATERIAL:			
FINISH:			

ITEM NO.	PART NUMBER	DESCRIPTION
PARTS LIST		

SIGNATURE		DATE
DRN BY		5/1/75
CHK BY		6/10/75
DFT APPD		6/17/75
ENGR APPD		6/16/75
AUTH BY		9/10/75
CODE:	SHEET 1 OF 9	

intel © INTEL 1975 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC FLOPPY DISK CONTROLLER CHANNEL

SIZE	DEPT	DRAWING NO.	REV
D	MCD	2000469	G

Figure 5-3. Schematic Drawing: Channel Board (Sheet 1 of 4)

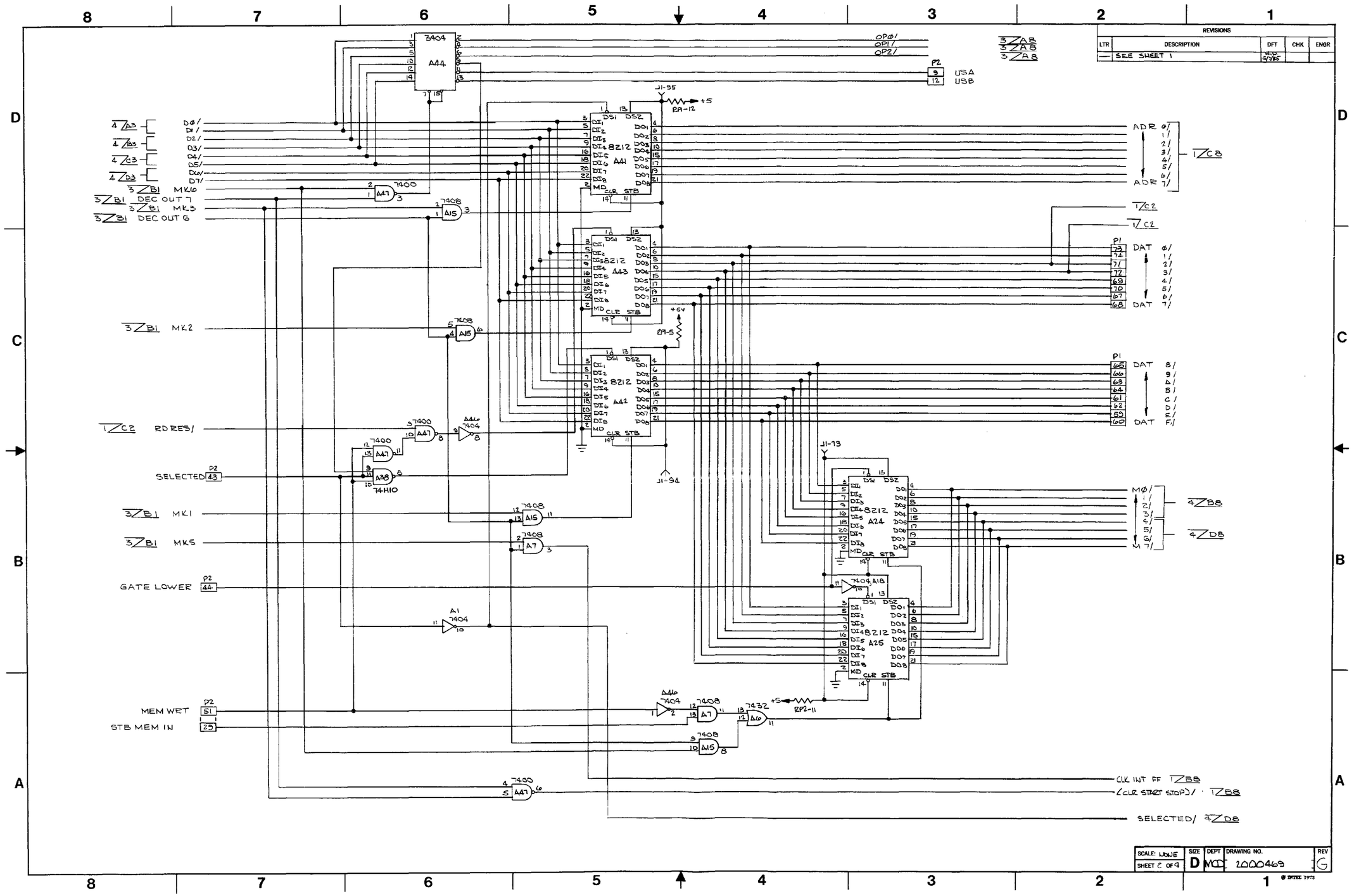


Figure 5-3. Schematic Drawing: Channel Board (Sheet 2 of 4)

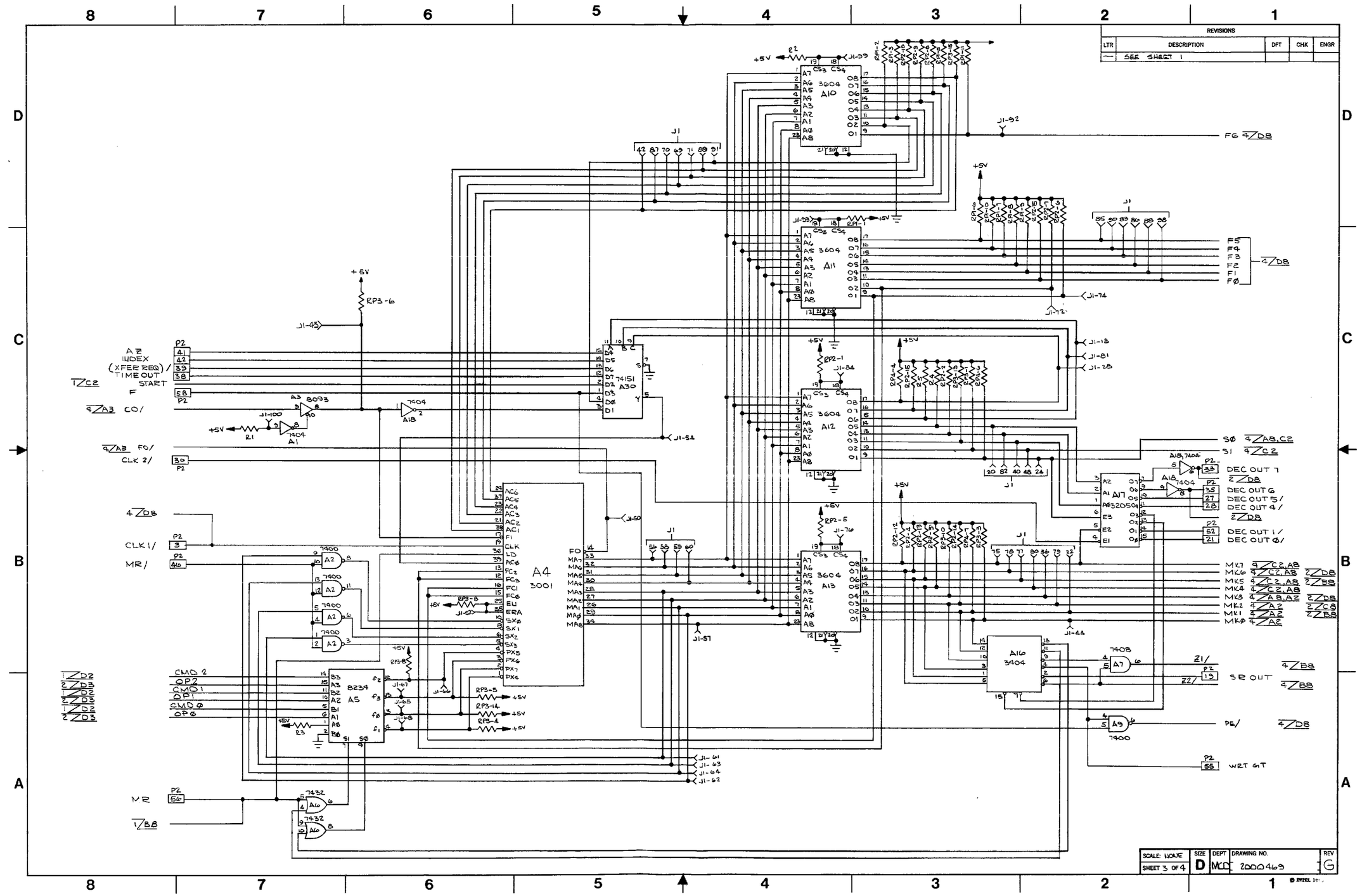


Figure 5-3. Schematic Drawing: Channel Board (Sheet 3 of 4)

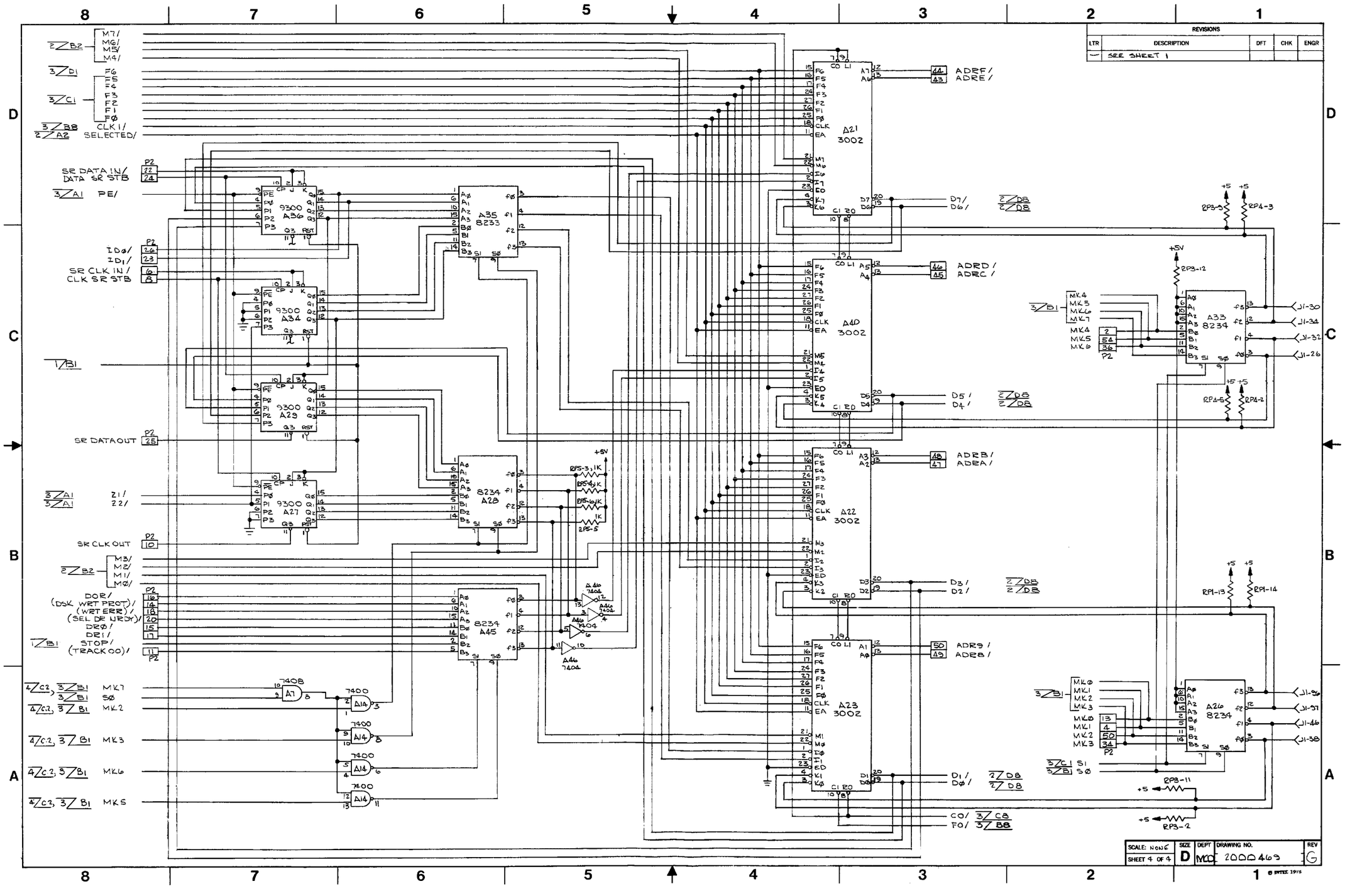
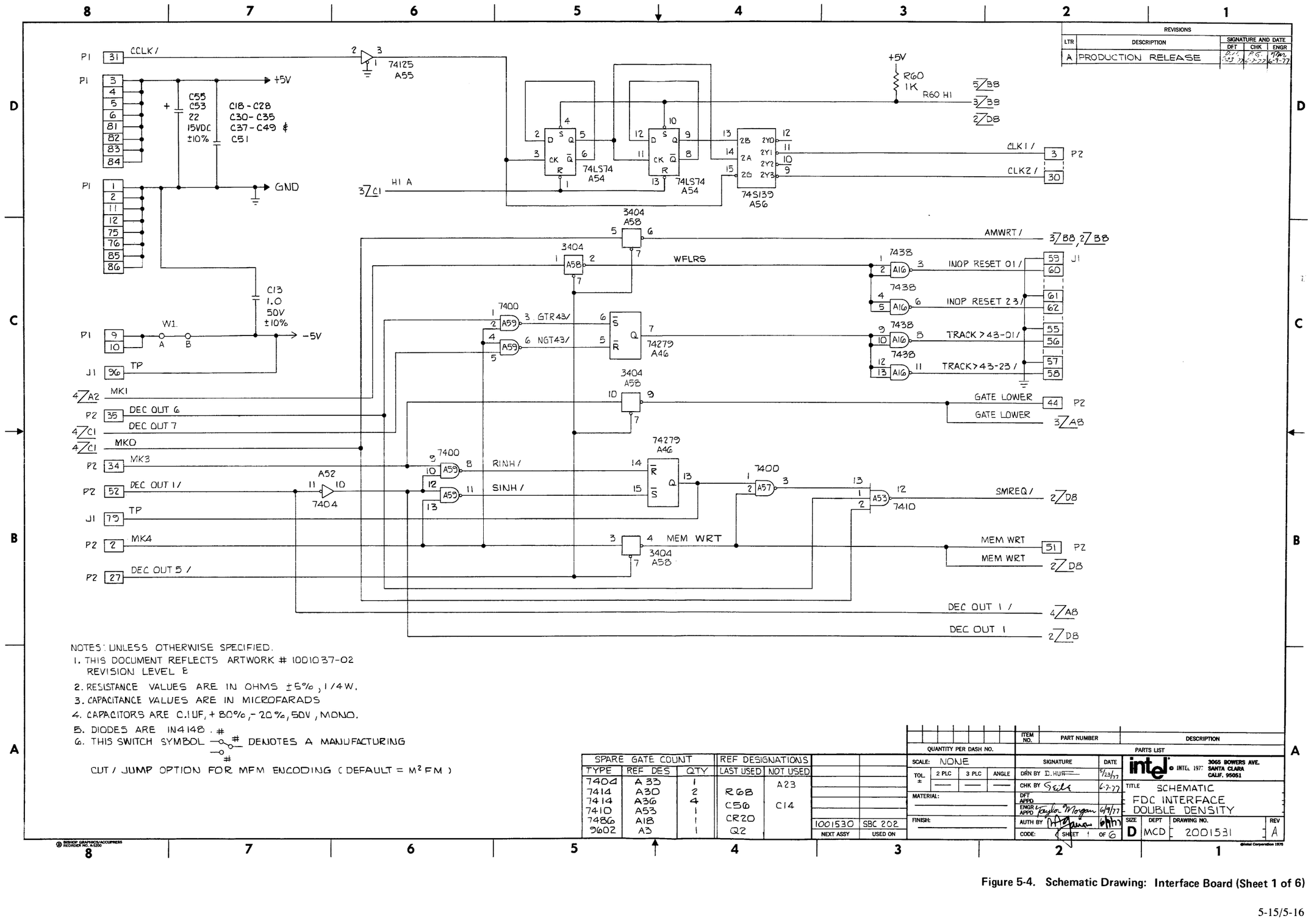


Figure 5-3. Schematic Drawing: Channel Board (Sheet 4 of 4)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. THIS DOCUMENT REFLECTS ARTWORK # 1001037-02 REVISION LEVEL B
2. RESISTANCE VALUES ARE IN OHMS ±5%, 1/4W.
3. CAPACITANCE VALUES ARE IN MICROFARADS
4. CAPACITORS ARE .1UF, +80%, -20%, 50V, MONO.
5. DIODES ARE IN4148. #
6. THIS SWITCH SYMBOL —o-#-o— DENOTES A MANUFACTURING —o-#-o— CUT/JUMP OPTION FOR MFM ENCODING (DEFAULT = M²FM)

SPARE GATE COUNT			REF DESIGNATIONS	
TYPE	REF DES	QTY	LAST USED	NOT USED
7404	A33	1		A23
7414	A30	2	R68	
7414	A36	4	C56	C14
7410	A53	1	CR20	
7486	A18	1		
9602	A3	1	Q2	

1001530 NEXT ASSY | SBC 202 USED ON

QUANTITY PER DASH NO.

ITEM NO.	PART NUMBER	DESCRIPTION

PARTS LIST

SCALE: NONE

TOL ± | 2 PLC | 3 PLC | ANGLE

MATERIAL:

FINISH:

SIGNATURE	DATE
DRN BY D. HUA	5/23/77
CHK BY Seitz	6-7-77
DFT APPD	
ENGR APPD Taylor Morgan	6/9/77
AUTH BY M. Hanna	6/9/77

CODE: SHEET 1 OF 6

intel® INTEL 1977 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE SCHEMATIC FDC INTERFACE DOUBLE DENSITY

SIZE D | DEPT MCD | DRAWING NO. 2001531 | REV A

Global Corporation 1976

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-5200

Figure 5-4. Schematic Drawing: Interface Board (Sheet 1 of 6)

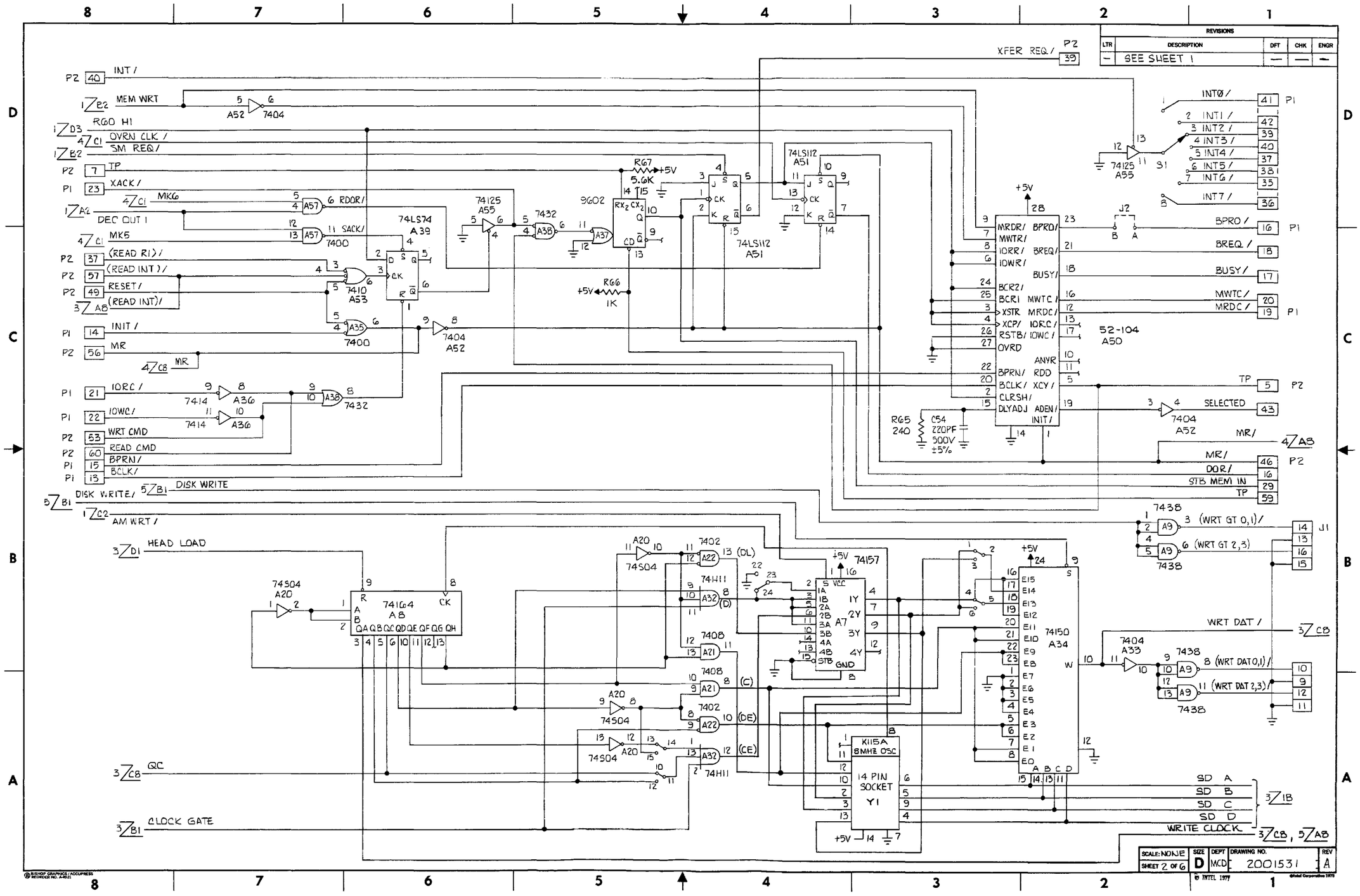


Figure 5-4. Schematic Drawing: Interface Board (Sheet 2 of 6)

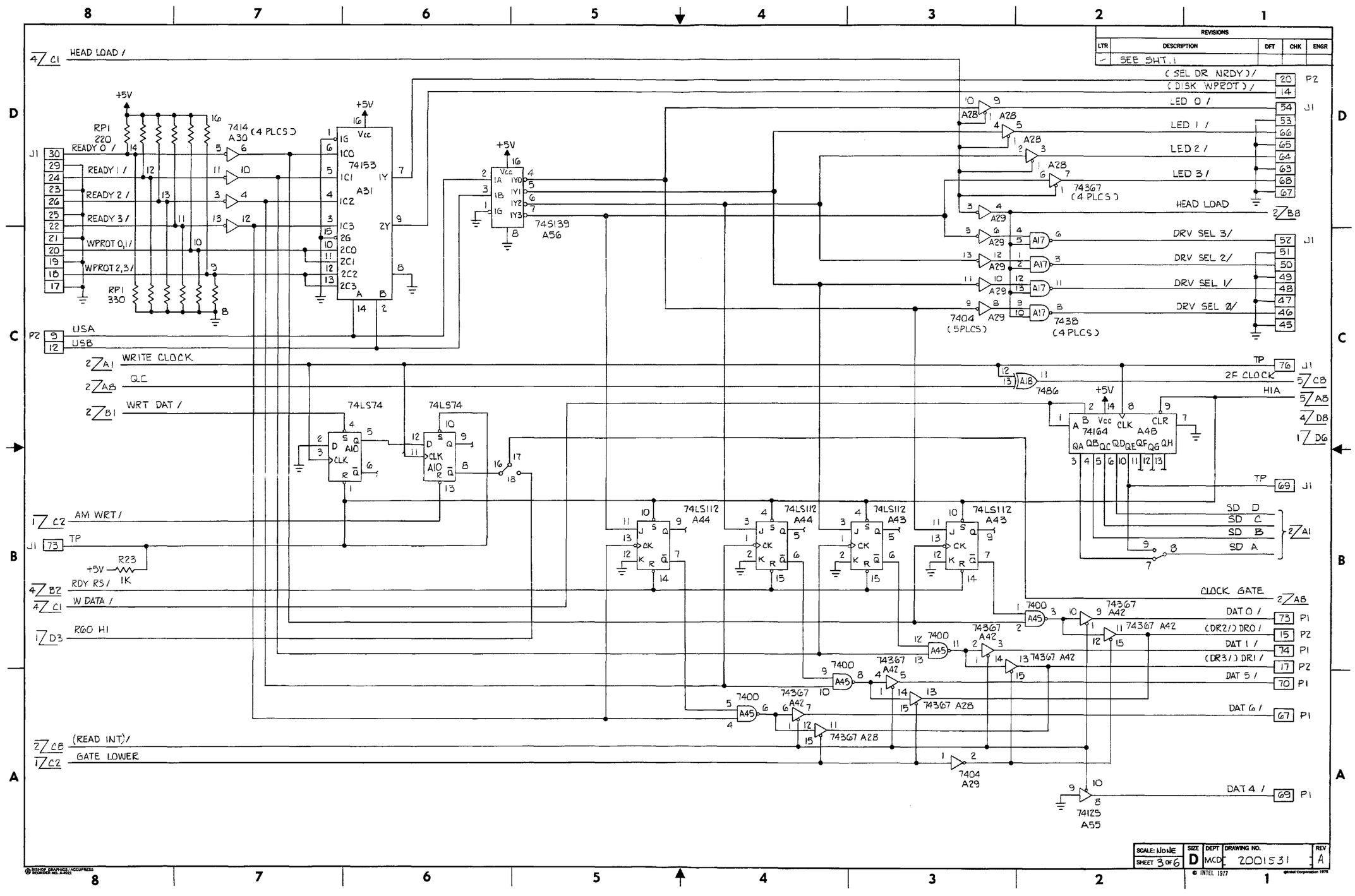


Figure 5-4. Schematic Drawing: Interface Board (Sheet 3 of 6)

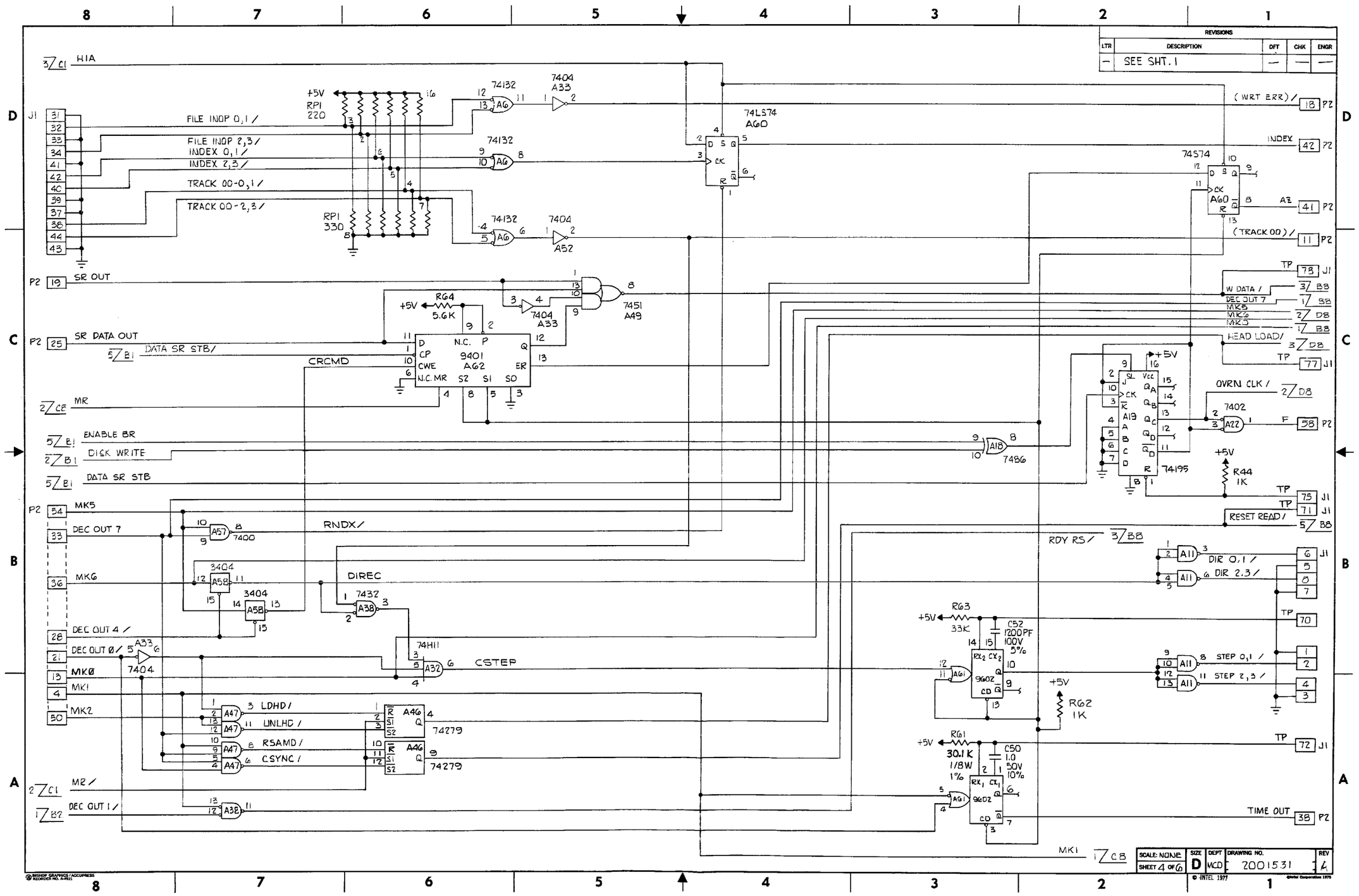


Figure 5-4. Schematic Drawing: Interface Board (Sheet 4 of 6)

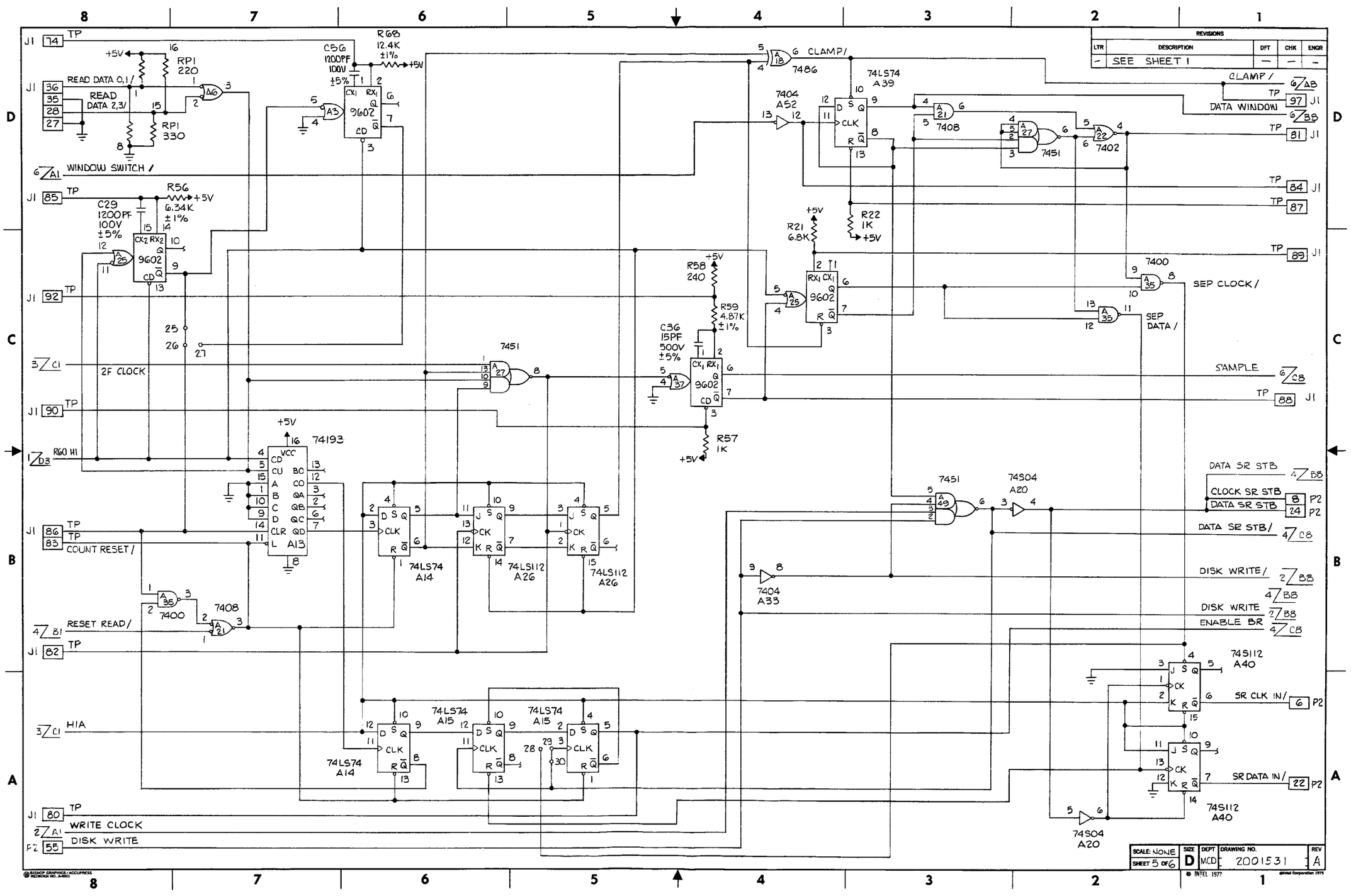


Figure 5-4. Schematic Drawing: Interface Board (Sheet 5 of 6)

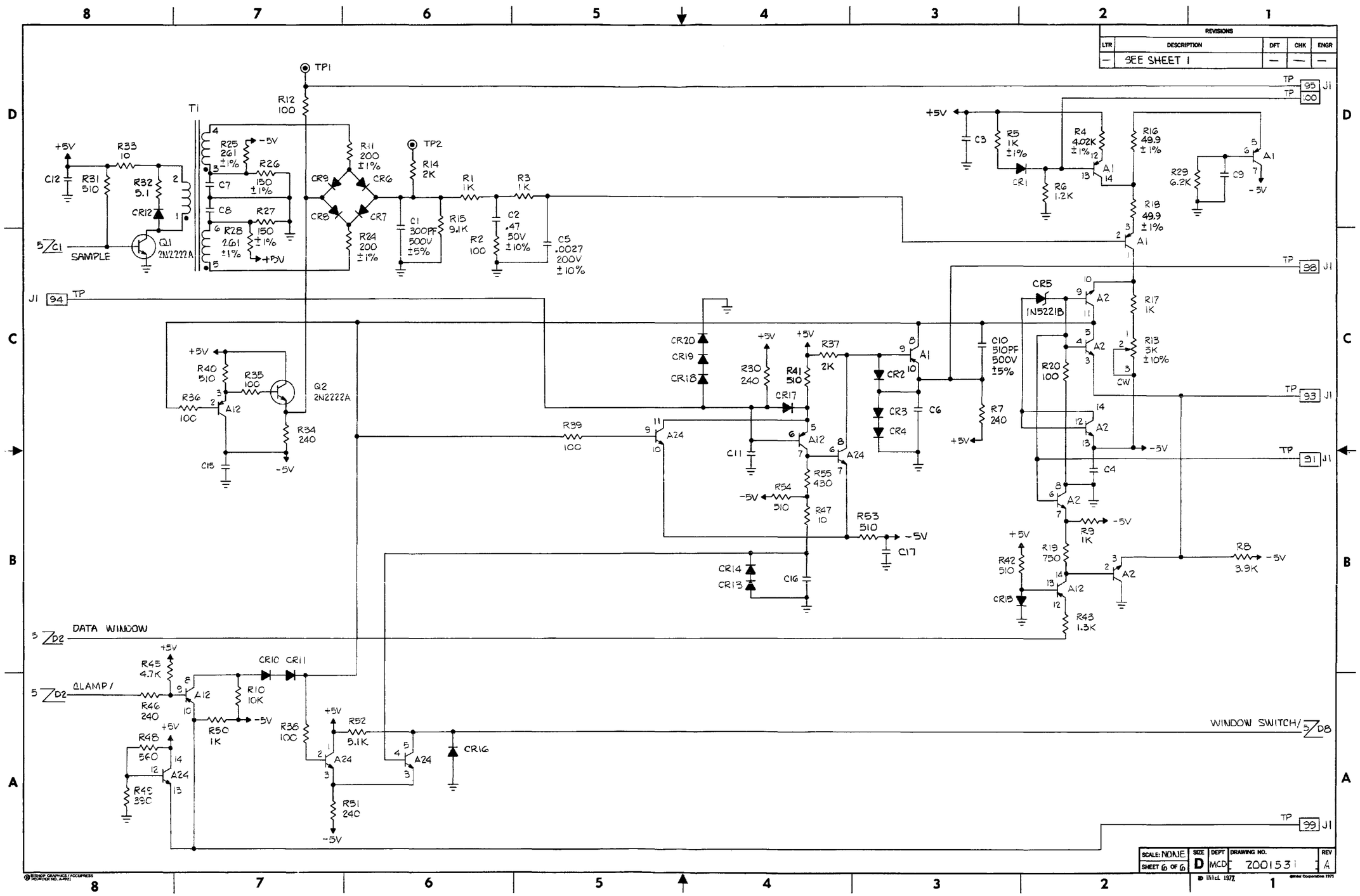


Figure 5-4. Schematic Drawing: Interface Board (Sheet 6 of 6)

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