OEM COMPUTER SYSTEMS

SBC 80/10 SINGLE BOARD COMPUTER

8080A Central Processing Unit

1 K bytes of read/write memory

Sockets for 4K bytes of programmable or masked read-only memory

48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators

Programmable Synchronous/Asynchronous communications interface with selectable teletype or RS232C compatibility

Six interrupt request lines

Bus drivers for memory and I/O expansion

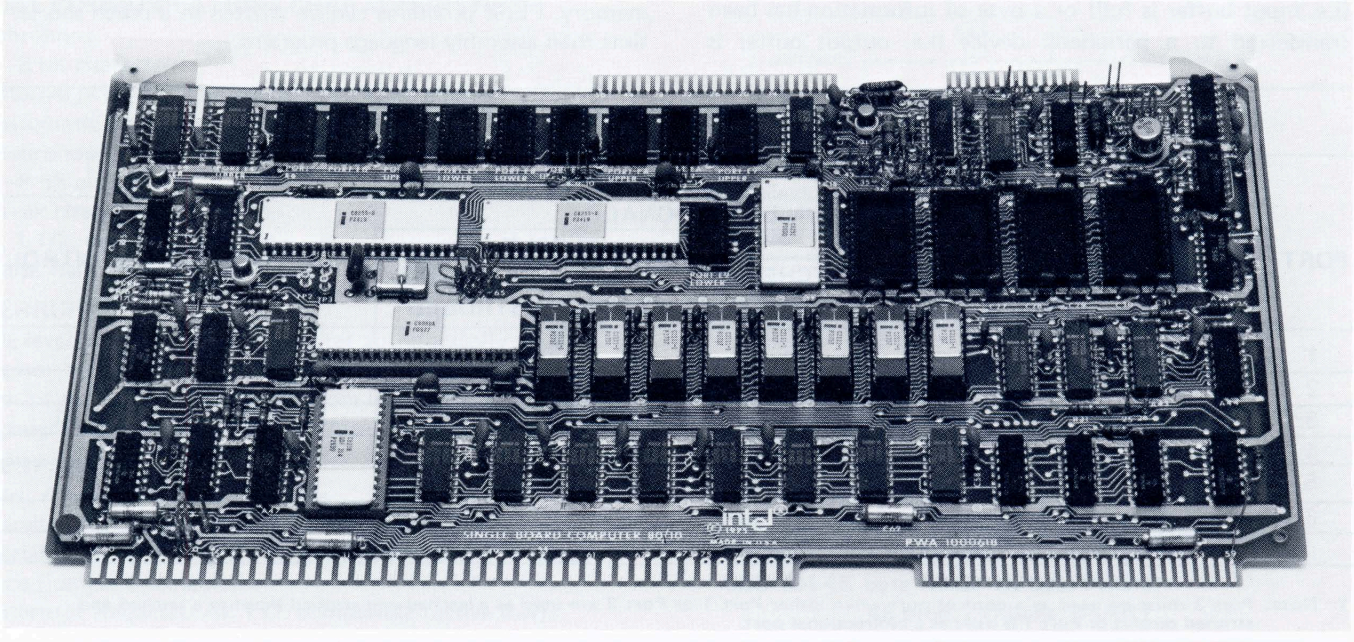
Compatible with optional memory and I/O expansion boards.

The SBC 80/10 is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer based solutions for OEM applications. The SBC 80/10 is a complete computer system on a single 6.75-by-12 inch printed circuit card. The CPU, system clock, read/write memory, non-volatile read-only-memory, I/O ports and drivers, serial communications interface, bus control logic and drivers all reside on the board.

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the SBC 80/10. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators.

The 8080A has a 16-bit program counter which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last in/first out stack to store the contents of the program counter, flags, accumulator and all of the six general purpose registers. A sixteen bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting that is bounded only by memory size.

The SBC 80/10 contains 1K bytes of read/write memory using Intel 8111 low power static RAM. All on-board RAM read and write operations are performed at maximum processor speed. Sockets for up to 4K bytes of non-volatile read-only memory are provided on the board. Read only memory may be added in 1K byte increments using Intel 8708 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 8308 masked ROMs. All on-board ROM read operations are performed at maximum processor speed.



The SBC 80/10 contains 48 programmable parallel I/O lines implemented using two Intel 8255 Programmable Peripheral Interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bi-directional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50 pin edge connectors that mate with flat-cable or round-cable.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A jumper selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e. synchronous or asynchronous), data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double buffered transmission and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of jumper selectable teletype or RS232C compatible interfaces on the board, in conjunction with the USART provide a direct interface to teletypes, CRTs, RS232 compatible cassettes, asynchronous and synchronous modems. The RS232C or teletype command lines, serial data lines, and signal ground lines are brought out to a 25-pin edge connector that mates with RS232C compatible flat or round cable.

Interrupt requests may originate from six sources. Two jumper selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface when a byte of information is ready to be transferred to the CPU (i.e. input buffer is full) or a byte of information has been transferred to a peripheral device (i.e. output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e. receive channel buffer is full) or a character is ready to be transmitted (i.e. transmit channel data buffer is empty). These four interrupt request lines are all individually maskable under program control. Two interrupt request lines may be interfaced directly to user designated peripheral devices; one via the system bus and the other via the I/O edge connector. The six interrupt request lines share a single CPU interrupt level. When an interrupt request is recognized, a RESTART 7 instruction is generated. The processor responds by suspending program execution and executing a user defined interrupt service routine originating at location 38_{16}.

SBC 80 memory and I/O capacity may be increased by adding standard Intel memory and I/O boards. Memory may be expanded to 64K bytes by adding user specified combinations of SBC-016 16K RAM boards, SBC-416 16K PROM boards, and SBC-406 6K PROM boards. Input/output capacity may be increased to 504 input lines and 504 output lines using SBC-508 I/O boards, containing 32 input lines and 32 output lines per board. Memory and I/O may be increased simultaneously by adding an SBC-104 board containing 4K bytes of RAM, sockets for 4K bytes of PROM, 48 programmable I/O lines and a USART. Modular expandable backplanes and card cages, with a four-board capacity, are available to support multi-board systems.

The development cycle of SBC 80/10 based products may be significantly reduced using the Intellec MDS Microcomputer Development System. The resident macro-assembler, text editor, and system monitor greatly simplify the design, development, and debug of SBC 80/10 system software. An optional Diskette Operating System allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique In-Circuit Emulator (ICE-80) option provides the capability of developing and debugging software directly on the SBC 80/10.

Intel's high-level programming language, PL/M, provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M programs can be written in a much shorter time than assembly language programs.

TABLE 1 INPUT/OUTPUT PORT MODES OF OPERATION

PORT	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	8	X		X			X[1]
4	8	X		X			
5	8	X		X			
6	4	X		X			
	4	X		X			

1. Note: Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output or Port 1 is used as a bidirectional port.

SPECIFICATIONS

WORD SIZE
Instruction: 8, 16, or 24 bits
Data: 8 bits

CYCLE TIME
Basic Instruction Cycle: 1.95 μsec
Note: Basic instruction cycle is defined as the fastest instruction (i.e. four clock cycles)

MEMORY ADDRESSING
On-Board ROM/PROM: 0-OFFF
On-Board RAM: 3C00-3FFF

MEMORY CAPACITY
On-Board ROM/PROM: 4K bytes (sockets only)
On-Board RAM: 1K bytes
Off-Board Expansion: Up to 65,536 bytes using user specified combinations of RAM, ROM, and PROM
Note: ROM/PROM may be added in 1K byte increments.

I/O ADDRESSING
On-Board Programmable I/O (See Table 1)

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O CAPACITY
Parallel: 48 programmable lines (See Table 1)
Note: Expansion to 504 input and 504 output lines can be accomplished using optional I/O boards.

SERIAL BAUD RATES

Frequency (KHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
307.2	–	19200	4800
153.6	–	9600	2400
76.8	–	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
3.49	3490	–	110

SERIAL COMMUNICATIONS CHARACTERISTICS
Synchronous:
5–8 bit characters
Internal or external character synchronization
Automatic Sync Insertion
Asynchronous:
5–8 bit characters
Break character generation
1, 1-1/2, or 2 stop bits
False start bit detectors

INTERRUPTS
Single-level with on-board logic that automatically vectors processor to location 38_{16} using RESTART 7 instruction. Interrupt requests may originate from user specified I/O (2) the programmable peripheral interface (2), or USART (2).

INTERFACES
Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Serial I/O: RS232C, or a 20 mil current loop TTY interface (jumper selectable)
Interrupt Requests: All TTL compatible (active low)

SYSTEM CLOCK
2.048 MHz ±0.1%

CONNECTORS

Interface	No. of double-sided pins	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O (Two)	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113

PHYSICAL CHARACTERISTICS
Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz. (484.4 gm)

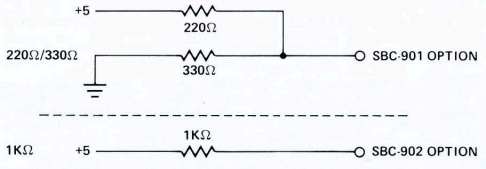
ELECTRICAL CHARACTERISTICS
DC Power:
V_{CC} = +5 ±5% I_{CC} = 2.9 A max
V_{DD} = +12 ±5% I_{DD} = 150 mA max
V_{BB} = –5V ±5% I_{BB} = 2 mA max
V_{AA} = –12V ±5% I_{AA} = 150 mA max
Note: Does not include power required for optional PROM, I/O drivers, and I/O terminators.

LINE DRIVERS AND TERMINATORS
I/O Drivers:
The following line drivers and terminators are all compatible with the I/O driver sockets on the SBC 80/10.

Driver	Characteristic	Sink Current (ma)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note: I = inverting N.I. = non-inverting OC = open collector

Port 1 has 25 nA totem pole drivers and 1 kΩ terminators.
I/O Terminators:
Terminators: 220Ω/330Ω divider or 1 kΩ pull up

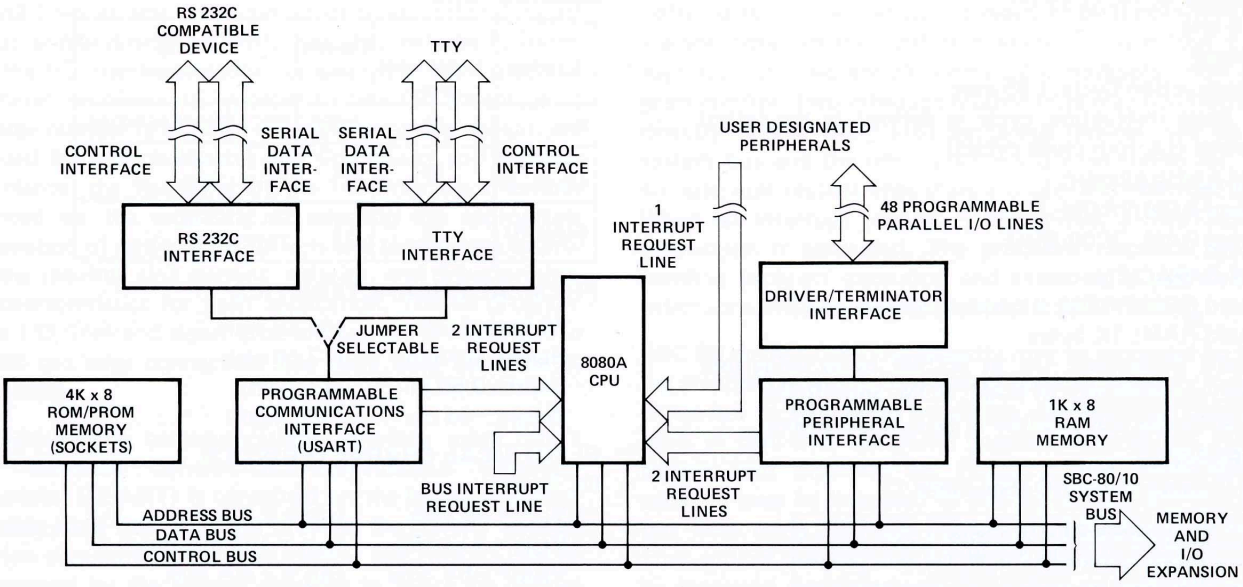


Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	Tri-State	25
Address	Tri-State	25
Commands	Tri-State	25

ENVIRONMENTAL
Operating Temperature: 0°C to 70°C

COMPATIBLE BOARDS
SBC-016 16K byte RAM
SBC-406 6K byte PROM
SBC-416 16K byte PROM
SBC-508 32 input lines/32 output lines
SBC-104 4K byte RAM, 4K byte PROM, 48 prog. I/O lines, USART



1. Interrupts originating from the Programmable Communications Interface and Programmable Peripheral Interface are jumper selectable.

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