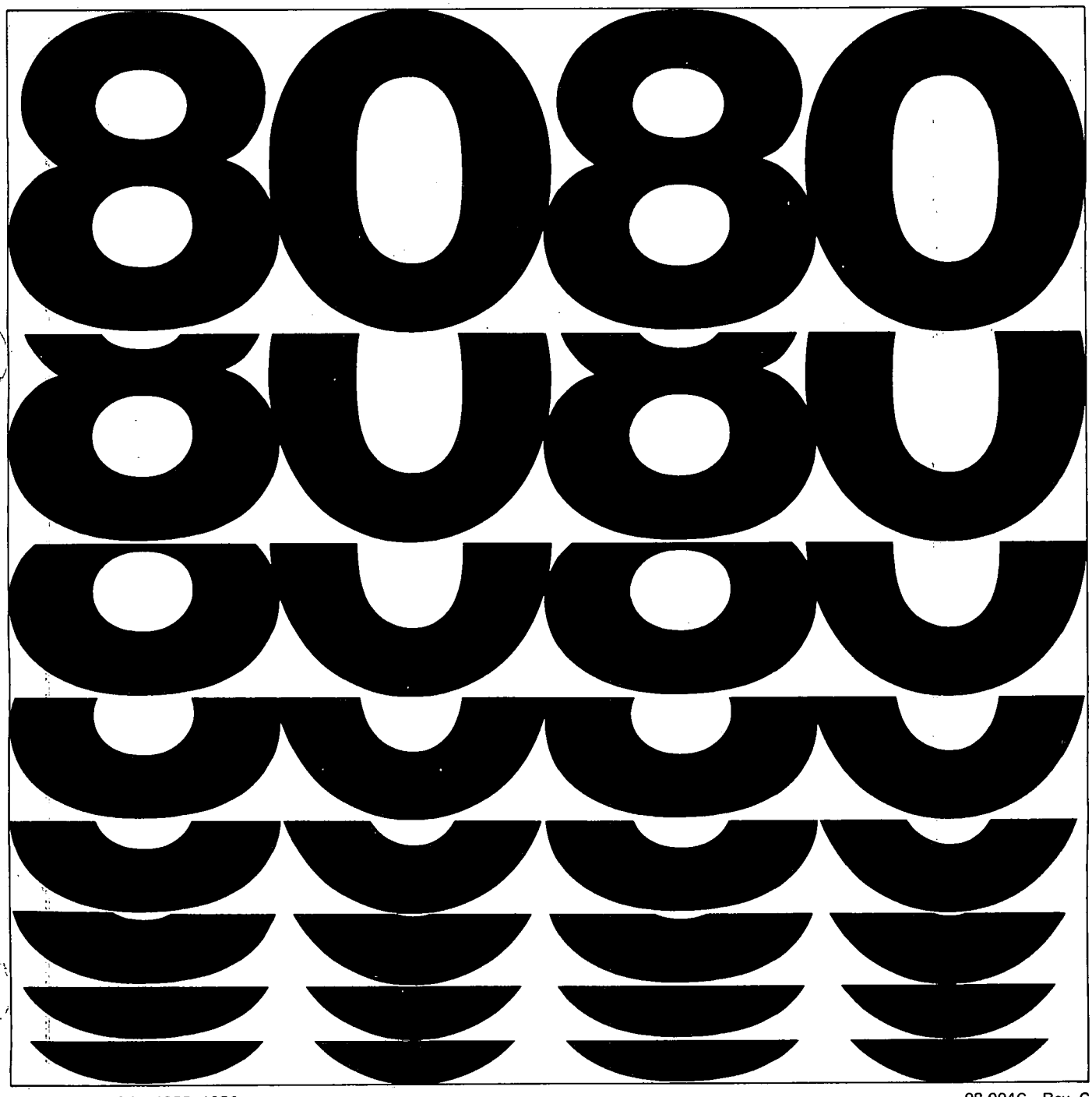
W. ZOLNEROVICH

intel®

8080 Assembly Language Programming Manual



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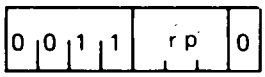
W. ZOLNEROVICH

8080 Assembly Language Programming Manual

This manual describes the assembly language format, and how to write assembly language programs for the Intel®8080 microprocessor. Detailed information on the operation of specific assemblers is available in the Operator's Manual and Installation Guide for each specific assembler.

TERMS	DESCRIPTION
Address	A 16-bit number assigned to a memory location corresponding to its sequential position.
Bit	The smallest unit of information which can be represented. (A bit may be in one of two states, represented by the binary digits 0 or 1).
Byte	A group of 8 contiguous bits occupying a single memory location.
Instruction	The smallest single operation that the computer can be directed to execute.
Object Program	A program which can be loaded directly into the computer's memory and which requires no alteration before execution. An object program is usually on paper tape, and is produced by assembling (or compiling) a source program. Instructions are represented by binary machine code in an object program.
Program	A sequence of instructions which, taken as a group, allow the computer to accomplish a desired task.
Source Program	A program which is readable by a programmer but which must be transformed into object program format before it can be loaded into the computer and executed. Instructions in an assembly language source program are represented by their assembly language mnemonic.
System Program	A program written to help in the process of creating user programs.
User Program	A program written by the user to make the computer perform any desired task.
Word	A group of 16 contiguous bits occupying two successive memory locations.
nnnnB	nnnn represents a number in binary format.
nnnnD	nnnn represents a number in decimal format.
nnnnO	nnnn represents a number in octal format.
nnnnQ	nnnn represents a number in octal format.
nnnnH	nnnn represents a number in hexadecimal format.
	A representation of a byte in memory. Bits which are fixed as 0 or 1 are indicated by 0 or 1; bits which may be either 0 or 1 in different circumstances are represented by letters; thus rp represents a three-bit field which contains one of the eight possible combinations of zeroes and ones.

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INTRODUCTION

This manual has been written to help the reader program the INTEL® 8080 microcomputer in assembly language. Accordingly, this manual assumes that the reader has a good understanding of logic, but may be completely unfamiliar with programming concepts.

For those readers who do understand programming concepts, several features of the INTEL 8080 microcomputer are described below. They include:

- 8-bit parallel CPU on a single chip
- 78 instructions, including extensive memory referencing, flexible jump-on-condition capability, and binary and decimal arithmetic modes
- Direct addressing for 65,536 bytes of memory
- Fully programmable stacks, allowing unlimited subroutine nesting and full interrupt handling capability
- Seven 8-bit registers

There are two ways in which programs for the 8080 may be assembled; either via the resident assembler or the cross assembler. The resident assembler is one of several system programs available to the user which run on the 8080. The cross assembler runs on any computer having a FORTRAN compiler whose word size is 32 bits or greater, and generates programs which run on the 8080.

The experienced programmer should note that the assembly language has a macro capability which allows users to tailor the assembly language to individual needs.

CHAPTER 1
COMPUTER ORGANIZATION

This section provides the programmer with a functional overview of the 8080. Information is presented in this section at a level that provides a programmer with necessary background in order to write efficient programs.

To the programmer, the computer is represented as consisting of the following parts:

(1) Seven working registers in which all data operations occur, and which provide one means for addressing memory.

(2) Memory, which may hold program instructions or data and which must be addressed location by location in order to access stored information.

(3) The program counter, whose contents indicate the next program instruction to be executed.

(4) The stack pointer, a register which enables various portions of memory to be used as *stacks*. These in turn facilitate execution of subroutines and handling of interrupts as described later.

(5) Input/Output, which is the interface between a program and the outside world.

WORKING REGISTERS

The 8080 provides the programmer with an 8-bit accumulator and six additional 8-bit "scratchpad" registers.

These seven working registers are numbered and referenced via the integers 0, 1, 2, 3, 4, 5, and 7; by convention, these registers may also be accessed via the letters B, C, D, E, H, L, and A (for the accumulator), respectively.

Some 8080 operations reference the working registers in pairs referenced by the letters B, D, H and PSW. These correspondences are shown as follows:

Register Pair	Registers Referenced
B	B and C (0 and 1)
D	D and E (2 and 3)
H	H and L (4 and 5)
PSW	A and Flags (see below)

Register pair PSW (Program Status Word) refers to register A (7) and a special byte which reflects the current status of the machine flags. This byte is described in detail in Chapter 2.

MEMORY

The 8080 can be used with read only memory, programmable read only memory and read/write memory. A program can cause data to be read from any type of memory, but can only cause data to be written into read/write memory.

The programmer visualizes memory as a sequence of bytes, each of which may store 8 bits (represented by two hexadecimal digits). Up to 65,536 bytes of memory may be

present, and an individual memory byte is addressed by its sequential number from 0 to 65,535D=FFFFH, the largest number which can be represented by 16 bits.

The bits stored in a memory byte may represent the encoded form of an instruction or may be data, as described in Chapter 2 in the section on Data Statements.

PROGRAM COUNTER

The program counter is a 16 bit register which is accessible to the programmer and whose contents indicate the address of the next instruction to be executed as described in this chapter under Computer Program Representation in Memory.

STACK POINTER

A *stack* is an area of memory set aside *by the programmer* in which data or addresses are stored and retrieved by stack operations. Stack operations are performed by several of the 8080 instructions, and facilitate execution of subroutines and handling of program interrupts. The programmer specifies which addresses the stack operations will operate upon via a special accessible 16-bit register called the *stack pointer.*

INPUT/OUTPUT

To the 8080, the outside world consists of up to 256 input devices and 256 output devices. Each device communicates with the 8080 via data bytes sent to or received from the accumulator, and each device is assigned a number from 0 to 255 which is not under control of the programmer. The instructions which perform these data transmissions are described in Chapter 2 under Input/Output Instructions.

COMPUTER PROGRAM REPRESENTATION IN MEMORY

A computer program consists of a sequence of instructions. Each instruction enables an elementary operation such as the movement of a data byte, an arithmetic or logical operation on a data byte, or a change in instruction execution sequence. Instructions are described individually in Chapter 2.

A program will be stored in memory as a sequence of bits which represent the instructions of the program, and which we will represent via hexadecimal digits. The memory address of the next instruction to be executed is held in the program counter. Just before each instruction is executed, the program counter is advanced to the address of the next sequential instruction. Program execution proceeds sequentially unless a transfer-of-control instruction (jump, call, or return) is executed, which causes the program counter to be set to a specified address. Execution then continues sequentially from this new address in memory.

Upon examining the contents of a memory byte, there is no way of telling whether the byte contains an encoded instruction or data. For example, the hexadecimal code 1FH has been selected to represent the instruction RAR (rotate the contents of the accumulator right through carry); thus, the value 1FH stored in a memory byte could either represent the instruction RAR, or it could represent the data value 1FH. It is up to the logic of a program to insure that data is not misinterpreted as an instruction code, but this is simply done as follows:

Every program has a starting memory address, which is the memory address of the byte holding the first instruction to be executed. Before the first instruction is executed, the program counter will automatically be advanced to address the next instruction to be executed, and this procedure will be repeated for every instruction in the program. 8080 instructions may require 1, 2, or 3 bytes to encode an instruction; in each case the program counter is automatically advanced to the start of the next instruction, as illustrated in Figure 1-1.

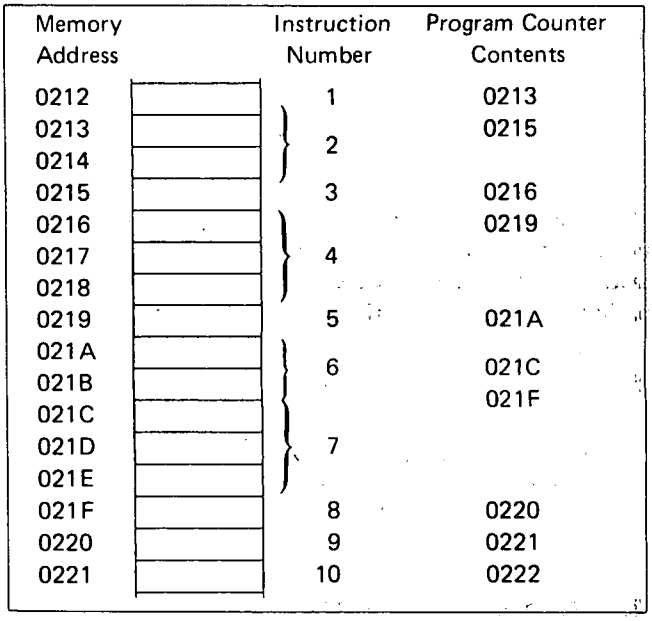


Figure 1-1. Automatic Advance of the Program Counter as Instructions Are Executed

In order to avoid errors, the programmer must be sure that a data byte does not follow an instruction when another instruction is expected. Referring to Figure 1-1, an instruction is expected in byte 021FH, since instruction 8 is to be executed after instruction 7. If byte 021FH held data, the program would not execute correctly. Therefore, when writing a program, do not store data in between adjacent instructions that are to be executed consecutively.

NOTE: If a program stores data into a location, that location should not normally appear among *any* program instructions. This is because user programs are (normally) executed from read-only memory, into which data cannot be stored.

A class of instructions (referred to as transfer-of-control instructions) cause program execution to branch to an instruction that may be anywhere in memory. The memory

address specified by the transfer of control instruction must be the address of another instruction; if it is the address of a memory byte holding data, the program will not execute correctly. For example, referring to Figure 1-1, say instruction 4 specifies a jump to memory byte 021FH, and say instructions 5, 6, and 7 are replaced by data; then following execution of instruction 4, the program would execute correctly. But if, in error, instruction 4 specifies a jump to memory byte 021EH, an error would result, since this byte now holds data. Even if instructions 5, 6, and 7 were not replaced by data, a jump to memory byte 021EH would cause an error, since this is not the first byte of the instruction.

Upon reading Chapter 2, you will see that it is easy to avoid writing an assembly language program with jump instructions that have erroneous memory addresses. Information on this subject is given rather to help the programmer who is debugging programs by entering hexadecimal codes directly into memory.

MEMORY ADDRESSING

By now it will have become apparent that addressing specific memory bytes constitutes an important part of any computer program; there are a number of ways in which this can be done, as described in the following subsections.

Direct Addressing

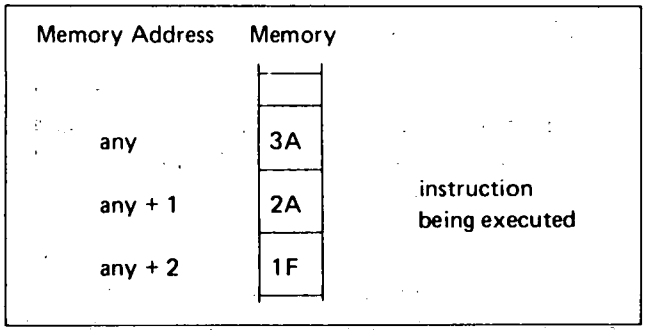
With direct addressing, an instruction supplies an exact memory address.

The instruction:

> "Load the contents of memory address 1F2A into the accumulator"

is an example of an instruction using direct addressing, 1F2A being the direct address.

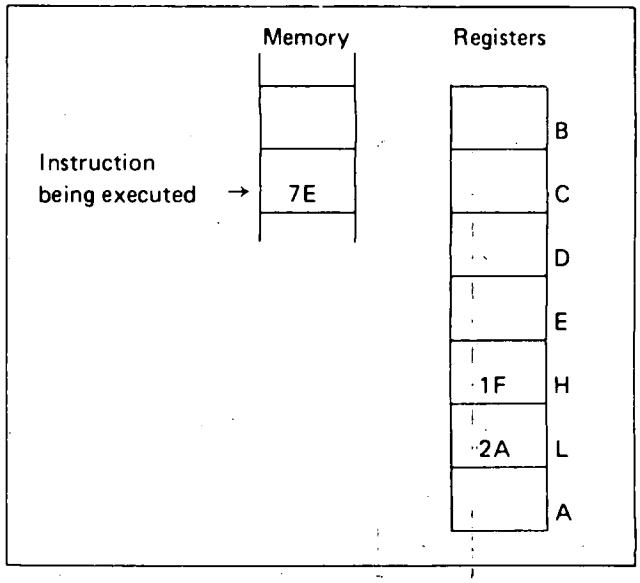
This would appear in memory as follows:



The instruction occupies three memory bytes, the second and third of which hold the direct address.

Register Pair Addressing

A memory address may be specified by the contents of a register pair. For almost all 8080 instructions, the H and L registers must be used. The H register contains the most significant 8 bits of the referenced address, and the L register contains the least significant 8 bits. A one byte instruction which will load the accumulator with the contents of memory byte 1F2A would appear as follows:



In addition, there are two 8080 instructions which use either the B and C registers or the D and E registers to address memory. As above, the first register of the pair holds the most significant 8 bits of the address, while the second register holds the least significant 8 bits. These instructions, STAX and LDAX, are described in Chapter 2 under Data Transfer Instructions.

Stack Pointer Addressing

Memory locations may be addressed via the 16-bit stack pointer register, as described below.

There are only two stack operations which may be performed; putting data into a stack is called a *push*, while retrieving data from a stack is called a *pop*.

NOTE: In order for stack push operations to operate, stacks must be located in read/write memory.

STACK PUSH OPERATION

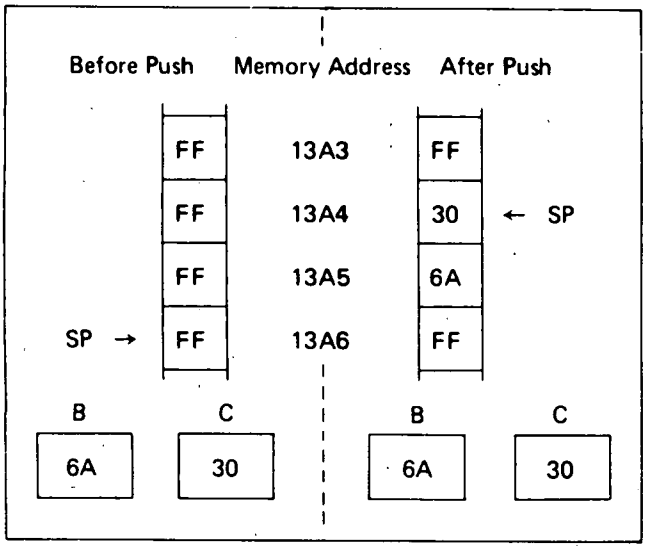
16 bits of data are transferred to a memory area (called a stack) from a register pair or the 16 bit program counter during any stack push operation. The addresses of the memory area which is to be accessed during a stack push operation are determined by using the stack pointer as follows:

(1) The most significant 8 bits of data are stored at the memory address one less than the contents of the stack pointer.

(2) The least significant 8 bits of data are stored at the memory address two less than the contents of the stack pointer.

(3) The stack pointer is automatically decremented by two.

For example, suppose that the stack pointer contains the address 13A6H, register B contains 6AH, and register C contains 30H. Then a stack push of register pair B would operate as follows:



STACK POP OPERATION

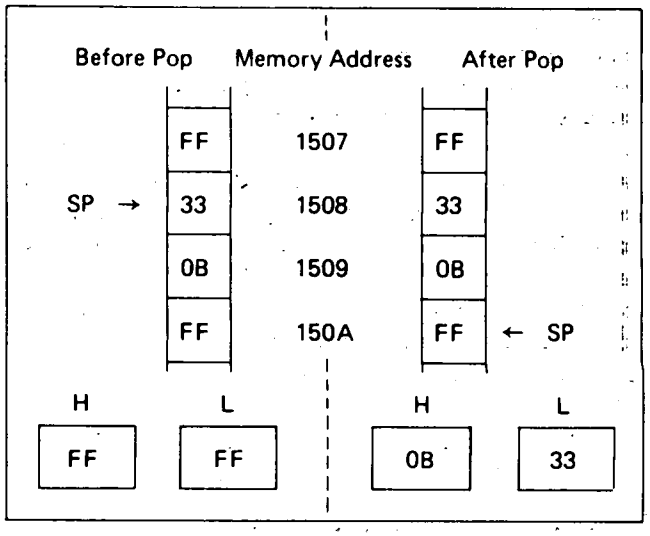
16 bits of data are transferred from a memory area (called a stack) to a register pair or the 16-bit program counter during any stack pop operation. The addresses of the memory area which is to be accessed during a stack pop operation are determined by using the stack pointer as follows:

(1) The second register of the pair, or the least significant 8 bits of the program counter, are loaded from the memory address held in the stack pointer.

(2) The first register of the pair, or the most significant 8 bits of the program counter, are loaded from the memory address one greater than the address held in the stack pointer.

(3) The stack pointer is automatically incremented by two.

For example, suppose that the stack pointer contains the address 1508H, memory location 1508H contains 33H, and memory location 1509H contains 0BH. Then a stack pop into register pair H would operate as follows:



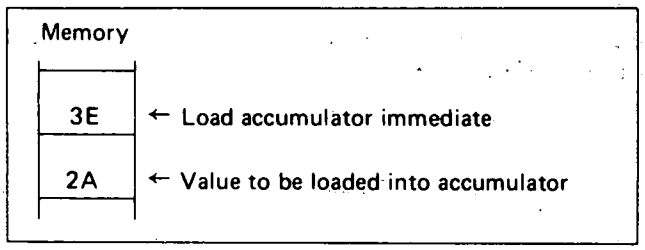
The programmer loads the stack pointer with any desired value by using the LXI instruction described in Chapter 2 under Load Register Pair-Immediate. The programmer must initialize the stack pointer before performing a stack operation, or erroneous results will occur.

Immediate Addressing

An immediate instruction is one that contains data. The following is an example of immediate addressing:

"Load the accumulator with the value 2AH."

The above instruction would be coded in memory as follows:

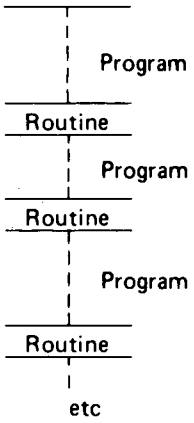


Immediate instructions do not reference memory; rather they contain data in the memory byte following the instruction code byte.

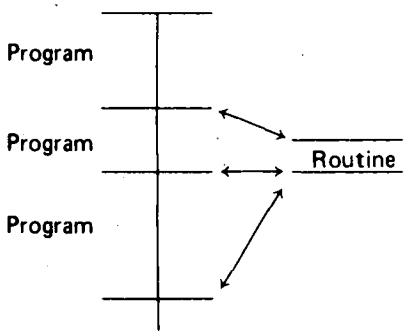
Subroutines and Use of the Stack for Addressing

Before understanding the purpose or effectiveness of the stack, it is necessary to understand the concept of a subroutine.

Consider a frequently used operation such as multiplication. The 8080 provides instructions to add one byte of data to another byte of data, but what if you wish to multiply these numbers? This will require a number of instructions to be executed in sequence. It is quite possible that this routine may be required many times within one program; to repeat the identical code every time it is needed is possible, but very wasteful of memory:

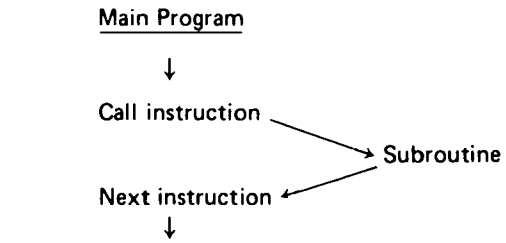


A more efficient means of accessing the routine would be to store it once, and find a way of accessing it when needed:



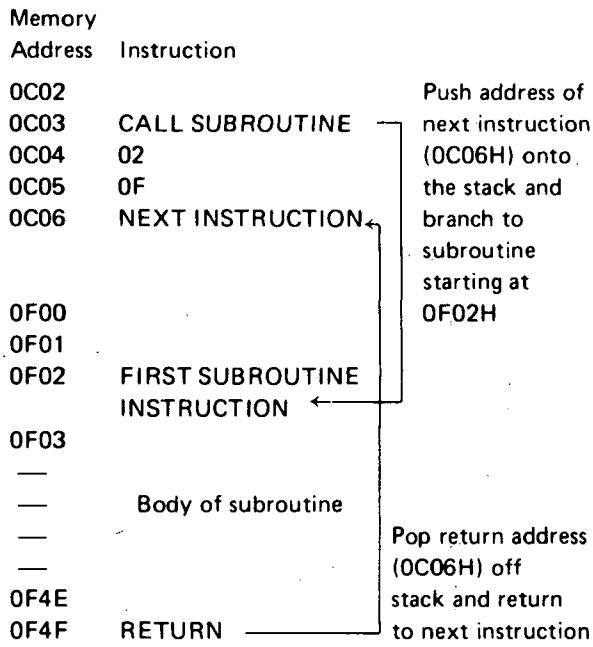
A frequently accessed routine such as the above is called a subroutine, and the 8080 provides instructions that call and return from subroutines.

When a subroutine is executed, the sequence of events may be depicted as follows:



The arrows indicate the execution sequence.

When the "Call" instruction is executed, the address of the "next" instruction (that is, the address held in the program counter), is pushed onto the stack, and the subroutine is executed. The last executed instruction of a subroutine will usually be a "Return Instruction," which pops an address off the stack into the program counter, and thus causes program execution to continue at the "Next" instruction as illustrated below:



Subroutines may be nested up to any depth limited only by the amount of memory available for the stack. For example, the first subroutine could itself call some other subroutine and so on. An examination of the sequence of stack pushes and pops will show that the return path will always be identical to the call path, even if the same subroutine is called at more than one level.

CONDITION BITS

Five condition (or status) bits are provided by the 8080 to reflect the results of data operations. All but one of these bits (the auxiliary carry bit) may be tested by program instructions which affect subsequent program execution. The descriptions of individual instructions in Chapter 2 specify which condition bits are affected by the execution of the instruction, and whether the execution of the instruction is dependent in any way on prior status of condition bits.

In the following discussion of condition bits, "setting" a bit causes its value to be 1, while "resetting" a bit causes its value to be 0.

Carry Bit

The Carry bit is set and reset by certain data operations, and its status can be directly tested by a program. The operations which affect the Carry bit are addition, subtraction, rotate, and logical operations. For example, addition of two one-byte numbers can produce a carry out of the high-order bit:

Bit No.	7	6	5	4	3	2	1	0
AE=	1	0	1	0	1	1	1	0
+74=	0	1	1	1	0	1	0	0
122	0	0	1	0	0	0	1	0

↳ carry-out = 1, sets Carry Bit = 1

An addition operation that results in a carry out of the high-order bit will set the Carry bit; an addition operation that could have resulted in a carry out but did not will reset the Carry bit.

NOTE: Addition, subtraction, rotate, and logical operations follow different rules for setting and resetting the Carry bit. See Chapter 2 under Two's Complement Representation and the individual instruction descriptions in Chapter 2 for details. The 8080 instructions which use the addition operation are ADD, ADC, ADI, ACI, and DAD. The instructions which use the subtraction operation are SUB, SBB, SUI, SBI, CMP, and CPI. Rotate operations are RAL, RAR, RLC, and RRC. Logical operations are ANA, ORA, XRA, ANI, ORI, and XRI.

Auxiliary Carry Bit

The Auxiliary Carry bit indicates carry out of bit 3. The state of the Auxiliary Carry bit cannot be directly tested by a program instruction and is present only to enable one instruction (DAA, described in Chapter 2) to perform its function. The following addition will reset the Carry bit and set the Auxiliary Carry bit:

Bit No.	7	6	5	4	3	2	1	0
2E=	0	0	1	0	1	1	1	0
+ 74=	0	1	1	1	0	1	0	0
A2	1	0	1	0	0	0	1	0

Carry=0 → Auxiliary Carry=1

The Auxiliary Carry bit will be affected by all addition, subtraction, increment, decrement, and compare instructions.

Sign Bit

As described in Chapter 2 under Two's Complement Representation, it is possible to treat a byte of data as having the numerical range -128_{10} to $+127_{10}$. In this case, by convention, the 7 bit will always represent the sign of the number; that is, if the 7 bit is 1, the number is in the range -128_{10} to -1. If bit 7 is 0, the number is in the range 0 to $+127_{10}$.

At the conclusion of certain instructions (as specified in the instruction description sections of Chapter 2), the Sign bit will be set to the condition of the most significant bit of the answer (bit 7).

Zero Bit

This condition bit is set if the result generated by the execution of certain instructions is zero. The Zero bit is reset if the result is not zero.

A result that has a carry but a zero answer byte, as illustrated below, will also set the Zero bit:

Bit No.	7	6	5	4	3	2	1	0
	1	0	1	0	0	1	1	1
+	0	1	0	1	1	0	0	1
[1]	0	0	0	0	0	0	0	0

Carry out of bit 7.

Zero answer

Zero bit set to 1.

Parity Bit

Byte "parity" is checked after certain operations. The number of 1 bits in a byte are counted, and if the total is odd, "odd" parity is flagged; if the total is even, "even" parity is flagged.

The Parity bit is set to 1 for even parity, and is reset to 0 for odd parity.

CHAPTER 2
THE 8080 INSTRUCTION SET

This section describes the 8080 assembly language instruction set.

For the reader who understands assembly language programming, Appendix A provides a complete summary of the 8080 instructions.

For the reader who is not completely familiar with assembly language, Chapter 2 describes individual instructions with examples and machine code equivalents.

ASSEMBLY LANGUAGE

How Assembly Language is Used

Upon examining the contents of computer memory, a program would appear as a sequence of hexadecimal digits, which are interpreted by the CPU as instruction codes, addresses, or data. It is possible to write a program as a sequence of digits (just as they appear in memory), but that is slow and expensive. For example, many instructions reference memory to address either a data byte or another instruction:

Hexadecimal Memory Address	
1432	7E
1433	C3
1434	C4
1435	14
1436	
•	
•	
14C3	FF
14C4	2E
14C5	36
14C6	77

Assuming that registers H and L contain 14H and C3H respectively, the program operates as follows:

Byte 1432 specifies that the accumulator is to be loaded with the contents of byte 14C3.

Bytes 1433 through 1435 specify that execution is to continue with the instruction starting at byte 14C4.

Bytes 14C4 and 14C5 specify that the L register is to be loaded with the number 36H.

Byte 14C6 specifies that the contents of the accumulator are to be stored in byte 1436.

Now suppose that an error discovered in the program logic necessitates placing an extra instruction after byte 1432. Program code would have to change as follows:

Hexadecimal Memory Address	Old Code	New Code
1432	7E	7E
1433	C3	New Instruction
1434	C4	C3
1435	14	C5
1436	•	14
1437	•	•
14C3	FF	•
14C4	2E	FF
14C5	36	2E
14C6	77	37
14C7		77

Most instructions have been moved and as a result many must be changed to reflect the new memory addresses of instructions or data. The potential for making mistakes is very high and is aggravated by the complete unreadability of the program.

Writing programs in assembly language is the first and most significant step towards economical programming; it

provides a readable notation for instructions, and separates the programmer from a need to know or specify absolute memory addresses.

Assembly language programs are written as a sequence of instructions which are converted to executable hexadecimal code by a special program called an ASSEMBLER. Use of the 8080 assembler is described in its operator's manual.

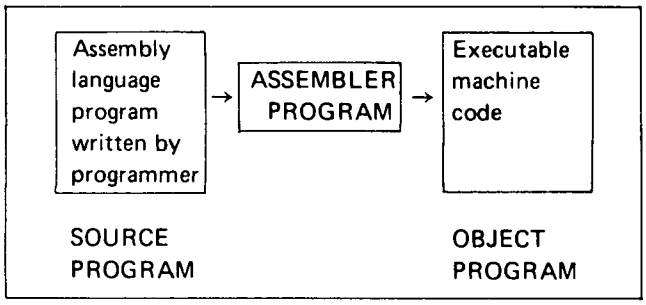


Figure 2-1. Assembler Program Converts Assembly Language Source Program to Object Program

As illustrated in Figure 2-1, the assembly language program generated by a programmer is called a SOURCE PROGRAM. The assembler converts the SOURCE PROGRAM into an equivalent OBJECT PROGRAM, which consists of a sequence of binary codes that can be loaded into memory and executed.

For example:

```
                                          One Possible
                                          Version of the
Source Program                            Object Program

NOW: MOV   A,B                               78
     CPI   'C'    → is converted  →          FE43
     JZ    LER      by the                   CA7C3D
      :             Assembler                 :
                    to
LER: MOV   M,A                               77
```

NOTE: In this and subsequent examples, it is not necessary to understand the operations of the individual instructions. They are presented only to illustrate typical assembly language statements. Individual instructions are described later in this chapter.

Now if a new instruction must be added, only one change is required. Even the reader who is not yet familiar with assembly language will see how simple the addition is:

```
NOW:        MOV         A,B
        (New instruction inserted here) -
            CPI         'C'
            JZ          LER

LER         MOV         M,A
```

The assembler takes care of the fact that a new instruction will shift the rest of the program in memory.

Statement Syntax

Assembly language instructions must adhere to a fixed set of rules as described in this section. An instruction has four separate and distinct parts or fields.

Field 1 is the LABEL field. It is a name used to reference the instruction's address.

Field 2 is the CODE field. It specifies the operation that is to be performed.

Field 3 is the OPERAND field. It provides any address or data information needed by the CODE field.

Field 4 is the COMMENT field. It is present for the programmer's convenience and is ignored by the assembler. The programmer uses comment fields to describe the operation and thus make the program more readable.

The assembler uses free fields; that is, any number of blanks may separate fields.

Before describing each field in detail, here are some general examples:

```
Label     Code    Operand
HERE:     MVI     C,O     ; Load the C register with 0
THERE:    DB      3AH     ; Create a one-byte data
                          ; constant
LOOP:     ADD     E       ; Add contents of E register
                            to the accumulator
          RLC             ; Rotate the accumulator left
```

NOTE: These examples and the ones which follow are intended to illustrate how the various fields appear in complete assembly language statements. It is not necessary at this point to understand the operations which the statements perform.

Label Field

This is an optional field, which, if present, may be from 1 to 5 characters long. The first character of the label must be a letter of the alphabet or one of the special characters @ (at sign) or ? (question mark). A colon (:) must follow the last character. (The operation codes, pseudo-instruction names, and register names are specially defined within the assembler and may not be used as labels. Operation codes and pseudo-instructions are given later in this chapter and Appendix A.

Here are some examples of valid label fields:

```
LABEL:
F14F:
@HERE:
?ZERO:
```

Here are some invalid label fields:

123:	begins with a decimal digit
LABEL	is not followed by a colon
ADD:	is an operation code
END:	is a pseudo-instruction

The following label has more than five characters; only the first five will be recognized:

INSTRUCTION: will be read as INSTR:

Since labels serve as instruction addresses, they cannot be duplicated. For example, the sequence:

```
HERE:    JMP     THERE
         ---
         ---
THERE:   MOV     C,D
         ---
         ---
THERE:   CALL    SUB
```

is ambiguous; the assembler cannot determine which address is to be referenced by the JMP instruction.

One instruction may have more than one label, however. The following sequence is valid:

```
LOOP1:                      ; First label
LOOP2:   MOV     C,D        ; Second label
         ---
         JMP     LOOP1
         ---
         JMP     LOOP2
```

Each JMP instruction will cause program control to be transferred to the same MOV instruction.

Code Field

This field contains a code which identifies the machine operation (add, subtract, jump, etc.) to be performed: hence the term operation code or op code. The instructions described later in this chapter are each identified by a mnemonic label which must appear in the code field. For example, since the "jump" instruction is identified by the letters "JMP," these letters must appear in the code field to identify the instruction as "jump."

There must be at least one space following the code field. Thus,

```
HERE:    JMP     THERE
```

is legal, but:

```
HERE:    JMPTHERE
```

is illegal.

Operand Field

This field contains information used in conjunction with the code field to define precisely the operation to be performed by the instruction. Depending upon the code field, the operand field may be absent or may consist of one item or two items separated by a comma.

There are four types of information [(a) through (d) below] that may be requested as items of an operand field, and the information may be specified in nine ways [(1) through (9) below], as summarized in the following table, and described in detail in the subsequent examples.

OPERAND FIELD INFORMATION

Information required	Ways of specifying
(a) Register	(1) Hexadecimal Data
(b) Register Pair	(2) Decimal Data
(c) Immediate Data	(3) Octal Data
(d) 16-bit Memory Address	(4) Binary Data
	(5) Location Counter ($)
	(6) ASCII Constant
	(7) Labels assigned values
	(8) Labels of instructions
	(9) Expressions

The nine ways of specifying information are as follows:

(1) Hexadecimal data. Each hexadecimal number must be followed by a letter 'H' and *must* begin with a numeric digit (0-9),

Example:

```
Label    Code   Operand    Comment
HERE:    MVI    C,0BAH     ; Load register C with the
                           ; hexadecimal number BA
```

(2) Decimal data. Each decimal number may optionally be followed by the letter 'D,' or may stand alone.

Example:

```
Label    Code   Operand    Comment
ABC:     MVI    E,105      ; Load register E with 105
```

(3) Octal data. Each octal number must be followed by one of the letters 'O' or 'Q.'

Example:

```
Label    Code   Operand    Comment
LABEL:   MVI    A,720      ; Load the accumulator with
                           ; the octal number 72
```

(4) Binary data. Each binary number must be followed by the letter 'B.'

Example:

```
Label   Code   Operand              Comment
NOW:    MVI    10B,11110110B  ; Load register two
                              ; (the D register) with
                              ; 0F6H
JUMP:   JMP    0010111011111010B  ; Jump to
                                  ; memory
                                  ; address 2EFA
```

(5) The current location counter. This is specified as the character '$' and is equal to the address of the current instruction.

Example:

```
Label   Code   Operand
GO:     JMP    $+6
```

The instruction above causes program control to be transferred to the address 6 bytes beyond the first byte of the current instruction.

(6) An ASCII constant. This is one or more ASCII characters enclosed in single quotes. Two successive single quotes must be used to represent one single quote within an ASCII constant. Appendix C contains a list of legal ASCII characters and their hexadecimal representations.

Example:

```
Label   Code   Operand   Comment
CHAR:   MVI    E,'*'     ; Load the E register with the
                         ; eight-bit ASCII representa-
                         ; tion of an asterisk
```

(7) Labels that have been assigned a numeric value by the assembler. The following assignments are built into the assembler and are therefore always active:

B	assigned to	0	representing	register B
C	"	1	"	" C
D	"	2	"	" D
E	"	3	"	" E
H	"	4	"	" H
L	"	5	"	" L
M	"	6	"	a memory reference
A	"	7	"	register A

Example:

Suppose VALUE has been equated to the hexadecimal number 9FH. Then the following instructions all load the D register with 9FH:

```
Label   Code   Operand
A1:     MVI    D,VALUE
A2:     MVI    2,9FH
A3:     MVI    2,VALUE
```

(8) Labels that appear in the label field of another instruction.

Example:

```
Label   Code   Operand   Comment
HERE:   JMP    THERE     ; Jump to instruction
                         ; at THERE
        ---
        ---
THERE:  MVI    D,9FH
```

(9) Arithmetic and logical expressions involving data types (1) to (8) above connected by the arithmetic operators (+) (addition), - (unary minus and subtraction), * (multiplication), / (division), MOD (modulo), the logical operators NOT, AND, OR, XOR, SHR (shift right), SHL (shift left), and left and right parentheses.

All operators treat their arguments as 16-bit unsigned quantities, and generate 16-bit quantities as their result.

The operator + produces the arithmetic sum of its operands.

The operator - produces the arithmetic difference of its operands when used as subtraction, or the arithmetic negative of its operand when used as unary minus.

The operator * produces the arithmetic product of its operands.

The operator / produces the arithmetic integer quotient of its operands, discarding any remainder.

The operator MOD produces the integer remainder obtained by dividing the first operand by the second.

The operator NOT complements each bit of its operand.

The operator AND produces the bit-by-bit logical AND of its operands.

The operator OR produces the bit-by-bit logical OR of its operands.

The operator XOR produces the bit-by-bit logical EXCLUSIVE-OR of its operands.

The SHR and SHL operators are linear shifts which shift their first operands right or left, respectively, by the number of bit positions specified by their second operands. Zeros are shifted into the high-order or low-order bits, respectively, of their first operands.

The programmer must insure that the result generated by any operation fits the requirements of the operation being coded. For example, the second operand of an MVI

instruction must be an 8-bit value.

Therefore the instruction:

```
MVI H,NOT 0
```

is invalid, since NOT 0 produces the 16-bit hexadecimal number FFFF. However, the instruction:

```
MVI H,NOT 0 AND 0FFH
```

is valid, since the most significant 8 bits of the result are insured to be 0, and the result can therefore be represented in 8 bits.

NOTE: An instruction in parentheses is a legal expression in an operand field. Its value is the leftmost byte of the encoding of the instruction. The same syntax rules for instructions apply when the instructions are parenthesized.

Examples:

Label	Code	Operand	Arbitrary Memory Address
HERE:	MVI	C, HERE SHR 8	2E1A

The above instruction loads the hexadecimal number 2EH (16-bit address of HERE shifted right 8 bits) into the C register.

Label	Code	Operand
NEXT:	MVI	D, 34+4 0H/2

The above instruction will load the value 34+ (64/2) = 34+32 = 66 into the D register.

Label	Code	Operand
INS:	DB	(ADD C)

The above instruction defines a byte of value 81H (the encoding of an ADD C instruction) at location INS.

Operators cause expressions to be evaluated in the following order:

1. Parenthesized expressions
2. *,/MOD, SHL, SHR
3. +, - (unary and binary)
4. NOT
5. AND
6. OR, XOR

In the case of parenthesized expressions, the most deeply parenthesized expressions are evaluated first:

Example:

The instruction:

```
MVI     D, (34+40H)/2
```

will load the value (34+64)/2=49 into the D register.

The operators MOD, SHL, SHR, NOT, AND, OR, and XOR must be separated from their operands by at least one blank. Thus the instruction:

```
MVI     C, VALUE ANDOFH
```

is invalid.

Using some or all of the above nine data specifications, the following four types of information may be requested:

(a) A register (or code indicating memory reference) to serve as the source or destination in a data operation—methods 1, 2, 3, 4, 7, or 9 may be used to specify the register or memory reference, but the specifications must finally evaluate to one of the numbers 0-7 as follows:

Value	Register
0	B
1	C
2	D
3	E
4	H
5	L
6	Memory Reference
7	A (accumulator)

Example:

Label	Code	Operand
INS1:	MVI	REG4, 2EH
INS2:	MVI	4H, 2EH
INS3:	MVI	8/2, 2EH

Assuming REG4 has been equated to 4, all the above instructions will load the value 2EH into register 4 (the H register).

(b) A register pair to serve as the source or destination in a data operation. Register pairs are specified as follows:

Specification	Register Pair
B	Registers B and C
D	Registers D and E
H	Registers H and L
PSW	Two bytes containing Register A and the state of the condition bits
SP	The 16-bit stack pointer register

NOTE: The binary value representing each register pair varies from instruction to instruction. Therefore, the programmer should always specify a register pair by its alphabetic designation.

Example:

```
Label   Code    Operand     Comment
        PUSH    D           ; Push registers D and
                            ; E onto stack
        INX     SP          ; Increment 16-bit
                            ; number in the stack
                            ; pointer
```

(c) Immediate data, to be used directly as a data item.

Example:

```
Label   Code    Operand     Comment
HERE:   MVI     H, DATA     ; Load the H register with
                            ; the value of DATA
```

Here are some examples of the form DATA could take:

ADDR AND 0FFH (where ADDR is a 16-bit address)
127
'*'
VALUE (where VALUE has been equated to a number)
3EH=10/2 (2 AND 2)

(d) A 16-bit address, or the label of another instruction in memory.

Example:

```
Label   Code    Operand     Comment
HERE:   JMP     THERE       ; Jump to the instruction
                            ; at THERE
        JMP     2EADH       ; Jump to address 2EAD
```

Comment Field

The only rule governing this field is that it must begin with a semicolon (;).

```
HERE:   MVI   C, 0ADH   ; This is a comment
```

A comment field may appear alone on a line:

```
;
; Begin loop here
;
```

TWO'S COMPLEMENT REPRESENTATION OF DATA

This section describes ways in which data can be specified in and interpreted by a program. Any 8-bit byte contains one of the 256 possible combinations of zeros and ones. Any particular combination may be interpreted in various ways. For instance, the code 1FH may be interpreted as a machine instruction (Rotate Accumulator Right Through Carry), as a hexadecimal value 1FH=31D, or merely as the bit pattern 00011111.

Arithmetic operations performed by the assembler and hardware are done on a modular basis. That is, arithmetic performed on 1-byte quantities is done modulo 256 and arithmetic performed on 2-byte quantities is done modulo 65,536. Neither run-time arithmetic (performed by the 8080 hardware instructions) nor assembly-time arithmetic generates overflow indications.

Arithmetic instructions assume that the data bytes upon which they operate are in a special format called "two's complement," and the operations performed on these bytes are called "two's complement arithmetic."

Using two's complement notation for binary numbers, any subtraction operation becomes a sequence of bit complementations and additions. Therefore, fewer circuits need be built to perform subtraction.

When a byte is interpreted as a signed two's complement number, the low-order 7 bits supply the magnitude of the number, while the high-order bit is interpreted as the sign of the number (0 for positive numbers, 1 for negative).

The range of positive numbers that can be represented in signed two's complement notation is, therefore, from 0 to 127:

0 = 00000000B = 0H
1 = 00000001B = 1H
.
.
.
126D = 01111110B = 7EH
127D = 01111111B = 7FH

To change the sign of a number represented in two's complement, the following rules are applied:

(a) Complement each bit of the number (producing the so-called one's complement.

(b) Add one to the result, ignoring any carry out of the high-order bit position.

Example: Produce the two's complement representation of -10D. Following the rules above:

+10D = 00001010B

Complement each bit : 11110101B
Add one : 11110110B

Therefore, the two's complement representation of -10D is F6H. (Note that the sign bit is set, indicating a negative number).

Example: What is the value of 86H interpreted as a signed two's complement number? The high-order bit is set, indicating that this is a negative number. To obtain its value, again complement each bit and add one.

86H = 1 0 0 0 0 1 1 0 B

Complement each bit : 0 1 1 1 1 0 0 1 B
Add one : 0 1 1 1 1 0 1 0 B

Thus, the value of 86H is -7AH = -122D

The range of negative numbers that can be represented in signed two's complement notation is from -1 to -128.

-1 = 1 1 1 1 1 1 1 1 B = FFH
-2 = 1 1 1 1 1 1 1 0 B = FEH
•
•
•
-127D = 1 0 0 0 0 0 0 1 B = 81H
-128D = 1 0 0 0 0 0 0 0 B = 80H

To perform the subtraction 1AH-0CH, the following operations are performed:

Take the two's complement of 0CH=F4H

Add the result to the minuend:

1AH = 0 0 0 1 1 0 1 0
+(-0CH) = F4H = 1 1 1 1 0 1 0 0
0 0 0 0 1 1 1 0 = 0EH the correct answer

When a byte is interpreted as an unsigned two's complement number, its value is considered positive and in the range 0 to 255_{10}:

0 = 0 0 0 0 0 0 0 0 B = 0H
1 = 0 0 0 0 0 0 0 1 B = 1H
•
•
127D = 0 1 1 1 1 1 1 1 B = 7FH
128D = 1 0 0 0 0 0 0 0 B = 80H
•
•
255D = 1 1 1 1 1 1 1 1 B = FFH

Two's complement arithmetic is still valid. When performing an addition operation, the Carry bit is set when the result is greater than 255D. When performing subtraction, the Carry bit is reset when the result is positive. If the Carry bit is set, the result is negative and present in its two's complement form. *Thus, the Carry bit when set indicates the occurrence of a "borrow."*

Example: Subtract 98D from 197D using unsigned two's complement arithmetic.

197D = 1 1 0 0 0 1 0 1 = C5H
-98D = 1 0 0 1 1 1 1 0 = 9EH
carry out → 1 0 1 1 0 0 0 1 1 = 63H = 99D

Since the carry out of bit 7 = 1, indicating that the answer is correct and positive, the subtract operation will reset the Carry bit to 0.

Example: Subtract 15D from 12D using unsigned two's complement arithmetic.

12D = 0 0 0 0 1 1 0 0 = 0CH
-15D = 1 1 1 1 0 0 0 1 = 0F1H
carry out → 0 1 1 1 1 1 1 0 1 = -3D

Since the carry out of bit 7 = 0, indicating that the answer is negative and in its two's complement form, the subtract operation will set the Carry bit indicating that a "borrow" occurred.

NOTE: The 8080 instructions which perform the subtraction operation are SUB, SUI, SBB, SBI, CMP, and CMI. Although the same result will be obtained by addition of a complemented number or subtraction of an uncomplemented number, the resulting Carry bit will be different.

EXAMPLE: If the result -3 is produced by performing an "ADD" operation on the numbers +12D and -15D, the Carry bit will be reset; if the same result is produced by performing a "SUB" operation on the numbers +12D and +15D, the Carry bit will be set. Both operations indicate that the result is negative; the programmer must be aware which operations set or reset the Carry bit.

"ADD" +12D and -15D

+12D = 0 0 0 0 1 1 0 0
+(-15D) = 1 1 1 1 0 0 0 1
0 1 1 1 1 1 1 0 1 = -3D
causes carry to be reset

"SUB" +15D from +12D

+12D = 0 0 0 0 1 1 0 0
-(+15D) = 1 1 1 1 0 0 0 1
0 1 1 1 1 1 1 0 1 = -3D
causes carry to be set

All assembly-time arithmetic is performed assuming unsigned 16-bit operands (that is, signed arithmetic is not implemented). In a user's assembly-language program, the program logic may be written to interpret numbers as either signed or unsigned quantities depending on the application.

DATA STATEMENTS

The operands of data statements that reserve a variable number of bytes (DB and DS) must be defined before the data statement is encountered. These operands may not make forward references.

DB Define Byte(s) of Data

Label	Code	Operand
oplab:	DB	list

"list" is a list of either:

(1) Arithmetic and logical expressions involving any of the arithmetic and logical operators, which evaluate to eight-bit data quantities

(2) Strings of ASCII characters enclosed in quotes

Description: The eight-bit value of each expression, or the eight-bit ASCII representation of each character is stored in the next available byte of memory starting with the byte addressed by "oplab." (The most significant bit of each ASCII character is always = 0).

Example:

Instruction			Assembled Data (hex)
HERE:	DB	0A3H	A3
WORD1:	DB	5*2, 2FH-0AH	0A25
WORD2:	DB	5ABCH SHR 8	5A
STR:	DB	'STRINGSpl'	535452494E472031
MINUS:	DB	-03H	FD

NOTE: In the first example above, the hexadecimal value A3 must be written as 0A3 since hexadecimal numbers must start with a decimal digit.

DW Define Word (Two Bytes) of Data

Format:

Label	Code	Operand
oplab:	DW	list

"list" is a list of expressions which evaluate to 16 bit data quantities.

Description: The least significant 8 bits of the expression are stored in the lower address memory byte (oplab), and the most significant 8 bits are stored in the next higher addressed byte (oplab +1). This reverse order of the high and low address bytes is normally the case when storing addresses in memory. This statement is usually used to create address constants for the transfer-of-control instructions; thus LIST is usually a list of one or more statement labels appearing elsewhere in the program.

Examples:

Assume COMP addresses memory location 3B1CH and FILL addresses memory location 3EB4H.

Instruction			Assembled Data (hex)
ADD1:	DW	COMP	1C3B
ADD2:	DW	FILL	B43E
ADD3:	DW	3C01H, 3CAEH	013CAE3C

Note that in each case, the data are stored with the least significant 8 bits first.

DS Define Storage (Bytes)

Format:

Label	Code	Operand
oplab:	DS	exp

"exp" is a single arithmetic or logical expression that can be evaluated at assembly time. Its value can range from 0H to 0FFFFH.

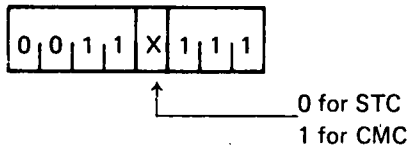
Description: The value of EXP specifies the number of memory bytes to be reserved for data storage. No data values are assembled into these bytes: in particular the programmer should not assume that they will be zero, or any other value. The next instruction will be assembled at memory location oplab+EXP (oplab+10 or oplab+16 in the example below).

Examples:

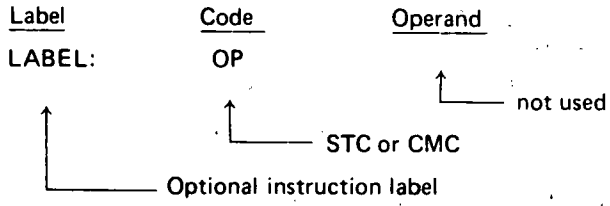
```
HERE:   DS    10    ; Reserve the next 10 bytes
        DS    10H   ; Reserve the next 16 bytes
```

CARRY BIT INSTRUCTIONS

This section describes the instructions which operate directly upon the Carry bit. Instructions in this class occupy one byte as follows:



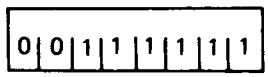
The general assembly language format is:



CMC Complement Carry

Format:

Label	Code	Operand
oplab:	CMC	—



Description: If the Carry bit = 0, it is set to 1. If the Carry bit = 1, it is reset to 0.

Condition bits affected: Carry

STC Set Carry

Format:

Label	Code	Operand
oplab:	STC	—

Description: The Carry bit is set to one.

Condition bits affected: Carry

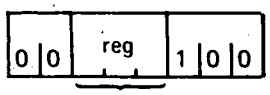
SINGLE REGISTER INSTRUCTIONS

This section describes instructions which operate on a single register or memory location. If a memory reference is specified, the memory byte addressed by the H and L registers is operated upon. The H register holds the most significant 8 bits of the address while the L register holds the least significant 8 bits of the address.

INR Increment Register or Memory

Format:

Label	Code	Operand
oplab:	INR	reg



B,C,D,E,H,L,M or A

000 for register B
001 for register C
010 for register D
011 for register E
100 for register H
101 for register L
110 for memory ref. M
111 for register A

Description: The specified register or memory byte is incremented by one.

Condition bits affected: Zero, Sign, Parity, Auxiliary Carry (Carry *not* affected)

Example:

If register C contains 99H, the instruction:

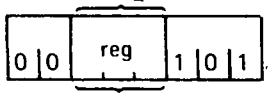
INR C

will cause register C to contain 9AH

DCR Decrement Register or Memory

Format:

Label	Code	Operand
oplab:	DCR	reg



B,C,D,E,H,L,M or A

000 for Register B
001 for register C
010 for register D
011 for register E
100 for register H
101 for register L
110 for memory ref. M
111 for register A

Description: The specified register or memory byte is decremented by one.

Condition bits affected: Zero, Sign, Parity, Auxiliary Carry (Carry *not* affected)

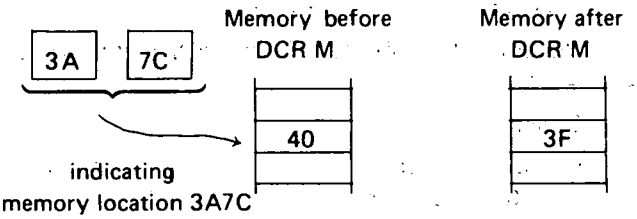
Example:

If the H register contains 3AH, the L register contains 7CH, and memory location 3A7CH contains 40H, the instruction:

DCR M

will cause memory location 3A7CH to contain 3FH. To illustrate:

DCR M references registers H and L

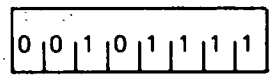


indicating memory location 3A7C

CMA Complement Accumulator

Format:

Label	Code	Operand
oplab:	CMA	—



Description: Each bit of the contents of the accumulator is complemented (producing the one's complement).

Condition bits affected: None

Example:

If the accumulator contains 51H, the instruction CMA will cause the accumulator to contain 0AEH.

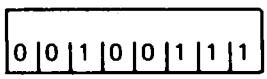
Accumulator = 0 1 0 1 0 0 0 1 = 51H

Accumulator = 1 0 1 0 1 1 1 0 = AEH

DAA Decimal Adjust Accumulator

Format:

Label	Code	Operand
oplab:	DAA	—



Description: The eight-bit hexadecimal number in the accumulator is adjusted to form two four-bit binary-coded-decimal digits by the following two step process:

(1) If the least significant four bits of the accumulator represents a number greater than 9, or if the Auxiliary Carry bit is equal to one, the accumulator is incremented by six. Otherwise, no incrementing occurs.

(2) If the most significant four bits of the accumulator now represent a number greater than 9, or if the normal carry bit is equal to one; the most significant four bits of the accumulator are incremented by six. Otherwise, no incrementing occurs.

If a carry out of the least significant four bits occurs during Step (1), the Auxiliary Carry bit is set; otherwise it is reset. Likewise, if a carry out of the most significant four

bits occurs during Step (2), the normal Carry bit is set; otherwise, it is unaffected:

NOTE: This instruction is used when adding decimal numbers. It is the only instruction whose operation is affected by the Auxiliary Carry bit.

Condition bits affected: Zero, Sign, Parity, Carry, Auxiliary Carry

Example:

Suppose the accumulator contains 9BH, and both carry bits = 0. The DAA instruction will operate as follows:

(1) Since bits 0-3 are greater than 9, add 6 to the accumulator. This addition will generate a carry out of the lower four bits, setting the Auxiliary Carry bit.

```
Bit No.          7 6 5 4 3 2 1 0
Accumulator = 1 0 0 1   1 0 1 1 = 9BH
  +6        =  _____   0 1 1 0
               1 0 1 0   0 0 0 1 = A1H
                         ↘
                          Auxiliary Carry = 1
```

(2) Since bits 4-7 now are greater than 9, add 6 to these bits. This addition will generate a carry out of the upper four bits, setting the Carry bit.

```
Bit No.          7 6 5 4 3 2 1 0
Accumulator = 1 0 1 0 0 0 0 1 = A1H
        +6 =  0 1 1 0
          1   0 0 0 0 0 0 0 1
          ↳ Carry = 1
```

Thus, the accumulator will now contain 1, and both Carry bits will be = 1.

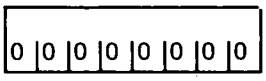
For an example of decimal addition using the DAA instruction, see Chapter 4.

NOP INSTRUCTION

The NOP instruction occupies one byte.

Format:

Label	Code	Operand
oplab	NOP	—



Description: No operation occurs. Execution proceeds with the next sequential instruction.

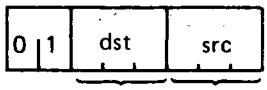
Condition bits affected: None

DATA TRANSFER INSTRUCTIONS

This section describes instructions which transfer data between registers or between memory and registers.

Instructions in this class occupy one byte as follows:

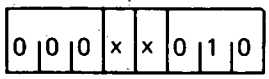
(a) For the MOV instruction:



000 for register B
001 for register C
010 for register D
011 for register E
100 for register H
101 for register L
110 for memory reference M
111 for register A

NOTE: dst and src cannot both = 110B

(b) For the remaining instructions:

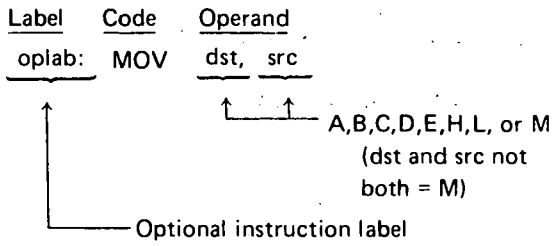


0 for register pair B
1 for register pair D

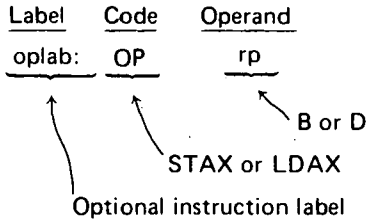
0 for STAX
1 for LDAX

When a memory reference is specified in the MOV instruction, the addressed location is specified by the H and L registers. The L register holds the least significant 8 bits of the address; the H register holds the most significant 8 bits.

The general assembly language format is:

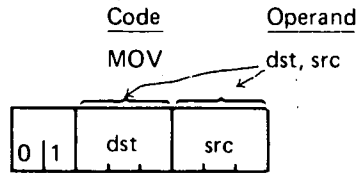


— or —



MOV Move Instruction

Format:



Description: One byte of data is moved from the register specified by src (the source register) to the register specified by dst (the destination register). The data replaces the contents of the destination register; the source remains unchanged.

Condition bits affected: None

Example 1:

```
Label   Code   Operand      Comment
        MOV    A,E          ; Move contents of the E
                            ; register to the A register
        MOV    D,D          ; Move contents of the
                            ; D register to the D
                            ; register, i.e., this is a
                            ; null operation
```

NOTE: Any of the null operation instructions MOV X,X can also be specified as NOP (no-operation). MOV M,M is not permitted, however.

Example 2:

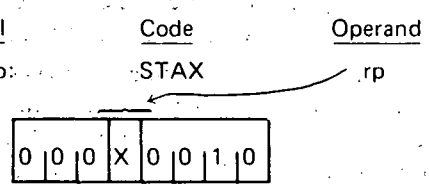
Assuming that the H register contains 2BH and the L register contains E9H, the instruction:

MOV M,A

will store the contents of the accumulator at memory location 2BE9H.

STAX Store Accumulator

Format:



Description: The contents of the accumulator are stored in the memory location addressed by registers B and C, or by registers D and E.

Condition bits affected: None

Example:

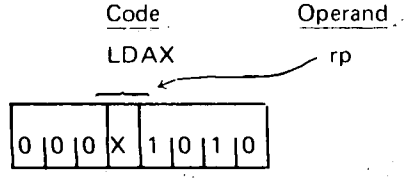
If register B contains 3FH and register C contains 16H, the instruction:

STAX B

will store the contents of the accumulator at memory location 3F16H.

LDAX Load Accumulator

Format:



Description: The contents of the memory location addressed by registers B and C, or by registers D and E, replace the contents of the accumulator.

Condition bits affected: None

Example:

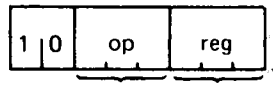
If register D contains 93H and register E contains 8BH, the instruction:

LDAX D

will load the accumulator from memory location 938BH.

REGISTER OR MEMORY TO ACCUMULATOR INSTRUCTIONS

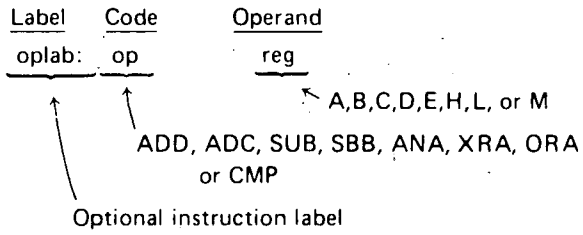
This section describes the instructions which operate on the accumulator using a byte fetched from another register or memory. Instructions in this class occupy one byte as follows:



000 for ADD	000 for register B
001 for ADC	001 for register C
010 for SUB	010 for register D
011 for SBB	011 for register E
100 for ANA	100 for register H
101 for XRA	101 for register L
110 for ORA	110 for memory reference M
111 for CMP	111 for register A

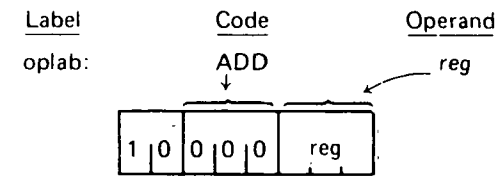
Instructions in this class operate on the accumulator using the byte in the register specified by REG. If a memory reference is specified, the instructions use the byte in the memory location addressed by registers H and L. The H register holds the most significant 8 bits of the address, while the L register holds the least significant 8 bits of the address. The specified byte will remain unchanged by any of the instructions in this class; the result will replace the contents of the accumulator.

The general assembly language instruction format is:



ADD Add Register or Memory to Accumulator

Format:



Description: The specified byte is added to the contents of the accumulator using two's complement arithmetic.

Condition bits affected: Carry, Sign, Zero, Parity, Auxiliary Carry

Example 1:

Assume that the D register contains 2EH and the accumulator contains 6CH. Then the instruction:

ADD D

will perform the addition as follows:

```
2EH = 00101110
6CH = 01101100
9AH = 10011010
```

The Zero and Carry bits are reset; the Parity and Sign bits are set. Since there is a carry out of bit A_3, the Auxiliary Carry bit is set. The accumulator now contains 9AH.

Example 2:

The instruction:

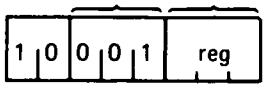
ADD A

will double the accumulator.

ADC Add Register or Memory to Accumulator With Carry

Format:

Label	Code	Operand
oplab:	ACD	reg



Description: The specified byte plus the content of the Carry bit is added to the contents of the accumulator.

Condition bits affected: Carry, Sign, Zero, Parity, Auxiliary Carry

Example:

Assume that register C contains 3DH, the accumulator contains 42H, and the Carry bit = 0. The instruction:

ADC C

will perform the addition as follows:

```
3DH = 0 0 1 1 1 1 0 1
42H = 0 1 0 0 0 0 1 0
CARRY =             0
RESULT = 0 1 1 1 1 1 1 1 = 7FH
```

The results can be summarized as follows:

Accumulator	=	7FH
Carry	=	0
Sign	=	0
Zero	=	0
Parity	=	0
Aux. Carry	=	0

If the Carry bit had been one at the beginning of the example, the following would have occurred:

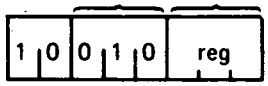
```
3DH = 0 0 1 1 1 1 0 1
42H = 0 1 0 0 0 0 1 0
CARRY =             1
RESULT = 1 0 0 0 0 0 0 0 = 80H
```

Accumulator	=	80H
Carry	=	0
Sign	=	1
Zero	=	0
Parity	=	0
Aux. Carry	=	1

SUB Subtract Register or Memory From Accumulator

Format:

Label	Code	Operand
oplab:	SUB	reg



Description: The specified byte is subtracted from the accumulator using two's complement arithmetic.

If there is *no* carry out of the high-order bit position, indicating that a borrow occurred, the Carry bit is *set*; otherwise it is reset. (Note that this differs from an add operation, which resets the carry if no overflow occurs).

Condition bits affected: Carry, Sign, Zero, Parity, Auxiliary Carry

Example:

Assume that the accumulator contains 3EH. Then the instruction:

SUB A

will subtract the accumulator from itself producing a result of zero as follows:

```
  3EH  = 0 0 1 1 1 1 1 0
+(-3EH) = 1 1 0 0 0 0 0 1 negate and add one
+                       1 to produce two's
                          complement
carry → 1 0 0 0 0 0 0 0 Result = 0
```

Since there was a carry out of the high-order bit position, and this is a subtraction operation, the Carry bit will be reset.

Since there was a carry out of bit A_3, the Auxiliary Carry bit will be set.

The Parity and Zero bits will also be set, and the Sign bit will be reset.

Thus the SUB A instruction can be used to reset the Carry bit (and zero the accumulator).

SBB Subtract Register or Memory From Accumulator With Borrow

Format:

Label	Code	Operand
oplab:	SBB	reg

Description: The Carry bit is internally added to the contents of the specified byte. This value is then subtracted from the accumulator using two's complement arithmetic.

This instruction is most useful when performing subtractions. It adjusts the result of subtracting two bytes when a previous subtraction has produced a negative result (a borrow). For an example of this, see the section on Multibyte Addition and Subtraction in Chapter 4.

Condition bits affected: Carry, Sign, Zero, Parity, Auxiliary Carry (see last section for details).

Example:

Assume that register L contains 2, the accumulator contains 4, and the Carry bit = 1. Then the instruction SBB L will act as follows:

02H + Carry = 03H
Two's Complement of 03H = 11111101

Adding this to the accumulator procedures:

Accumulator = 04H = 0 0 0 0 0 1 0 0
1 1 1 1 1 1 0 1
1 0 0 0 0 0 0 0 1 = 01H = Result

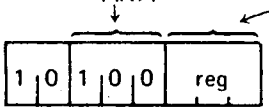
carry out = 1 causing the Carry bit to be reset

The final result stored in the accumulator is one, causing the Zero bit to be reset. The Carry bit is reset since this is a subtract operation and there was a carry out of the high-order bit position. The Auxiliary Carry bit is set since there was a carry out of bit A_3. The Parity and the Sign bits are reset.

ANA Logical And Register or Memory With Accumulator

Format:

Label	Code	Operand
oplab:	ANA	reg



Description: The specified byte is logically ANDed bit by bit with the contents of the accumulator. The Carry bit is reset to zero.

The logical AND function of two bits is 1 if and only if both the bits equal 1.

Condition bits affected: Carry, Zero, Sign, Parity, Auxiliary Carry.

Example:

Since any bit ANDed with a zero produces a zero and any bit ANDed with a one remains unchanged, the AND function is often used to zero groups of bits.

Assuming that the accumulator contains 0FCH and the C register contains 0FH, the instruction:

ANA C

will act as follows:

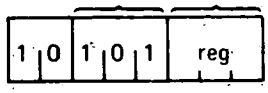
Accumulator = 1 1 1 1 1 1 0 0 = 0FCH
C Register = 0 0 0 0 1 1 1 1 = 0FH
Result in
Accumulator = 0 0 0 0 1 1 0 0 = 0CH

This particular example guarantees that the high-order four bits of the accumulator are zero, and the low-order four bits are unchanged.

XRA Logical Exclusive-Or Register or Memory With Accumulator (Zero Accumulator)

Format:

Label	Code	Operand
oplab:	XRA	reg



Description: The specified byte is EXCLUSIVE-ORed bit by bit with the contents of the accumulator. The Carry bit is reset to zero.

The EXCLUSIVE-OR function of two bits equals 1 if and only if the values of the bits are different.

Condition bits affected: Carry, Zero, Sign, Parity, Auxiliary Carry

Example 1:

Since any bit EXCLUSIVE-ORed with itself produces zero, the EXCLUSIVE-OR can be used to zero the accumulator.

Label	Code	Operand
	XRA	A
	MOV	B,A
	MOV	C,A

These instructions zero the A, B, and C registers.

Example 2:

Any bit EXCLUSIVE-ORed with a one is complemented (0 XOR 1 = 1, 1 XOR 1 = 0).

Therefore if the accumulator contains all ones (0FFH), the instruction:

XRA B

will produce the one's complement of the B register in the accumulator.

Example 3:

Testing for change of status.

Many times a byte is used to hold the status of several (up to eight) conditions within a program, each bit signifying whether a condition is true or false, enabled or disabled, etc.

The EXCLUSIVE-OR function provides a quick means of determining which bits of a word have changed from one time to another.

```
Label   Code   Operand
LA:     MOV    A,M      ; STAT2 to accumulator
        INX    H        ; Address next location
LB:     MOV    B,M      ; STAT1 to B register
CHNG:   XRA    B        ; EXCLUSIVE-OR
                        ; STAT1 and STAT2
STAT:   ANA    B        ; AND result with STAT1
STAT2:  DS     1
STAT1:  DS     1
```

Assume that logic elsewhere in the program has read the status of eight conditions and stored the corresponding string of eight zeros and ones at STAT1 and at some later time has read the same conditions and stored the new status at STAT2. Also assume that the H and L registers have been initialized to address location STAT2. The EXCLUSIVE-OR at CHNG produces a one bit in the accumulator wherever a condition has changed between STAT1 and STAT2.

For example:

```
Bit Number        7 6 5 4 3 2 1 0
STAT1 = 5CH =     0 1 0 1 1 1 0 0
STAT2 = 78H =     0 1 1 1 1 0 0 0
EXCLUSIVE-OR:     0 0 1 0 0 1 0 0
```

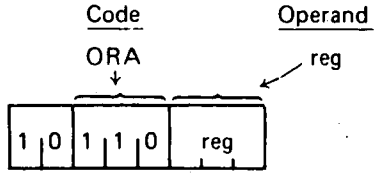
This shows that the conditions associated with bits 2 and 5 have changed between STAT1 and STAT2. Knowing this, the program can tell whether these bits were set or reset by ANDing the result with STAT1.

```
Result  = 0 0 1 0 0 1 0 0
STAT1   = 0 1 0 1 1 1 0 0
AND     = 0 0 0 0 0 1 0 0
```

Since bit 2 is now one, it was set between STAT1 and STAT2; since bit 5 is zero it is reset.

ORA Logical Or Register or Memory With Accumulator

Format:



Description: The specified byte is logically ORed bit by bit with the contents of the accumulator. The carry bit is reset to zero.

The logical OR function of two bits equals zero if and only if both the bits equal zero.

Condition bits affected: Carry, Zero, Sign, Parity, Auxiliary Carry.

Example:

Since any bit ORed with a one produces a one, and any bit ORed with a zero remains unchanged, the OR function is often used to set groups of bits to one.

Assuming that register C contains 0FH and the accumulator contains 33H, the instruction:

```
ORA C
```

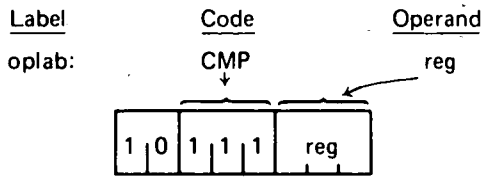
acts as follows:

```
          Accumulator = 0 0 1 1 0 0 1 1 = 33H
          C Register  = 0 0 0 0 1 1 1 1 = 0FH
Result =  Accumulator = 0 0 1 1 1 1 1 1 = 3FH
```

This particular example guarantees that the low-order four bits of the accumulator are one, and the high-order four bits are unchanged.

CMP Compare Register or Memory With Accumulator

Format:



Description: The specified byte is compared to the contents of the accumulator. The comparison is performed by internally subtracting the contents of REG from the accumulator (leaving both unchanged) and setting the condition bits according to the result. In particular, the Zero bit is set if the quantities are equal, and reset if they are unequal. Since a subtract operation is performed, the Carry bit will be set if there is no carry out of bit 7, indicating that the contents of REG are greater than the contents of the accumulator, and reset otherwise.

NOTE: If the two quantities to be compared differ in sign, the sense of the Carry bit is reversed.

Condition bits affected: Carry, Zero, Sign, Parity, Auxiliary Carry

Example 1:

Assume that the accumulator contains the number 0AH and the E register contains the number 05H. Then the instruction CMP E performs the following internal subtractions:

```
Accumulator   = 0AH = 0 0 0 0 1 0 1 0
+ (-E Register) = -5H = 1 1 1 1 1 0 1 1
                      1 0 0 0 0 0 1 0 1 = result
                      |
                      carry = 1, causing the Carry bit to be reset
```

The accumulator still contains 0AH and the E register still contains 05H; however, the Carry bit is reset and the zero bit reset, indicating E less than A.

Example 2:

If the accumulator had contained the number 2H, the internal subtraction would have produced the following:

```
Accumulator      = 02H = 00000010
+ (-E Register)  = -5H = 11111011
                  0 11111101 = result
carry = 0, Carry bit = 1
```

The Zero bit would be reset and the Carry bit set, indicating E greater than A.

Example 3:

Assume that the accumulator contains -1BH. The internal subtraction now produces the following:

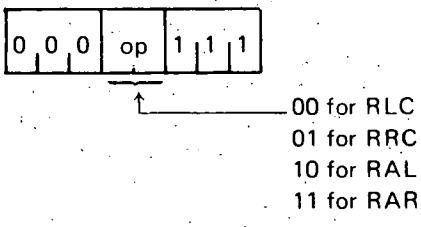
```
Accumulator      = -1BH = 11100101
+ (-E Register)  = -5H  = 11111011
                  1 11100000
carry = 1, causing carry to be reset
```

Since the two numbers to be compared differed in sign, the resetting of the Carry bit now indicates E greater than A.

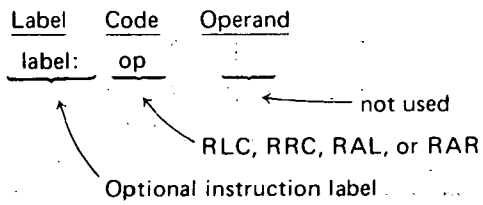
ROTATE ACCUMULATOR INSTRUCTIONS

This section describes the instructions which rotate the contents of the accumulator. No memory locations or other registers are referenced.

Instructions in this class occupy one byte as follows:

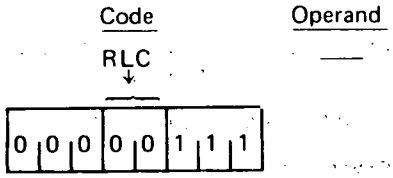


The general assembly language instruction format is:



RLC Rotate Accumulator Left

Format:



Description: The Carry bit is set equal to the high-order bit of the accumulator. The contents of the accumulator are rotated one bit position to the left, with the high-order bit being transferred to the low-order bit position of the accumulator.

Condition bits affected: Carry

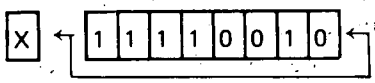
Example:

Assume that the accumulator contains 0F2H. Then the instruction:

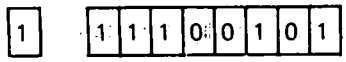
RLC

acts as follows:

Before RLC is executed: Carry Accumulator



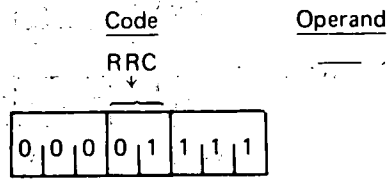
After RLC is executed:



Carry = 1 A = 0E5H

RRC Rotate Accumulator Right

Format:



Description: The carry bit is set equal to the low-order bit of the accumulator. The contents of the accumulator are rotated one bit position to the right, with the low-order bit being transferred to the high-order bit position of the accumulator.

Condition bits affected: Carry

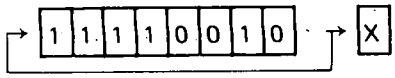
Example:

Assume that the accumulator contains 0F2H. Then the instruction:

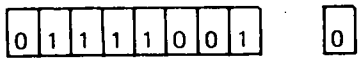
RRC

acts as follows:

Before RRC is executed: Accumulator Carry



After RRC is executed:

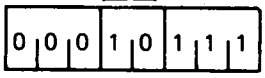


A = 79H Carry=0

RAL Rotate Accumulator Left Through Carry

Format:

Label	Code	Operand
oplab:	RAL	—



Description: The contents of the accumulator are rotated one bit position to the left.

The high-order bit of the accumulator replaces the Carry bit, while the Carry bit replaces the low-order bit of the accumulator.

Condition bits affected: Carry

Example:

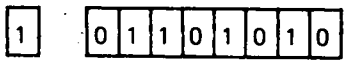
Assume that the accumulator contains 0B5H. Then the instruction:

RAL

acts as follows:

Before RAL is executed: Carry Accumulator

After RAL is executed:



Carry=1 A = 6AH

RAR Rotate Accumulator Right Through Carry

Format:

Label	Code	Operand
oplab:	RAR	—

Description: The contents of the accumulator are rotated one bit position to the right.

The low-order bit of the accumulator replaces the carry bit, while the carry bit replaces the high-order bit of the accumulator.

Condition bits affected: Carry

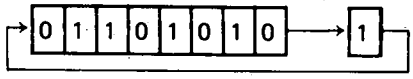
Example:

Assume that the accumulator contains 6AH. Then the instruction:

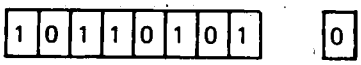
RAR

acts as follows:

Before RAR is executed: Accumulator Carry



After RAR is executed:



A = 0B5H Carry=0

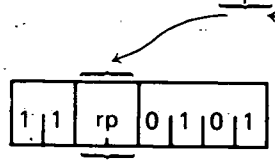
REGISTER PAIR INSTRUCTIONS

This section describes instructions which operate on pairs of registers.

PUSH Push Data Onto Stack

Format:

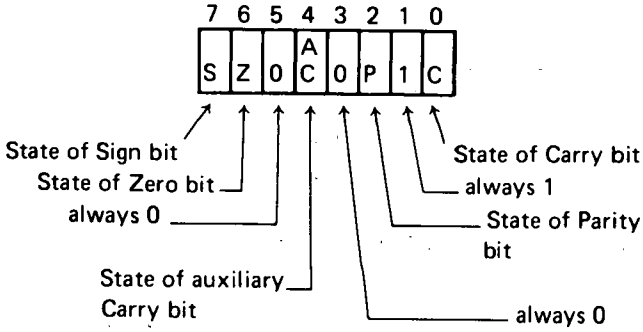
Label	Code	Operand
oplab:	PUSH	rp



00 for registers B and C
01 for registers D and E
10 for registers H and L
11 for register A and flags

Description: The contents of the specified register pair are saved in two bytes of memory indicated by the stack pointer SP.

The contents of the first register are saved at the memory address one less than the address indicated by the stack pointer; the contents of the second register are saved at the address two less than the address indicated by the stack pointer. If register pair PSW is specified, the first byte of information saved holds the contents of the A register; the second byte holds the settings of the five condition bits, i.e., Carry, Zero, Sign, Parity, and Auxiliary Carry. The format of this byte is:



In any case, after the data has been saved, the stack pointer is decremented by two.

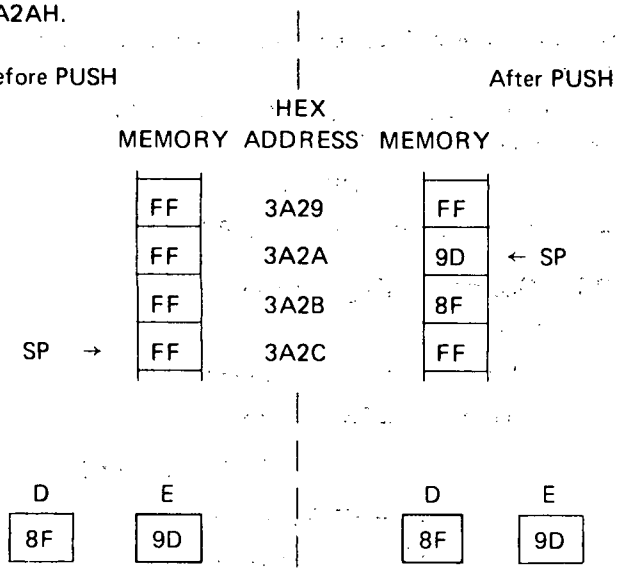
Condition bits affected: None

Example 1:

Assume that register D contains 8FH, register E contains 9DH, and the stack pointer contains 3A2CH. Then the instruction:

PUSH D

stores the D register at memory address 3A2BH, stores the E register at memory address 3A2AH, and then decrements the stack pointer by two, leaving the stack pointer equal to 3A2AH.



Example 2:

Assume that the accumulator contains 1FH, the stack pointer contains 502AH, the Carry, Zero and Parity bits all equal 1, and the Sign and Auxiliary Carry bits all equal 0. Then the instruction:

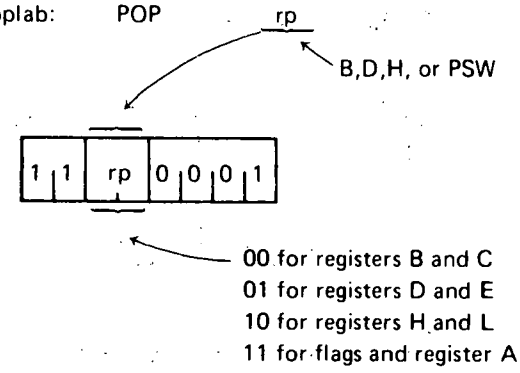
PUSH PSW

stores the accumulator (1FH) at location 5029H, stores the value 47H, corresponding to the flag settings, at location 5028H, and decrements the stack pointer to the value 5028H.

POP Pop Data Off Stack

Format:

Label	Code	Operand
oplab:	POP	rp



Description: The contents of the specified register pair are restored from two bytes of memory indicated by the stack pointer SP. The byte of data at the memory address indicated by the stack pointer is loaded into the second register of the register pair; the byte of data at the address one greater than the address indicated by the stack pointer is loaded into the first register of the pair. If register pair PSW is specified, the byte of data indicated by the contents of the stack pointer is used to restore the values of the five condition bits (Carry, Zero, Sign, Parity, and Auxiliary Carry), using the format described in the last section.

In any case, after the data has been restored, the stack pointer is incremented by two.

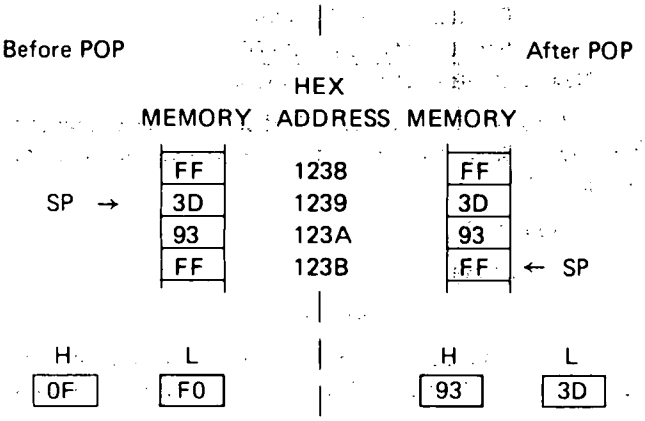
Condition bits affected: If register pair PSW is specified, Carry, Sign, Zero, Parity, and Auxiliary Carry may be changed. Otherwise, none are affected.

Example 1:

Assume that memory locations 1239H and 123AH contain 3DH and 93H, respectively, and that the stack pointer contains 1239H. Then the instruction:

POP H

loads register L with the value 3DH from location 1239H, loads register H with the value 93H from location 123AH, and increments the stack pointer by two, leaving it equal to 123BH.

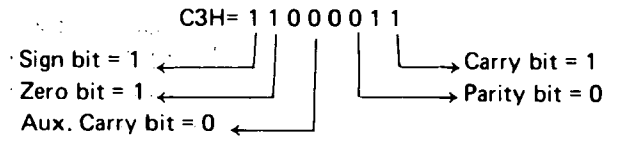


Example 2:

Assume that memory locations 2C00H and 2C01H contain C3H and FFH respectively, and that the stack pointer contains 2C00H. Then the instruction:

POP PSW

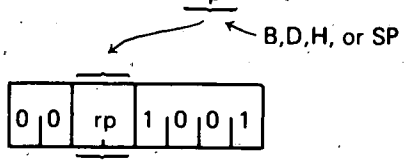
will load the accumulator with FFH and set the condition bits as follows:



DAD Double Add

Format:

Label	Code	Operand
oplab:	DAD	rp



00 for registers B and C
01 for registers D and E
10 for registers H and L
11 for register SP

Description: The 16-bit number in the specified register pair is added to the 16-bit number held in the H and L registers using two's complement arithmetic. The result replaces the contents of the H and L registers.

Condition bits affected: Carry

Example 1:

Assume that register B contains 33H, register C contains 9FH, register H contains A1H, and register L contains 7BH. Then the instruction:

DAD B

performs the following addition:

```
    Registers B and C = 339F
+   Registers H and L = A17B
New contents of H and L = D51A
```

Register H now contains D5H and register L now contains 1AH. Since no carry out was produced, the Carry bit is reset = 0.

Example 2:

The instruction:

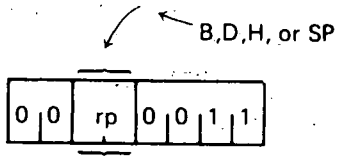
DAD H

will double the 16-bit number in the H and L registers (which is equivalent to shifting the 16 bits one position to the left).

INX Increment Register Pair

Format:

Label	Code	Operand
oplab:	INX	rp



00 for registers B and C
01 for registers D and E
10 for registers H and L
11 for register SP

Description: The 16-bit number held in the specified register pair is incremented by one.

Condition Bits affected: None

Example:

If registers D and E contain 38H and FFH respectively, the instruction:

INX D

will cause register D to contain 39H and register E to contain 00H.

If the stack pointer SP contains FFFFH, the instruction:

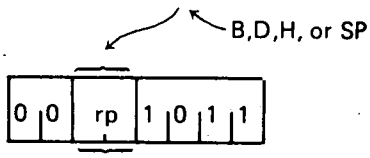
INX SP

will cause register SP to contain 0000H.

DCX Decrement Register Pair

Format:

Label	Code	Operand
oplab:	DCX	rp



00 for registers B and C
01 for registers D and E
10 for registers H and L
11 for register SP

Description: The 16-bit number held in the specified register pair is decremented by one.

Condition bits affected: None

Example:

If register H contains 98H and register L contains 00H, the instruction:

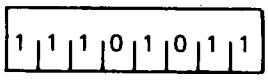
DCX H

will cause register H to contain 97H and register L to contain FFH.

XCHG Exchange Registers

Format:

Label	Code	Operand
oplab:	XCHG	—



Description: The 16 bits of data held in the H and L registers are exchanged with the 16 bits of data held in the D and E registers.

Condition bits affected: None

Example:

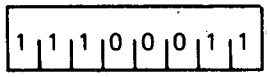
If register H contains 00H, register L contains FFH, register D contains 33H and register E contains 55H, the instruction XCHG will perform the following operation:

Before XCHG		After XCHG	
D	E	D	E
33	55	00	FF
H	L	H	L
00	FF	33	55

XTHL Exchange Stack

Format:

Label	Code	Operand
oplab:	XTHL	—

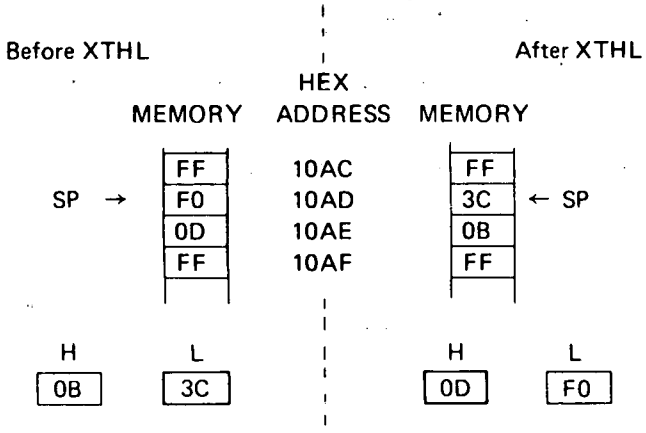


Description: The contents of the L register are exchanged with the contents of the memory byte whose address is held in the stack pointer SP. The contents of the H register are exchanged with the contents of the memory byte whose address is one greater than that held in the stack pointer.

Condition bits affected: None

Example:

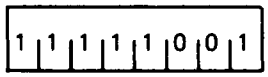
If register SP contains 10ADH, registers H and L contain 0BH and 3CH respectively, and memory locations 10ADH and 10AEH contain F0H and 0DH respectively, the instruction XTHL will perform the following operation:



SPHL Load SP From H And L

Format:

Label	Code	Operand
oplab:	SPHL	—



Description: The 16 bits of data held in the H and L registers replace the contents of the stack pointer SP. The contents of the H and L registers are unchanged.

Condition bits affected: None

Example:

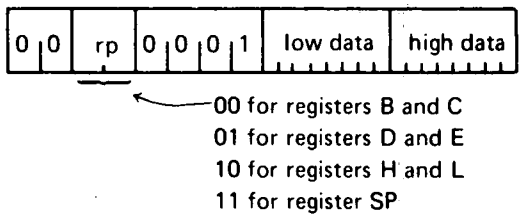
If registers H and L contain 50H and 6CH respectively, the instruction SPHL will load the stack pointer with the value 506CH.

IMMEDIATE INSTRUCTIONS

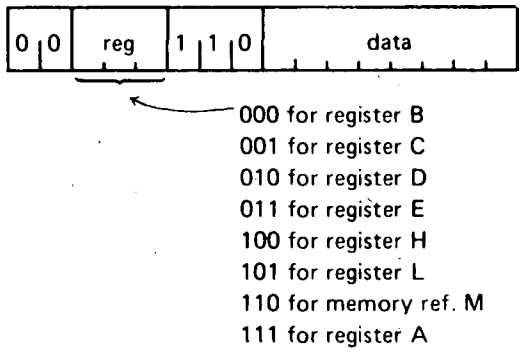
This section describes instructions which perform operations using a byte or bytes of data which are part of the instruction itself.

Instructions in this class occupy two or three bytes as follows:

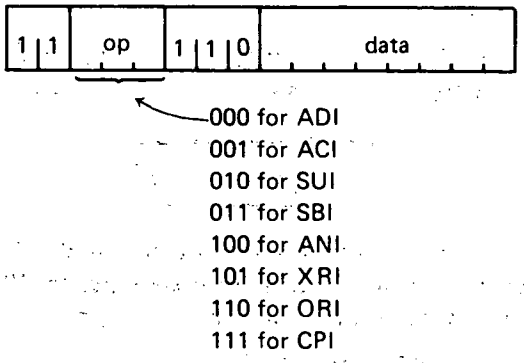
(a) For the LXI data instruction (3 bytes):



(b) For the MVI data instruction (2 bytes):



(c) For the remaining instructions (2 bytes):

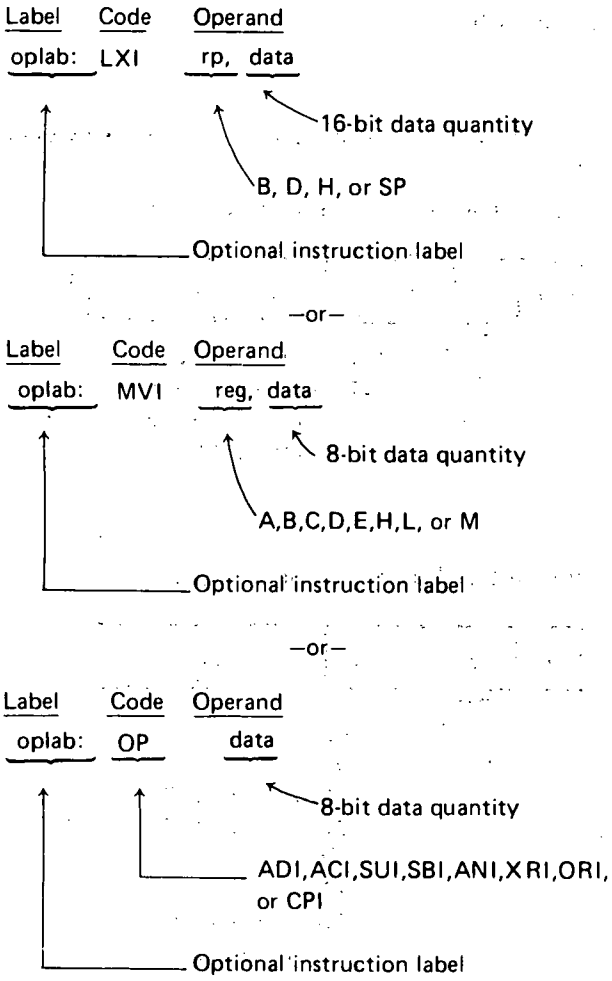


The LXI instruction operates on the register pair specified by RP using two bytes of immediate data.

The MVI instruction operates on the register specified by REG using one byte of immediate data. If a memory reference is specified, the instruction operates on the memory location addressed by registers H and L. The H register holds the most significant 8 bits of the address, while the L register holds the least significant 8 bits of the address.

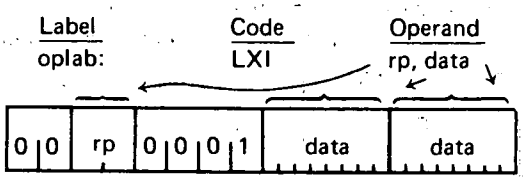
The remaining instructions in this class operate on the accumulator using one byte of immediate data. The result replaces the contents of the accumulator.

The general assembly language instruction format is:



LXI Load Register Pair Immediate

Format:



Description: The third byte of the instruction (the most significant 8 bits of the 16-bit immediate data) is loaded into the first register of the specified pair, while the second byte of the instruction (the least significant 8 bits of the 16-bit immediate data) is loaded into the second register of the specified pair. If SP is specified as the register pair, the second byte of the instruction replaces the least significant 8 bits of the stack pointer, while the third byte of the instruction replaces the most significant 8 bits of the stack pointer.

Condition bits affected: None

NOTE: The immediate data for this instruction is a 16-bit quantity. All other immediate instructions require an 8-bit data value.

Example 1:

Assume that instruction label STRT refers to memory location 103H (=259). Then the following instructions will each load the H register with 01H and the L register with 03H:

```
LXI H,103H
LXI H,259
LXI H,STRT
```

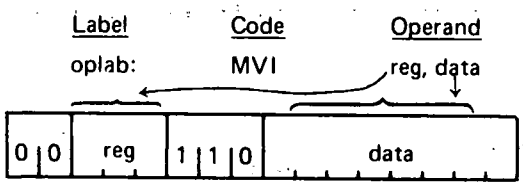
Example 2:

The following instruction loads the stack pointer with the value 3ABCH:

```
LXI SP,3ABCH
```

MVI Move Immediate Data

Format:



Description: The byte of immediate data is stored in the specified register or memory byte.

Condition bits affected: None

Example

Label	Code	Operand	Assembled Data
M1:	MVI	H, 3CH	26EC
M2:	MVI	L, 0F4H	2EF4
M3:	MVI	M, 0FFH	36FF

The instructions at M1 loads the H register with the byte of data at M1 + 1, i.e., 3CH.

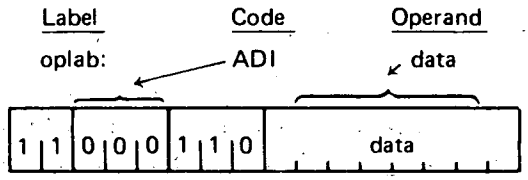
Likewise, the instruction at M2 loads the L register with 0F4H. The instruction at M3 causes the data at M3 + 1 (0FFH) to be stored at memory location 3CF4H. The memory location is obtained by concatenating the contents of the H and L registers into a 16-bit address.

NOTE: The instructions at M1 and M2 above could be replaced by the single instruction:

LXI H, 3CF4H

ADI Add Immediate To Accumulator

Format:



Description: The byte of immediate data is added to the contents of the accumulator using two's complement arithmetic.

Condition bits affected: Carry, Sign, Zero, Parity, Auxiliary Carry

Example:

Label	Code	Operand	Assembled Data
AD1:	MVI	A, 20	3E14
AD2:	ADI	66	C642
AD3:	ADI	-66	C6BE

The instruction at AD1 loads the accumulator with 14H. The instruction at AD2 performs the following addition:

Accumulator = 14H = 00010100
AD2 Immediate Data = 42H = 01000010
Result = 01010110 = 56H = New accumulator

The parity bit is set. Other status bits are reset.

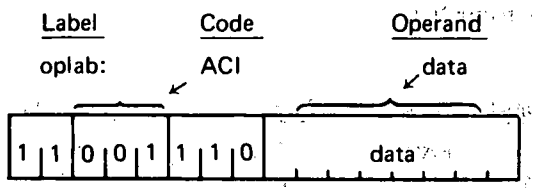
The instruction at AD3 restores the original contents of the accumulator by performing the following addition:

Accumulator = 56H = 01010110
AD3 Immediate Data = 0BEH = 10111110
Result = 00010100 = 14H

The Carry, Auxiliary Carry, and Parity bits are set. The Zero and Sign bits are reset.

ACI Add Immediate To Accumulator With Carry

Format:



Description: The byte of immediate data is added to the contents of the accumulator plus the contents of the carry bit.

Condition bits affected: Carry, Sign, Zero, Parity, Auxiliary Carry

Example:

Label	Code	Operand	Assembled Data
C1:	MVI	A, 56H	3E56
C2:	ACI	-66	CEBE
C3:	ACI	66	CE42

Assuming that the Carry bit = 0 just before the instruction at C2 is executed, this instruction will produce the same result as instruction AD3 in the example of Section 3.10.3.

That is:

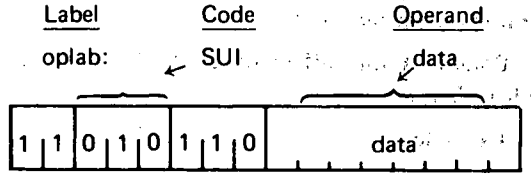
Accumulator = 14H
Carry = 1

The instruction at C3 then performs the following addition:

Accumulator = 14H = 00010100
C3 Immediate Data = 42H = 01000010
Carry bit = 1 = 1
Result = 01010111 = 57H

SUI Subtract Immediate From Accumulator

Format:



Description: The byte of immediate data is subtracted from the contents of the accumulator using two's complement arithmetic.

Since this is a subtraction operation, the carry bit is set, indicating a borrow, if there is no carry out of the high-order bit position, and reset if there is a carry out.

Condition bits affected: Carry, Sign, Zero, Parity, Auxiliary Carry

Example:

This instruction can be used as the equivalent of the DCR instruction.

Label	Code	Operand	Assembled Data
	MVI	A, 0	3E00
S1:	SUI	1	D601

The MVI instruction loads the accumulator with zero. The SUI instruction performs the following subtraction:

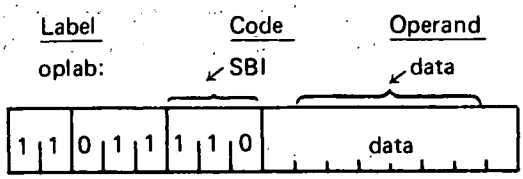
```
    Accumulator =  0H = 00000000
-S1 Immediate Data = -1H = 11111111 two's complement
          Result       = 11111111 = -1H
```

Since there was no carry, and this is a subtract operation, the Carry bit is set, indicating a borrow.

The Zero and Auxiliary Carry bits are also reset, while the Sign and Parity bits are set.

SBI Subtract Immediate from Accumulator With Borrow

Format:



Description: The Carry bit is internally added to the byte of immediate data. This value is then subtracted from the accumulator using two's complement arithmetic.

This instruction and the SBB instruction are most useful when performing multibyte subtractions. For an example of this, see the section on Multibyte Addition and Subtraction in Chapter 4.

Since this is a subtraction operation, the carry bit is set if there is no carry out of the high-order position, and reset if there is a carry out.

Condition bits affected: Carry, Sign, Zero, Parity, Auxiliary Carry

Example:

Label	Code	Operand	Assembled Data
	XRA	A	AF
	SBI	1	DE01

The XRA instruction will zero the accumulator (see example earlier in this chapter). If the Carry bit is zero, the SBI instruction will then perform the following operation:

```
Immediate Data + Carry = 01H
Two's Complement of 01H = 11111111

Adding this to the accumulator produces:

Accumulator = 0H = 00000000
                   11111111
                  -11111111 = -1H = Result
                   carry out = 0 causing the Carry bit to be set
```

The Carry bit is set, indicating a borrow. The Zero and Auxiliary Carry bits are reset, while the Sign and Parity bits are set.

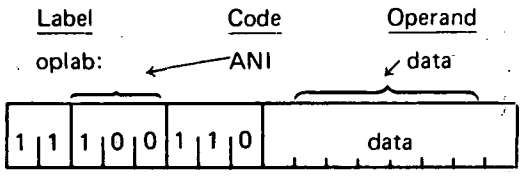
If, however, the Carry bit is one, the SBI instruction will perform the following operation:

```
Immediate Data + Carry = 02H
Two's Complement of 02H = 11111110

Adding this to the accumulator produces:

Accumulator = 0H = 00000000
                   11111111
                  -11111110 = -2H = Result
                   carry out = 0 causing the Carry bit to be set
```

This time the Carry and sign bits are set, while the zero, parity, and auxiliary Carry bits are reset.

ANI And Immediate With Accumulator

Format:



Description: The byte of immediate data is logically ANDed with the contents of the accumulator. The Carry bit is reset to zero.

Condition bits affected: Carry, Zero, Sign, Parity, Auxiliary Carry.

Example:

Label	Code	Operand	Assembled Data
	MOV	A, C	79
A1:	ANI	0FH	E60F

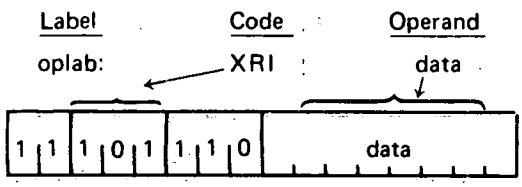
The contents of the C register are moved to the accumulator. The ANI instruction then zeroes the high-order four bits, leaving the low-order four bits unchanged. The Zero bit will be set if and only if the low-order four bits were originally zero.

If the C register contained 3AH, the ANI would perform the following:

```
          Accumulator = 3AH = 00111010
AND (A1 Immediate Data) = 0FH = 00001111
                Result =      00001010 = 0AH
```

XRI Exclusive-Or Immediate With Accumulator

Format:



Description: The byte of immediate data is EXCLUSIVE-ORed with the contents of the accumulator. The carry bit is set to zero.

Condition bits affected: Carry, Zero, Sign, Parity, Auxiliary Carry.

Example:

Since any bit EXCLUSIVE-ORed with a one is complemented, and any bit EXCLUSIVE-ORed with a zero is unchanged, this instruction can be used to complement specific bits of the accumulator. For instance, the instruction:

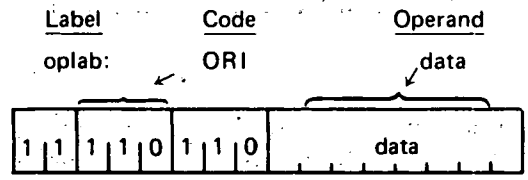
XRI 81H

will complement the least and most significant bits of the accumulator, leaving the rest unchanged. If the accumulator contained 3BH, the process would work as follows:

Accumulator = 3BH = 00111011
XRI Immediate data = 81H = 10000001
Result = 10111010

ORI Or Immediate With Accumulator

Format:



Description: The byte of immediate data is logically ORed with the contents of the accumulator.

The result is stored in the accumulator. The Carry bit is reset to zero, while the Zero, Sign, and Parity bits are set according to the result.

Condition bits affected: Carry, Zero, Sign, Parity, Auxiliary Carry.

Example:

Label	Code	Operand	Assembly Data
	MOV	A,C	79
OR1:	ORI	0FH	F60F

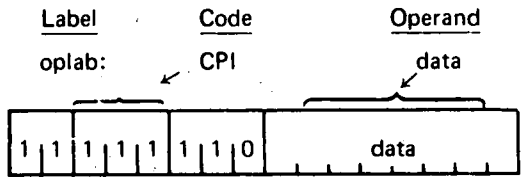
The contents of the C register are moved to the accumulator. The ORI instruction then sets the low-order four bits to one, leaving the high-order four bits unchanged.

If the C register contained 0B5H, the ORI would perform the following:

Accumulator = 0B5H = 10110101
OR (OR1 Immediate data) = 0FH = 00001111
Result = 10111111 = 0BFH

CPI Compare Immediate With Accumulator

Format:



Description: The byte of immediate data is compared to the contents of the accumulator.

The comparison is performed by internally subtracting the data from the accumulator using two's complement arithmetic, leaving the accumulator unchanged but setting the condition bits by the result.

In particular, the zero bit is set if the quantities are equal, and reset if they are unequal.

Since a subtract operation is performed, the Carry bit will be set if there is no carry out of bit 7, indicating the immediate data is greater than the contents of the accumulator, and reset otherwise.

NOTE: If the two quantities to be compared differ in sign, the sense of the Carry bit is reversed.

Condition bits affected: Carry, Zero, Sign, Parity, Auxiliary Carry

Example:

Label	Code	Operand	Assembled Data
	MVI	A, 4AH	3E4A
	CPI	40H	FE40

The CPI instruction performs the following operation:

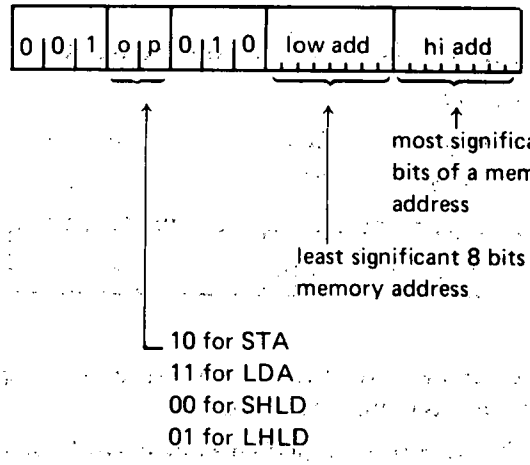
Accumulator = 4AH = 01001010
+(-Immediate data) = -40H = 11000000
1 00001010 = Result

carry out = 1 causing the Carry bit to be reset

The accumulator still contains 4AH, but the zero bit is reset indicating that the quantities were unequal, and the carry bit is reset indicating DATA is less than the accumulator.

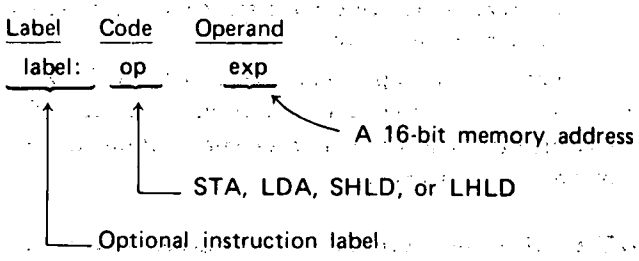
DIRECT ADDRESSING INSTRUCTIONS

This section describes instructions which reference memory by a two-byte address which is part of the instruction itself. Instructions in this class occupy three bytes as follows:



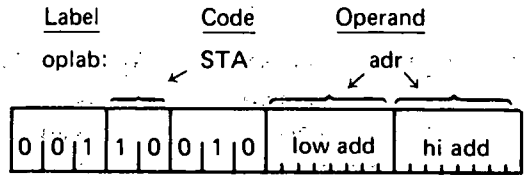
Note that the address is held least significant byte first.

The general assembly language format is:



STA Store Accumulator Direct

Format:



Description: The contents of the accumulator replace the byte at the memory address formed by concatenating HI ADD with LOW ADD.

Condition bits affected: None

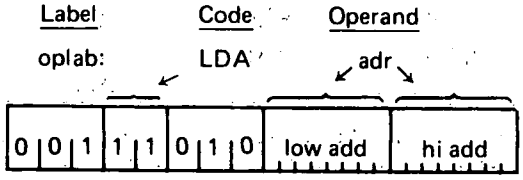
Example:

The following instructions will each store the contents of the accumulator at memory address 5B3H:

```
SAC:    STA  5B3H
        STA  1459
LAB:    STA  0101101100011B
```

LDA Load Accumulator Direct

Format:



Description: The byte at the memory address formed by concatenating HI ADD with LOW ADD replaces the contents of the accumulator.

Condition bits affected: None

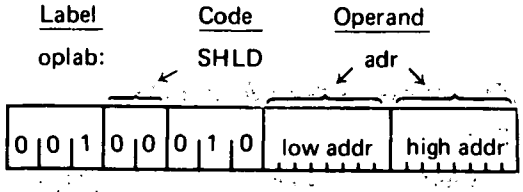
Example:

The following instructions will each replace the accumulator contents with the data held at location 300H:

```
LOAD:   LDA   300H
        LDA   3*(16*16)
GET:    LDA   200H+256
```

SHLD Store H and L Direct

Format:



Description: The contents of the L register are stored at the memory address formed by concatenating HI ADD with LOW ADD. The contents of the H register are stored at the next higher memory address.

Condition bits affected: None

Example:

If the H and L registers contain AEH and 29H respectively, the instruction:

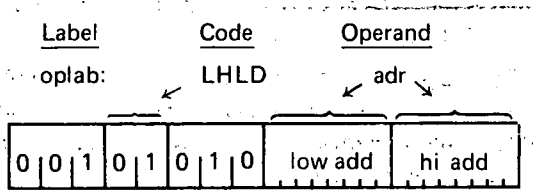
```
SHLD  10AH
```

will perform the following operation:

Memory Before SHLD	HEX ADDRESS	Memory After SHLD
00	109	00
00	10A	29
00	10B	AE
00	10C	00

LHLD Load H And L Direct

Format:



Description: The byte at the memory address formed by concatenating HI ADD with LOW ADD replaces the contents of the L register. The byte at the next higher memory address replaces the contents of the H register.

Condition bits affected: None

Example:

If memory locations 25BH and 25CH contain FFH and 03H respectively, the instruction:

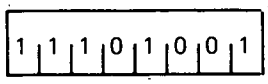
LHLD 25BH

will load the L register with FFH, and will load the H register with 03H.

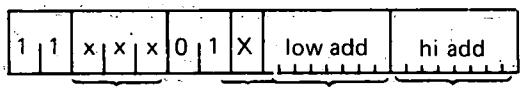
JUMP INSTRUCTIONS

This section describes instructions which alter the normal execution sequence of instructions. Instructions in this class occupy one or three bytes as follows:

(a) For the PCHL instruction (one byte):



(b) For the remaining instructions (three bytes):



most significant 8 bits of a memory address

least significant 8 bits of a memory address

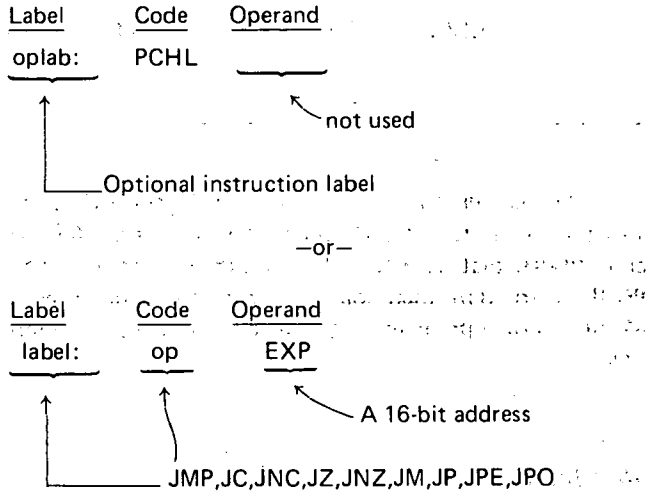
1 for JMP, 0 otherwise

000 for JMP or JNZ
001 for JZ
010 for JNC
011 for JC
100 for JPO
101 for JPE
110 for JP
111 for JM

Note that, just as addresses are normally stored in memory with the low-order byte first, so are the addresses represented in the Jump instructions.

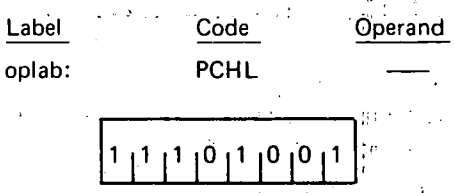
The three-byte instructions in this class cause a transfer of program control depending upon certain specified conditions. If the specified condition is true, program execution will continue at the memory address formed by concatenating the 8 bits of HI ADD (the third byte of the instruction) with the 8 bits of LOW ADD (the second byte of the instruction). If the specified condition is false, program execution will continue with the next sequential instruction.

The general assembly language format is:



PCHL Load Program Counter

Format:



Description: The contents of the H register replace the most significant 8 bits of the program counter, and the contents of the L register replace the least significant 8 bits of the program counter. This causes program execution to continue at the address contained in the H and L registers.

Condition bits affected: None

Example 1:

If the H register contains 41H and the L register contains 3EH, the instruction:

PCHL

will cause program execution to continue with the instruction at memory address 413EH.

Example 2:

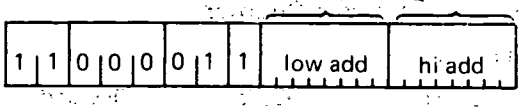
Arbitrary Memory Address	Label	Code	Operand	Assembled Data
40C0	ADR:	DW	LOC	0042
		.		.
		.		.
		.		.
4100	STRT:	LHLD	ADR	2AC040
		PCHL		E9
		.		.
		.		.
		.		.
4200	LOC:	NOP		00
		.		
		.		
		.		

Program execution begins at STRT. The LHLD instruction loads registers H and L from locations 40C1H and 40C0H; that is, with 42H and 00H, respectively. The PCHL instruction then loads the program counter with 4200H, causing program execution to continue at location LOC.

JMP Jump

Format:

Label	Code	Operand
oplab:	JMP	adr



Description: Program execution continues unconditionally at memory address adr.

Condition bits affected: None

Example:

Arbitrary Memory Address	Label	Code	Operand	Assembled Data
3C00		JMP	CLR	C3003E
3C03	AD:	ADI	2	C602
3D00	LOAD:	MVI	A, 3	3E03
3D02		JMP	3C03H	C3033C
3E00	CLR:	XRA	A	AF
3E01		JMP	$-101H	C3003D

The execution sequence of this example is as follows:

The JMP instruction at 3C00H replaces the contents of the program counter with 3E00H. The next instruction executed is the XRA at CLR, clearing the accumulator. The JMP at 3E01H is then executed.

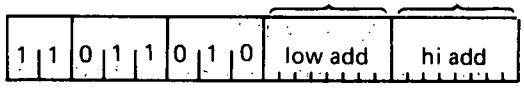
The program counter is set to 3D00H, and the MVI at this address loads the accumulator with 3. The JMP at 3D02H sets the program counter to 3C03H, causing the ADI instruction to be executed.

From here, normal program execution continues with the instruction at 3C05H.

JC Jump If Carry

Format:

Label	Code	Operand
oplab:	JC	adr



Description: If the Carry bit is one, program execution continues at the memory address adr.

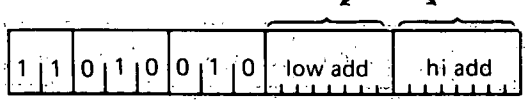
Condition bits affected: None

For a programming example, see the section on JPO later in this chapter.

JNC Jump If No Carry

Format:

Label	Code	Operand
oplab:	JNC	adr



Description: If the Carry bit is zero, program execution continues at the memory address adr.

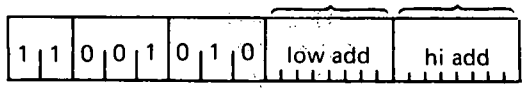
Condition bits affected: None

For a programming example see the section on JPO later in this chapter.

JZ Jump If Zero

Format:

Label	Code	Operand
oplab:	JZ	adr



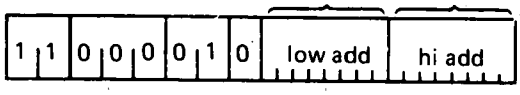
Description: If the zero bit is one, program execution continues at the memory address adr.

Condition bits affected: None

JNZ Jump If Not Zero

Format:

Label	Code	Operand
oplab:	JNZ	adr



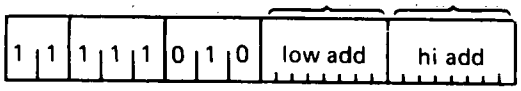
Description: If the Zero bit is zero, program execution continues at the memory address adr.

Condition bits affected: None

JM Jump If Minus

Format:

Label	Code	Operand
oplab:	JM	adr



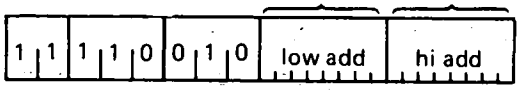
Description: If the Sign bit is one (indicating a negative result), program execution continues at the memory address adr.

Condition bits affected: None

JP Jump If Positive

Format:

Label	Code	Operand
oplab:	JP	adr



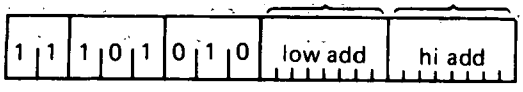
Description: If the sign bit is zero (indicating a positive or zero result), program execution continues at the memory address adr.

Condition bits affected: None

JPE Jump If Parity Even

Format:

Label	Code	Operand
oplab:	JPE	adr



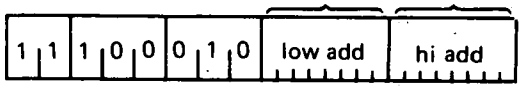
Description: If the parity bit is one (indicating a result with even parity), program execution continues at the memory address adr.

Condition bits affected: None

JPO Jump If Parity Odd

Format:

Label	Code	Operand
oplab:	JPO	adr



Description: If the Parity bit is zero (indicating a result with odd parity), program execution continues at the memory address adr.

Condition bits affected: None

Examples of jump instructions:

This example shows three different but equivalent methods for jumping to one of two points in a program based upon whether or not the Sign bit of a number is set. Assume that the byte to be tested is in the C register.

Label	Code	Operand	Assembled Data
ONE:	MOV	A,C	79
	ANI	80H	E680
	JZ	PLUS	CAXXXX
	JNZ	MINUS	C2XXXX
TWO:	MOV	A,C	79
	RLC		07
	JNC	PLUS	D2XXXX
	JMP	MINUS	C3XXXX
THREE:	MOV	A,C	79
	ADI	0	C600
	JM	MINUS	FAXXXX
PLUS:		SIGN BIT RESET	
MINUS:		SIGN BIT SET	

The AND immediate instruction in block ONE zeroes all bits of the data byte except the Sign bit, which remains unchanged. If the Sign bit was zero, the Zero condition bit will be set, and the JZ instruction will cause program control to be transferred to the instruction at PLUS. Otherwise, the JZ instruction will merely update the program counter by three, and the JNZ instruction will be executed, causing control to be transferred to the instruction at MINUS. (The Zero bit is unaffected by all jump instructions).

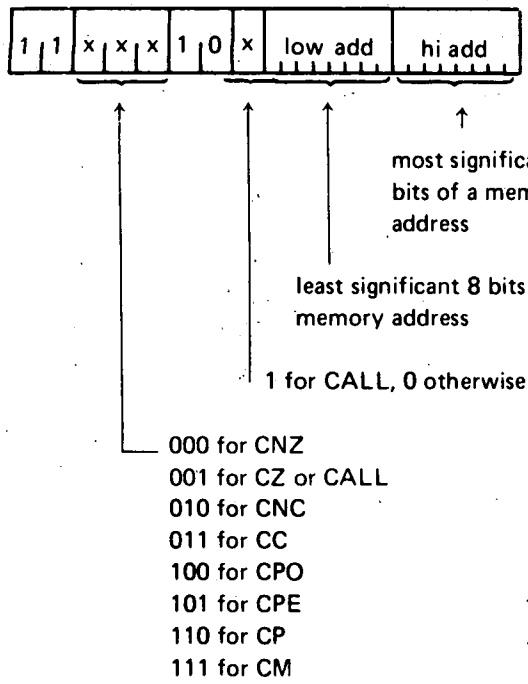
The RLC instruction in block TWO causes the Carry bit to be set equal to the Sign bit of the data byte. If the Sign bit was reset, the JNC instruction causes a jump to PLUS. Otherwise the JMP instruction is executed, unconditionally transferring control to MINUS. (Note that, in this instance, a JC instruction could be substituted for the unconditional jump with identical results).

The add immediate instruction in block THREE: causes the condition bits to be set. If the sign bit was set, the JM instruction causes program control to be transferred to MINUS. Otherwise, program control flows automatically into the PLUS routine.

CALL SUBROUTINE INSTRUCTIONS

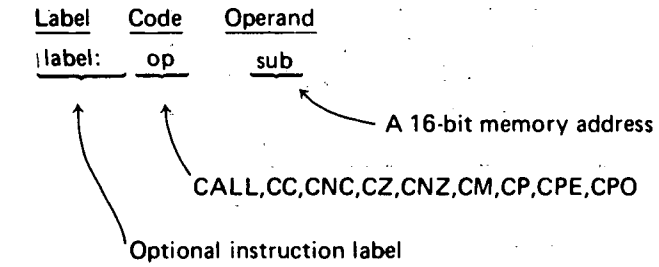
This section describes the instructions which call subroutines. These instructions operate like the jump instructions, causing a transfer of program control. In addition, a return address is pushed onto the stack for use by the RETURN instructions (see Return From Subroutine Instructions later in this chapter).

Instructions in this class occupy three bytes as follows:



Note that, just as addresses are normally stored in memory with the low-order byte first, so are the addresses represented in the call instructions.

The general assembly language instruction format is:

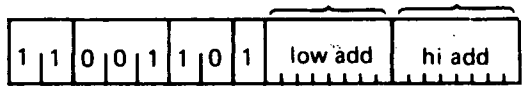


Instructions in this class call subroutines upon certain specified conditions. If the specified condition is true, a return address is pushed onto the stack and program execution continues at memory address SUB, formed by concatenating the 8 bits of HI ADD with the 8 bits of LOW ADD. If the specified condition is false, program execution continues with the next sequential instruction.

CALL Call

Format:

Label	Code	Operand
oplab:	CALL	sub



Description: A call operation is unconditionally performed to subroutine sub.

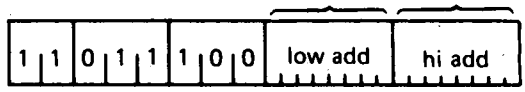
Condition bits affected: None

For programming examples see Chapter 4.

CC Call If Carry

Format:

Label	Code	Operand
oplab:	CC	sub



Description: If the Carry bit is one, a call operation is performed to subroutine sub.

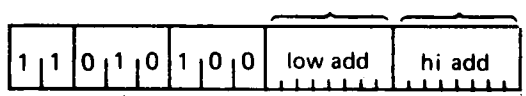
Condition bits affected: None

For programming examples using subroutines, see Chapter 4.

CNC Call If No Carry

Format:

Label	Code	Operand
oplab:	CNC	sub



Description: If the Carry bit is zero, a call operation is performed to subroutine sub.

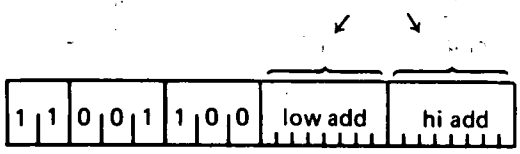
Condition bits affected: None

For programming examples using subroutines, see Chapter 4.

CZ Call If Zero

Format:

Label	Code	Operand
oplab:	CZ	sub



Description: If the Zero bit is set (=1), a call operation is performed to subroutine sub.

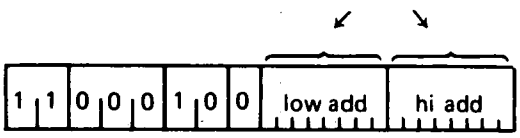
Condition bits affected: None

For programming examples using subroutines, see Chapter 4.

CNZ Call If Not Zero

Format:

Label	Code	Operand
oplab:	CNZ	sub



Description: If the Zero bit is reset (=0), a call operation is performed to subroutine sub.

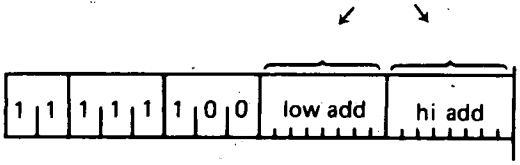
Condition bits affected: None

For programming examples using subroutines, see Chapter 4.

CM Call If Minus

Format:

Label	Code	Operand
oplab:	CM	sub



Description: If the Sign bit is one (indicating a minus result), a call operation is performed to subroutine sub.

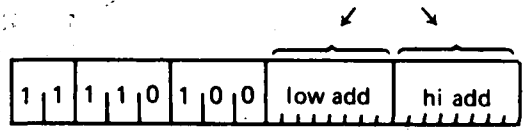
Condition bits affected: None

For programming examples using subroutines, see Chapter 4.

CP Call If Plus

Format:

Label	Code	Operand
oplab:	CP	sub



Description: If the Sign bit is zero (indicating a positive result), a call operation is performed to subroutine sub.

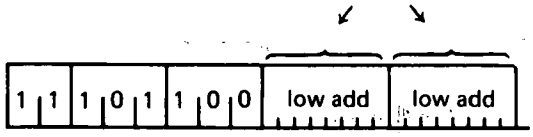
Condition bits affected: None

For programming examples using subroutines, see Chapter 4.

CPE Call If Parity Even

Format:

Label	Code	Operand
oplab:	CPE	sub



Description: If the Parity bit is one (indicating even parity), a call operation is performed to subroutine sub.

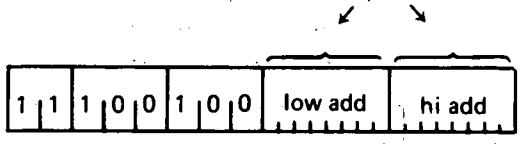
Condition bits affected: None

For programming examples using subroutines, see Chapter 4.

CPO Call If Parity Odd

Format:

Label	Code	Operand
oplab:	CPO	sub



Description: If the Parity bit is zero (indicating odd parity), a call operation is performed to subroutine sub.

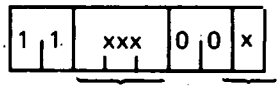
Condition bits affected: None

For programming examples using subroutines, see Chapter 4.

RETURN FROM SUBROUTINE INSTRUCTIONS

This section describes the instructions used to return from subroutines. These instructions pop the last address saved on the stack into the program counter, causing a transfer of program control to that address.

Instructions in this class occupy one byte as follows:



1 for RET,
0 otherwise

000 for RNZ
001 for RZ or RET
010 for RNC
011 for RC
100 for RPO
101 for RPE
110 for RP
111 for RM

The general assembly language instruction format is:

Label	Code	Operand
oplab:	op	

not used

RET,RC,RNC,RZ,RNZ,RM,RP,RPE,RPO

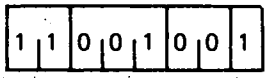
Optional statement label

Instructions in this class perform RETURN operations upon certain specified conditions. If the specified condition is true, a return operation is performed. Otherwise, program execution continues with the next sequential instruction.

RET Return

Format:

Label	Code	Operand
oplab:	RET	—



Description: A return operation is unconditionally performed.

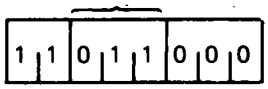
Thus, execution proceeds with the instruction immediately following the last call instruction.

Condition bits affected: None

RC Return If Carry

Format:

Label	Code	Operand
oplab:	RC	—



Description: If the Carry bit is one, a return operation is performed.

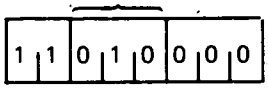
Condition bits affected: None

For programming examples, see Chapter 4.

RNC Return If No Carry

Format:

Label	Code	Operand
oplab:	RNC	—



Description: If the carry bit is zero, a return operation is performed.

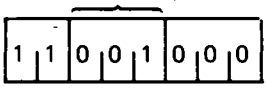
Condition bits affected: None

For programming examples, see Chapter 4.

RZ Return If Zero

Format:

Label	Code	Operand
oplab:	RZ	—



Description: If the Zero bit is one, a return operation is performed.

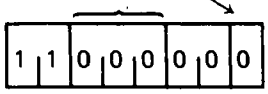
Condition bits affected: None

For programming examples, see Chapter 4.

RNZ Return If Not Zero

Format:

Label	Code	Operand
oplab:	RNZ	—



Description: If the Zero bit is zero, a return operation is performed.

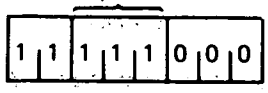
Condition bits affected: None

For programming examples, see Chapter 4.

RM Return If Minus

Format:

Label	Code	Operand
oplab:	RM	—



Description: If the Sign bit is one (indicating a minus result), a return operation is performed.

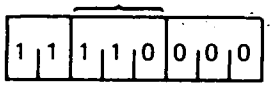
Condition bits affected: None

For programming examples, see Chapter 4.

RP Return If Plus

Format:

Label	Code	Operand
oplab:	RP	—



Description: If the Sign bit is zero (indicating a positive result), a return operation is performed.

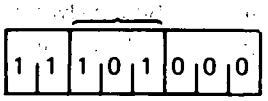
Condition bits affected: None

For programming examples, see Chapter 4.

RPE Return If Parity Even

Format:

Label	Code	Operand
oplab:	RPE	—



Description: If the Parity bit is one (indicating even parity), a return operation is performed.

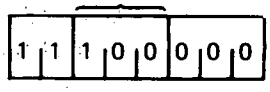
Condition bits affected: None

For programming examples, see Chapter 4.

RPO Return If Parity Odd

Format:

Label	Code	Operand
oplab:	RPO	—



Description: If the Parity bit is zero (indicating odd parity), a return operation is performed.

Condition bits affected: None

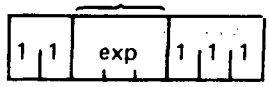
For programming examples, see Chapter 4.

RST INSTRUCTION

This section describes the RST (restart) instruction, which is a special purpose subroutine jump. This instruction occupies one byte.

Format:

Label	Code	Operand
oplab:	RST	exp 0-7



NOTE: "exp" must evaluate to a number in the range 000B to 111B.

Description: The contents of the program counter are pushed onto the stack, providing a return address for later use by a RETURN instruction.

Program execution continues at memory address:

0 0 0 0 | 0 0 0 0 | 0 0 E X | P 0 0 0 | B (Binary)

Normally, this instruction is used in conjunction with up to eight eight-byte routines in the lower 64 words of memory in order to service interrupts to the processor. The interrupting device causes a particular RST instruction to be executed, transferring control to a subroutine which deals with the situation as described in Section 5.

A RETURN instruction then causes the program which was originally running to resume execution at the instruction where the interrupt occurred.

Condition bits affected: None

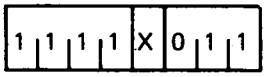
Example:

```
Label   Code    Operand     Comment
        RST     10 - 7      ; Call the subroutine at
                            ; address 24 (011000B)
        RST     E SHL 1     ; Call the subroutine at
                            ; address 48 (110000B). E
                            ; is equated to 11B.
        RST     8           ; Invalid instruction - must be ≤7
        RST     3           ; Call the subroutine at
                            ; address 24 (011000B)
```

For detailed examples of interrupt handling, see Chapter 5.

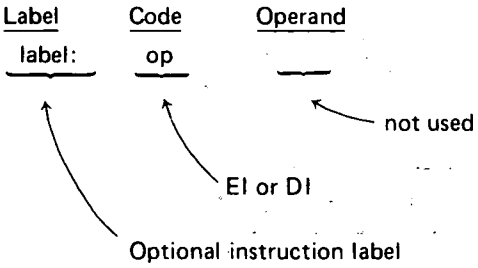
INTERRUPT FLIP-FLOP INSTRUCTIONS

This section describes the instructions which operate directly upon the Interrupt Enable flip-flop INTE. Instructions in this class occupy one byte as follows:



1 for EI
0 for DI

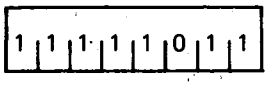
The general assembly language format is:



EI Enable Interrupts

Format:

Label	Code	Operand
oplab:	EI	—



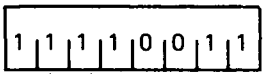
Description: This instruction sets the INTE flip-flop, enabling the CPU to recognize and respond to interrupts. The interrupt is acknowledged after a 1-instruction wait.

Condition bits affected: None.

DI Disable Interrupts

Format:

Label	Code	Operand
oplab:	DI	—

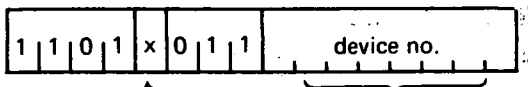


Description: This instruction resets the INTE flip-flop, causing the CPU to ignore all interrupts.

Condition bits affected: None

INPUT/OUTPUT INSTRUCTIONS

This section describes the instructions which cause data to be input to or output from the 8080. Instructions in this class occupy two bytes as follows:

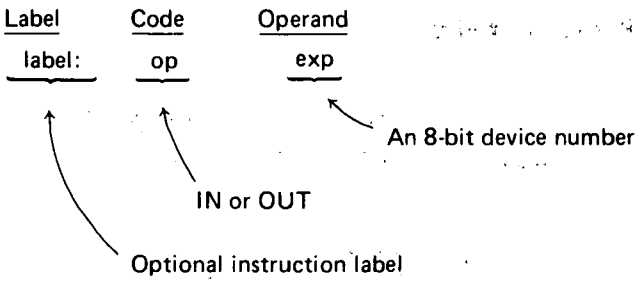


8-bit device number

1 for IN
0 for OUT

The device number is a hardware characteristic of the input or output device, not under the programmer's control.

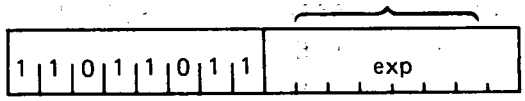
The general assembly language format is:



IN Input

Format:

Label	Code	Operand
oplab:	IN	exp



Description: An eight-bit data byte is read from input device number exp and replaces the contents of the accumulator.

Condition bits affected: None

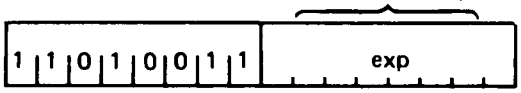
Example:

```
Label   Code    Operand         Comment
        IN      0               ; Read one byte from input
                                ; device # 0 into the
                                ; accumulator
        IN      10/2            ; Read one byte from input
                                ; device # 5 into the
                                ; accumulator
```

OUT Output

Format:

Label	Code	Operand
oplab:	OUT	exp



Description: The contents of the accumulator are sent to output device number exp.

Condition bits affected: None

Example:

```
Label  Code   Operand      Comment
       OUT    10           ; Write the contents of the
                           ; accumulator to output
                           ; device # 10
       OUT    1FH          ; Write the contents of the
                           ; accumulator to output
                           ; device # 31
```

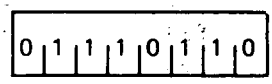
HLT HALT INSTRUCTION

This section describes the HLT instruction, which occupies one byte.

Format:

Label	Code	Operand
oplab:	HLT	

not used



Description: The program counter is incremented to the address of the next sequential instruction. The CPU then enters the STOPPED state and no further activity takes place until an interrupt occurs.

PSEUDO – INSTRUCTIONS

This section describes pseudo-instructions recognized by the assembler. A pseudo-instruction is written in the same fashion as the machine instructions described earlier in this chapter, but does not cause any object code to be generated. It acts merely to provide the assembler with information to be used subsequently while generating object code.

The general assembly language format of a pseudo-instruction is:

Label	Code	Operand	Comment
name	op	opnd	

Operand, may be optional

ORG,EQU,SET,END,IF,ENDIF,MACRO, ENDM, TITLE

name may be required, optional, or illegal

NOTE: Names on pseudo-instructions are not followed by a colon, as are labels. *Names* are required in the label field of MACRO, EQU, and SET pseudo-instructions. The label fields of the remaining pseudo-instructions may contain optional labels, exactly like the labels on machine instructions. In this case, the label refers to the memory location immediately following the last previously assembled machine instruction. If present, names may be 1 to 5 characters long.

ORG Origin

Format:

Label	Code	Operand
oplab:	ORG	exp

A 16-bit address

Description: The assembler's location counter is set to the value of exp, which must be a valid 16-bit memory address. The next machine instruction or data byte(s) generated will be assembled at address exp, exp+1, etc.

If no ORG appears before the first machine instruction or data byte in the program, assembly will begin at location 0. "Exp" must be defined before the ORG statement is encountered.

Example 1:

Hex Memory Address	Label	Code	Operand	Assembled Data
		ORG	1000H	
1000		MOV	A,C	79
1001		ADI	2	C602
1003		JMP	NEXT	C35010
	HERE:	ORG	1050H	
1050	NEXT:	XRA	A	AF

The first ORG pseudo-instruction informs the assembler that the object program will begin at memory address 1000H. The second ORG tells the assembler to set its location counter to 1050H and continue assembling machine instructions or data bytes from that point. The label HERE refers to memory location 1006H, since this is the address immediately following the jump instruction. Note that the range of memory from 1006H to 104FH is still included in the object program, but does not contain assembled data. In particular, the programmer should not assume that these locations will contain zero, or any other value.

Example 2:

The ORG pseudo-instruction can perform a function equivalent to the DS (define storage) instruction (see the section on DS earlier in this chapter). The following two sections of code are exactly equivalent:

Memory Address	Label	Code	Operand	Label	Code	Operand	Assbl. Data
2C00		MOV	A,C		MOV	A,C	79
2C01		JMP	NEXT		JMP	NEXT	C3102C
2C04		DS	12		ORG	$+12	
2C10	NEXT:	XRA	A	NEXT:	XRA	A	AF

Multiple ORGs need not be listed in ascending order, but this practice creates potential segment overlapping problems.

EQU Equate

Format:

Label	Code	Operand
name	EQU	exp

↑ An expression

Required name

Description: The symbol "name" is assigned the value by EXP by the assembler. Whenever the symbol "name" is encountered subsequently in the assembly, this value will be used.

NOTE: A symbol may appear in the name field of only one EQU pseudo-instruction; i.e., an EQU symbol may not be redefined.

Example:

Label	Code	Operand	Assembled Data
PTO	EQU	8	
		.	
		.	
		.	
	OUT	PTO	D308

The OUT instruction in this example is equivalent to the statement:

OUT 8

If at some later time the programmer wanted the name PTO to refer to a different output port, it would be necessary only to change the EQU statement, not every OUT statement.

SET

Format:

Label	Code	Operand
name	SET	exp

↑ An expression

Required name

Description: The symbol "name" is assigned the value of exp by the assembler. Whenever the symbol "name" is encountered subsequently in the assembly, this value will be used unless changed by another SET instruction.

This is identical to the EQU equation, except that symbols may be defined more than once.

Example 1:

Label	Code	Operand	Assembled Data
IMMED	SET	5	
	ADI	IMMED	C605
IMMED	SET	10H-6	
	ADI	IMMED	C60A

Example 2:

Before every assembly, the assembler performs the following SET statements:

Label	Code	Operand
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
A	SET	7
PSW	SET	6
SP	SET	6

If this were not done, a statement like:

MOV D,A

would be invalid, forcing the programmer to write:

MOV 2,7

END End Of Assembly

Format:

Label	Code	Operand
oplab:	END	exp

↑ an expression

Description: The END statement signifies to the assembler that the physical end of the program has been reached, and that generation of the object program and (possibly) listing of the source program should now begin.

One and only one END statement must appear in every assembly, and it must be the (physically) last statement of the assembly.

The operand field can contain an expression representing the starting address for a loader that performs a "load and go" function. The address field of the listing and the end record of the object code will contain this starting address. If the expression is omitted, zero is assumed.

IF AND ENDIF Conditional Assembly

Format:

Label	Code	Operand
oplab:	IF	exp

↑ an expression

s t a t e m e n t s

oplab: ENDIF —

Description: The assembler evaluates exp. If exp evaluates to zero, the statements between IF and ENDIF are ignored. Otherwise the intervening statements are assembled as if the IF and ENDIF were not present. IF-ENDIF pseudo-instructions can be nested to eight levels.

Example:

Label	Code	Operand	Assembled Data
COND	SET	0FFH	
	IF	COND	
	MOV	A, C	79
	ENDIF		
COND	SET	0	
	IF	COND	
	MOV	A, C	
	ENDIF		
	XRA	C	A9

MACRO AND ENDM Macro Definition

Format:

Label	Code	Operand
name	MACRO	list

↑ *Required* name

↑ A list of expressions, normally ASCII constants

s t a t e m e n t s

oplab: ENDM —

Description: For a detailed explanation of the definition and use of macros, together with programming examples, see Chapter 3.

The assembler accepts the statements between MACRO and ENDM as the definition of the macro named "name." Upon encountering "name" in the code field of an instruction, the assembler substitutes the parameters specified in the operand field of the instruction for the occurrences of "list" in the macro definition, and assembles the statements.

NOTE: The pseudo-instruction MACRO may not appear in the list of statements between MACRO and ENDM. That is, macro definitions may not be nested. However, macro calls can be nested up to five levels in resident assemblers and up to nine levels in the cross assembler.

TITLE Page Title

Format:

Label	Code	Operand
oplab	TITLE	string

↑ String of ASCII characters enclosed in quotation marks

Description: The string of up to 66 characters specified in the TITLE pseudo-instruction is printed beneath the page header on all pages following the specification of the title until a new title is specified. The absence of this pseudo-instruction in a program forces a blank line below the page header on each page. The first instance of TITLE forces the string specified to appear on page 1 and all succeeding pages until a new title request is encountered.

CHAPTER 3
PROGRAMMING WITH MACROS

Macros (or macro instructions) are an extremely important tool provided by the assembler. Properly utilized, they will increase the efficiency of programming and the readability of programs. It is strongly suggested that the user become familiar with the use of macros and utilize them to tailor programming to suit his specific needs.

WHAT ARE MACROS?

A macro is a means of specifying to the assembler that a symbol (the *macro name*) appearing in the code field of a statement actually stands for a group of instructions. Both the macro name and the instructions for which it stands are chosen by the programmer.

Consider a simple macro which shifts the contents of the accumulator one bit position to the right, while a zero is shifted into the high-order bit position. We will call this macro SHRT, and define it by writing the following instructions in the program:

```
Label   Code    Operand
SHRT    MACRO
        RRC             ; Rotate accumulator
                        ; right
        ANI     7FH     ; Clear high-order bit
        ENDM
```

We can now reference the macro by placing the following instructions later in the same program:

```
Label   Code    Operand
        LDA     TEMP    ; Load accumulator
        SHRT
```

which would be equivalent to writing:

```
Label   Code    Operand
        LDA     TEMP    ; Load accumulator
        RRC
        ANI     7FH
```

The example above illustrates the three aspects of a macro: the definition, the reference, and the expansion.

The *definition* specifies the instruction sequence that is to be represented by the macro name. Thus:

```
Label   Code    Operand
SHRT    MACRO
        RRC
        ANI     7FH
        ENDM
```

is the definition of SHRT, and specifies that SHRT stands for the two instructions:

```
        RRC
        ANI     7FH
```

Every macro must be defined once and only once in a program before it is referenced.

The *reference* is the point in a program where the macro is referenced. A macro may be referenced in any number of statements by inserting the macro name in the code field of the statements:

```
Label   Code    Operand
        LDA     TEMP
        SHRT            ; Macro expansion
        STA     TEMP
```

The *expansion* of a macro is the complete instruction sequence represented by the macro reference:

```
Label   Code    Operand
        LDA     TEMP    \
        RRC             |
        ANI     7FH     | ; Macro expansion
        STA     TEMP    /
```

The macro expansion will not be present in a source program, but its machine language equivalent will be generated by the assembler in the object program.

Now consider a more complex case, a macro that shifts the accumulator right by a variable number of bit positions specified by the D register contents.

This macro is named SHV, and defined as follows:

```
Label   Code    Operand
SHV     MACRO
LOOP:   RRC             ; Rotate right once
        ANI     7FH     ; Clear the high-order bit
        DCR     D       ; Decrement shift counter
        JNZ     LOOP    ; Return for another shift
        ENDM
```

The SHV macro may then be referenced as follows:

```
Label   Code    Operand
        LDA     TEMP
        MVI     D, 3    ; Specify 3 right shifts
        SHV
        STA     TEMP
```

The above instruction sequence is equivalent to the expression:

```
Label   Code    Operand
        LDA     TEMP
        MVI     D, 3
LOOP:   RRC
        ANI     7FH
        DCR     D
        JNZ     LOOP
        STA     TEMP
```

Note that the D register contents will change whenever the SHV macro is referenced, since it is used to specify shift count.

A better method is to write a macro which uses an arbitrary register into which it loads its own shift amount using *macro parameters.* (Such a macro is defined as follows:

```
Label   Code    Operand
SHV     MACRO   REG,AMT
        MVI     REG,AMT     ; Load shift count
                            ; into register
                            ; specified
                            ; by REG
LOOP:   RRC                 ; Perform right rotate
        ANI     7FH         ; Clear high-order bit
        DCR     REG         ; Decrement shift
                            ; counter
        JNZ     LOOP
        ENDM
```

SHV may now be referenced as follows:

```
Label   Code    Operand
        LDA     TEMP
; Assume Register C is free, and a 5-place shift is needed
        SHV     C, 5
```

the expansion of which is given by:

```
Label   Code    Operand
        MVI     C, 5
LOOP:   RRC
        ANI     7FH
        DCR     C
        JNZ     LOOP
```

Here is another example of an SHV reference:

```
Label   Code    Operand
; Assume Register E is free, and a 2-place shift is needed
        SHV     E, 2
```

and the equivalent expansion:

```
Label   Code    Operand
        MVI     E, 2
LOOP:   RRC
        ANI     7FH
        DCR     E
        JNZ     LOOP
```

While the preceding examples will provide a general idea of the efficiency and capabilities of macros, a rigorous description of each aspect of macro programming is given in the next section.

MACRO TERMS AND USE

The previous section explains how a macro must be defined, is then referenced, and how every reference has an equivalent expansion. Each of these three aspects of a macro will be described in the following subsections.

Macro Definition

Format:

```
Label       Code        Operand
name        MACRO       plist
        m a c r o   b o d y
            ENDM
```

Description: The macro definition produces no assembled data in the object program. It merely indicates to the assembler that the symbol "name" is to be considered equivalent to the group of statements appearing between the pseudo instructions MACRO and ENDM (see Chapter 2 - MACRO and ENDM Macro Definition). This group of statements, called the macro body, may consist of assembly language instructions, pseudo-instructions (except MACRO or ENDM), comments, or references to other macros.

"plist" is a list of unquoted character strings identifying the dummy parameters appearing in the body of the macro definition. Subsequent macro references or calls specifying the actual parameters to be substituted for the dummy parameters must adhere to the positionality of the parameters as indicated in "plist."

Example:

The following macro takes the memory address of the

label specified by the macro reference, loads the most significant 8 bits of the address into the C register, and loads the least significant 8 bits of the address into the B register. (This is the opposite of what the instruction LXI B,ADDR would do).

```
Label     Code     Operand
LOAD      MACRO    ADDR
          MVI      C, ADDR SHR 8
          MVI      B, ADDR AND 0FFH
          ENDM
LABEL:    ——
          ——
INST:     ——
          ——
```

The reference:

```
          Code     Operand
          LOAD     LABEL
```

is equivalent to the expansion:

```
          Code     Operand
          MVI      C, LABEL SHR 8
          MVI      B, LABEL AND 0FFH
```

The reference:

```
          Code     Operand
          LOAD     INST
```

is equivalent to the expansion:

```
          Code     Operand
          MVI      C, INST SHR 8
          MVI      B, INST AND 0FFH
```

The MACRO and ENDM statements inform the assembler that when the symbol LOAD appears in the code field of a statement, the characters appearing in the operand field of the statement are to be substituted everywhere the symbol ADDR appears in the macro body, and the two MVI instructions are to be inserted into the statements at that point of the program and assembled.

Macro Reference Or Call

Format:

```
Label     Code     Operand
oplab:    name     plist
```

"oplab" is an optional label for the macro call.

"name" must be the name of a macro; that is, "name" appears in the label field of a MACRO pseudo-instruction.

"plist" is a list of expressions. Each expression is substituted into the macro body as indicated by the operand field of the MACRO pseudo-instruction. Substitution proceeds left to right; that is, the first string of "plist" replaces every occurrence of the first dummy parameter in the macro body, the second replaces the second, and so on.

If fewer parameters appear in the macro reference than in the definition, a null string is substituted for the remaining expressions in the definition.

If more parameters appear in the reference than the definition, the extras are ignored.

Example:

Given the macro definition:

```
Label     Code     Operand
MAC1      MACRO    P1, P2, COMMENT
          XRA      P2
          DCR      P1      COMMENT
          ENDM
```

The reference:

```
          Code     Operand
          MAC1     C, D, '; DECREMENT C'
```

is equivalent to the expansion:

```
          Code     Operand
          XRA      D
          DCR      C  ; DECREMENT C
```

The reference:

```
          Code     Operand
          MAC1     E, B
```

is equivalent to the expansion:

```
          Code     Operand
          XRA      B
          DCR      E
```

Macro Expansion

The result obtained by substituting the macro parameters into the macro body is called the macro expansion. The assembler assembles the statements of the expansion exactly as it assembles any other statements. In particular, every statement produced by expanding the macro must be a legal assembler statement.

Example:

Given the macro definition:

```
Label     Code     Operand
MAC       MACRO    P1
          PUSH     P1
          ENDM
```

the reference:

```
          MAC      B
```

will produce the legal expansion:

```
          PUSH     B
```

but the reference:

```
          MAC      C
```

will produce the illegal expansion:

```
          PUSH     C
```

which will be flagged as an error.

Scope of Labels and Names Within Macros

In this section, the terms *global* and *local* are important. For our purposes, they will be defined as follows: A symbol is globally defined in a program if its value is known and can be referenced by any statement in the program, whether or not the statement was produced by the expansion of a macro. A symbol is locally defined if its value is known and can be referenced only within a particular macro expansion.

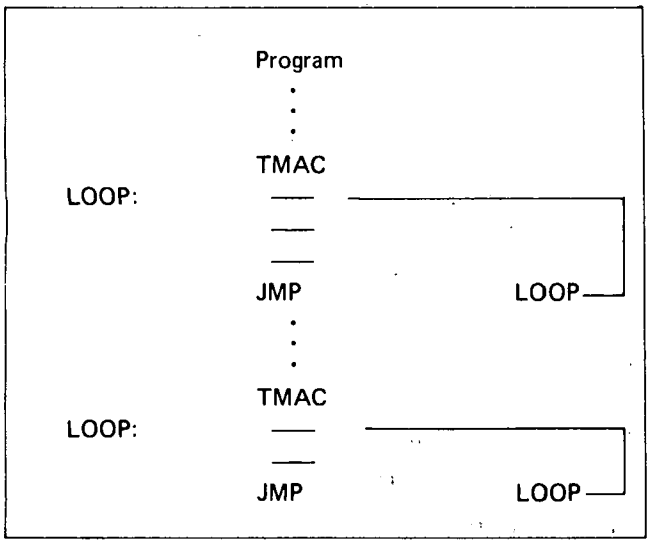
Instruction Labels: Normally a symbol may appear in the label field of only one instruction. If a label appears in the body of a macro, however, it will be generated whenever the macro is referenced. To avoid multiple-label conflicts, the assembler treats labels within macros as local labels, applying only to a particular expansion of a macro. Thus, each "jump to LOOP" instruction generated in the first example of the chapter refers uniquely to the label LOOP generated in the local macro expansion.

Conversely, if the programmer wishes to generate a global label from a macro expansion, he must follow the label with two colons in the macro definition, rather than one. Now, this global label must not be generated more than once, since it is global and therefore must be unique in the program.

For example, consider the macro definition:

```
Label     Code      Operand
TMAC      MACRO
            —
LOOP:       —
            —
            —
          JMP       LOOP
          ENDM
```

If two references to TMAC appear in a program, the label LOOP will be a local label and each JMP LOOP instruction will refer to the label generated within its own expansion:



If in the macro definition, LOOP had been followed by two successive colons, LOOP would be generated as a global label by the first reference to TMAC, while the second reference would be flagged as an error.

"Equate" Names: Names on equate statements within a macro are *always* local, defined only within the expansion in which they are generated.

For example, consider the following macro definition:

```
Label     Code      Operand
EQMAC     MACRO
VAL       EQU       8
          DB        VAL
          ENDM
```

The following program section is valid:

```
Label     Code      Operand     Assembled Data
VAL       EQU       6
DB1:      DB        VAL             06
          EQMAC
VAL       EQU       8
          DB        VAL             08
DB2:      DB        VAL             06
```

VAL is first defined globally with a value of 6. Therefore the reference to VAL at DB1 produces a byte equal to 6. The macro reference EQMAC generates a symbol VAL defined only within the macro expansion with a value of 8; therefore the reference to VAL by the second statement of the macro produces a byte equal to 8. Since this statement ends the macro expansion, the reference to VAL at DB2 refers to the global definition of VAL. The statement at DB2 therefore produces a byte equal to 6.

"Set" Names: Suppose that a "set" statement is generated by a macro. If its name has already been defined globally by another set statement, the generated statement will change the global value of the name for all subsequent references. Otherwise, the name is defined locally, applying only within the current macro expansion. These cases are illustrated as follows:

Consider the macro definition:

```
Label     Code      Operand
STMAC     MACRO
SYM       SET       5
          DB        SYM
          ENDM
```

The following program section is valid:

Label	Code	Operand	Assembled Data
SYM	SET	0	
DB1:	DB	SYM	00
	STMAC		
SYM	SET	5	
	DB	SYM	05
DB2:	DB	SYM	05

SYM is first defined globally with a value of zero, causing the reference at DB1 to produce a byte of 0. The macro reference STMAC resets this global value to 5, causing the second statement of the macro to produce a value of 5. Although this ends the macro expansion, the value of SYM remains equal to 5, as shown by the reference at DB2.

Using the same macro definition as above, the following program section is invalid:

Label	Code	Operand	Assembled Data
	STMAC		
SYM	SET	5	
	DB	SYM	05
DB3:	DB	SYM	**ERROR**

Since in this case SYM is first defined in a macro expansion, its value is defined locally. Therefore the second (and final) statement of the macro expansion produces a byte equal to 5. The statement at DB3 is invalid, however, since SYM is unknown globally.

Macro Parameter Substitution

The value of macro parameters is determined and passed into the macro body at the time the macro is referenced, before the expansion is produced. This evaluation may be delayed by enclosing a parameter in quotes, causing the actual character string to be passed into the macro body. The string will then be evaluated when the macro expansion is produced.

Example:

Suppose that the following macro MAC4 is defined at the beginning of the program:

```
Label   Code    Operand
MAC4    MACRO   P1
ABC     SET     14
        DB      P1
        ENDM
```

Further suppose that the statement:

```
ABC     SET     3
```

has been written before the first reference to MAC4, setting the value of ABC to 3.

Then the macro reference:

```
MAC4    ABC
```

will cause the assembler to evaluate ABC and to substitute the value 3 for parameter P1, then produce the expansion:

```
ABC     SET     14
        DB      3
```

If, however, the user had *instead* written the macro reference:

```
MAC4    'ABC'
```

the assembler would evaluate the expression 'ABC,' producing the characters ABC as the value of parameter P1. Then the expansion is produced, and, since ABC is altered by the first statement of the expansion, P1 will now produce the value 14.

Expansion produced:

```
ABC     SET     14
        DB      ABC ; Assembles as 14
```

REASONS FOR USING MACROS

The use of macros is an important programming technique that can substantially ease the user's task in the following ways:

(a) Often, a small group of instructions must be repeated many times throughout a program with only minor changes for each repetition.

Macros can reduce the tedium (and resultant increased chance for error) associated with these operations.

(b) If an error in a macro definition is discovered, the program can be corrected by changing the definition and reassembling. If the same routine had been repeated many times throughout the program without using macros, each occurrence would have to be located and changed. Thus debugging time is decreased.

(c) Duplication of effort between programmers can be reduced. Once the most efficient coding of a particular function is discovered, the macro definition can be made available to all other programmers.

(d) As has been seen with the SHRT (shift right) macro, new and useful instructions can be easily simulated.

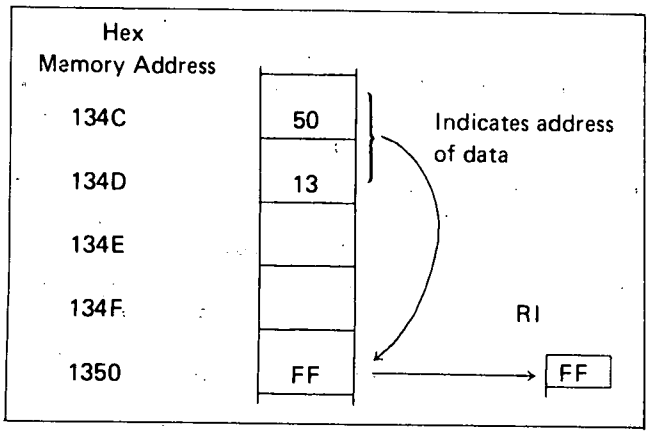
USEFUL MACROS

Load Indirect Macro

The following macro, LIND, loads register RI indirect from memory location INADD.

That is, location INADD will be assumed to hold a two-byte memory address (least significant byte first) from which register RI will be loaded.

Example:



If the address of INADD is 134CH, register RI will be loaded from the address held in memory locations 134CH and 134DH, which is 1350H.

Macro definition:

```
Label   Code    Operand          Comment
LIND    MACRO   RI, INADD
        LHLD    INADD    ; Load indirect address
                         ; into H and L registers
        MOV     RI, M    : Load data into RI
        ENDM
```

Macro reference:

```
Label       Code        Operand
; Load register C indirect with the contents of memory
; location LABEL.
            LIND        C, LABEL
```

Macro expansion:

```
Label       Code        Operand
            LHLD        LABEL
            MOV         C, M
```

Other Indirect Addressing Macros

Refer to the LIND macro definition in the last section. Only the MOV RI,M instruction need be altered to create any other indirect addressing macro. For example, substituting MOV M,RI will create a "store indirect" macro. Providing RI is the accumulator, substituting ADD M will create an "add to accumulator indirect" macro.

As an alternative to having load indirect, store indirect, and other such indirect macros, we could have a "create indirect address" macro, followed by selected instructions. This alternative approach is illustrated for indexed addressing in the next section.

Create Indexed Address Macro

The following macro, IXAD, loads registers H and L with the base address BSADD, plus the 16-bit index formed by register pair REGPR (REGPR=B,D,H, or SP).

Macro definition:

```
Label   Code    Operand          Comment
IXAD    MACRO   REGPR, BSADD
        LXI     H, BSADD ; Load the base address
        DAD     REGPR    ; Add index to base
                         ; address
        ENDM
```

Macro reference:

```
Label       Code        Operand
; The address created in H and L by the following macro
; call will be Label + 012EH
            MVI         D, 1
            MVI         E, 2EH
            IXAD        D, LABEL
```

Macro expansion:

```
Label       Code        Operand
            MVI         D, 1
            MVI         E, 2EH
            LXI         H, BSADD
            DAD         D
```

CHAPTER 4
PROGRAMMING TECHNIQUES

This section describes some techniques other than macros which may be of help to the programmer.

BRANCH TABLES PSEUDO-SUBROUTINE

Suppose a program consists of several separate routines, any of which may be executed depending upon some initial condition (such as a number passed in a register). One way to code this would be to check each condition sequentially and branch to the routines accordingly as follows:

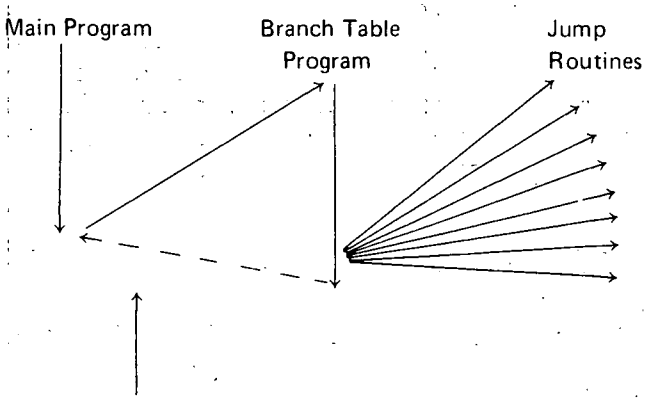
```
CONDITION = CONDITION 1?
IF YES BRANCH TO ROUTINE 1
CONDITION = CONDITION 2?
IF YES BRANCH TO ROUTINE 2
        .
        .
        .
BRANCH TO ROUTINE N
```

A sequence as above is inefficient, and can be improved by using a branch table.

The logic at the beginning of the branch table program computes a pointer into the branch table. The branch table itself consists of a list of starting addresses for the routines to be branched to. Using the pointer, the branch table program loads the selected routine's starting address into the address bytes of a jump instruction, then executes the jump. For example, consider a program that executes one of eight routines depending on which bit of the accumulator is set:

Jump to routine 1	if	the	accumulator	holds	00000001
"	"	"	2	"	"	"	"	00000010
"	"	"	3	"	"	"	"	00000100
"	"	"	4	"	"	"	"	00001000
"	"	"	5	"	"	"	"	00010000
"	"	"	6	"	"	"	"	00100000
"	"	"	7	"	"	"	"	01000000
"	"	"	8	"	"	"	"	10000000

A program that provides the above logic is given at the end of this section. The program is termed a "pseudo-subroutine" because it is treated as a subroutine by the programmer (i.e., it appears just once in memory), but it is entered via a regular JUMP instruction rather than via a CALL instruction. This is possible because the branch routine controls subsequent execution, and will never return to the instruction following the call:



```
Label    Code    Operand
START:   LXI     H, BTBL  ; Registers H and L will
                          ; point to branch table.
GTBIT:   RAR
         JC      GETAD
         INX     H        ; (H,L)=(H,L)+2 to
         INX     H        ; point to next address
                          ; in branch table.
         JMP     GTBIT
GETAD:   MOV     E,M      ; A one bit was found.
         INX     H        ; Get address in D and
                          ; E.
         MOV     D,M
         XCHG             ; Exchange D and E
                          ; with H and L.
         PCHL             ; Jump to routine
                          ; address.
         _____
         _____
         _____
BTBL:    DW      ROUT1    ; Branch table. Each
         DW      ROUT2    ; entry is a two-byte
                          ; address
         DW      ROUT3    ; held least significant
         DW      ROUT4    ; byte first.
         DW      ROUT5
         DW      ROUT6
         DW      ROUT7
         DW      ROUT8
```

The control routine at START uses the H and L registers as a pointer into the branch table (BTBL) corresponding to the bit of the accumulator that is set. The routine at GETAD then transfers the address held in the corresponding branch table entry to the H and L registers via the D and E registers, and then uses a PCHL instruction, thus transferring control to the selected routine.

SUBROUTINES

Frequently, a group of instructions must be repeated many times in a program. As we have seen in Chapter 3, it is sometimes helpful to define a macro to produce these groups. If a macro becomes too lengthy or must be repeated many times, however, better economy can be obtained by using subroutines.

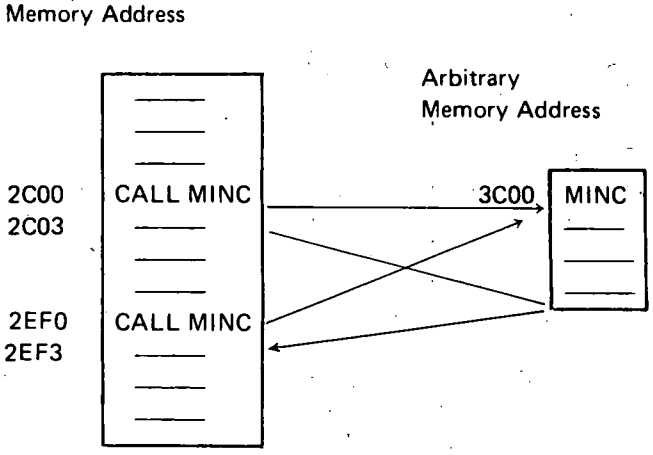
A subroutine is coded like any other group of assembly language statements, and is referred to by its name, which is the label of the first instruction. The programmer references a subroutine by writing its name in the operand field of a CALL instruction. When the CALL is executed, the address of the next sequential instruction after the CALL is pushed onto the stack (see the section on the Stack Pointer in Chapter 1), and program execution proceeds with the first instruction of the subroutine. When the subroutine has completed its work, a RETURN instruction is executed, which causes the top address in the stack to be popped into the program counter, causing program execution to continue with the instruction following the CALL. Thus, one copy of a subroutine may be called from many different points in memory, preventing duplication of code.

Example:

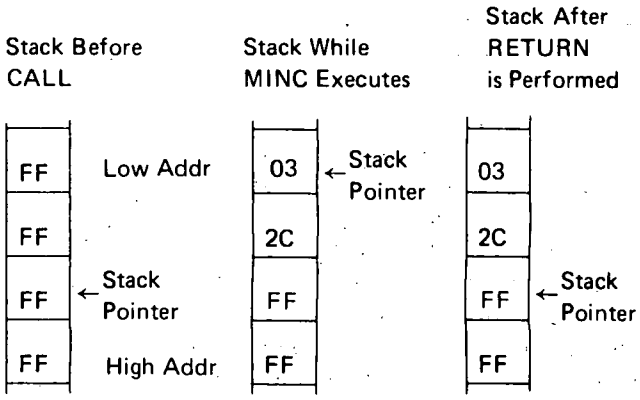
Subroutine MINC increments a 16-bit number held least-significant-byte first in two consecutive memory locations, and then returns to the instruction following the last CALL statement executed. The address of the number to be incremented is passed in the H and L registers.

```
Label    Code    Operand    Comment
MINC:    INR     M          ; Increment low-order byte
         RNZ                ; If non-zero, return to
                            ; calling routine
         INX     H          ; Address high-order byte
         INR     M          ; Increment high-order byte
         RET                ; Return unconditionally
```

Assume MINC appears in the following program:



When the first call is executed, address 2C03H is pushed onto the stack indicated by the stack pointer, and control is transferred to 3C00H. Execution of either RETURN statement in MINC will cause the top entry to be popped off the stack into the program counter, causing execution to continue at 2C03H (since the CALL statement is three bytes long).



When the second call is executed, address 2EF3H is pushed onto the stack, and control is again transferred to MINC. This time, either RETURN instruction will cause execution to resume at 2EF3H.

Note that MINC could have called another subroutine during its execution, causing another address to be pushed onto the stack. This can occur as many times as necessary, limited only by the size of memory available for the stack.

Note also that any subroutine could push data onto the stack for temporary ssorage without affecting the call and return sequences as long as the same amount of data is popped off the stack before executing a RETURN statement.

Transferring Data To Subroutines

A subroutine often requires data to perform its operations. In the simplest case, this data may be transferred in one or more registers. Subroutine MINC in the last section, for example, receives the memory address which it requires in the H and L registers.

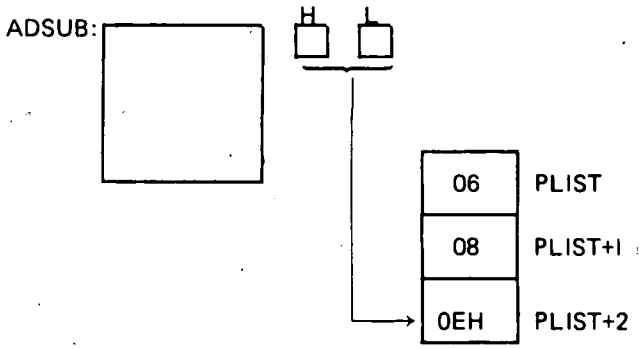
Sometimes it is more convenient and economical to let the subroutine load its own registers. One way to do this is to place a list of the required data (called a parameter list) in some data area of memory, and pass the address of this list to the subroutine in the H and L registers.

For example, the subroutine ADSUB expects the address of a three-byte parameter list in the H and L registers. It adds the first and second bytes of the list, and stores the result in the third byte of the list:

```
Label   Code    Operand      Comment
        LXI     H, PLIST ; Load H and L with
                         ; addresses of the param-
                         ; eter list
        CALL    ADSUB    ; Call the subroutine
RET1:   ----
        ----
PLIST:  DB      6        ; First number to be added
        DB      8        ; Second number to be
                         ; added
        DS      1        ; Result will be stored here
        LXI     H, LIST2 ; Load H and L registers
        CALL    ADSUB    ; for another call to ADSUB
RET2:   ----
        ----
LIST2:  DB      10
        DB      35
        DS      1
        ----
        ----
ADSUB:  MOV     A, M     ; Get first parameter
        INX     H        ; Increment memory
                         ; address
        MOV     B, M     ; Get second parameter
        ADD     B        ; Add first to second
        INX     H        ; Increment memory
                         ; address
        MOV     M, A     ; Store result at third
                         ; parameter store
        RET              ; Return unconditionally
```

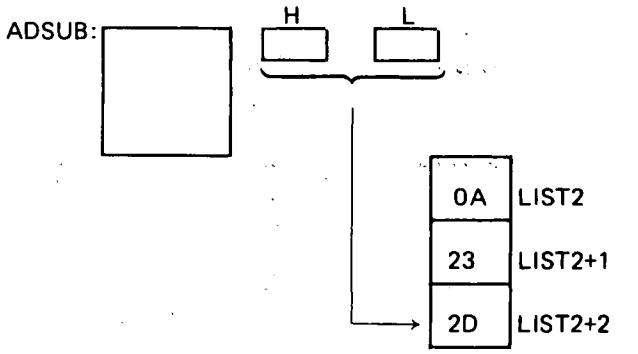
The first time ADSUB is called, it loads the A and B registers from PLIST and PLIST+1 respectively, adds them, and stores the result in PLIST+2. Return is then made to the instruction at RET1.

First call to ADSUB:



The second time ADSUB is called, the H and L registers point to the parameter list LIST2. The A and B registers are loaded with 10 and 35 respectively, and the sum is stored at LIST2 + 2. Return is then made to the instruction at RET2.

Second call to ADSUB:

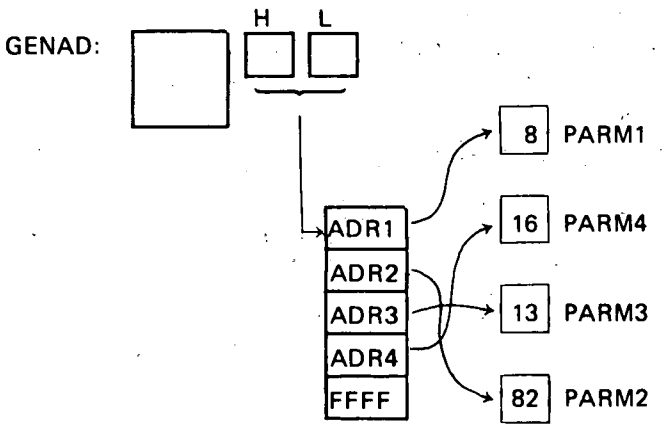


Note that the parameter lists PLIST and LIST2 could appear anywhere in memory without altering the results produced by ADSUB.

This approach does have its limitations, however. As coded, ADSUB must receive a list of two and only two numbers to be added, and they must be contiguous in memory. Suppose we wanted a subroutine (GENAD) which would add an arbitrary number of bytes, located anywhere in memory, and leave the sum in the accumulator.

This can be done by passing the subroutine a parameter list which is a list of *addresses* of parameters, rather than the parameters themselves, and signifying the end of the parameter list by a number whose first byte is FFH (assuming that no parameters will be stored above address FF00H).

Call to GENAD:



As implemented below, GENAD saves the current sum (beginning with zero) in the C register. It then loads the address of the first parameter into the D and E registers. If this address is greater than or equal to FF00H, it reloads the accumulator with the sum held in the C register and returns to the calling routine. Otherwise, it loads the parameter into the accumulator and adds the sum in the C register to the accumulator. The routine then loops back to pick up the remaining parameters.

```
Label     Code    Operand      Comment
          LXI     SP, 1000H    ; Assume this stack size is adequate
          LXI     H, PLIST     ; Calling program
          CALL    GENAD
          ———
          ———
          HALT
PLIST:    DW      PARM1        ; List of parameter addresses
          DW      PARM2
          DW      PARM3
          DW      PARM4
          DW      0FFFFH       ; Terminator
          ———
          ———
PARM1:    DB      6
PARM4:    DB      16
          ———
          ———
PARM3:    DB      13
          ———
          ———
          ———
PARM2:    DB      82
          ———
          ———
GENAD:    XRA     A            ; Clear accumulator
LOOP:     MOV     C, A         ; Save current total in C
          MOV     E, M         ; Get low order address byte
                               ; of first parameter
          INX     H
          MOV     A, M         ; Get high order address byte
                               ; of first parameter
          CPI     0FFH         ; Compare to FFH
          JZ      BACK         ; If equal, routine is complete
          MOV     D, A         ; D and E now address parameter
          LDAX    D            ; Load accumulator with parameter
          ADD     C            ; Add previous total
          INX     H            ; Increment H and L to point
                               ; to next parameter address
          JMP     LOOP         ; Get next parameter
BACK:     MOV     A, C         ; Routine done—restore total
          RET                  ; Return to calling routine
          END
```

Note that GENAD could add any combination of the parameters with no change to the parameters themselves.

The sequence:

```
        LXI     H, PLIST
        CALL    GENAD
        ---
        ---
        ---
PLIST:  DW      PARM4
        DW      PARM1
        DW      0FFFFH
```

would cause PARM1 and PARM4 to be added, no matter where in memory they might be located (excluding addresses above FF00H).

Many variations of parameter passing are possible. For example, if it was necessary to allow parameters to be stored at any address, a calling program could pass the total number of parameters as the first parameter; the subroutine would load this first parameter into a register and use it as a counter to determine when all parameters had been accepted.

SOFTWARE MULTIPLY AND DIVIDE

The multiplication of two unsigned 8-bit data bytes may be accomplished by one of two techniques: repetitive addition, or use of a register shifting operation.

Repetitive addition provides the simplest, but slowest, form of multiplication. For example, 2AH·74H may be generated by adding 74H to the (initially zeroed) accumulator 2AH times.

Using shift operations provides faster multiplication. Shifting a byte left one bit is equivalent to multiplying by 2, and shifting a byte right one bit is equivalent to dividing by 2. The following process will produce the correct 2-byte result of multiplying a one byte multiplicand by a one byte multiplier:

(a) Test the least significant bit of the multiplier. If zero, go to step b. If one, add the multiplicand to the *most* significant byte of the result.

(b) Shift the entire two-byte result right one bit position.

(c) Repeat steps a and b until all 8 bits of the multiplier have been tested.

For example, consider the multiplication:

2AH·3CH=9D8H

	MULTIPLIER	MULTIPLICAND	HIGH-ORDER BYTE OF RESULT	LOW-ORDER BYTE OF RESULT
Start	00111100	00101010	00000000	00000000
Step 1 a				
b			00000000	00000000
Step 2 a				
b			00000000	00000000
Step 3 a			00101010	00000000
b			00010101	00000000
Step 4 a			00111111	00000000
b			00011111	10000000
Step 5 a			01001001	10000000
b			00100100	11000000
Step 6 a			01001110	11000000
b			00100111	01100000
Step 7 a				
b			00010011	10110000
Step 8 a				
b			00001001	11011000

Step 1: Test multiplier 0-bit; it is 0, so shift 16-bit result right one bit.

Step 2: Test multiplier 1-bit; it is 0, so shift 16-bit result right one bit.

Step 3: Test multiplier 2-bit; it is 1, so add 2AH to high-order byte of result and shift 16-bit result right one bit.

Step 4: Test multiplier 3-bit; it is 1, so add 2AH to high-order byte of result and shift 16-bit result right one bit.

Step 5: Test multiplier 4-bit; it is 1, so add 2AH to high-order byte of result and shift 16-bit result right one bit.

Step 6: Test multiplier 5-bit; it is 1, so add 2AH to high-order byte of result and shift 16-bit result right one bit.

Step 7: Test multiplier 6-bit; it is 0, so shift 16-bit result right one bit.

Step 8: Test multiplier 7-bit; it is 0, so shift 16-bit result right one bit.

The result produced is 09D8.

The process works for the following reason:

The result of any multiplication may be written:

Equation 1: $BIT7 \cdot MCND \cdot 2^7 + BIT6 \cdot MCND \cdot 2^6 + \ldots + BIT0 \cdot MCND \cdot 2^0$

where BIT0 through BIT8 are the bits of the multiplier (each equal to zero or one), and MCND is the multiplicand.

For example:

MULTIPLICAND · MULTIPLIER =

$00001010 \cdot 00000101 =$

$0 \cdot 0AH \cdot 2^7 + 0 \cdot 0AH \cdot 2^6 + 0 \cdot 0AH \cdot 2^5 + 0 \cdot 0AH \cdot 2^4 +$

$0 \cdot 0AH \cdot 2^3 + 1 \cdot 0AH \cdot 2^2 + 0 \cdot 0AH \cdot 2^1 + 1 \cdot 0AH \cdot 2^0 =$

$00101000 + 00001010 = 00110010 = 50_{10}$

Adding the multiplicand to the high-order byte of the result is the same as adding $MCND \cdot 2^8$ to the full 16-bit result; shifting the 16-bit result one position to the right is equivalent to multiplying the result by 2^{-1} (dividing by 2).

Therefore, step one above produces:

$(BIT0 \cdot MCND \cdot 2^8) \cdot 2^{-1}$

Step two produces:

$((BIT0 \cdot MCND \cdot 2^8) \cdot 2^{-1} + (BIT1 \cdot MCND \cdot 2^8)) \cdot 2^{-1}$

$= BIT0 \cdot MCND \cdot 2^6 + BIT1 \cdot MCND \cdot 2^7$

And so on, until step eight produces:

$BIT0 \cdot MCND \cdot 2^0 + BIT1 \cdot MCND \cdot 2^1 + \ldots + BIT7 \cdot MCND \cdot 2^7$

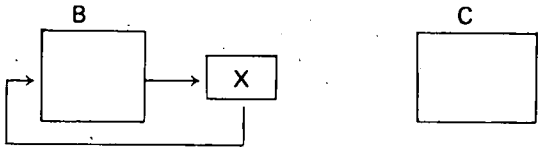
which is equivalent to Equation 1 above, and therefore is the correct result.

Since the multiplication routine described above uses a number of important programming techniques, a sample program is given with comments.

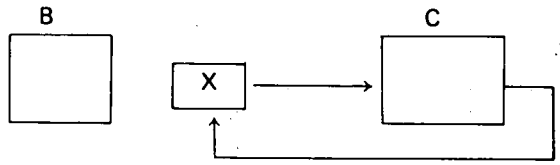
The program uses the B register to hold the most significant byte of the result, and the C register to hold the least significant byte of the result.

The 16-bit right shift of the result is performed by two rotate-right-through-carry instructions:

Zero carry and then rotate B



Then rotate C to complete the shift



Register D holds the multiplicand, and register C originally holds the multiplier.

```
MULT:   MVI   B, 0   ; Initialize most significant byte
                     ; of result
        MVI   E, 9   ; Bit counter
MULT0:  MOV   A, C   ; Rotate least significant bit of
        RAR          ; multiplier to carry and shift
        MOV   C, A   ; low-order byte of result
        DCR   E
        JZ    DONE ; Exit if complete
        MOV   A, B
        JNC   MULT1
        ADD   D      ; Add multiplicand to high-
                     ; order byte of result if bit
                     ; was a one
MULT1:  RAR          ; Carry=0 here; shift high-
                     ; order byte of result
        MOV   B, A
        JMP   MULT0
DONE:
```

An analogous procedure is used to divide an unsigned 16-bit number by an unsigned 16-bit number. Here, the process involves subtraction rather than addition, and rotate-left instructions instead of rotate-right instructions.

The following reentrant program uses the B and C registers to hold the dividend and quotient, and the D and E registers to hold the divisor and remainder. The H and L registers are used to store data temporarily.

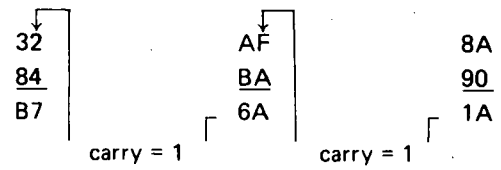
```
DIV: MOV     A,D     ; Negate the divisor
     CMA
     MOV     D,A
     MOV     A,E
     CMA
     MOV     E,A
     INX     D       ; For two's complement
     LXI     H,0     ; initial value for remainder
     MVI     A,17    ; initialize loop counter
DV0: PUSH    H       ; Save remainder
     DAD     D       ; subtract divisor (add negative)
     JNC     DV1     ; under flow, restore HL
     XTHL
DV1: POP     H
     PUSH    PSW     ; Save loop counter (A)
     MOV     A,C     ; 4 register left shift
     RAL             ; with carry
     MOV     C,A     ; CY -> C -> B -> L -> H
     MOV     A,B
     RAL
     MOV     B,A
     MOV     A,L
     RAL
     MOV     L,A
     MOV     A,H
     RAL
     MOV     H,A
     POP     PSW     ; Restore loop counter (A)
     DCR     A       ; decrement it
     JNZ     DV0     ; keep looping
;
; Post-divide clean up
; shift remainder right and return in DE
;
     ORA     A
     MOV     A,H
     RAR
     MOV     D,A
     MOV     A,L
     RAR
     MOV     E,A
     RET
     END
```

MULTIBYTE ADDITION AND SUBTRACTION

The carry bit and the ADC (add with carry) instructions may be used to add unsigned data quantities of arbitrary length. Consider the following addition of two three-byte unsigned hexadecimal numbers:

```
  32AF8A
+ 84BA90
  B76A1A
```

This addition may be performed on the 8080 by adding the two low-order bytes of the numbers, then adding the resulting carry to the two next-higher-order bytes, and so on:

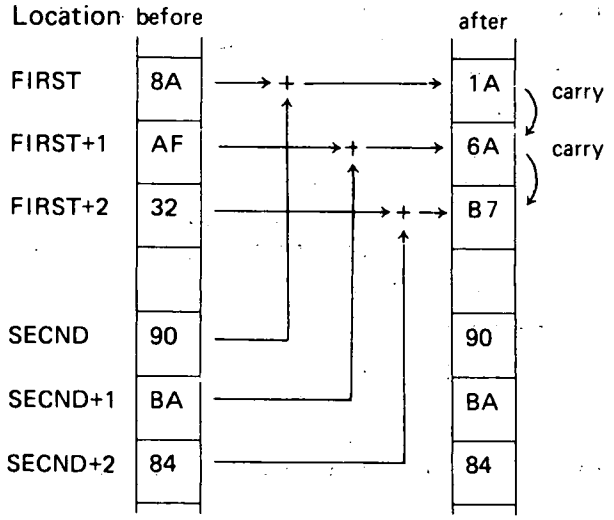


The following routine will perform this multibyte addition, making these assumptions:

The E register holds the length of each number to be added (in this case, 3).

The numbers to be added are stored from low-order byte to high-order byte beginning at memory locations FIRST and SECND, respectively.

The result will be stored from low-order byte to high-order byte beginning at memory location FIRST, replacing the original contents of these locations.




```
Label   Code    Operand     Comment
MADD:   LXI     B,FIRST     ; B and C address FIRST
        LXI     H,SECND     ; H and L address SECND
        XRA     A           ; Clear carry bit
LOOP:   LDAX    B           ; Load byte of FIRST
        ADC     M           ; Add byte of SECND
                            ; with carry
        STAX    B           ; Store result at FIRST
        DCR     E           ; Done if E = 0
        JZ      DONE
        INX     B           ; Point to next byte of
                            ; FIRST
        INX     H           ; Point to next byte of
                            ; SECND
        JMP     LOOP        ; Add next two bytes
DONE:   ---
        ---
FIRST:  DB      90H
        DB      0BAH
        DB      84H
SECND:  DB      8AH
        DB      0AFH
        DB      32H
```

Since none of the instructions in the program loop affect the carry bit except ADC, the addition with carry will proceed correctly.

When location DONE is reached, bytes FIRST through FIRST+2 will contain 1A6AB7, which is the sum shown at the beginning of this section arranged from low-order to high-order byte.

The carry (or borrow) bit and the SBB (subtract with borrow) instruction may be used to subtract unsigned data quantities of arbitrary length. Consider the following subtraction of two two-byte unsigned hexadecimal numbers:

```
  1301
- 0503
  0DFE
```

This subtraction may be performed on the 8080 by subtracting the two low-order bytes of the numbers, then using the resulting carry bit to adjust the difference of the two higher-order bytes if a borrow occurred (by using the SBB instruction).

Low-order subtraction (carry bit = 0 indicating no borrow):

```
00000001 = 01H
11111101 = -(03H+carry)
11111110 = 0FEH, the low-order result
```

carry out = 0, setting the Carry bit = 1, indicating a borrow

High-order subtraction:

```
00010011 = 13H
11111010 = -(05H+carry)
00001101
```

carry out = 1, resetting the Carry bit indicating no borrow

Whenever a borrow has occurred, the SBB instruction increments the subtrahend by one, which is equivalent to borrowing one from the minuend.

In order to create a multibyte subtraction routine, it is necessary only to duplicate the multibyte addition routine of this section, changing the ADC instruction to an SBB instruction. The program will then subtract the number beginning at SECND from the number beginning at FIRST, placing the result at FIRST.

DECIMAL ADDITION

Any 4-bit data quantity may be treated as a decimal number as long as it represents one of the decimal digits from 0 through 9, and does not contain any of the bit patterns representing the hexadecimal digits A through F. In order to preserve this decimal interpretation when performing addition, the value 6 must be added to the 4-bit quantity whenever the addition produces a result between 10 and 15. This is because each 4-bit data quantity can hold 6 more combinations of bits than there are decimal digits.

Decimal addition is performed on the 8080 by letting each 8-bit byte represent two 4-bit decimal digits. The bytes are summed in the accumulator in standard fashion, and the DAA (decimal adjust accumulator) instruction is then used as in Section 3, to convert the 8-bit binary result to the correct representation of 2 decimal digits. The settings of the carry and auxiliary carry bits also affect the operation of the DAA, permitting the addition of decimal numbers longer than two digits.

To perform the decimal addition:

```
  2985
+ 4936
  7921
```

the process works as follows:

(1) Clear the Carry and add the two lowest-order digits of each number (remember that each 2 decimal digits are represented by one byte).

```
    85 = 10000101B
    36 = 00110110B
 carry =        0
     0 10111011B
```

Carry = 0 Auxiliary Carry = 0

The accumulator now contains BBH.

(2) Perform a DAA operation. Since the rightmost four bits are ⩾ 10D, 6 will be added to the accumulator.

```
Accumulator = 10111011B
          6 =     0110B
            11000001B
```

Since the leftmost 4 bits are now 910, 6 will be added to these bits, setting the Carry bit.

```
Accumulator = 11000001B
          6 = 0110    B
            1 00100001B
```

Carry bit = 1

The accumulator now contains 21H. Store these two digits.

(3) Add the next group of two digits:

```
    29 = 00101001B
    49 = 01001001B
 carry =        1
     0 01110011B
```

Carry = 0 Auxiliary Carry = 1

The accumulator now contains 73H.

(4) Perform a DAA operation. Since the Auxiliary Carry bit is set, 6 will be added to the accumulator.

```
Accumulator = 01110011B
          6 =     0110B
            0 01111001B
```

carry bit = 0

Since the leftmost 4 bits are <10 and the Carry bit is reset, no further action occurs.

Thus, the correct decimal result 7921 is generated in two bytes.

A routine which adds decimal numbers, then, is exactly analogous to the multibyte addition routine MADD of the last section, and may be produced by inserting the instruction DAA after the ADC M instruction of that example.

Each iteration of the program loop will add two decimal digits (one byte) of the numbers.

DECIMAL SUBTRACTION

Each 4-bit data quantity may be treated as a decimal number as long as it represents one of the decimal digits 0 through 9. The DAA (decimal adjust accumulator) instruction may be used to permit subtraction of one byte (representing a 2-digit decimal number) from another, generating a 2-digit decimal result. In fact, the DAA permits subtraction of multidigit decimal numbers.

The process consists of generating the hundred's complement of the subtrahend digit (the difference between the subtrahend digit and 100 decimal), and adding the result to the minuend digit. For instance, to subtract 34D from 56D, the hundred's complement of 34D (100D-34D=66D) is added to 56D, producing 122D, which when truncated to 8 bits gives 22D, the correct result. If a borrow was generated by the previous subtraction, the 99's complement of the subtrahend digit is produced to compensate for the borrow.

In detail, the procedure for subtracting one multi-digit decimal from another is as follows:

(1) Set the Carry bit = 1 indicating no borrow.

(2) Load the accumulator with 99H, representing the number 99 decimal.

(3) Add zero to the accumulator with carry, producing either 99H or 9AH, and resetting the Carry bit.

(4) Subtract the subtrahend digits from the accumulator, producing either the 99's or 100's complement.

(5) Add the minuend digits to the accumulator.

(6) Use the DAA instruction to make sure the result in the accumulator is in decimal format, and to indicate a borrow in the Carry bit if one occurred.

Save this result.

(7) If there are more digits to subtract, go to step 2.

Otherwise, stop.

Example:

Perform the decimal subtraction:

```
  4358D
- 1362D
  2996D
```

(1) Set carry = 1.

(2) Load accumulator with 99H.

(3) Add zero with carry to the accumulator, producing 9AH.

```
Accumulator = 10011001B
          0 = 00000000B
      Carry =        1
              10011010B = 9AH
```

(4) Subtract the subtrahend digits 62H from the accumulator.

```
Accumulator = 10011010B
        62H = 10011110B
            1 00111000B
```

(5) Add the minuend digits 58H to the accumulator.

```
Accumulator = 00111000B
        58H = 01011000B
            0 10010000B = 90H
```

Carry = 0 ↗ ↖ Auxiliary Carry = 1

(6) DAA converts accumulator to 96H (since Auxiliary Carry = 1) and leaves Carry bit = 0 indicating that a borrow occurred.

(7) Load accumulator with 99H.

(8) Add zero with carry to accumulator, leaving accumulator = 99H.

(9) Subtract the subtrahend digits 13H from the accumulator.

```
Accumulator = 10011001B
        13H = 11101101B
            1 10000110B
```

(10) Add the minuend digits 43H to the accumulator.

```
Accumulator = 10000110B
        43H = 01000011B
            0 11001001B = C9H
```

Carry = 0 ↗ ↖ Auxiliary Carry = 0

(11) DAA converts accumulator to 29H and sets the carry bit = 1, indicating no borrow occurred.

Therefore, the result of subtracting 1362D from 4358D is 2996D.

The following subroutine will subtract one 16-digit decimal number from another using the following assumptions:

The minuend is stored least significant (2) digits first beginning at location MINU.

The subtrahend is stored least significant (2) digits first beginning at location SBTRA.

The result will be stored least significant (2) digits first, replacing the minuend.

```
Label   Code    Operand     Comment
DSUB:   LXI     D, MINU     ; D and E address minuend
        LXI     H,SBTRA     ; H and L address subtra-
                            ; hend
        MVI     C, 8        ; Each loop subtracts 2
                            ; digits (one byte),
                            ; therefore program will
                            ; subtract 16 digits.
        STC                 ; Set Carry indicating
                            ; no borrow
LOOP:   MVI     A, 99H      ; Load accumulator
                            ; with 99H.
        ACI     0           ; Add zero with Carry
        SUB     M           ; Produce complement
                            ; of subtrahend
        XCHG                ; Switch D and E with
                            ; H and L
        ADD     M           ; Add minuend
        DAA                 ; Decimal adjust
                            ; accumulator
        MOV     M, A        ; Store result
        XCHG                ; Reswitch D and E
                            ; with H and L
        DCR     C           ; Done if C = 0
        JZ      DONE
        INX     D           ; Address next byte
                            ; of minuend
        INX     H           ; Address next byte
                            ; of subtrahend
        JMP     LOOP        ; Get next 2 decimal digits
DONE:   NOP
```

ALTERING MACRO EXPANSIONS

This section describes how a macro may be written such that identical references to the macro produce different expansions. As a useful example of this, consider a macro SBMAC which needs to call a subroutine SUBR to perform its function. One way to provide the macro with the necessary subroutine would be to include a separate copy of the subroutine in any program which contains the macro. A better method is to let the macro itself generate the subroutine during the first macro expansion, but skip the generation of the subroutine on any subsequent expansion. This may be accomplished as follows:

Consider the following program section which consists of one global set statement and the definition of SBMAC (dashes indicate those assembly language statements necessary to the program, but irrelevant to this discussion):

```
Label   Code    Operand
FIRST   SET     0FFH
SBMAC   MACRO
        --
        --
        CALL    SUBR
        --
        --
        IF      FIRST
FIRST   SET     0
        JMP     OUT
SUBR::  --
        --
        RET
OUT:    NOP
        ENDIF
        ENDM
```

The symbol FIRST is set to FFH, then the macro SBMAC is defined.

The first time SBMAC is referenced, the expansion produced will be the following:

```
Label   Code    Operand
        SBMAC
        --
        --
        CALL    SUBR
        --
        --
        IF      FIRST
FIRST   SET     0
        JMP     OUT
SUBR:   --
        --
        RET
OUT:    NOP
```

Since FIRST is non-zero when encountered during this expansion, the statements between the IF and ENDIF are assembled into the program. The first statement thus assembled sets the value of FIRST to 0, while the remaining statements are the necessary subroutine SUBR and a jump around the subroutine. When this portion of the program is executed, the subroutine SUBR will be called, but program execution will not flow into the subroutine's definition.

On any subsequent reference to SBMAC in the program, however, the following expansion will be produced:

```
Label   Code    Operand
        SBMAC
        --
        --
        CALL    SUBR
        --
        --
        IF      FIRST
```

Since FIRST is now equal to zero, the IF statement ends the macro expansion and does not cause the subroutine to be generated again. The label SUBR is known during this expansion because it was defined globally (followed by two colons in the definition).

CHAPTER 5
INTERRUPTS

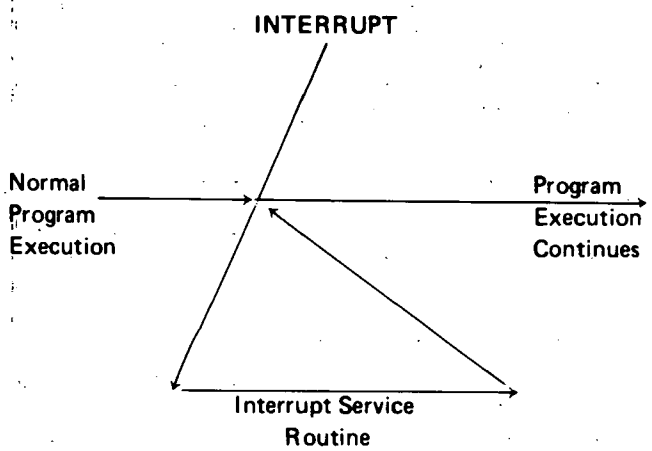
Often, events occur external to the central processing unit which require immediate action by the CPU. For example, suppose a device is receiving a string of 80 characters from the CPU, one at a time, at fixed intervals. There are two ways to handle such a situation:

(a) A program could be written which inputs the first character, waits until the next character is ready (e.g., executes a timeout by incrementing a sufficiently large counter), then inputs the next character, and proceeds in this fashion until the entire 80 character string has been received.

This method is referred to as programmed Input/Output.

(b) The device controller could interrupt the CPU when a character is ready to be input, forcing a branch from the executing program to a special interrupt service routine.

The interrupt sequence may be illustrated as follows:



The 8080 contains a bit named INTE which may be set or reset by the instructions EI and DI described in Chapter 2. Whenever INTE is equal to 0, the entire interrupt handling system is disabled, and no interrupts will be accepted.

When the CPU recognizes an interrupt request from an external device, the following actions occur:

(1) The instruction currently being executed is completed.

(2) The interrupt enable bit, INTE, is reset = 0.

(3) The interrupting device supplies, via hardware, one instruction which the CPU executes. This instruction does not appear anywhere in memory, and the programmer has no control over it, since it is a function of the interrupting device's controller design. The program counter is not incremented before this instruction.

The instruction supplied by the interrupting device is normally an RST instruction (see Chapter 2), since this is an efficient one byte call to one of 8 eight-byte subroutines located in the first 64 words of memory. For instance, the teletype may supply the instruction:

RST 0H

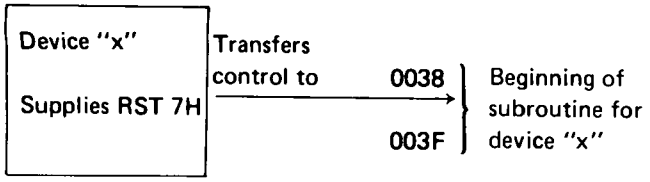
with each teletype input interrupt. Then the subroutine which processes data transmitted from the teletype to the CPU will be called into execution via an eight-byte instruction sequence at memory locations 0000H to 0007H.

A digital input device may supply the instruction:

RST 1H

Then the subroutine that processes the digital input signals will be called via a sequence of instructions occupying memory locations 0008H to 000FH.

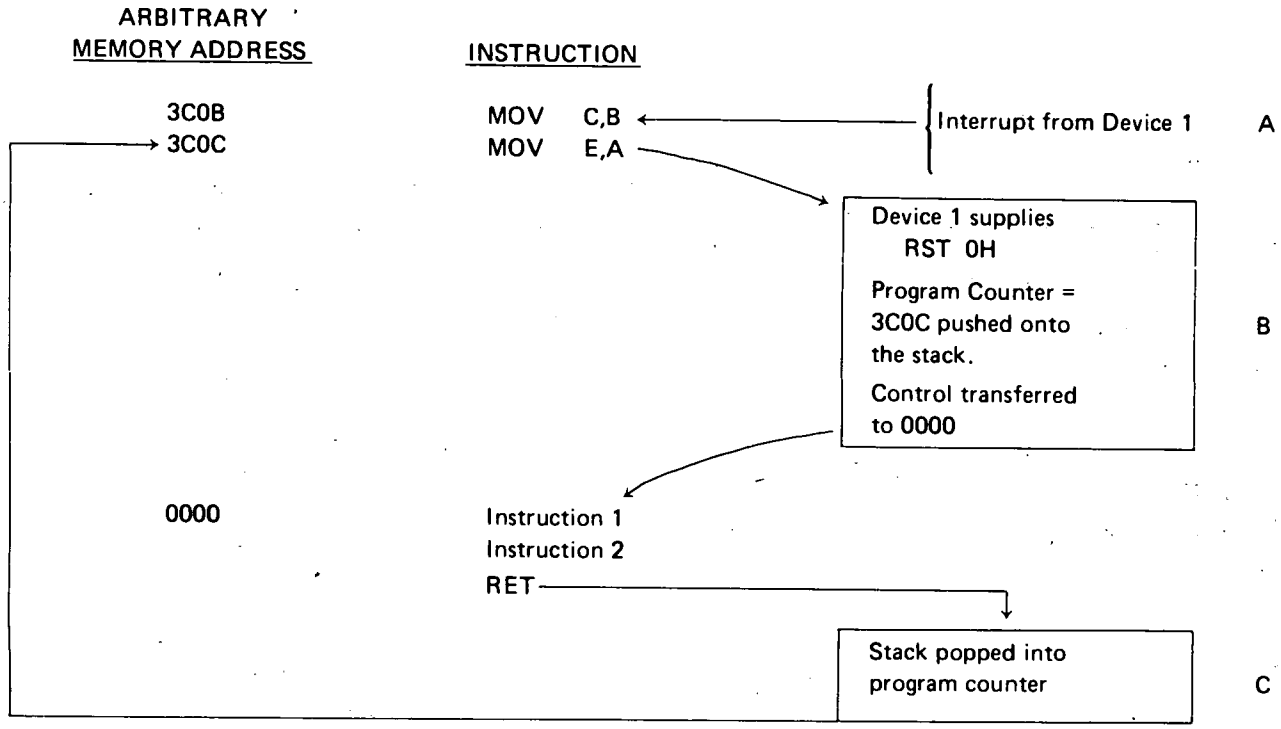
Device "a" Supplies RST 0H	Transfers control to	0000 0007	Beginning of subroutine for device "a"
Device "b" Supplies RST 1H	Transfers control to	0008 000F	Beginning of subroutine for device "b"



Note that any of these 8-byte subroutines may in turn call longer subroutines to process the interrupt, if necessary.

Any device may supply an RST instruction (and indeed may supply any 8080 instruction).

The following is an example of an Interrupt sequence:



Device 1 signals an interrupt as the CPU is executing the instruction at 3C0B. This instruction is completed. The program counter remains set to 3C0C, and the instruction RST 0H supplied by device 1 is executed. Since this is a call to location zero, 3C0C is pushed onto the stack and program control is transferred to location 0000H. (This subroutine may perform jumps, calls, or any other operation.) When the RETURN is executed, address 3C0C is popped off the stack and replaces the contents of the program counter, causing execution to continue at this point.

WRITING INTERRUPT SUBROUTINES

In general, any registers or condition bits changed by an interrupt subroutine must be restored before returning to the interrupted program, or errors will occur.

For example, suppose a program is interrupted just prior to the instruction:

JC LOC

and the carry bit equals 1. If the interrupt subroutine happens to zero the carry bit just before returning to the interrupted program, the jump to LOC which should have occurred will not, causing the interrupted program to produce erroneous results.

Like any other subroutine then, any interrupt subroutine should save at least the condition bits and restore them before performing a RETURN operation. (The obvious and most convenient way to do this is to save the data in the stack, using PUSH and POP operations.)

Further, the interrupt enable system is automatically disabled whenever an interrupt is acknowledged. Except in special cases, therefore, an interrupt subroutine should include an EI instruction somewhere to permit detection and handling of future interrupts. One instruction after an EI is executed, the interrupt subroutine may itself be interrupted. This process may continue to any level, but as long as all pertinent data are saved and restored, correct program execution will continue automatically.

A typical interrupt subroutine, then, could appear as follows:

```
Code    Operand          Comment
PUSH    PSW     ; Save condition bits and accumulator
EI              ; Re-enable interrupts
 .              ;
 .              ; Perform necessary actions to service
 .              ; the interrupt
 .
 .
POP     PSW     ; Restore machine status
RET             ; Return to interrupted program
```

APPENDIX A
INSTRUCTION SUMMARY

This appendix provides a summary of 8080 assembly language instructions. Abbreviations used are as follows:

A	The accumulator (register A)
A_n	Bit n of the accumulator contents, where n may have any value from 0 to 7 and 0 is the least significant (rightmost) bit
ADDR	Any memory address
Aux. carry	The auxiliary carry bit
Carry	The carry bit
CODE	An operation code
DATA	8 bits (one byte) of data
DATA16	16 bits (2 bytes) of data
DST	Destination register or memory byte
EXP	A constant or mathematical expression
INTE	The 8080 interrupt enable flip-flop
LABEL:	Any instruction label
M	A memory byte
Parity	The parity bit
PC	Program Counter
PCH	The most significant 8 bits of the program counter
PCL	The least significant 8 bits of the program counter
REGM	Any register or memory byte

REGPR	A register pair. Legal register pair symbols are: B for registers B and C D for registers D and E H for registers H and L SP for the 16 bit stack pointer PSW for register A and flag bits
RP1	The first register of register pair RP
RP2	The second register of register pair RP
Sign	The sign bit
SP	The 16-bit stack pointer register
SRC	Source register or memory byte
Zero	The zero bit
XY	The value obtained by concatenating the values X and Y
[ ]	An optional field enclosed by brackets
( )	Contents of register or memory byte enclosed by parentheses
←	Replace value on lefthand side of arrow with value on righthand side of arrow
$	Present contents of program counter

CARRY BIT INSTRUCTIONS

Format:

```
[LABEL:]          CODE
```

CODE	DESCRIPTION	
STC	(Carry) ← 1	Set carry
CMC	(Carry) ← ($\overline{\text{Carry}}$)	Complement carry

Condition bits affected: Carry

SINGLE REGISTER INSTRUCTIONS

Format:

```
[LABEL:]    INR     REGM
            -or-
[LABEL:]    DCR     REGM
            -or-
[LABEL:]    CMA
            -or-
[LABEL:]    DAA
```

CODE	DESCRIPTION	
INR	(REGM) ← (REGM)+1	Increment register REGM
DCR	(REGM) ← (REGM)-1	Decrement register REGM
CMA	(A) ← ($\overline{A}$)	Complement accumulator
DAA	If $(A_0\text{-}A_3) > 9$ or (Aux. Carry)=1, (A) ← (A)+6 Then if $(A_4\text{-}A_7) > 9$ or (Carry)= 1 (A) = (A) + 6 · 2^4	Convert accumulator contents to form two decimal digits

Condition bits affected:
INR,DCR : Zero, sign, parity, aux. carry
CMA : None
DAA : Zero, sign, parity, carry, aux. carry

NOP INSTRUCTION

Format:

[LABEL:] NOP

CODE	DESCRIPTION
NOP	No operation

Condition bits affected: None

DATA TRANSFER INSTRUCTIONS

Format:

[LABEL:] MOV DST,SRC
—or—
[LABEL:] CODE REGPR

NOTE: SRC and DST not both = M

NOTE: RP = B or D

CODE	DESCRIPTION	
MOV	(DST) ← (SRC)	Load register DST from register SRC
STAX	((REGPR)) ← (A)	Store accumulator at memory location referenced by the specified register pair
LDAX	(A) ← ((REGPR))	Load accumulator from memory location referenced by the specified register pair

Condition bits affected: None

REGISTER OR MEMORY TO ACCUMULATOR INSTRUCTIONS

Format:

[LABEL:] CODE REGM

CODE	DESCRIPTION	
ADD	(A) ← (A)+(REGM)	Add REGM to accumulator
ADC	(A) ← (A)+(REGM)+(Carry)	Add REGM to accumulator with carry
SUB	(A) ← (A)-(REGM)	Subtract REGM from accumulator
SBB	(A) ← (A)-(REGM)-(Carry)	Subtract REGM from accumulator with borrow
ANA	(A) ← (A) AND (REGM)	AND accumulator with REGM
XRA	(A) ← (A) XOR (REGM)	EXCLUSIVE-ORaccumulator with REGM
ORA	(A) ← (A) OR (REGM)	OR accumulator with REGM
CMP	Condition bits set by (A)-(REGM)	Compare REGM with accumulator

Condition bits affected:

ADD, ADC, SUB, SBB: Carry, Sign, Zero, Parity, Aux. Carry
ANA, XRA, ORA: Sign, Zero, Parity. Carry and Aux. Carry are reset.
CMP: Carry, Sign, Zero, Parity, Aux. Carry. Zero set if (A)=(REGM)
Zero reset if (A) ≠ (REGM)
Carry set if (A) < (REGM)
Carry reset if (A) ⩾ (REGM)
Note: CMP treats (A) and (REGM) as unsigned 8-bit quantities.

ROTATE ACCUMULATOR INSTRUCTIONS

Format:

[LABEL:] CODE

CODE	DESCRIPTION	
RLC	(Carry) ← A_7, A_{n+1}, ← A_n, A_0 ← A_7	Set Carry = A_7, rotate accumulator left
RRC	(Carry) ← A_0, A_n ← A_{n+1}, A_7 ← A_0	Set Carry = A_0, rotate accumulator right
RAL	A_{n+1} ← A_n, (Carry) ← A_7, A_0 ← (Carry)	Rotate accumulator left through the Carry
RAR	A_n ← A_{n+1}, (Carry) ← A_0, A_7 ← (Carry)	Rotate accumulator right through Carry

Condition bits affected: Carry

REGISTER PAIR INSTRUCTIONS

Format:

[LABEL:]	CODE1	REGPR
	—or—	
[LABEL:]	CODE2	

NOTE: For PUSH and POP, REGPR=B, D, H, or PSW
For DAD, INX, and DCX, REGPR=B, D, H, or SP

CODE1	DESCRIPTION	
PUSH	((SP)-1) ← (REGPR1), ((SP)-2) ← (REGPR2), (SP) ← (SP)-2	Save REGPR on the stack REGPR=PSW saves accumulator and condition bits
POP	(REGPR1) ← ((SP)+1), (REGPR2) ← ((SP)), (SP) ← (SP)+2	Restore REGPR from the stack REGPR=PSW restores accumulator and condition bits
DAD	(HL) ← (HL) + (REGPR)	Add REGPR to the 16-bit number in H and L
INX	(REGPR) ← (REGPR)+1	Increment REGPR by 1
DCX	(REGPR) ← (REGPR)–1	Decrement REGPR by 1
CODE2	**DESCRIPTION**	
XCHG	(H) ⟷ (D), (L) ⟷ (E)	Exchange the 16 bit number in H and L with that in D and E
XTHL	(L) ⟷ ((SP)), (H) ⟷ ((SP)+1)	Exchange the last values saved in the stack with H and L
SPHL	(SP) ← (H):(L)	Load stack pointer from H and L

Condition bits affected:

PUSH, INX, DCX, XCHG, XTHL, SPHL: None
POP : If REGPR=PSW, all condition bits are restored from the stack, otherwise none are affected.
DAD : Carry

IMMEDIATE INSTRUCTIONS

Format:

[LABEL:]	LXI	REGPR, DATA16
	—or—	
[LABEL:]	MVI	REGM, DATA
	—or—	
[LABEL:]	CODE	REGM

NOTE: REGPR=B, D, H, or SP

CODE	DESCRIPTION	
LXI	(REGPR) ← DATA 16	Move 16-bit immediate Data into REGPR
MVI	(REGM) ← DATA	Move immediate DATA into REGM
ADI	(A) ← (A) + DATA	Add immediate data to accumulator
ACI	(A) ← (A) + DATA + (Carry)	Add immediate data to accumulator with Carry
SUI	(A) ← (A) - DATA	Subtract immediate data from accumulator
SBI	(A) ← (A) - DATA - (Carry)	Subtract immediate data from accumulator with borrow
ANI	(A) ← (A) AND DATA	AND accumulator with immediate data
XRI	(A) ← (A) XOR DATA	EXCLUSIVE-OR accumulator with immediate data
ORI	(A) ← (A) OR DATA	OR accumulator with immediate data
CPI	Condition bits set by (A)-DATA	Compare immediate data with accumulator

Condition bits affected:

LXI, MVI: None
ADI, ACI, SUI, SBI: Carry, Sign, Zero, Parity, Aux. Carry
ANI, XRI, ORI: Zero, Sign, Parity. Carry and Aux. Carry are reset.
CPI: Carry, Sign, Zero, Parity, Aux. Carry. Zero set if (A) = DATA
Zero reset if (A) ≠ DATA
Carry set if (A) < DATA
Carry reset if (A) ≥ DATA
Note: CPI treats (A) and DATA as unsigned 8-bit quantities.

DIRECT ADDRESSING INSTRUCTIONS

Format:

[LABEL:] CODE ADDR

CODE	DESCRIPTION	
STA	(ADDR) ← (A)	Store accumulator at location ADDR
LDA	(A) ← (ADDR)	Load accumulator from location ADDR
SHLD	(ADDR) ← (L), (ADDR+1) ← (H)	Store L and H at ADDR and ADDR+1
LHLD	(L) ← (ADDR), (H) ← (ADDR+!)	Load L and H from ADDR and ADDR+1

Condition bits affected: None

JUMP INSTRUCTIONS

Format:

[LABEL:] PCHL
—or—
[LABEL:] CODE ADDR

CODE	DESCRIPTION	
PCHL	(PC) ← (HL)	Jump to location specified by register H and L
JMP	(PC) ← ADDR	Jump to location ADDR
JC	If (Carry) = 1, (PC) ← ADDR If (Carry) = 0, (PC) ← (PC)+3	Jump to ADDR if Carry set
JNC	If (Carry) = 0, (PC) ← ADDR If (Carry) = 1, (PC) ← (PC)+3	Jump to ADDR if Carry reset
JZ	If (Zero) = 1, (PC) ← ADDR If (Zero) = 0, (PC) ← (PC)+3	Jump to ADDR if Zero set
JNZ	If (Zero) = 0, (PC) ← ADDR If (Zero) = 1, (PC) ← (PC)+3	Jump to ADDR if Zero reset
JP	If (Sign) = 0, (PC) ← ADDR If (Sign) = 1, (PC) ← (PC)+3	Jump to ADDR if plus
JM	If (Sign) = 1, (PC) ← ADDR If (Sign) = 0, (PC) ← (PC)+3	Jump to ADDR if minus
JPE	If (Parity) = 1, (PC) ← ADDR If (Parity) = 0, (PC) ← (PC)+3	Jump to ADDR if parity even
JPO	If (Parity) = 0, (PC) ← ADDR If (Parity) = 1, (PC) ← (PC)+3	Jump to ADDR if parity odd

Condition bits affected: None

CALL INSTRUCTIONS

Format:

[LABEL:] CODE ADDR

CODE	DESCRIPTION
CALL	((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR Call subroutine and push return address onto stack
CC	If (Carry) = 1, ((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR If (Carry) = 0, (PC) ← (PC)+3 Call subroutine if Carry set
CNC	If (Carry) = 0, ((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR If (Carry) = 1, (PC) ← (PC)+3 Call subroutine if Carry reset
CZ	If (Zero) = 1, ((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR If (Zero) = 0, (PC) ← (PC)+3 Call subroutine if Zero set
CNZ	If (Zero) = 0, ((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR If (Zero) = 1, (PC) ← (PC)+3 Call subroutine if Zero reset
CP	If (Sign) = 0, ((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR If (Sign) = 1, (PC) ← (PC)+3 Call subroutine if Sign plus
CM	If (Sign) = 1, ((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR If (Sign) = 0, (PC) ← (PC)+3 Call subroutine if Sign minus
CPE	If (Parity) = 1, ((SP) -1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR If (Parity) = 0, (PC) ← (PC)+3 Call subroutine if Parity even
CPO	If (Parity) = 0, ((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2, (PC) ← ADDR If (Parity) = 1, (PC) ← (PC)+3 Call subroutine if Parity odd

Condition bits affected: None

RETURN INSTRUCTIONS

Format:

[LABEL:] CODE

CODE	DESCRIPTION
RET	(PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP)+2 Return from subroutine
RC	If (Carry) = 1, (PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP) +2 If (Carry) = 0, (PC) ← (PC)+1 Return if Carry set
RNC	If (Carry) = 0, (PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP)+2 If (Carry) = 1, (PC) ← (PC)+1 Return if Carry reset
RZ	If (Zero) = 1, (PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP)+2 If (Zero) = 0, (PC) ← (PC)+1 Return if Zero set
RNZ	If (Zero) = 0, (PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP) ← (SP)+2 If (Zero) = 1, (PC) ← (PC)+1 Return if Zero reset
RM	If (Sign) = 1, (PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP)+2 If (Sign) = 0, (PC) ← (PC)+1 Return if minus
RP	If (Sign) = 0, (PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP)+2 If (Sign) = 1, (PC) ← (PC)+1 Return if plus
RPE	If (Parity) = 1, (PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP)+2 If (Parity) = 0, (PC) ← (PC)+1 Return if parity even
RPO	If (Parity) = 0, (PCL) ← ((SP)), (PCH) ← ((SP)+1), (SP) ← (SP)+2 If (Parity) = 1, (PC) ← (PC)+1 Return if parity odd

Condition bits affected: None

RST INSTRUCTION

Format:

[LABEL:] RST EXP

NOTE: 000B ⩽ EXP ⩽ 111B

CODE	DESCRIPTION
RST	((SP)-1) ← (PCH), ((SP)-2) ← (PCL), (SP) ← (SP) -2 (PC) ← 0000000000EXP000B Call subroutine at address specified by EXP

Condition bits affected: None

INTERRUPT FLIP-FLOP INSTRUCTIONS

Format:

[LABEL:] CODE

CODE	DESCRIPTION	
EI	(INTE) ← 1	Enable the interrupt system
DI	(INTE) ← 0	Disable the interrupt system

Condition bits affected: None

INPUT/OUTPUT INSTRUCTIONS

Format:

[LABEL:] CODE EXP

CODE	DESCRIPTION	
IN	(A) ← input device	Read a byte from device EXP into the accumulator
OUT	output device ← (A)	Send the accumulator contents to device EXP

Condition bits affected: None

HLT INSTRUCTION

Format:

[LABEL:] HLT

CODE	DESCRIPTION	
HLT	----------	Instruction execution halts until an interrupt occurs

Condition bits affected: None

PSEUDO – INSTRUCTIONS

ORG PSEUDO – INSTRUCTION

Format:

ORG EXP

CODE	DESCRIPTION	
ORG	LOCATION COUNTER ← EXP	Set Assembler location counter to EXP

EQU PSEUDO – INSTRUCTION

Format:

NAME EQU EXP

CODE	DESCRIPTION	
EQU	NAME ← EXP	Assign the value EXP to the symbol NAME

SET PSEUDO – INSTRUCTION

Format:

NAME SET EXP

CODE	DESCRIPTION	
SET	NAME ← EXP	Assign the value EXP to the symbol NAME, which may have been previously SET.

END PSEUDO – INSTRUCTION

Format:

END

CODE	DESCRIPTION
END	End the assembly

CONDITIONAL ASSEMBLY PSEUDO – INSTRUCTIONS

Format:

IF EXP

–and–

ENDIF

CODE	DESCRIPTION
IF	If EXP = 0, ignore assembler statements until ENDIF is reached. Otherwise, continue assembling statements
ENDIF	End range of preceding IF

MACRO DEFINITION PSEUDO – INSTRUCTIONS

Format:

NAME MACRO LIST

–and–

ENDM

CODE	DESCRIPTION
MACRO	Define a macro named NAME with parameters LIST
ENDM	End Macro definition

TITLE PSEUDO – INSTRUCTION

Format:

TITLE 'STRING'

CODE	DESCRIPTION
TITLE	Define 'title' to appear beneath page header.

APPENDIX B
INSTRUCTION EXECUTION TIMES AND BIT PATTERNS AND OPERATION CODES

This appendix summarizes the bit patterns and number of time states associated with every 8080 CPU instruction.

The instructions are listed in both mnemonic (alphabetical) and operation code (numerical) sequence.

When using this summary, note the following symbology:

1) DDD represents a destination register. SSS represents a source register. Both DDD and SSS are interpreted as follows:

DDD or SSS	Interpretation
000	Register B
001	Register C
010	Register D
011	Register E
100	Register H
101	Register L
110	A memory register
111	The accumulator

2) Instruction execution time equals number of time periods multiplied by the duration of a time period.

A time period may vary from 480 nanosecs to 2 μsec.

Where two numbers of time periods are shown (eq. 5/11), it means that the smaller number of time periods will be required if a condition is not met, and the larger number of time periods will be required if the condition is met.

MNEMONIC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	NUMBER OF TIME PERIODS
CALL	1	1	0	0	1	1	0	1	17
CC	1	1	0	1	1	1	0	0	11/17
CNC	1	1	0	1	0	1	0	0	11/17
CZ	1	1	0	0	1	1	0	0	11/17
CNZ	1	1	0	0	0	1	0	0	11/17
CP	1	1	1	1	0	1	0	0	11/17
CM	1	1	1	1	1	1	0	0	11/17
CPE	1	1	1	0	1	1	0	0	11/17
CPO	1	1	1	0	0	1	0	0	11/17
RET	1	1	0	0	1	0	0	1	10
RC	1	1	0	1	1	0	0	0	5/11
RNC	1	1	0	1	0	0	0	0	5/11
RZ	1	1	0	0	1	0	0	0	5/11
RNZ	1	1	0	0	0	0	0	0	5/11
RP	1	1	1	1	0	0	0	0	5/11
RM	1	1	1	1	1	0	0	0	5/11
RPE	1	1	1	0	1	0	0	0	5/11
RPO	1	1	1	0	0	0	0	0	5/11

MNEMONIC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	NUMBER OF TIME PERIODS
RST	1	1	A	A	A	1	1	1	11
IN	1	1	0	1	1	0	1	1	10
OUT	1	1	0	1	0	0	1	1	10
LXI B	0	0	0	0	0	0	0	1	10
LXI D	0	0	0	1	0	0	0	1	10
LXI H	0	0	1	0	0	0	0	1	10
LXI SP	0	0	1	1	0	0	0	1	10
PUSH B	1	1	0	0	0	1	0	1	11
PUSH D	1	1	0	1	0	1	0	1	11
PUSH H	1	1	1	0	0	1	0	1	11
PUSH PSW	1	1	1	1	0	0	0	1	11
POP B	1	1	0	0	0	0	0	1	10
POP D	1	1	0	1	0	0	0	1	10
POP H	1	1	1	0	0	0	0	1	10
POP PSW	1	1	1	1	0	0	0	1	10
STA	0	0	1	1	0	0	1	0	13
LDA	0	0	1	1	1	0	1	0	13
XCHG	1	1	1	0	1	0	1	1	4
XTHL	1	1	1	0	0	0	1	1	18
SPHL	1	1	1	1	1	0	0	1	5
PCHL	1	1	1	0	1	0	0	1	5
DAD B	0	0	0	0	1	0	0	1	10
DAD D	0	0	0	1	1	0	0	1	10
DAD H	0	0	1	0	1	0	0	1	10
DAD SP	0	0	1	1	1	0	0	1	10
STAX B	0	0	0	0	0	0	1	0	7
STAX D	0	0	0	1	0	0	1	0	7
LDAX B	0	0	0	0	1	0	1	0	7
LDAX D	0	0	0	1	1	0	1	0	7
INX B	0	0	0	0	0	0	1	1	5
INX D	0	0	0	1	0	0	1	1	5
INX H	0	0	1	0	0	0	1	1	5
INX SP	0	0	1	1	0	0	1	1	5
MOV r_1, r_2	0	1	D	D	D	S	S	S	5
MOV M, r	0	1	1	1	0	S	S	S	7
MOV r, M	0	1	D	D	D	1	1	0	7
HLT	0	1	1	1	0	1	1	0	7
MVI r	0	0	D	D	D	1	1	0	7
MVI M	0	0	1	1	0	1	1	0	10
INR	0	0	D	D	D	1	0	0	5
DCR	0	0	D	D	D	1	0	1	5
INR A	0	0	1	1	1	1	0	0	5
DCR A	0	0	1	1	1	1	0	1	5
INR M	0	0	1	1	0	1	0	0	10
DCR M	0	0	1	1	0	1	0	1	10
ADD r	1	0	0	0	0	S	S	S	4
ADC r	1	0	0	0	1	S	S	S	4
SUB r	1	0	0	1	0	S	S	S	4
SBB r	1	0	0	1	1	S	S	S	4
AND r	1	0	1	0	0	S	S	S	4
XRA r	1	0	1	0	1	S	S	S	4
ORA r	1	0	1	1	0	S	S	S	4
CMP r	1	0	1	1	1	S	S	S	4
ADD M	1	0	0	0	0	1	1	0	7
ADC M	1	0	0	0	1	1	1	0	7

MNEMONIC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	NUMBER OF TIME PERIODS
SUB M	1	0	0	1	0	1	1	0	7
SBB M	1	0	0	1	1	1	1	0	7
AND M	1	0	1	0	0	1	1	0	7
XRA M	1	0	1	0	1	1	1	0	7
ORA M	1	0	1	1	0	1	1	0	7
CMP M	1	0	1	1	1	1	1	0	7
ADI	1	1	0	0	0	1	1	0	7
ACI	1	1	0	0	1	1	1	0	7
SUI	1	1	0	1	0	1	1	0	7
SBI	1	1	0	1	1	1	1	0	7
ANI	1	1	1	0	0	1	1	0	7
XRI	1	1	1	0	1	1	1	0	7
ORI	1	1	1	1	0	1	1	0	7
CPI	1	1	1	1	1	1	1	0	7
RLC	0	0	0	0	0	1	1	1	4
RRC	0	0	0	0	1	1	1	1	4
RAL	0	0	0	1	0	1	1	1	4
RAR	0	0	0	1	1	1	1	1	4
JMP	1	1	0	0	0	0	1	1	10
JC	1	1	0	1	1	0	1	0	10
JNC	1	1	0	1	0	0	1	0	10
JZ	1	1	0	0	1	0	1	0	10
JNZ	1	1	0	0	0	0	1	0	10
JP	1	1	1	1	0	0	1	0	10
JM	1	1	1	1	1	0	1	0	10
JPE	1	1	1	0	1	0	1	0	10
JPO	1	1	1	0	0	0	1	0	10
DCX B	0	0	0	0	1	0	1	1	5
DCX D	0	0	0	1	1	0	1	1	5
DCX H	0	0	1	0	1	0	1	1	5
DCX SP	0	0	1	1	1	0	1	1	5
CMA	0	0	1	0	1	1	1	1	4
STC	0	0	1	1	0	1	1	1	4
CMC	0	0	1	1	1	1	1	1	4
DAA	0	0	1	0	0	1	1	1	4
SHLD	0	0	1	0	0	0	1	0	16
LHLD	0	0	1	0	1	0	1	0	16
EI	1	1	1	1	1	0	1	1	4
DI	1	1	1	1	0	0	1	1	4
NOP	0	0	0	0	0	0	0	0	4

8080 CPU INSTRUCTIONS IN OPERATION CODE SEQUENCE

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M
01	LXI B,D16	2C	INR L	57	MOV D,A
02	STAX B	2D	DCR L	58	MOV E,B
03	INX B	2E	MVI L,D8	59	MOV E,C
04	INR B	2F	CMA	5A	MOV E,D
05	DCR B	30	---	5B	MOV E,E
06	MVI B,D8	31	LXI SP,D16	5C	MOV E,H
07	RLC	32	STA Adr	5D	MOV E,L
08	---	33	INX SP	5E	MOV E,M
09	DAD B	34	INR M	5F	MOV E,A
0A	LDAX B	35	DCR M	60	MOV H,B
0B	DCX B	36	MVI M,D8	61	MOV H,C
0C	INR C	37	STC	62	MOV H,D
0D	DCR C	38	---	63	MOV H,E
0E	MVI C,D8	39	DAD SP	64	MOV H,H
0F	RRC	3A	LDA Adr	65	MOV H,L
10	---	3B	DCX SP	66	MOV H,M
11	LXI D,D16	3C	INR A	67	MOV H,A
12	STAX D	3D	DCR A	68	MOV L,B
13	INX D	3E	MVI A,D8	69	MOV L,C
14	INR D	3F	CMC	6A	MOV L,D
15	DCR D	40	MOV B,B	6B	MOV L,E
16	MVI D,D8	41	MOV B,C	6C	MOV L,H
17	RAL	42	MOV B,D	6D	MOV L,L
18	---	43	MOV B,E	6E	MOV L,M
19	DAD D	44	MOV B,H	6F	MOV L,A
1A	LDAX D	45	MOV B,L	70	MOV M,B
1B	DCX D	46	MOV B,M	71	MOV M,C
1C	INR E	47	MOV B,A	72	MOV M,D
1D	DCR E	48	MOV C,B	73	MOV M,E
1E	MVI E,D8	49	MOV C,C	74	MOV M,H
1F	RAR	4A	MOV C,D	75	MOV M,L
20	---	4B	MOV C,E	76	HLT
21	LXI H,D16	4C	MOV C,H	77	MOV M,A
22	SHLD Adr	4D	MOV C,L	78	MOV A,B
23	INX H	4E	MOV C,M	79	MOV A,C
24	INR H	4F	MOV C,A	7A	MOV A,D
25	DCR H	50	MOV D,B	7B	MOV A,E
26	MVI H,D8	51	MOV D,C	7C	MOV A,H
27	DAA	52	MOV D,D	7D	MOV A,L
28	---	53	MOV D,E	7E	MOV A,M
29	DAD H	54	MOV D,H	7F	MOV A,A
2A	LHLD Adr	55	MOV D,L	80	ADD B

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
81	ADD C	AC	XRA H	D7	RST 2
82	ADD D	AD	XRA L	D8	RC
83	ADD E	AE	XRA M	D9	---
84	ADD H	AF	XRA A	DA	JC Adr
85	ADD L	B0	ORA B	DB	IN D8
86	ADD M	B1	ORA C	DC	CC Adr
87	ADD A	B2	ORA D	DD	---
88	ADC B	B3	ORA E	DE	SBI D8
89	ADC C	B4	ORA H	DF	RST 3
8A	ADC D	B5	ORA L	E0	RPO
8B	ADC E	B6	ORA M	E1	POP H
8C	ADC H	B7	ORA A	E2	JPO Adr
8D	ADC L	B8	CMP B	E3	XTHL
8E	ADC M	B9	CMP C	E4	CPO Adr
8F	ADC A	BA	CMP D	E5	PUSH H
90	SUB B	BB	CMP E	E6	ANI D8
91	SUB C	BC	CMP H	E7	RST 4
92	SUB D	BD	CMP L	E8	RPE
93	SUB E	BE	CMP M	E9	PCHL
94	SUB H	BF	CMP A	EA	JPE Adr
95	SUB L	C0	RNZ	EB	XCHG
96	SUB M	C1	POP B	EC	CPE Adr
97	SUB A	C2	JNZ Adr	ED	---
98	SBB B	C3	JMP Adr	EE	XRI D8
99	SBB C	C4	CNZ Adr	EF	RST 5
9A	SBB D	C5	PUSH B	F0	RP
9B	SBB E	C6	ADI D8	F1	POP PSW
9C	SBB H	C7	RST 0	F2	JP Adr
9D	SBB L	C8	RZ	F3	DI
9E	SBB M	C9	RET Adr	F4	CP Adr
9F	SBB A	CA	JZ	F5	PUSH PSW
A0	ANA B	CB	---	F6	ORI D8
A1	ANA C	CC	CZ Adr	F7	RST 6
A2	ANA D	CD	CALL Adr	F8	RM
A3	ANA E	CE	ACI D8	F9	SPHL
A4	ANA H	CF	RST 1	FA	JM Adr
A5	ANA L	D0	RNC	FB	EI
A6	ANA M	D1	POP D	FC	CM Adr
A7	ANA A	D2	JNC Adr	FD	---
A8	XRA B	D3	OUT D8	FE	CPI D8
A9	XRA C	D4	CNC Adr	FF	RST 7
AA	XRA D	D5	PUSH D		
AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16-bit address.

APPENDIX C ASCII TABLE

The 8080 uses the seven-bit ASCII code, with the high-order eighth bit (parity bit) always reset.

GRAPHIC OR CONTROL	ASCII (HEXADECIMAL)
NUL	00
SOH	01
STX	02
ETX	03
EOT	04
ENQ	05
ACK	06
BEL	07
BS	08
HT	09
LF	0A
VT	0B
FF	0C
CR	0D
SO	0E
SI	0F
DLE	10
DC1 (X-ON)	11
DC2 (TAPE)	12
DC3 (X-OFF)	13
DC4 ~~(TAPE)~~	14
NAK	15
SYN	16
ETB	17
CAN	18
EM	19
SUB	1A
ESC	1B
FS	1C
GS	1D
RS	1E

GRAPHIC OR CONTROL	ASCII (HEXADECIMAL)
US	1F
SP	20
!	21
"	22
#	23
$	24
%	25
&	26
/	27
(	28
)	29
*	2A
+	2B
,	2C
–	2D
.	2E
/	2F
0	30
1	31
2	32
3	33
4	34
5	35
6	36
7	37
8	38
9	39
:	3A
;	3B
<	3C

GRAPHIC OR CONTROL	ASCII (HEXADECIMAL)
=	3D
>	3E
?	3F
@	40
A	41
B	42
C	43
D	44
E	45
F	46
G	47
H	48
I	49
J	4A
K	4B
L	4C
M	4D
N	4E
O	4F
P	50
Q	51
R	52
S	53
T	54
U	55
V	56
W	57
X	58
Y	59
Z	5A
[	5B
\	5C
]	5D
^ (↑)	5E

GRAPHIC OR CONTROL	ASCII (HEXADECIMAL)
_ (←)	5F
\	60
a	61
b	62
c	63
d	64
e	65
f	66
g	67
h	68
i	69
j	6A
k	6B
l	6C
m	6D
n	6E
o	6F
p	70
q	71
r	72
s	73
t	74
u	75
v	76
w	77
x	78
y	79
z	7A
{	7B
|	7C
} (ALT MODE)	7D
~	7E
DEL (RUB OUT)	7F

APPENDIX D
BINARY—DECIMAL —HEXADECIMAL CONVERSION TABLES

POWERS OF TWO

2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0.000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552	41	0.000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104	42	0.000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208	43	0.000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	44	0.000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832	45	0.000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664	46	0.000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328	47	0.000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	48	0.000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625
562 949 953 421 312	49	0.000 000 000 000 001 776 356 839 400 250 464 677 810 668 945 312 5
1 125 899 906 842 624	50	0.000 000 000 000 000 888 178 419 700 125 232 338 905 334 472 656 25
2 251 799 813 685 248	51	0.000 000 000 000 000 444 089 209 850 062 616 169 452 667 236 328 125
4 503 599 627 370 496	52	0.000 000 000 000 000 222 044 604 925 031 308 084 726 333 618 164 062 5
9 007 199 254 740 992	53	0.000 000 000 000 000 111 022 302 462 515 654 042 363 166 809 082 031 25
18 014 398 509 481 984	54	0.000 000 000 000 000 055 511 151 231 257 827 021 181 583 404 541 015 625
36 028 797 018 963 968	55	0.000 000 000 000 000 027 755 575 615 628 913 510 590 791 702 270 507 812 5
72 057 594 037 927 936	56	0.000 000 000 000 000 013 877 787 807 814 456 755 295 395 851 135 253 906 25
144 115 188 075 855 872	57	0.000 000 000 000 000 006 938 893 903 907 228 377 647 697 925 567 676 950 125
288 230 376 151 711 744	58	0.000 000 000 000 000 003 469 446 951 953 614 188 823 848 962 783 813 476 562 5
576 460 752 303 423 488	59	0.000 000 000 000 000 001 734 723 475 976 807 094 411 924 481 391 906 738 281 25
1 152 921 504 606 846 976	60	0.000 000 000 000 000 000 867 361 737 988 403 547 205 962 240 695 953 369 140 625
2 305 843 009 213 693 952	61	0.000 000 000 000 000 000 433 680 868 994 201 773 602 981 120 347 976 684 570 312 5
4 611 686 018 427 387 904	62	0.000 000 000 000 000 000 216 840 434 497 100 886 801 490 560 173 988 342 285 156 25
9 223 372 036 854 775 808	63	0.000 000 000 000 000 000 108 420 217 248 550 443 400 745 280 086 994 171 142 578 125

TABLE OF POWERS OF SIXTEEN$_{10}$

16^n	n	16^{-n}
1	0	0.10000 00000 00000 00000 x 10
16	1	0.62500 00000 00000 00000 x 10^{-1}
256	2	0.39062 50000 00000 00000 x 10^{-2}
4 096	3	0.24414 06250 00000 00000 x 10^{-3}
65 536	4	0.15258 78906 25000 00000 x 10^{-4}
1 048 576	5	0.95367 43164 06250 00000 x 10^{-6}
16 777 216	6	0.59604 64477 53906 25000 x 10^{-7}
268 435 456	7	0.37252 90298 46191 40625 x 10^{-8}
4 294 967 296	8	0.23283 06436 53869 62891 x 10^{-9}
68 719 476 736	9	0.14551 91522 83668 51807 x 10^{-10}
1 099 511 627 776	10	0.90949 47017 72928 23792 x 10^{-12}
17 592 186 044 416	11	0.56843 41886 08080 14870 x 10^{-13}
281 474 976 710 656	12	0.35527 13678 80050 09294 x 10^{-14}
4 503 599 627 370 496	13	0.22204 46049 25031 30808 x 10^{-15}
72 057 594 037 927 936	14	0.13877 78780 78144 56755 x 10^{-16}
1 152 921 504 606 846 976	15	0.86736 17379 88403 54721 x 10^{-18}

TABLE OF POWERS OF TEN IN BASE 16

10^n	n	10^{-n}
1	0	1.0000 0000 0000 0000
A	1	0.1999 9999 9999 999A
64	2	0.28F5 C28F 5C28 F5C3 x 16^{-1}
3E8	3	0.4189 374B C6A7 EF9E x 16^{-2}
2710	4	0.68DB 8BAC 710C B296 x 16^{-3}
1 86A0	5	0.A7C5 AC47 1B47 8423 x 16^{-4}
F 4240	6	0.10C6 F7A0 B5ED 8D37 x 16^{-4}
98 9680	7	0.1AD7 F29A BCAF 4858 x 16^{-5}
5F5 E100	8	0.2AF3 1DC4 6118 73BF x 16^{-6}
3B9A CA00	9	0.44B8 2FA0 9B5A 52CC x 16^{-7}
2 540B E400	10	0.6DF3 7F67 SEF6 EADF x 16^{-8}
17 4876 E800	11	0.AFEB FF0B CB24 AAFF x 16^{-9}
E8 D4A5 1000	12	0.1197 9981 2DEA 1119 x 16^{-9}
918 4E72 A000	13	0.1C25 C268 4976 81C2 x 16^{-10}
5AF3 107A 4000	14	0.2D09 370D 4257 3604 x 16^{-11}
3 8D7E A4C6 8000	15	0.480E BE7B 9D58 566D x 16^{-12}
23 8652 6FC1 0000	16	0.734A CA5F 6226 F0AE x 16^{-13}
163 4578 5D8A 0000	17	0.B877 AA32 36A4 B449 x 16^{-14}
DE0 B6B3 A764 0000	18	0.1272 5DD1 D243 ABA1 x 16^{-14}
8AC7 2304 89E8 0000	19	0.1D83 C94F B6D2 AC35 x 16^{-15}

HEXADECIMAL-DECIMAL INTEGER CONVERSION

The table below provides for direct conversions between hexadecimal integers in the range 0-FFF and decimal integers in the range 0-4095. For conversion of larger integers, the table values may be added to the following figures:

Hexadecimal	Decimal	Hexadecimal	Decimal
01 000	4 096	20 000	131 072
02 000	8 192	30 000	196 608
03 000	12 288	40 000	262 144
04 000	16 384	50 000	327 680
05 000	20 480	60 000	393 216
06 000	24 576	70 000	458 752
07 000	28 672	80 000	524 288
08 000	32 768	90 000	589 824
09 000	36 864	A0 000	655 360
0A 000	40 960	B0 000	720 896
0B 000	45 056	C0 000	786 432
0C 000	49 152	D0 000	851 968
0D 000	53 248	E0 000	917 504
0E 000	57 344	F0 000	983 040
0F 000	61 440	100 000	1 048 576
10 000	65 536	200 000	2 097 152
11 000	69 632	300 000	3 145 728
12 000	73 728	400 000	4 194 304
13 000	77 824	500 000	5 242 880
14 000	81 920	600 000	6 291 456
15 000	86 016	700 000	7 340 032
16 000	90 112	800 000	8 388 608
17 000	94 208	900 000	9 437 184
18 000	98 304	A00 000	10 485 760
19 000	102 400	B00 000	11 534 336
1A 000	106 496	C00 000	12 582 912
1B 000	110 592	D00 000	13 631 488
1C 000	114 688	E00 000	14 680 064
1D 000	118 784	F00 000	15 728 640
1E 000	122 880	1 000 000	16 777 216
1F 000	126 976	2 000 000	33 554 432

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
010	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
020	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
030	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
040	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
050	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
060	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
070	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
080	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
090	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A0	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B0	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C0	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D0	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E0	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F0	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255

HEXADECIMAL-DECIMAL INTEGER CONVERSION (Cont'd)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
100	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
110	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
120	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
130	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
140	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0331	0333	0334	0335
150	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
160	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
170	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
180	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
190	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A0	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B0	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C0	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D0	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E0	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F0	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511
200	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
210	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
220	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
230	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
240	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
250	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
260	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
270	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
280	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
290	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A0	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B0	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C0	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D0	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E0	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F0	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767
300	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
310	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
320	0800	0301	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
330	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
340	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
350	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
360	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
370	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
380	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
390	0212	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A0	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B0	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C0	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D0	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E0	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F0	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

HEXADECIMAL-DECIMAL INTEGER CONVERSION (Cont'd)

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410	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
420	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
430	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
440	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
450	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
460	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
470	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
480	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
490	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A0	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B0	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C0	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D0	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E0	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F0	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
500	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
510	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
520	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
530	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
540	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
550	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
560	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
570	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
580	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
590	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A0	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B0	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C0	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D0	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E0	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F0	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535
600	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
610	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
620	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
630	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
640	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
650	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
660	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
670	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
680	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
690	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A0	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B0	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C0	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D0	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E0	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F0	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791

HEXADECIMAL-DECIMAL INTEGER CONVERSION (Cont'd)

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710	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
720	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
730	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
740	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
750	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
760	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
770	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
780	1920	1921	1922	1923	1924	1925	1926	1927	1928	1929	1930	1931	1932	1933	1934	1935
790	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A0	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B0	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C0	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D0	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E0	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F0	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047
800	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
810	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
820	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
830	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
840	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
850	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
860	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
870	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
880	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
890	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A0	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B0	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C0	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D0	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E0	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F0	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303
900	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
910	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
920	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
930	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
940	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
950	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
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980	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
990	2448	2449	2450	2451	2452	2453	2454	2455	2456	2457	2458	2459	2460	2461	2462	2463
9A0	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B0	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C0	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D0	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E0	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F0	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559

HEXADECIMAL-DECIMAL INTEGER CONVERSION (Cont'd)

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A10	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A20	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A30	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A40	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A50	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A60	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A70	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A80	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A90	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA0	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB0	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC0	2752	2753	2754	2755	2756	2757	2758	2759	2760	4761	2762	2763	2764	2765	2766	2767
AD0	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE0	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF0	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B00	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B10	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B20	2848	2849	2850	3851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B30	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B40	2880	2881	2882	2883	2884	2885	2866	2887	2888	2889	2890	2891	2892	2893	2894	2895
B50	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B60	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B70	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B80	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B90	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA0	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB0	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC0	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD0	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE0	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF0	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071
C00	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C10	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C20	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C30	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C40	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C50	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C60	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C70	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C80	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C90	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA0	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB0	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC0	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD0	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE0	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF0	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327

HEXADECIMAL-DECIMAL INTEGER CONVERSION (Cont'd)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
D00	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D10	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D20	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D30	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D40	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D50	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D60	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D70	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D80	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D90	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA0	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB0	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC0	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD0	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE0	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF0	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583
E00	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E10	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E20	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E30	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E40	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E50	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E60	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E70	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E80	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E90	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA0	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB0	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC0	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED0	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE0	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF0	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F00	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F10	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F20	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F30	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F40	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F50	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F60	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F70	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F80	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F90	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA0	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB0	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC0	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD0	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE0	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF0	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

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