AP-375

APPLICATION NOTE

82557 Test Access Port (TAP) Appendix

November 1996

Order Number: 650145-002

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

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 CG-041493

1.0. INTRODUCTION

This application note provides information on how to use the 82557 Test Access Port (TAP). The port is used to facilitate board level testing and debug with minimal cost and complexity. The 82557 TAP is a non-standard, serial-in/serial-out port from which all test modes are selected and operated.

NOTE

This document contains specific information on the 82557 TAP. For additional information on the 82557, refer to the 82557 Data Sheet and 82557 User's Manual, available from your local Intel Sales Representative.

2.0. PIN DEFINITIONS

Figure 1 shows pin numbering and signal identification for the 82557 and includes the Test Access Port pins.

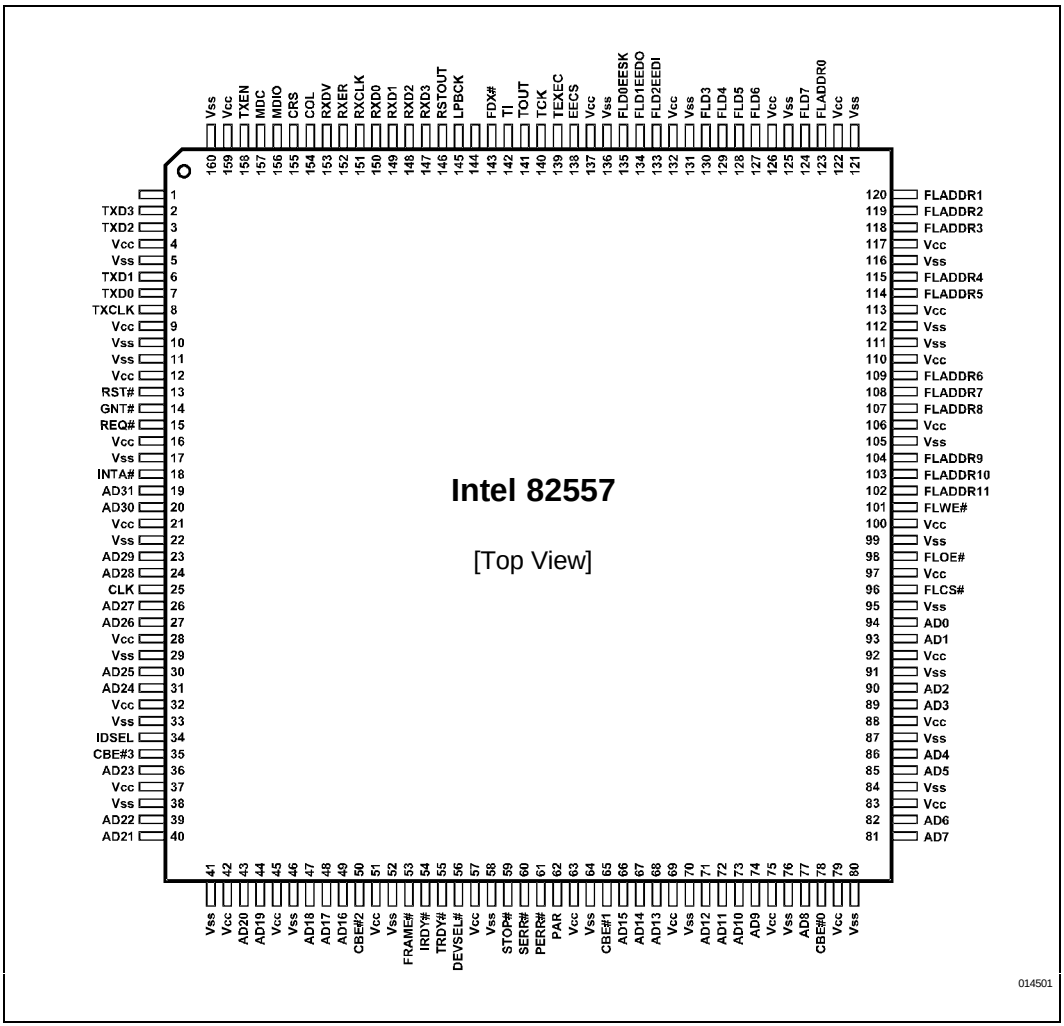

Figure 1. 82557 Pinout Diagram

3.0. TEST ACCESS PORT

3.1. Hardware Logic Glossary

- **TISR** - Test Instruction Shift Register - 4 bit long shift register. The TISR has a serial input and output as well as parallel output. The serial input of the TISR is connected to the device Test Input (TI) pin. The serial output is connected to the Test Output(TOUT) control logic.
- **TIR** - Test Instruction Register - 4 bit wide register. It has a parallel output and input. The register load enable is connected to the device TEXEC input pin.
- **TOUT Control** - Uses the selected source and current values of the TOUT output pin according to the current instruction of the TIR.
- **IR Decoder** - The decoding logic of the TIR instruction. The 4 bit instruction is decoded and 8 control signals are generated and sent to the 82557 blocks as command specific signals.

3.2. 82557 TAP Pinout Summary

The 82557 Test Access Port consists of four pins: TI, TOUT, TCK, and TEXEC. The following table summarizes the signal descriptions for these pins.

Signal Name	I/O	Pin#	Pin Description
TI	I	142	Test input port. A serial input of test command data.
TOUT	O	141	Test output port. A serial output of test command data. TOUT is determined according to the last test command executed.
TCK	I	140	Test input clock. The clock of the test access port logic. TI data is sampled into the test command logic.
TEXEC	I	139	Load Instruction Test Register. When asserted the new test command is issued. The command is loaded serially via the TI input and then sampled to the Instruction Test Register.

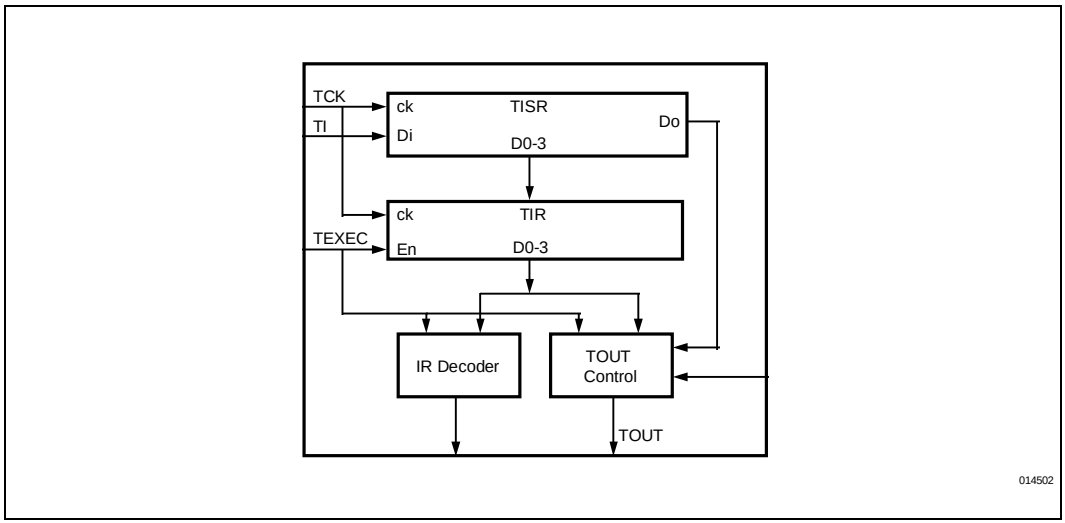

Figure 2. TAP Block Logic Diagram

3.3. Test Function Description

The 82557 TAP function supports the following test modes (test instruction codes are listed in parenthesis next to the test mode) :

TRI-STATE MODE (0010)

When active, this command sets all 82557 outputs and I/O pins into a HIGH-Z state.

NAND-TREE TEST MODE (0011)

When active, this command sets all the outputs of the input-buffers in the device periphery into a nand tree scheme. The TI input pin is connected to the NAND tree chain input. TOUT output pin is connected to the nand tree output. All the output drivers of the output buffers except the TOUT pin, are put into HIGH-Z state.

3.4. TAP Description

Test instructions are shifted in serially through the TI input pin into the TISR. The TI input is sampled into the TISR on the rising edge of TCK input. The instruction is loaded from the TISR to the TIR when the TEXEC input is sampled high on the rising edge of TCK input. As a general rule, all Test Access Port input and output pins are activated by TCK rising edge clock. If TCK input is a constant clock signal then TEXEC must be 1 clock width signal.

Once the new instruction resides in the TIR, it is decoded into control signals and synchro-nized to the 82557 PCI CLK input clock. These control signals set the 82557 blocks into various test modes. In order to achieve stable synchronization between CLK and TCK, the frequency of TCK input signals should be less than or equal to half the frequency of the PCI CLK input signal. TOUT output is activated by the TCK rising edge clock.

NOTE

The TAP must be Hardware reset during power up, not Software reset or Selective reset.

3.5. TAP Timings

This section provides TAP timing information. Figure 3 shows the timing waveforms. Timing values are shown in the table.

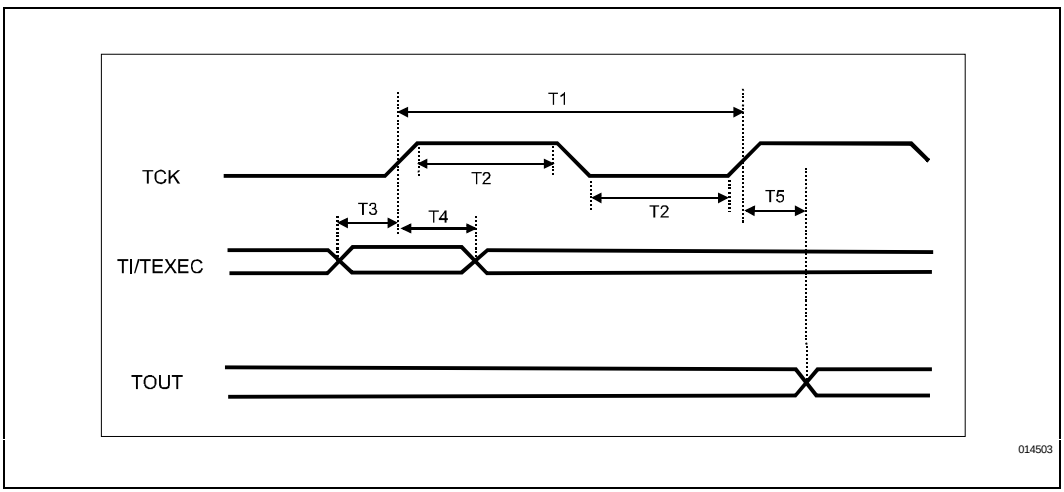

Figure 3. TAP Timings

Symbol	Parameter	Min	Max	Units	Notes
T1	TCK Cycle Time	100	--	ns	1
T2	TCK High/Low Time	30	--	ns	--
T3	TI/TEXEC Setup Time	10	--	ns	2
T4	TI/TEXEC Hold Time	10	--	ns	2
T5	TOUT Valid Delay	0	15	ns	2

NOTES:

1. TCK is an aperiodic signal. When not active, TCK should be left high.
2. All TAP timings are relative to TCK rising edge.

4.0. ADDITIONAL INFORMATION

For additional information on the TAP or the Intel 82557, contact your local Intel Sales Office.