3 Volt Intel® StrataFlash™ Memory to NEC V_R4121 CPU Design Guide

Application Note 731

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Contents

Revision History

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1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the NEC's V_R4121 processor.

This application note was based on information about 3 Volt Intel StrataFlash memory at the time of publication (refer to Appendix A). Any subsequent changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page mode timings. Before 3 Volt Intel StrataFlash memory's page mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory:28F128J3A, 28F640J3A, 28F320J3A* datasheet.

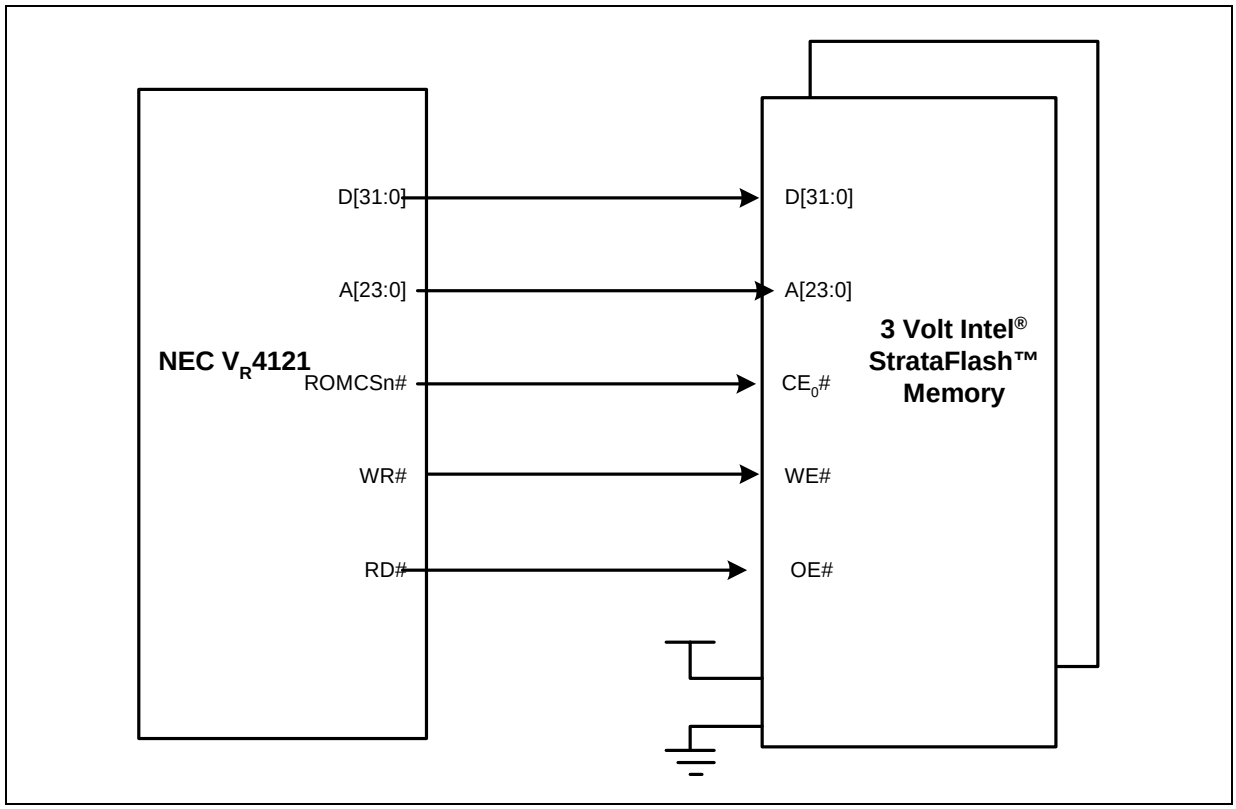
3.0 Interfacing 3 Volt Intel® StrataFlash™ to the V_R4121 Processor by NEC

NEC's V_R4121 microprocessor is designed around MIPS RISC architecture. The V_R4121 microprocessor includes such features as 16-KB of instruction cache, 8-KB of data cache, and a built-in memory management unit that enable high performance in a compact, low-cost chip. The processor's high speed and low power consumption make it ideal for use in a battery-driven, portable handheld systems.

3.1 Interface Considerations

In this interface, V_R4121 directly controls the 3 Volt Intel StrataFlash memory interface. It also internally decodes the address bus to generate chip select signals, which can be directly connected to the 3 Volt Intel StrataFlash memory's chip enable signal. Both the processor and the flash can be powered from and interface at 3.3 V. Figure 1 is a block diagram of the interface. The designers should use two 128-Mbit Intel StrataFlash memory to match the 32-bit data bus of the processor.

Figure 1. 0.25 µm 3 Volt Intel® StrataFlash™ Memory/V_R4121 Interface



3.2 Processor Interface Signals

This interface uses the following signals provided by the NEC V_R4121 processor:

$A_{23:0}$: The multiplexed address bus provides addresses to memory. It must be latched to generate the full address.

$D_{15:0}$: The lower half of the 32-bit data bus. This is the portion used for connections to 16-bit memory.

ROMCS(0:3)# are chip select signals generated by the processor.

WR#: Indicates writes from the processor to the system.

RD#: Indicates the processor is reading from the flash

3.3 Controlling the Interface

The memory configuration registers in the V_R4121processor should be set as necessary for proper operation. This includes setting the bus width, the access time for the flash, and enabling page mode for the memory region containing the 3 Volt Intel StrataFlash memory. The V_R4121 processor and the 3 Volt Intel StrataFlash memory both use a four-word page. To set the page

mode as a 4-Word read and in the 32-bit mode, WPROM[13:12] and WROMA[2:0] in the BCUSPEEDREG register should be set to 01 and 011, respectively. The initial access is six clock cycles and two clock cycles each for the rest of the data

Read all appropriate documentation before attempting this interface.

Table 1. V_R4121 Processor Bus Timing Names

Symbol	Description
t_{WLWH}	WE# Pulse Width
t_{DH}	Data Hold Time
t_{OE}	Access Time from RD#
t_{AVWL}	Address Setup to WE# going Low
t_{WHDX}	DATA Hold from WR# going High
t_{WLWH}	WR# Pulse Width
t_{AVAV}	Write Cycle Time

Figure 2 is a timing diagram of the 3 Volt Intel StrataFlash memory and the V_R4121 processor with page mode reads. TCLK, which is the internal clock in the V_R4121 processor, runs at 33.33 MHz, and is of what all timing specifications from the V_R4121 processor are given.

Figure 2. 3 Volt Intel® StrataFlash™ Memory/V_R4121 Processor Page Mode Reads

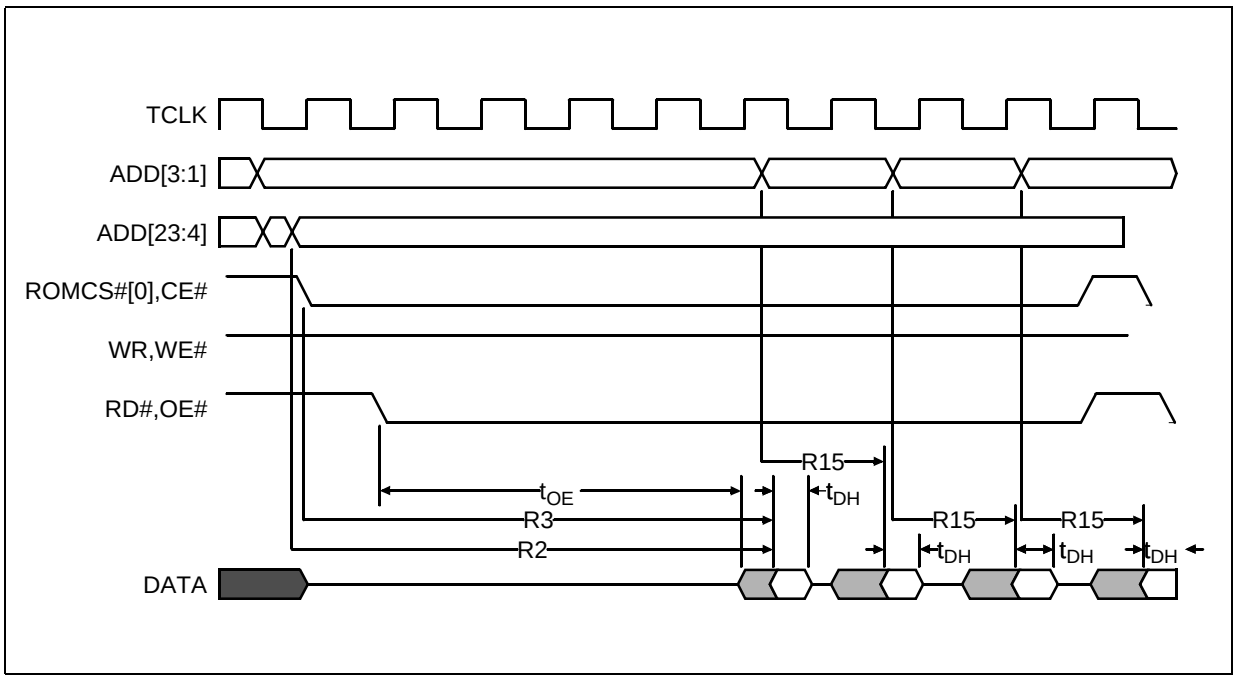
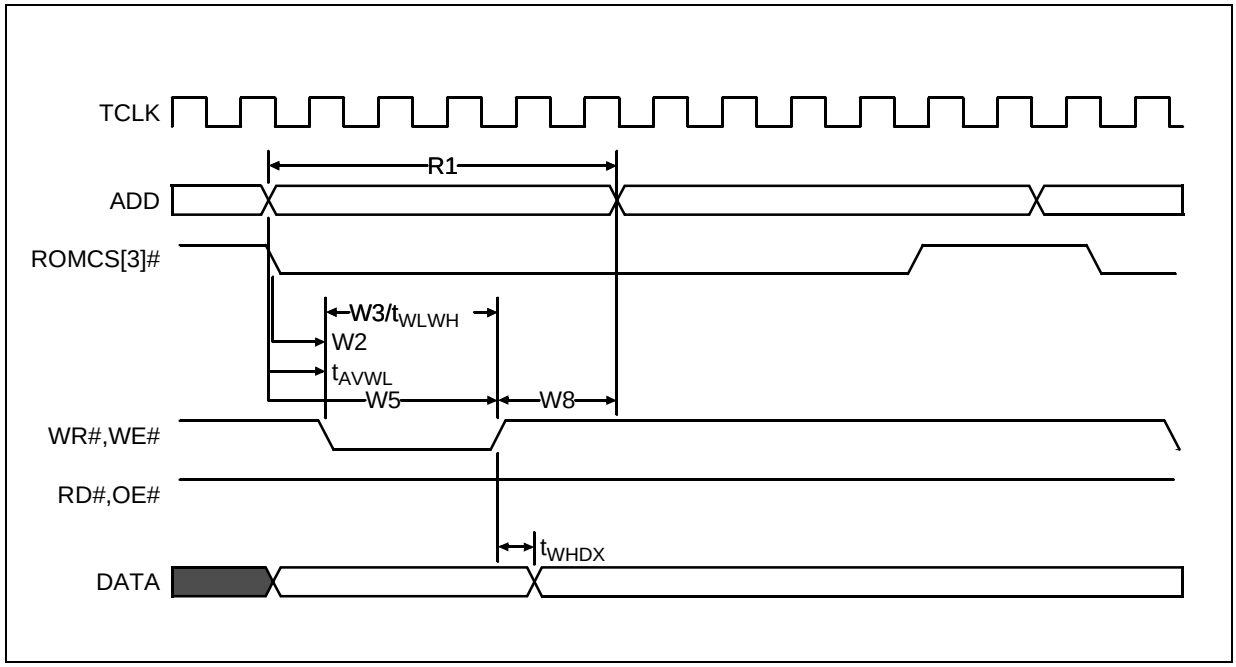


Figure 3 is a timing diagram of a typical write cycle. WE# is held low long enough to meet the Write Pulse Width time (t_{WLWH}). When it goes high, the address and data is latched. In between write cycles, WE# must remain high for at least t_{WHWL}. Refer to Table 1 for the signal delay and signal constraint descriptions. This were pulled out of the NEC V_R4121 datasheet and user manual.

Figure 3. 3 Volt Intel® StrataFlash™ Memory/V_R4121 Write Cycles



Several considerations must be taken into account when resetting or powering on the 3 Volt Intel StrataFlash memory. When resetting, RP# must remain low for at least a time of t_{PLPH} (35 µs). In addition, the first output is not valid until 310 ns (t_{PHQV} + t_{PHRH}) after RP# goes high. The VR4121 processor power management feature is used with the 3 Volt StrataFlash memory. The period where the CPU is initialized by RSTCRST is approximately 350 ms. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page mode.

Consult all appropriate datasheets and manuals before attempting this interface (see Appendix A for a list of additional information).

4.0 Summary

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page mode reads. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required. Finally, it has “glueless” interface with the processor which will help reduce the power consumption.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A* datasheet
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.