3 Volt Intel® StrataFlash™ Memory to Hitachi SH7708 (SH-3) CPU Design Guide

Application Note 706

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Contents

Revision History

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07/20/99	-001	Original version
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1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the Hitachi SH7708 (SH-3) processor.

This document was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory:28F128J3A, 28F640J3A, 28F320J3A* datasheet.

3.0 Interfacing 3 Volt Intel® StrataFlash™ Memory to Hitachi SH7708 (SH-3) at 60 MHz

The SH7708 (SH-3) series of 32-bit RISC microprocessors include an 8-Kbyte cache and an on-chip Bus State Controller including a wait-state generator that allows for a near glueless interface to the 3 Volt Intel StrataFlash memory.

3.1 Interface Considerations

This sample interface uses one 3 Volt Intel StrataFlash memory in 16-bit mode. Timing diagrams were made with the 32-Mbit 3 Volt Intel StrataFlash memory and a 60 MHz bus. This interface requires two inverters, two OR gates, an AND gate, and six flip-flops. These may be integrated into an ASIC or a PLD. All parts can run from and interface at 3.0 V–3.6 V. The bus width settings on the SH-3 for the area the 3 Volt Intel StrataFlash memory occupies should be 16 bits.

3.2 Processor Interface Signals

The interface uses the following signals provided by the SH7708:

$A_{25–0}$: The address bus signals the memory which piece of information is to be accessed.

$D_{31–0}$: The 32-bit data bus. The 3 Volt Intel StrataFlash memory is connected to $D_{31–}D_0$.

CSn#: The Chip Select signal generated by the SH-3 for the memory region the 3 Volt Intel StrataFlash memory is placed in.

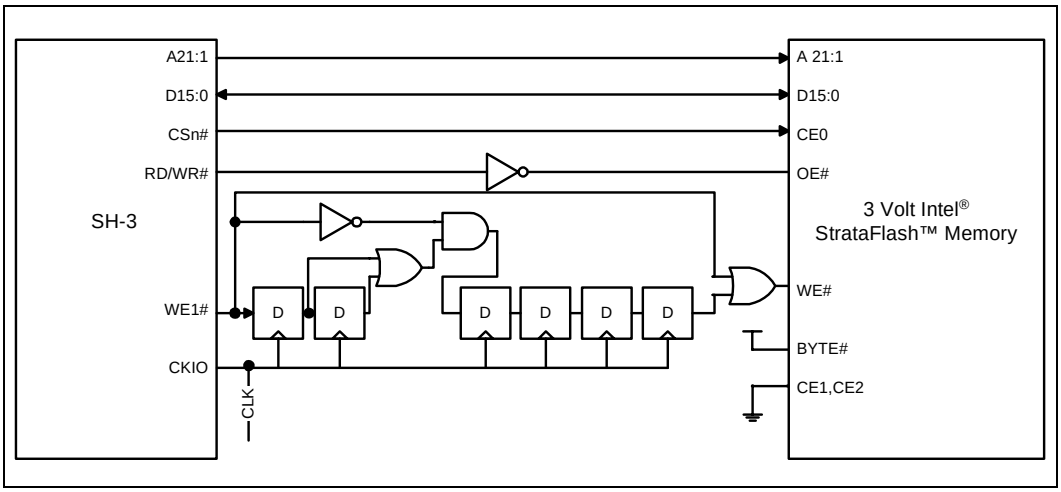
RD/WR#:Read/Write indicates the direction of the current data transfer.

WEn#: A Write Enable signal is generated for each 8-bit portion of the bus.

3.3 Control Signal Generation

The only 3 Volt Intel StrataFlash memory signals not directly to the SH-3 connected are OE# and WE#. RD/WR# is inverted to generate OE#. The logic between WE1# on the SH-3 and WE# on the 3 Volt Intel StrataFlash memory is meant to allow WE# to go low on the 3 Volt Intel StrataFlash memory at nearly the same time as WE1# goes low, but making it go high earlier so WE# pulse high times can be met. Figure 1 is a block diagram of the interface.

Figure 1. 3 Volt Intel® StrataFlash™ Memory/SH-3 Interface



The SH-3 can internally generate wait-states based on register settings. Figure 2 is a timing diagram of a four-word read with page-mode enabled. This diagram assumes the wait-states have been configured by setting the appropriate registers.

Figure 2. 3 Volt Intel® StrataFlash™ Memory/SH-3 Page Mode Reads

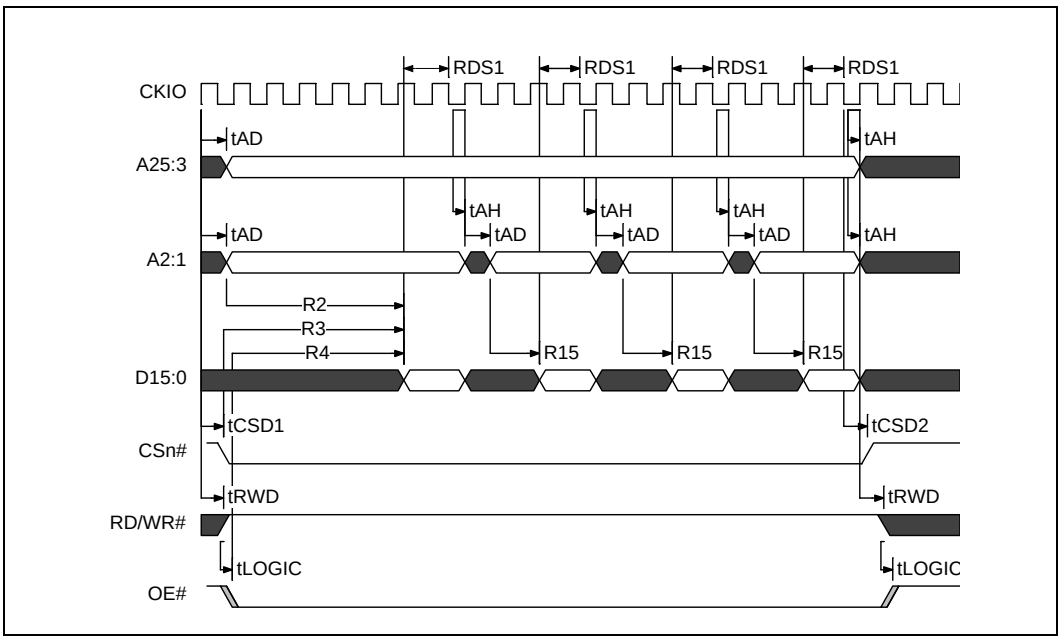
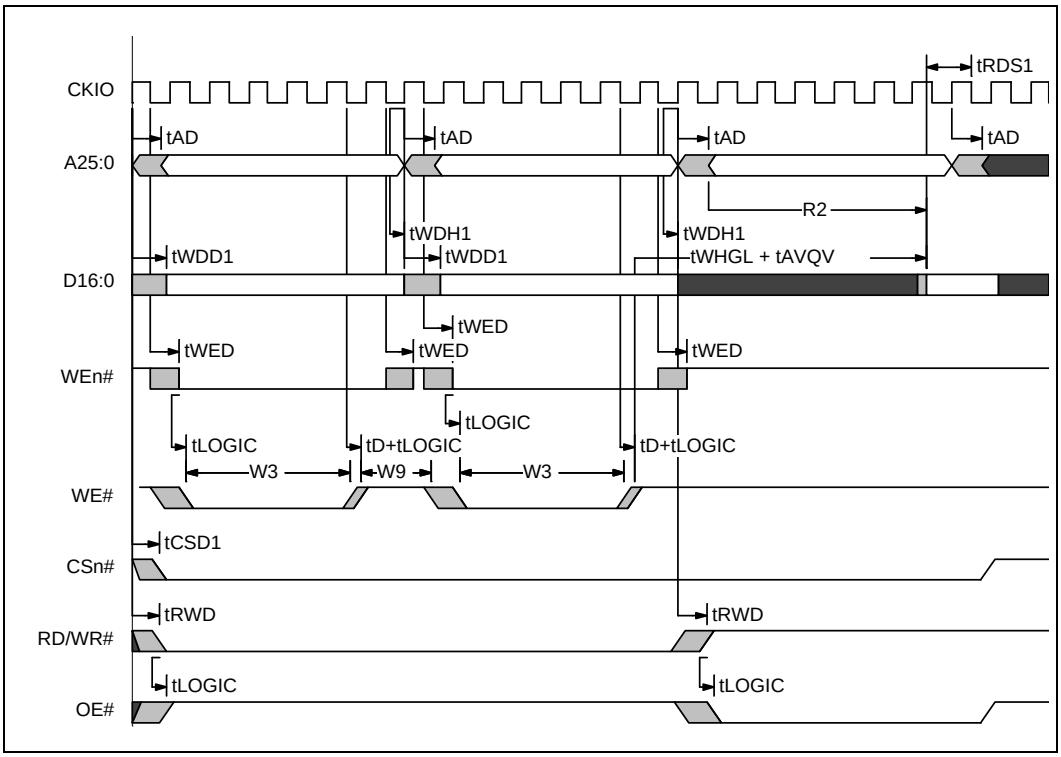


Figure 3 is a timing diagram of two write cycles followed by a read cycle. Note that the 3 Volt Intel StrataFlash memory's WE# signal goes high earlier than the WE1# signal from the SH-3. This signal is generated to meet WE# pulse high and write recovery before read timing requirements. The six flipflops allow the signal to be low long enough to meet WE# pulse low time before going high again.

Figure 3. 3 Volt Intel® StrataFlash™ Memory/SH-3 Write Cycles Followed by a Read



Several considerations must be taken into account when resetting the 3 Volt Intel StrataFlash memory. If a block erase, program, or lock-bit configuration command is executing, RP# must be held low for a minimum of time of t_{PLPH} (35 µs). When returning from reset, the 3 Volt Intel StrataFlash memory the RP# high to output delay (310 ns = t_{PHQV} + t_{PHRH}) must be met. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

The 3 Volt Intel StrataFlash memory may only be mapped to certain areas of the processor's memory. Certain areas may not be used for flash or other static memories. If the 3 Volt Intel StrataFlash memory is to be used as the booting memory, it should be placed in area 0 and located so that it can be accessed by the initial Program Counter value of A000000h. A complete address map of the SH7708 processor is available in the user's manual for that processor.

Read all appropriate documentation before attempting this interface.

4.0 Summary

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. Interfaces between 3 Volt Intel StrataFlash components and various processors can generally be accomplished with a PLD to generate wait-states and WE#, and a decoder to generate chip enable signals. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A* datasheet
298130	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP} RP#, and WP#*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.