3 Volt Intel® StrataFlash™ Memory to i960® H CPU Design Guide

Application Note 705

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Revision History

Date of Revision	Version	Description
07/20/99	-001	Original version
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1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the Intel® i960® HA/HD/HT processors.

This document was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory:28F128J3A, 28F640J3A, 28F320J3A* datasheet.

3.0 Interfacing 3 Volt Intel® StrataFlash™ Memory to i960® H Processor at 40 MHz

The Intel® i960 HA/HD/HT processor series provides higher performance levels while maintaining backward compatibility with the i960® CA/CF processors. The i960 HA/HD/HT processors can run at 1x, 2x, or 3x bus speed, and execute up to 150 million instructions per second. This sample interface with the 3 Volt Intel StrataFlash memory device is written with a bus speed of 40 MHz, and timings use the 32-Mb flash component.

3.1 Interface Considerations

The interface uses two 3 Volt Intel StrataFlash memory components to match the i960 H processor's 32-bit data bus, a decoder to generate CE_0, and a PLD to generate WE#. The decoder for this interface should have a delay no greater than 22 ns. The i960 Hx processor and the 3 Volt Intel StrataFlash memory can both have power supplies and input/outputs of 3.3 V. The i960 processor has an internal wait-state generator with programmable wait-states and other attributes. The address space that the 3 Volt Intel StrataFlash memory occupies should be set for non-pipeline, burstable (for page-mode accesses), nonparity, with READY# enabled, a 32-bit data bus width, and N_{RAD}=4, N_{RDD}=1, N_{WAD}=4, N_{WDD}=3, and N_{XDA}=0.

3.2 Processor Interface Signals

The interface uses the following signals provided by the i960 H processor:

$A_{31:2}$: The upper 30 bits of the address. Used to identify all addresses within a 4-byte boundary.

$D_{31:0}$: The 32-bit data bus.

W/R#: Write/Read indicates whether the current transfer is a read or a write. It is low for read and high for write.

WAIT#: Output from the i960 processor indicates the status of the i960 H processor's internal wait-state generator.

READY#:Input to the i960 processor to indicate if wait-states are needed in addition to those programmed in the processor's wait-state generator.

3.3 Control Signal Generation

Figure 1 is a block diagram of the interface. CE_0 is taken directly from the decoder. CE_1 and CE_2 are tied low. OE# is taken from W/R#. WE# and READY# are generated inside the PLD from W/R# and WAIT#. The PLD asserts WE# and READY# for write cycles. For read cycles, READY# does not need to be asserted because the i960 H processor's internal wait-state generator can create the necessary wait-states.

Figure 1. 3 Volt Intel® StrataFlash™ Memory/i960® H Processor Interface

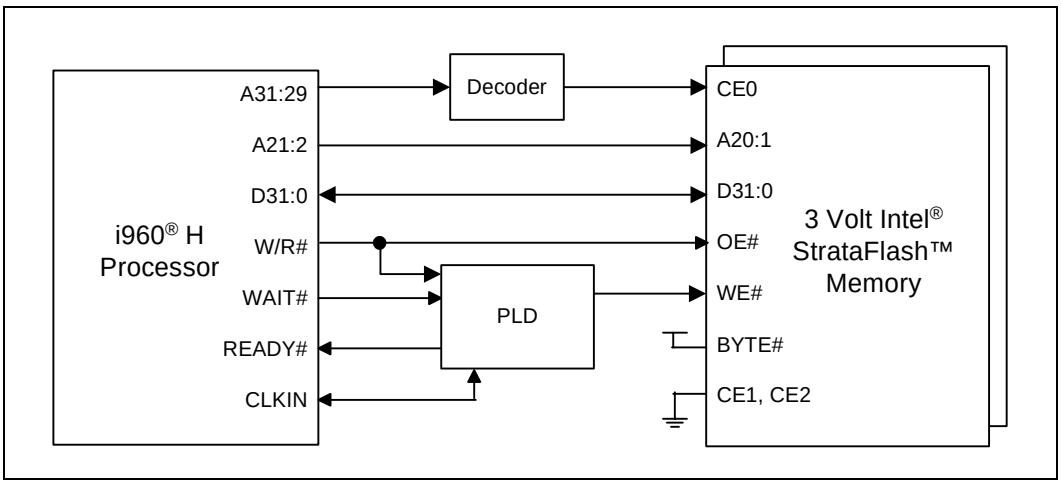
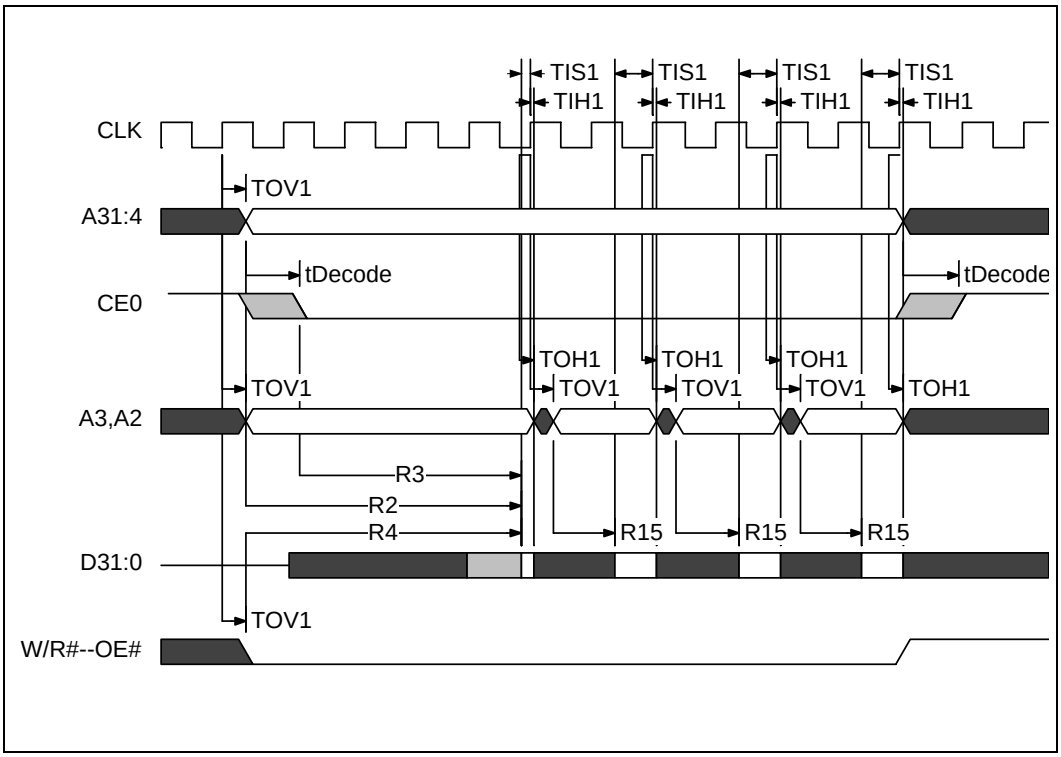


Figure 2 is a timing diagram of four reads. Burst mode is enabled on the i960 H CPU so that all four addresses in the page can be read in the minimum amount of time. The initial read must be at a page boundary for the timing in this figure. If not all accesses are within a page boundary, additional wait-states must be added for the first access in another page.

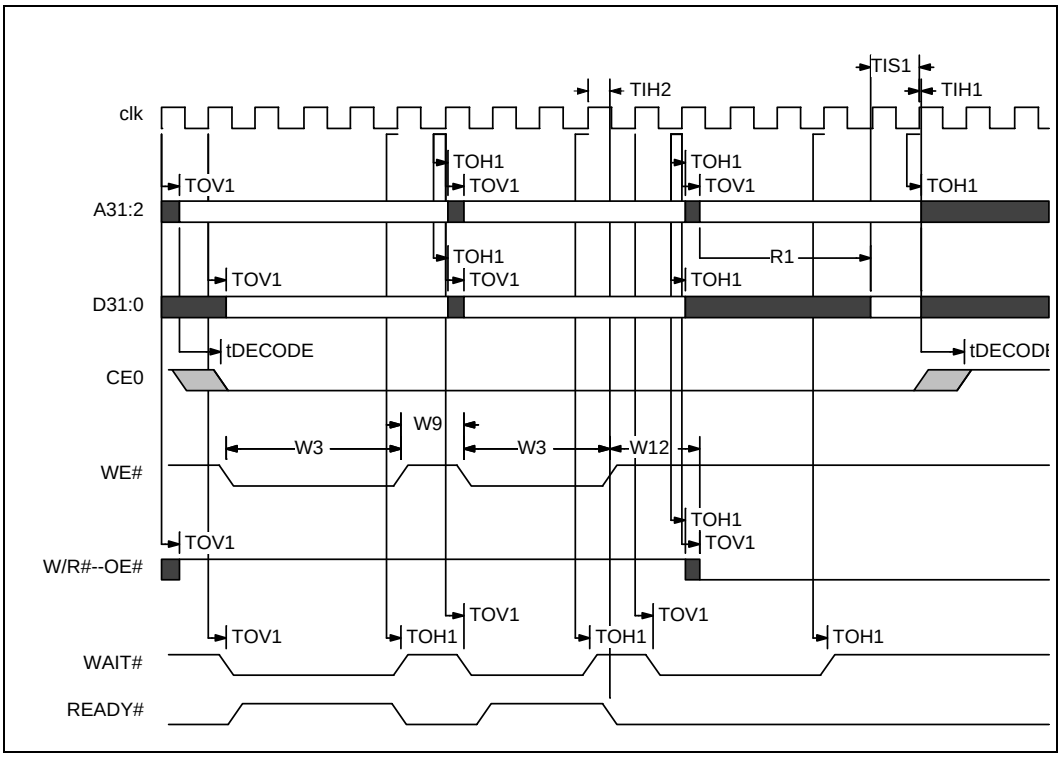
Figure 2. 3 Volt Intel® StrataFlash™ Memory/i960® H Processor Page Mode Reads



NOTE: The address line labels in this diagram refer to the labels on the i960 H CPU. Ax on the i960 H CPUis connected to Ax-1 on 3 Volt Intel® StrataFlash™ memory.

Figure 3 shows two writes followed by a single read. Either WE# or chip enable may be used to start a write. In this case, WE# is used to latch the address and data. It is generated from WAIT# and W/R# in the PLD. The i960 H processor generates a maximum of three wait-states for sequential writes, so READY# is only needed to add one additional wait-state after WAIT# goes high for the second and subsequent write accesses to the 3 Volt Intel StrataFlash memory.

Figure 3. 3 Volt Intel® StrataFlash™ Memory/i960® H Processor Write Cycles Followed by Read



Several considerations must be taken into account when resetting. If a block erase, program, or lock-bit configuration command is executing, RP# must be held low for a minimum of time of t_{PLPH} (35 µs). When returning from reset, the i960 H processor takes 23 to 67 CLKIN cycles until the first bus activity. At 40 MHz, 23 clock cycles is 575 ns. This is greater than the min. time required from RP# high to output delay (310 ns = t_{PHQV} + t_{PHRH}) on the 3 Volt Intel StrataFlash memory device. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

Certain areas of the i960 H processor's memory map may not be used by flash memory. These include 00000000h to 000007FFh and FF000000 to FFFFFFFFh which is used for accesses internal to the processor such as registers. Most other areas can be configured for use by the 3 Volt Intel StrataFlash memory.

Read all appropriate datasheets before attempting this interface (see Appendix A for a list of additional information).

4.0 Summary

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. Interfaces between 3 Volt Intel StrataFlash components and various processors can generally be accomplished with a PLD to generate wait-states and WE#, and a decoder to generate chip enable signals. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A* datasheet
298130	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.