



3 Volt Intel[®] StrataFlash[™] Memory to MPC603e CPU Design Guide

Application Note 704

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Contents

1.0	Introduction	1
2.0	Hardware Interface	1
3.0	Interfacing 3 Volt Intel® StrataFlash™ Memory to MPC603e at 66 MHZ	2
	3.1 Interface Considerations	2
	3.2 Processor Interface Signals	3
	3.3 Control Signal Generation	3
4.0	Summary	6
A	Additional Information	7

Revision History

Date of Revision	Version	Description
07/20/99	-001	Original version
03/20/00	-002	Reformatted document

1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the PowerPC* MPC603e (PPC603e) processor.

This document was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC} : Device power supply. 2.7 V – 3.6 V

V_{CCQ} : Output buffer power supply. This voltage controls the device's output voltages. 5 V \pm 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

CE_{0,2}: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE₁ and CE₂ are tied to ground. CE₀ is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the 3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

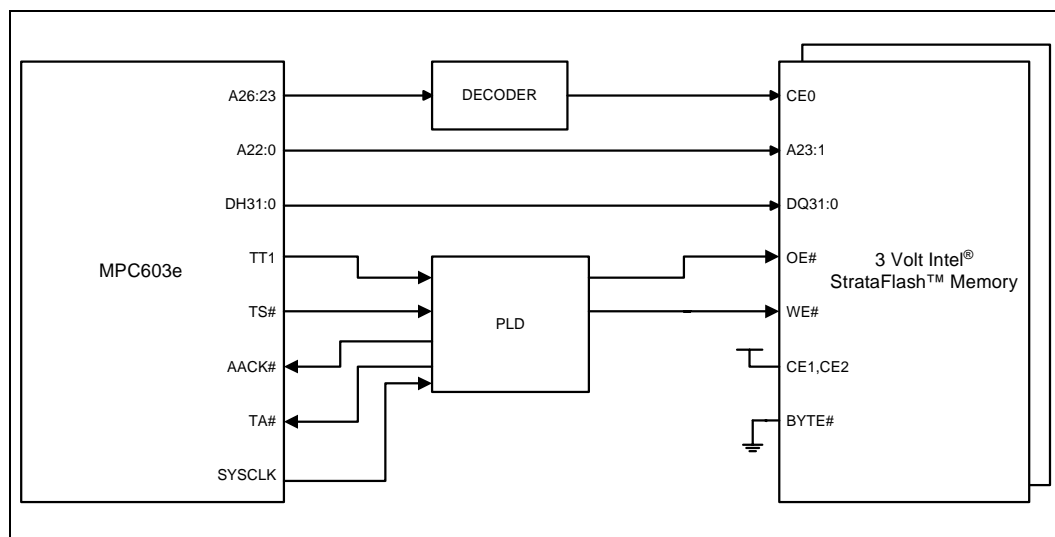
This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

3.0 Interfacing 3 Volt Intel® StrataFlash™ Memory to MPC603e at 66 MHz

The MPC603 (PPC603e) PowerPC microprocessor by IBM and Motorola is a low power implementation of the PowerPC family of RISC microprocessors. This superscalar processor can issue and retire as many as three instructions at once. It supports bus speeds between 25 MHz and 66 MHz. This interface was written with a 66 MHz bus. All examples and diagrams were made with the 32-Mbit 3 Volt Intel StrataFlash memory device as a reference. Figure 1 is a block diagram of the interface between the MPC603e and the 3 Volt Intel StrataFlash memory.

Figure 1. 3 Volt Intel® StrataFlash Memory/MPC603e Interface



3.1 Interface Considerations

The interface uses two of the 3 Volt Intel StrataFlash memory components to match the MPC603e's data bus in 32-bit mode. It also uses a PLD and a decoder. These may be integrated into an ASIC. Connecting address lines directly to the 3 Volt Intel StrataFlash memory's three chip enable pins could eliminate the need for a decoder and decrease the time for the initial memory access. All components can run on a 2.7 V–3.6 V power supply. The minimum and maximum delay specifications for the PLD and decoder as shown in Figure 3 and Figure 5 are in the table below. This interface assumes that all bus arbitration signals have been used so that the MPC603e is the bus master.

Device	Min	Max
Decoder	0 ns	11 ns
PLD	0 ns	18 ns

3.2 Processor Interface Signals

This interface uses the following signals provided by the MPC603e:

A_{31:0}: The 32-bit address bus transfers addresses from the processor to memory.

DH_{31:0}: The half of the 64-bit data bus that is used in 32-bit mode. Transfers information between processor and memory.

TS#: The Transfer Start indicates that a transfer is will start in the next clock cycle.

AACK#:The Address Acknowledge is received by the processor after memory no longer needs the address on the bus.

TA#: The Transfer Acknowledge is received by the processor when the data has been placed on the bus.

TT1: The Transfer Type 1 signal is part of an encoding about the transfer in progress.

3.3 Control Signal Generation

The 3 Volt Intel StrataFlash memory’s CE₀ signal is taken directly from the decoder. CE₁ and CE₂ are tied low. Inverting TT1 in the PLD gives OE#. TA# and AACK# are generated by a wait-state generator in the PLD. In read operations with a 32-Mbit part, they are high for five clock cycles after TS# is asserted, then go low for one clock cycle. AACK# must always go low before TA#. Figure 2 is a diagram of the internal PLD configuration.

Figure 2. 3 Volt Intel® StrataFlash™ Memory/MPC603e Configuration

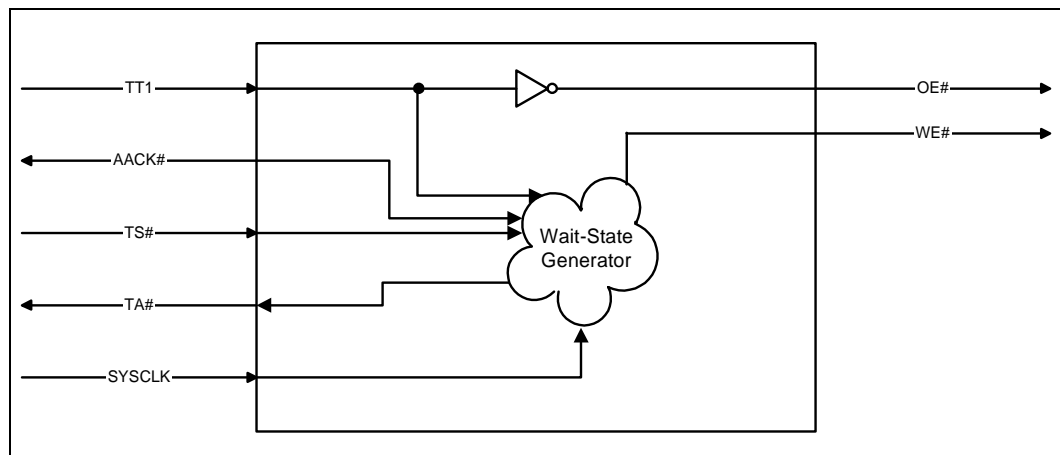


Figure 3 is a timing diagram of a single read. At the start of the transfer, the processor asserts TS# low. AACK# is used to make the processor hold the address until the 3 Volt Intel StrataFlash memory has output the data. Several clock cycles after TS# is asserted, the PLD forces AACK# and TA# low. For subsequent accesses within the page, AACK# and TA# can be asserted one full clock cycle after TS# is pulsed low. If the 3 Volt Intel StrataFlash memory is being accessed sequentially, the lower two address lines can be used by the PLD to tell when the memory access is off the page. Figure 4 is possible logic for the PLD wait-state generator.

Figure 3. 3 Volt Intel® StrataFlash™ Memory/MPC603e Page-Mode Reads at 66 MHz

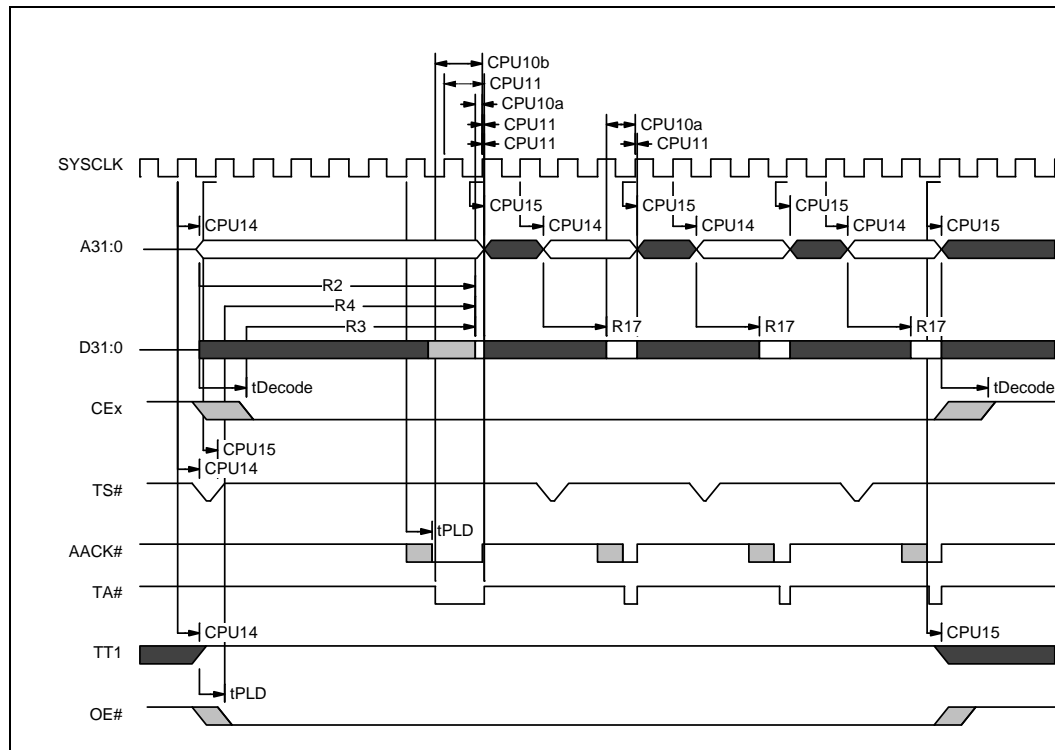


Figure 4. 3 Volt Intel® StrataFlash™ Memory/MPC603e Wait-State Logic

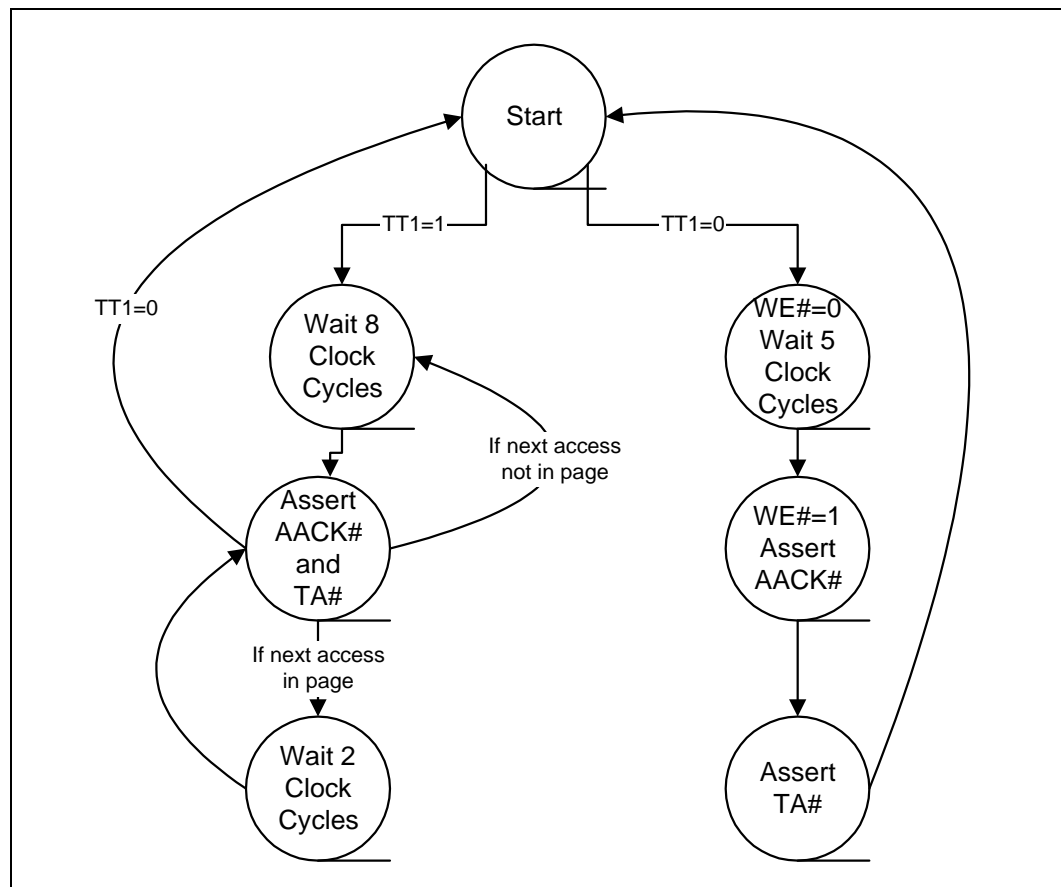
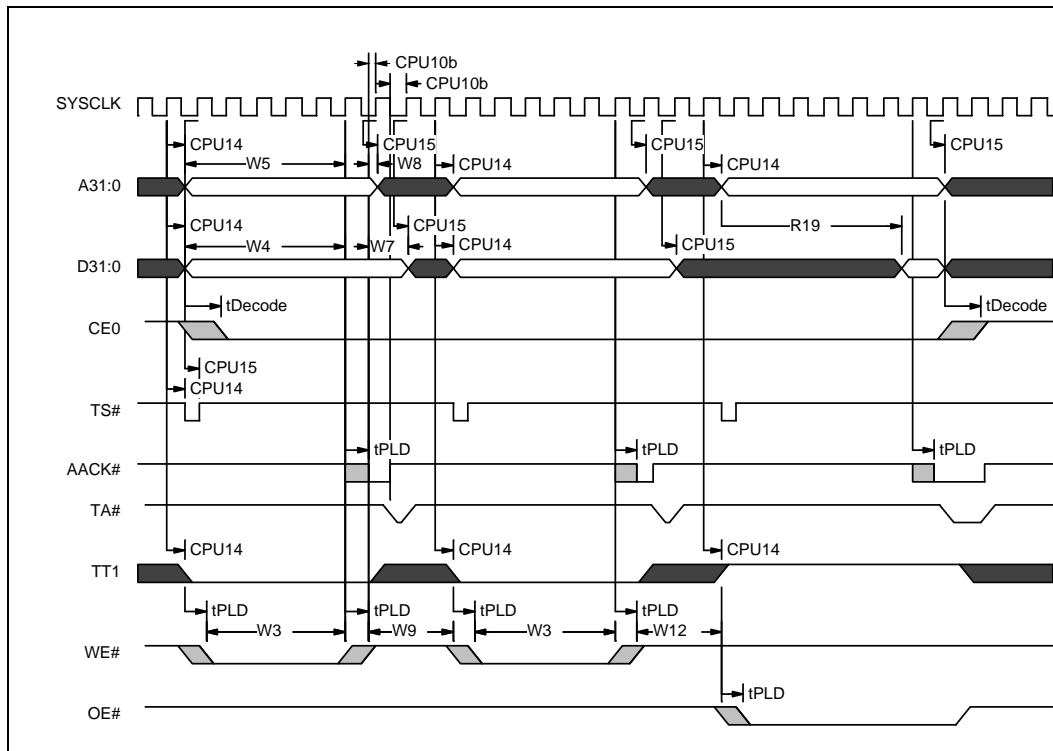


Figure 5 shows two writes followed by a read. In write operations, the PLD must generate WE# in addition to pulsing AACK# and TA#. TT1 is used to trigger WE# low, which must be deasserted in the fifth clock cycle after TS# pulses with 66 MHz clock. AACK# should be pulsed low on the same clock cycle WE# goes high, and TA# pulsed low one clock cycle after that.

Figure 5. 3 Volt Intel® StrataFlash™ Memory/MPC603e Write Cycles Followed by Read Cycle



Several timing considerations must be taken into account for reset. When asserted, RP# on the 3 Volt Intel StrataFlash memory must be held low for a time of at least t_{PLPH} (35 μ s) when block erase, program, or lock-bit configuration commands are being executed. When HRESET# is used to reset the MPC603e, the processor requires it to be held low for at least 255 clock cycles, which at 66 MHz is 3.8 μ s. If RP# is connected directly to HRESET# or SRESET#, the time t_{PLPH} (35 μ s) must be taken into account. In addition, the 3 Volt Intel StrataFlash memory has a delay of 310 ns ($t_{PHQV} + t_{PHRH}$) after RP# becomes high until the first output is available. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

Read all pertinent datasheets before attempting an interface.

4.0 Summary

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. Interfaces between 3 Volt Intel StrataFlash components and various processors can generally be accomplished with a PLD to generate wait-states and WE#, and a decoder to generate chip enable signals. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	<i>Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A datasheet</i>
298130	<i>Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update</i>
297859	<i>AP-677 Intel® StrataFlash™ Memory Technology</i>
292222	<i>AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture</i>
292221	<i>AP-663 Using the Intel® StrataFlash™ Memory Write Buffer</i>
292218	<i>AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory</i>
292204	<i>AP-646 Common Flash Interface (CFI) and Command Sets</i>
292172	<i>AP-617 Additional Flash Data Protection Using V_{PP} RP#, and WP#</i>

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at <http://www.intel.com> for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at <http://developer.intel.com/design/flash/isf>.

