3 Volt Intel® StrataFlash™ Memory to Motorola MC68060 CPU Design Guide

Application Note 703

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Contents

Revision History

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07/20/99	-001	Original version
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1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the Motorola MC68060 processor.

This document was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory:28F128J3A, 28F640J3A, 28F320J3A* datasheet.

3.0 Interfacing 3 Volt Intel® StrataFlash™ Memory to MC68060 at 66 MHz

The MC68060 series of microprocessors by Motorola offers performance of over 100 MIPS at 66 MHz. The RISC-based processor includes separate 8-kilobyte instruction and data caches. The MC68060 comes with both a floating point unit and a memory management unit, and the MC68LC060 comes with a Memory Management Unit (MMU) but no Floating Point Unit (FPU), and the MC68EC060 comes with neither an MMU nor an FPU.

3.1 Interface Considerations

This sample interface between the MC68060 and 3 Volt Intel StrataFlash memory uses two 3 Volt Intel StrataFlash memory chips to match the MC68060's 32-bit bus, and standard system logic such as a decoder and a PLD. The timing diagrams and other specifications were made assuming a 66 MHz bus and the 32-Mbit 3 Volt Intel StrataFlash memory. Other bus speeds and memory sizes could be used by modifying this slightly. Both the MC68060 and the 3 Volt Intel StrataFlash memory can interface at 3 V and 5 V. Minimum and maximum delays for the decoder and PLD are shown in the table below. These min/max numbers are used for the timings shown in Figure 3 and Figure 4. This sample interface does not include information about bus arbitration signals such as BG#, BB#, and BTT#. They should be asserted or negated as necessary for bus control.

Device	Min	Max
Decoder	0 ns	19 ns
PLD	0 ns	9 ns

3.2 Processor Interface Signals

$A_{31:2}$: The address bus transfers address from processor to memory.

$D_{31:0}$: The data bus carries data between the processor and memory.

TS#: Transfer Start is asserted by the processor at the start of a bus cycle.

TA#: Transfer Acknowledge is asserted to the processor to acknowledge a data transfer.

CLA: Cycle Long-Word Address can be toggled to change A3 and A2.

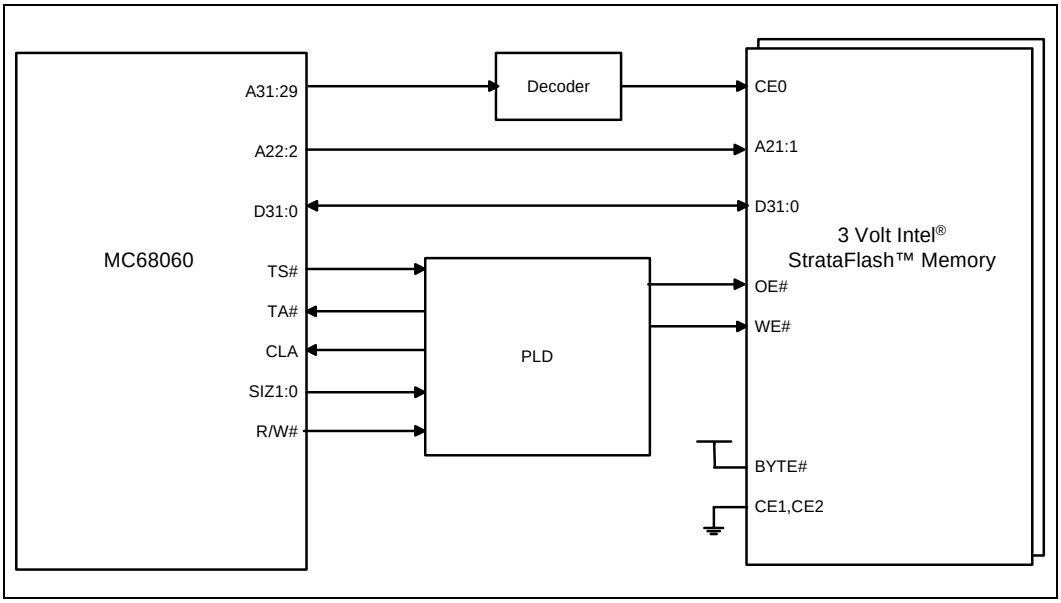
SIZ1:0: Defines the size of the transfer in progress and indicates if the current transfer is a cache line transfer.

R/W#: Indicates if current transfer is a read or a write.

3.3 Control Signal Generation

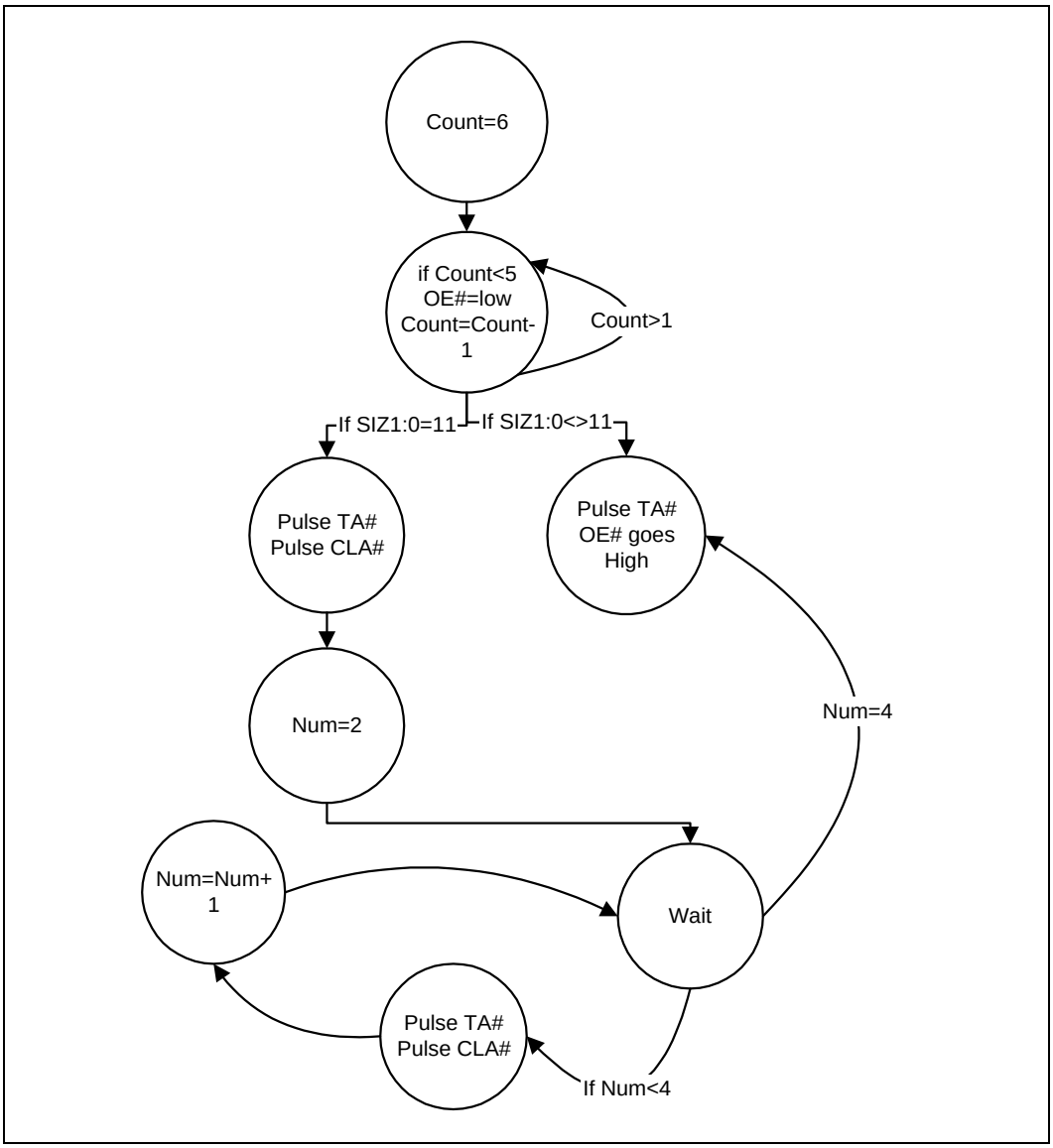
Figure 1 is a block diagram of the interface. CE_0 is generated from a decoder; CE_1 and CE_2 are tied to ground. OE# and WE# are generated by the PLD. R/W# is used to determine if the cycle is a read or a write. TS# indicates the start of a transfer cycle. SIZ1:0 are used by the PLD to determine if the transfer is a single transfer or a cache line transfer. TA# is used to indicate the completion of a transfer and can be used to create wait-states. CLA is used to control the changing of the lower addresses on cache line transfers.

Figure 1. 3 Volt Intel® StrataFlash™ Memory/MC68060 Interface



The PLD logic used to generate TA#, CLA, and OE# for read operations is outlined in Figure 2. TS# is used to initiate all data transfers. If R/W# indicates a write, WE# should be asserted. If R/W# indicates a read, the PLD should wait several cycles before asserting OE#. This is to make certain that the specified time from WE# high to OE# low (t_{WHGL}) has elapsed before the assertion of OE# in case the previous transaction was a write. TA# should be asserted when the 3 Volt Intel StrataFlash memory has placed valid data on the bus. If SIZ1:0 is 11b, CLA should also be asserted with TA#, and if the cycle is a read, page-mode timings should be used.

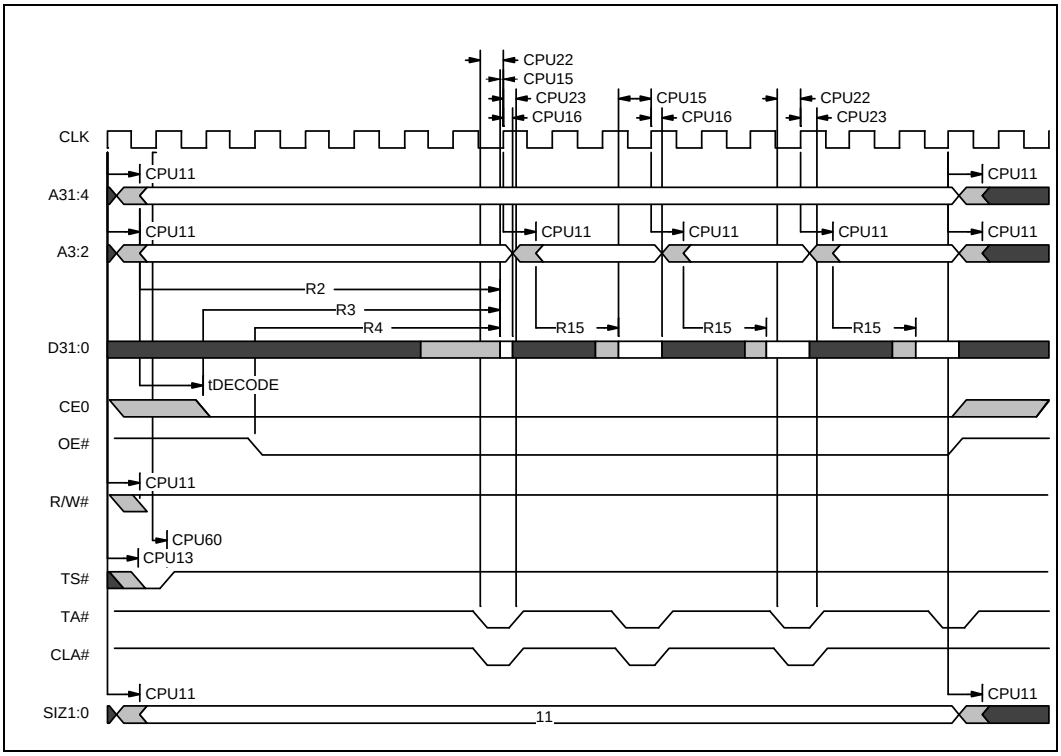
Figure 2. 3 Volt Intel® StrataFlash™ Memory/MC68060 Wait-State Generator Logic Diagram for Read Operations



NOTE: Diagram assumes page-mode is enabled and accesses are sequential. Initial wait-states are for 32-Mbit 3 Volt Intel® StrataFlash™ memory.

Figure 3 is a timing diagram of a line read transfer. The transfer is initiated when TS# is pulsed low by the processor. In the same clock cycle, address and other information is placed on the bus. OE# is asserted later, and when the data becomes valid, TA# is pulsed to complete the first word transfer and CLA# is pulsed to change the lower addresses. In the case of a line read transfer, the next three addresses are inside the page, so page-mode timings can be used. The processor does not pulse TS# a second time, but TA# and CLA# are asserted like the first transfer.

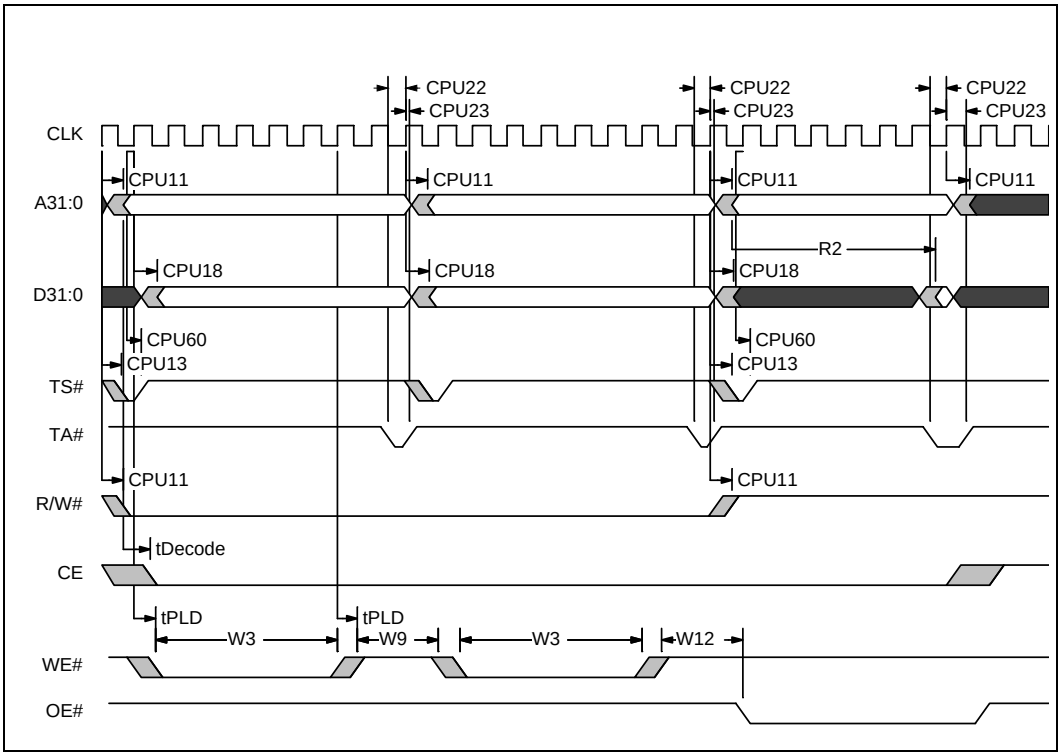
Figure 3. 3 Volt Intel® StrataFlash™ Memory/MC68060 Page-Mode Reads at 66 MHz



NOTE: The address line labels in this diagram refer to the labels on the 68060. Ax on the 68060 is Ax-1 on 3 Volt Intel® StrataFlash™ memory

Figure 4 is a timing diagram of two writes followed by a single read. The PLD asserts WE# low the cycle after TS# is asserted. It then must wait for WE# pulse low (t_{WP}) to elapse before making WE# high. After WE# is high, TA# can be pulsed low so the next cycle can begin. For consecutive writes or reads following writes, the WE# pulse high and write recovery before read times must be met.

Figure 4. 3 Volt Intel® StrataFlash™ Memory/MC68060 Write Cycles Followed by Read Cycle at 66 MHz



Several considerations must be taken into account for reset. If a block erase, program, or lock-bit configuration is taking place when RP# is asserted, RP# must be held low for a period of t_{PLPH} (35 µs). After RP# is high, there is a time of 310 ns (t_{PHQV} + t_{PHRH}) before data from a read can be returned. For external resets to the MC68060, after RSTI# goes high, the processor is held in reset internally for 27 clock cycles, which is enough to meet t_{PHQV} + t_{PHRH}. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

The only portion of the MC68060 processor's memory map that is fixed is the initial reset vector. All other addresses can be translated using the MC68060 processor's internal Memory Management Unit. The initial reset vector is located at 000h, so to boot from the 3 Volt Intel StrataFlash memory, it should be placed at that address. For purposes other than initial reset, the 3 Volt Intel StrataFlash memory may be placed in the portion of the memory map that makes it most convenient for the user.

Read all appropriate datasheets before attempting an interface (see Appendix A for a list of additional information).

4.0 Summary

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. Interfaces between 3 Volt Intel StrataFlash components and various processors can generally be accomplished with a PLD to generate wait-states and WE#, and a decoder to generate chip enable signals. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A* datasheet
298130	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP} RP#, and WP#*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.