3 Volt Intel® StrataFlash™ Memory to Intel® StrongARM* SA-110 CPU Design Guide

Application Note 701

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Contents

Revision History

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07/20/99	-001	Original version
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1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the StrongARM* SA-110.

This document was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory:28F128J3A, 28F640J3A, 28F320J3A* datasheet.

3.0 Interfacing 3 Volt Intel® StrataFlash™ Memory to the StrongARM* SA-110 at 40 MHz

The StrongARM SA-110 microprocessor is capable of bus frequencies between 27 MHz and 66 MHz. This interface was written for a 40 MHz bus and a 32-Mbit 3 Volt Intel StrataFlash memory device, but could be modified to any of the other available processor frequencies or sizes of the 3 Volt Intel StrataFlash memory devices.

3.1 Interface Considerations

The interface uses two 3 Volt Intel StrataFlash memory components to match the SA-110's 32-bit data bus width. A PLD and a decoder are used to generate necessary signals for this interface. All components can interface at 3.3 V. The SA-110 runs from a 1.65 V or 2.0 V power supply, and the 3 Volt Intel StrataFlash memory uses a 2.7 V to 3.6 V. Both can interface between 2.7 V and 3.6 V. Minimum and maximum delay specifications for the PLD and decoder are listed in the table below. These minimum and maximum times are those used in Figure 3 and Figure 4.

Device	Min	Max
Decoder	0 ns	9 ns
PLD	2 ns	9 ns

3.2 Processor Interface Signals

The interface uses the following signals provided by the SA-110:

$A_{31–0}$: The 32-bit address bus transmits instruction and data addresses to memory. Because $A_{1:0}$ are for 16- or 8-bit operation, A_2 on the SA-110 will correspond to A_1 on the 3 Volt Intel StrataFlash memory.

$D_{31–0}$: The bi-directional data bus transfers data between the processor and memory.

nWAIT: The Not Wait pin signals for a bus stall lasting one clock cycle. nWAIT must be changed when MCLK is low.

nRW: The Not Read/Write pin indicates whether the current cycle is a read or a write.

MCLK: The memory clock governs all memory accesses.

CLF: Cache Line Fill indicates if the current transfer is a burst transfer.

3.3 Control Signal Generation

In this interface, the SA-110 controls OE# directly with nRW. WE# is the same as nWAIT while nRW is high, and WE# is high at all other times. The decoder uses the upper addresses to generate chip enable signals. NWAIT is generated by a state machine in the PLD. Figure 1 is a block diagram of the interface, and Figure 2 is possible logic that could be used to generate nWAIT and WE#.

Figure 1. 3 Volt Intel® StrataFlash™ Memory/SA-110 Interface

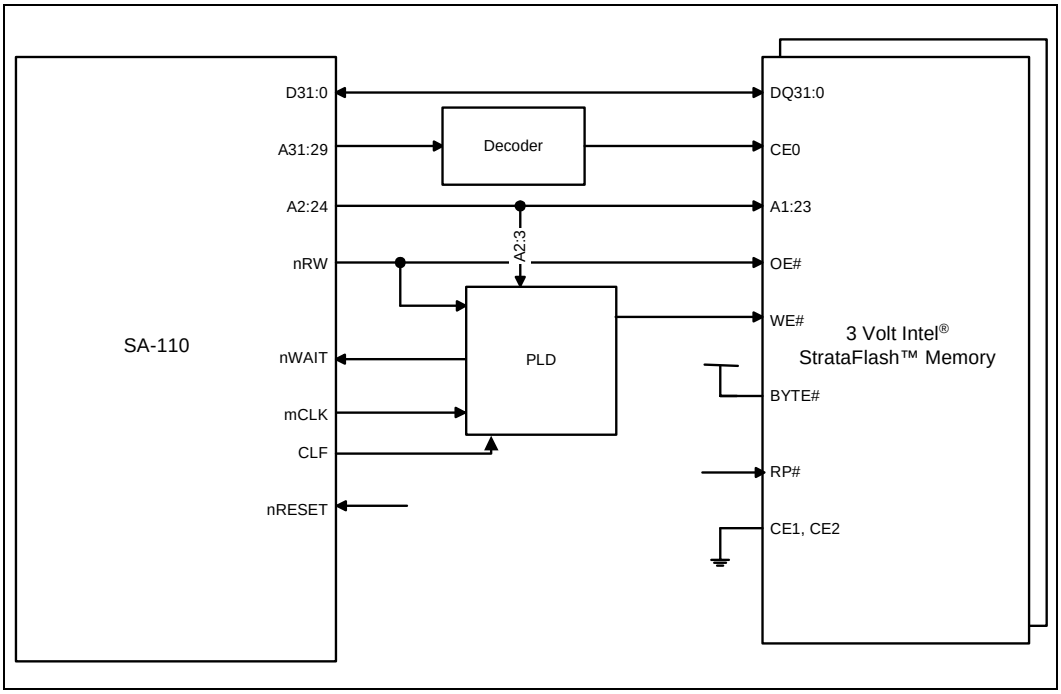
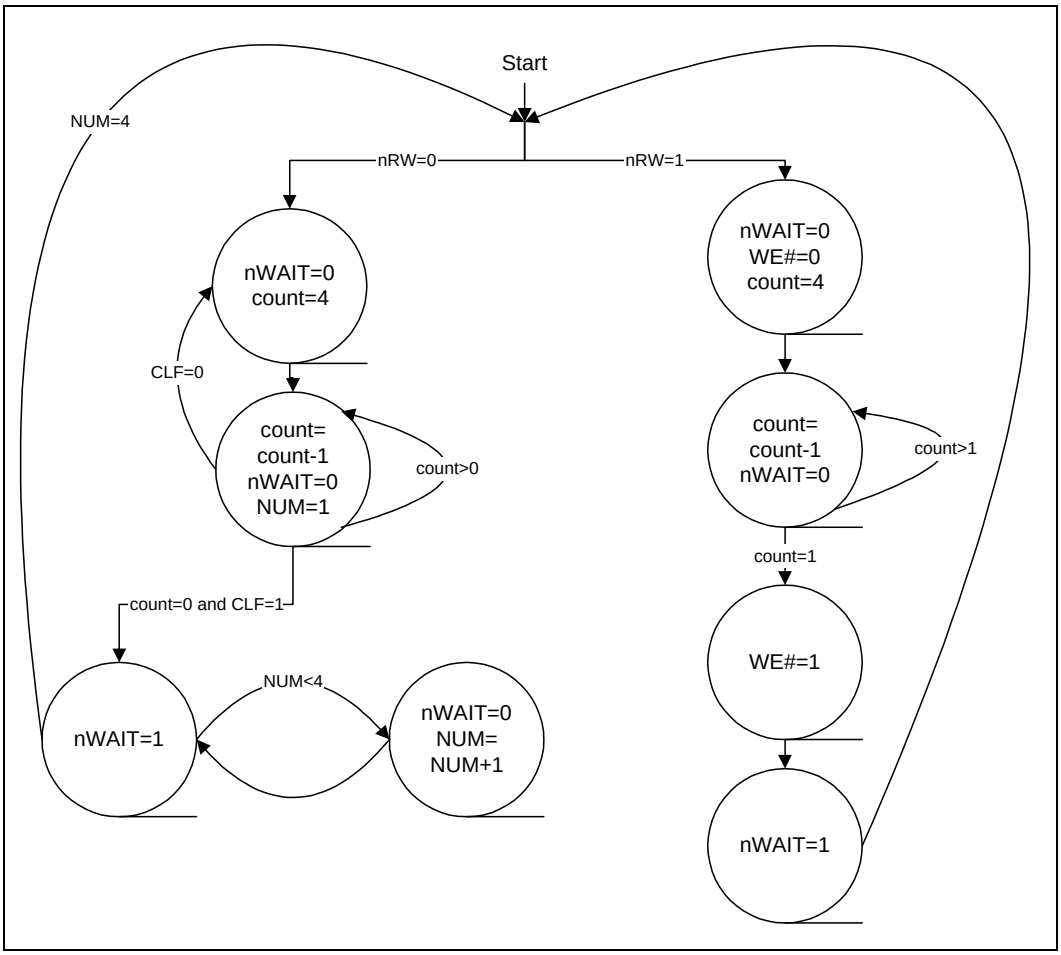


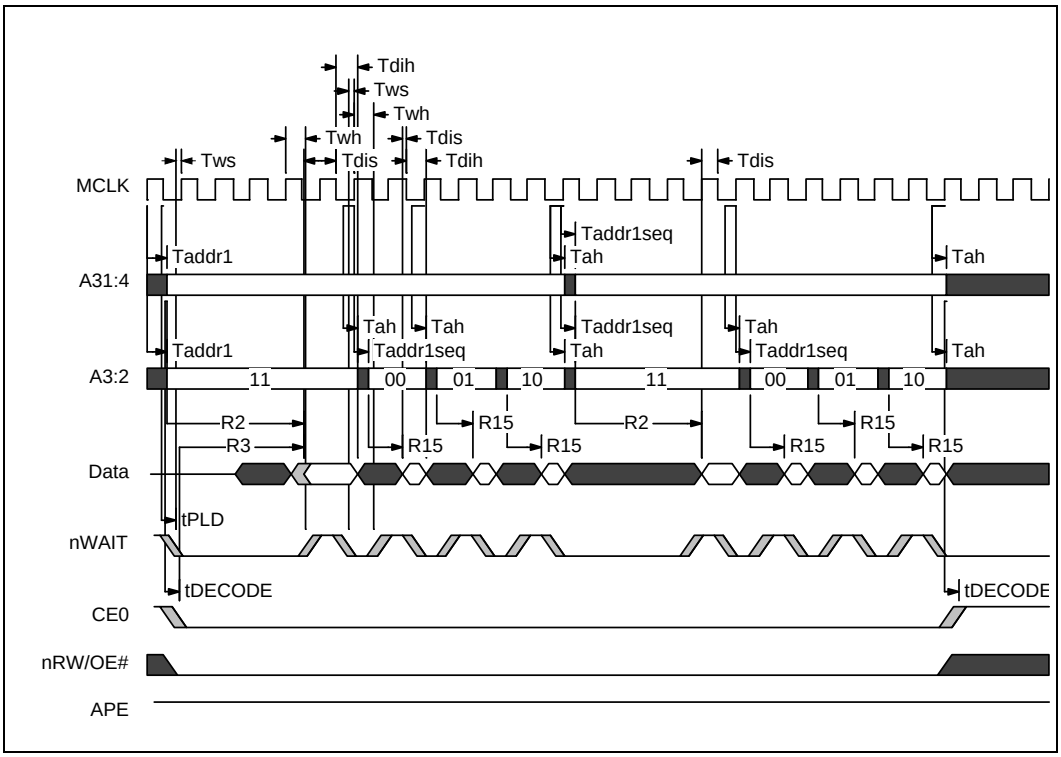
Figure 2. 3 Volt Intel® StrataFlash™ Memory/SA-110 PLD Wait-State Generator Logic



NOTE: This diagram assumes page-mode is enabled. Initial read waits assume 32-Mbit 3 Volt Intel® StrataFlash™ memory.

Figure 3 is a timing diagram of an 8-word cache line fill that does not start on a 4-word boundary. This shows the maximum delay that will be found for a cache line fill on the 32-Mbit, 3 Volt Intel StrataFlash memory.

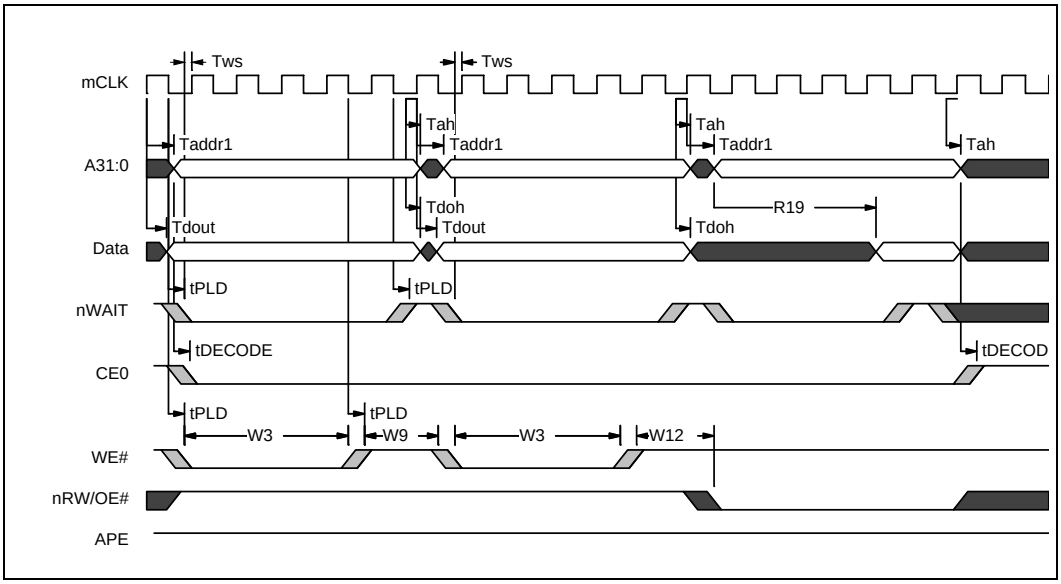
Figure 3. 3 Volt Intel® StrataFlash™ Memory/SA-110 Cache Line Fill at 40 MHz



NOTE: Address line labels in the diagram refer to address lines on the SA-110. Address Ax on the SA-110 is connected to Ax-1 on 3 Volt Intel® StrataFlash™ memory.

Figure 4 is a diagram of two writes followed by a single read. Either WE# or chip enable can be used to start a write. The address and data are latched on either WE# going high or the first chip enable change that disables the device. WE# goes high one clock cycle before nWAIT so that timing specifications for WE# pulse high and write recovery before read can be met.

Figure 4. 3 Volt Intel® StrataFlash™ Memory/SA-110 Write Cycles Followed by Read



If a reset occurs when a block erase, program, or lock-bit configuration operation is taking place, RP# must remain low for a time of t_{PLPH} (35 µs). This is less than the time when the SA-110 holds nRESET_OUT low. Therefore, this should not be a concern if RP# is connected to nRESET_OUT. The 3 Volt Intel StrataFlash memory has a longer time between RP# going high to valid data (310 ns = t_{PHQV} + t_{PHRH}) than a normal initial read. This must be taken into account if the 3 Volt Intel StrataFlash memory is the first device to be read from after a reset. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

Consult the appropriate datasheets for specific information about the individual components in the interface (see Appendix A for a list of additional information).

4.0 Summary

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. Interfaces between 3 Volt Intel StrataFlash components and various processors can generally be accomplished with a PLD to generate wait-states and WE#, and a decoder to generate chip enable signals. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A* datasheet
298130	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.