3 Volt Intel® StrataFlash™ Memory to ARM7TDMI CPU Design Guide

Application Note 700

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Contents

Revision History

Date of Revision	Version	Description
07/20/99	-001	Original version
03/30/00	-002	Reformatted document

1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memories with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory's interface to the ARM7TDMI processor.

This document was written with preliminary information about 3 Volt Intel StrataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash memory components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

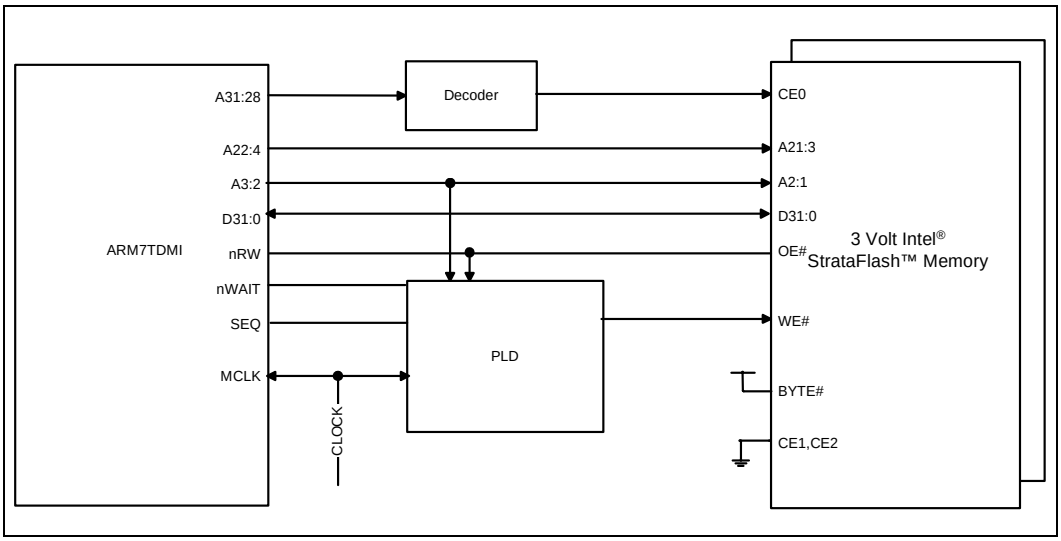
This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

All interfaces in this document use page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set using the Set Read Configuration Register command. For more information on the RCR bits see the *3 Volt Intel® StrataFlash™ Memory:28F128J3A, 28F640J3A, 28F320J3A* datasheet.

3.0 Interfacing 3 Volt Intel® StrataFlash™ Memory to ARM7TDMI at 33 MHz

The ARM7TDMI microprocessor by Advanced RISC Machines, Ltd. uses both a 32-bit ARM instruction set and a 16-bit THUMB instruction set. This allows for 16-bit instructions on a 32-bit architecture. This interface uses two 3 Volt Intel StrataFlash components to match the 32-bit data bus on the ARM7TDMI. Figure 1 is a block diagram of the interface between the 3 Volt Intel StrataFlash memory and ARM7TDMI.

Figure 1. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI Interface



3.1 Interface Considerations

In addition to the two 3 Volt Intel StrataFlash memory components, this interface uses address decoding to generate a chip enable signal and a PLD to aid in generating other signals. The additional hardware may be integrated into an ASIC. All components can operate with a power supply between 2.7 V and 3.6 V. RCR.16 should be set to enable page-mode before page-mode timings are used.

Device	Min	Max
Decoder	0 ns	14 ns
PLD	2 ns	12 ns

NOTE: These delays are for timings as shown in diagrams in this section, not necessarily the only possibilities for an interface.

3.2 Processor Interface Signals

The following signals are provided by the ARM7TDMI.

$A_{31:0}$: The 32-bit address bus transmits addresses to memory from the processor.

$D_{31:0}$: The 32-bit data bus transfers data between the processor and memory.

MCLK: The Memory Clock signal times all memory requests.

nRW: The Not Read/Write indicates whether the current data transfer is a read or a write.

nWAIT: The Not Wait input indicates to the processor that a bus stall is needed. nWAIT can only change when MCLK is low.

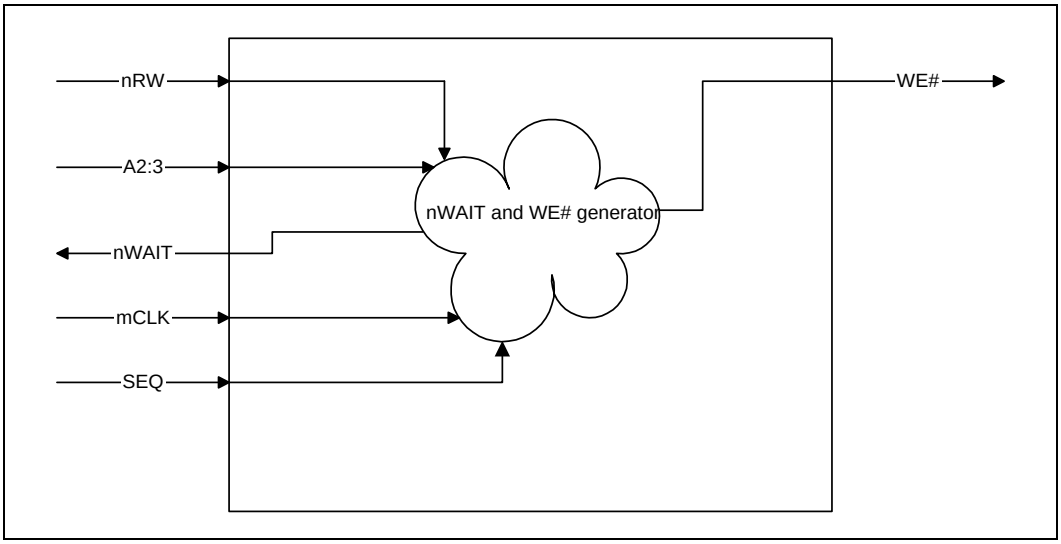
SEQ: The Sequential Address signal indicates if the next address will follow the previous one.

APE: Address Pipeline Enable is used to modify the timing of signals put on the bus. In this interface, it is always low.

3.3 Control Signal Generation

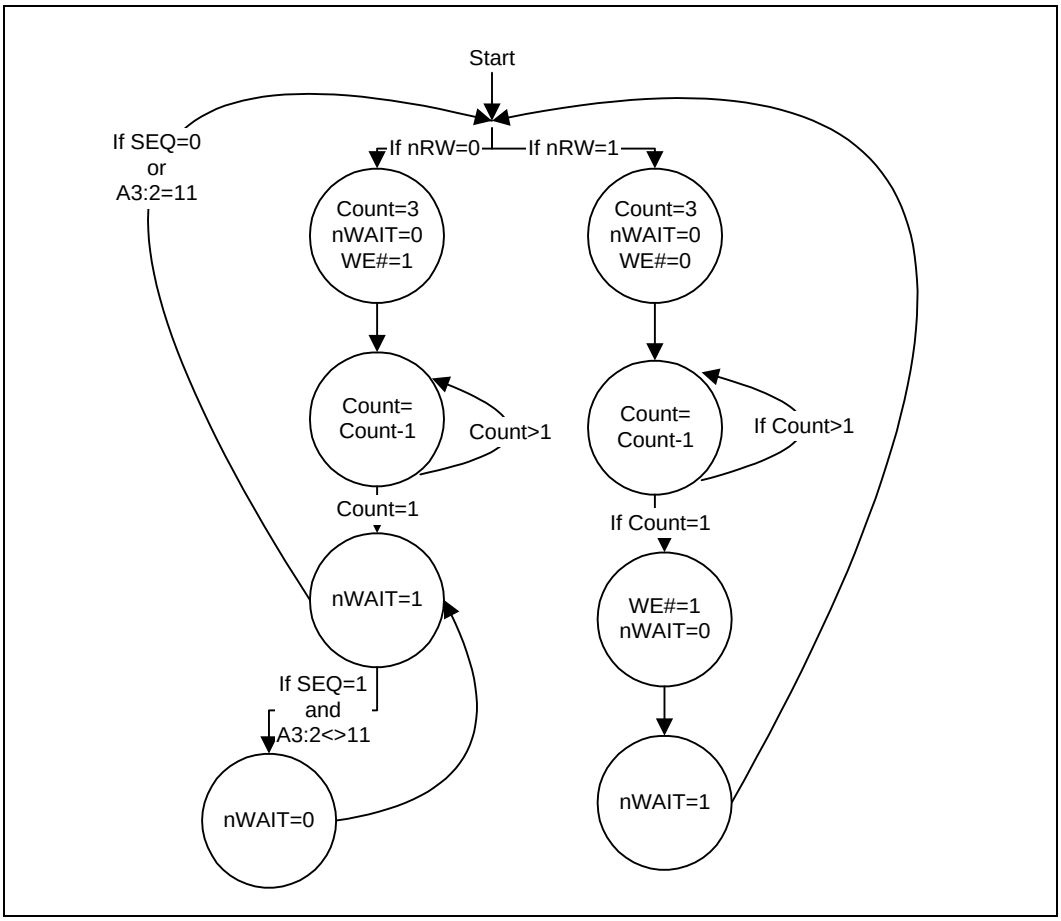
The address decoding generates the chip enable signal from the higher address lines. The PLD generates all other signals that are not directly connected. The 3 Volt Intel StrataFlash memory's OE# can be directly connected to the ARM7TDMI nRW. SEQ, nRW, and the lower address lines are used to generate nWAIT, which is the same as WE# for write operations. Figure 2 is a diagram of the PLD configuration.

Figure 2. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI PLD Configuration



For read operations, SEQ and $A_{3:2}$ are used to determine how many wait-states are necessary—the delay of an initial read or the shorter time necessary for a page-mode read. Wait-states for a page-mode read should be inserted when SEQ was asserted in the previous cycle and $A_{3:2}$ do not switch from 11 to 00. If either SEQ was not asserted in the previous cycle or $A_{3:2}$ switch from 11 to 00, wait-states for an initial read should be inserted. Figure 3 is a diagram of the wait-state logic.

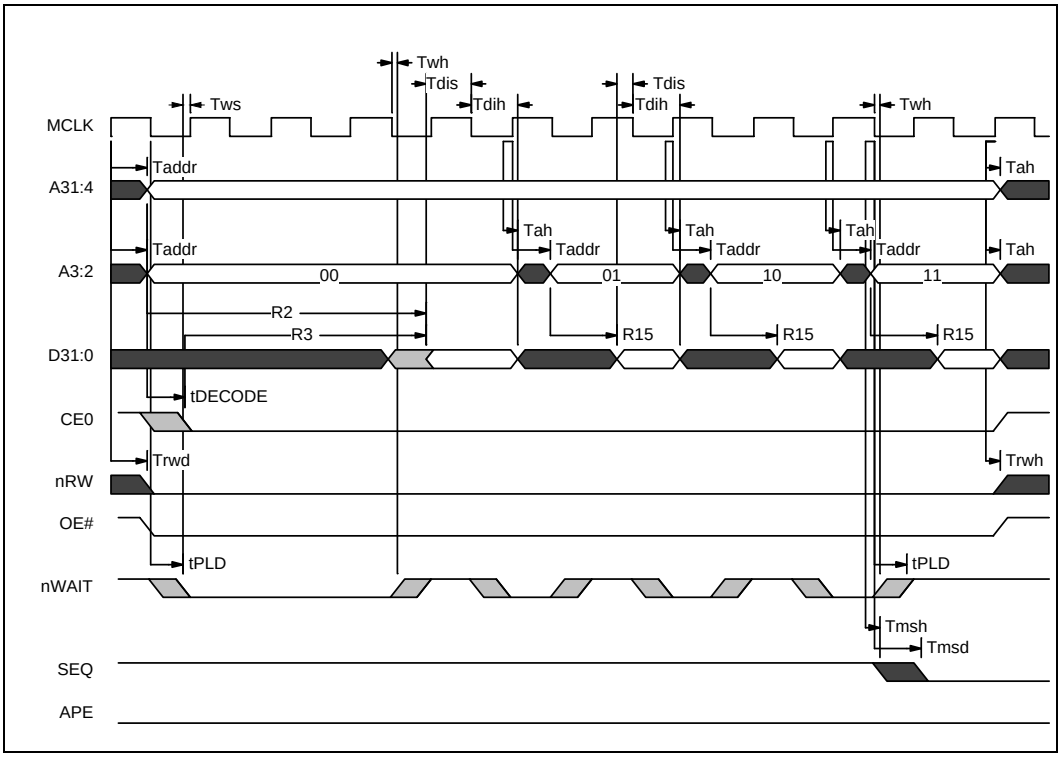
Figure 3. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI Wait-State Logic



NOTE: Diagram assumes page-mode is enabled. Initial wait-states are for 32-Mbit 3 Volt Intel® StrataFlash™ memory.

Figure 4 is a timing diagram of four reads using page-mode accesses. nWAIT is used to delay the processor for several clock cycles on the initial access and for one clock cycle on subsequent accesses. Note that in Figure 4 it is assumed that the access is the first access in the memory region, so the ARM7TDMI inserts an extra wait-state without being signaled by nWAIT.

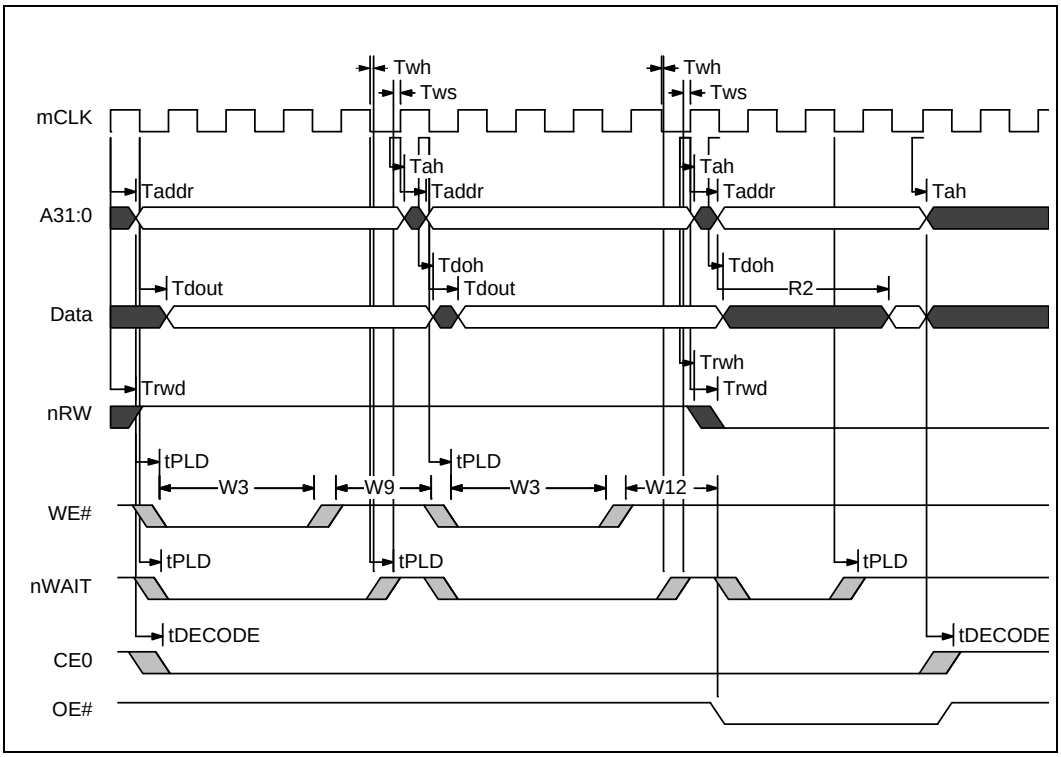
Figure 4. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI Four Word Read at 33 MHz with Page Mode Enabled



NOTE: The address line labels in this diagram refer to the labels on the ARM7TDMI. Ax on the ARM7TDMI is Ax-1 on 3 Volt Intel® StrataFlash™ memory.

Figure 5 is a timing diagram of two writes followed by a read. WE# and nWAIT should go low at the same time, but WE# should go high one clock cycle before nWAIT. This allows for the WE# pulse high and write recovery before read specifications to be met.

Figure 5. 3 Volt Intel® StrataFlash™ Memory/ARM7TDMI Write Cycles Followed by Read



Several considerations must be taken into account when resetting or powering down the system. When block erase, program, or lock-bit configuration is taking place and RP# is asserted low to the 3 Volt Intel StrataFlash memory, RP# must be held low for a time of t_{PLPH} (35 µs). The 3 Volt Intel StrataFlash memory also has a time of 310 ns (t_{PHQV} + t_{PHRH}) before output is valid after RP# goes high. This is longer than a normal initial page access, so if the ARM7TDMI makes its first access from the 3 Volt Intel StrataFlash memory, this must be taken into account. Whenever the 3 Volt Intel StrataFlash memory comes out of reset/power down, RCR.16 must be set to enable page-mode.

Consult the appropriate datasheets for specific information about the individual components in this interface (see Appendix A for a list of additional information).

4.0 Summary

3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. Interfaces between 3 Volt Intel StrataFlash components and various processors can generally be accomplished with a PLD to generate wait-states and WE#, and a decoder to generate chip enable signals. 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. 3 Volt Intel StrataFlash memory is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A* datasheet
298130	*Intel® StrataFlash™ Memory; 28F128J3A, 28F640J3A, 38F320J3A Specification Update*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP}, RP#, and WP#*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.