3 Volt Intel® StrataFlash™ Memory to Hitachi SH7750 (SH-4) CPU Design Guide

Application Note 699

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Contents

Revision History

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07/20/99	-001	Original version
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1.0 Introduction

3 Volt Intel® StrataFlash™ memory provides reliable two-bit-per-cell technology at a low cost. This product offers higher performance than previous 5 Volt Intel® StrataFlash™ memory with faster read times and a page-mode interface for increased speed. Other benefits include more density in less space, high-speed interface, support for code and data storage in the same device, and Common Flash Interface (CFI) for easy migration to future devices.

This application note will cover the 3 Volt Intel StrataFlash memory interfaces to Hitachi SuperH® SH7750 (SH-4).

This document was written with preliminary information about 3 Volt Intel StataFlash memory. Any changes in those specifications may not be reflected in this document. These interfaces have not been implemented in hardware. Refer to the appropriate documents or sales personnel for the most current information.

2.0 Hardware Interface

This section describes signals and considerations that occur in most of the interfaces.

The interfaces in this document use the following signals generated by the 3 Volt Intel StrataFlash memory:

V_{CC}: Device power supply. 2.7 V – 3.6 V

V_{CCQ}: Output buffer power supply. This voltage controls the device's output voltages. 5 V ± 10% or 2.7 V – 3.6 V

OE#: Output enable is an active low signal that activates the device's outputs during a read operation. Any data remaining on the bus after this signal is driven high will be lost. This signal must remain inactive during a write operation.

WE#: Write enable is an active low signal that controls writes to the Command User Interface, write buffer, and array blocks. The rising edge of this signal latches addresses and data. WE# must remain inactive during read access, and must toggle between consecutive writes.

$CE_{0:2}$: The three chip enable signals activate the device's control logic, input buffers, decoders, and sense amplifiers. Multiple chip enable signals allow switching between several 3 Volt Intel StrataFlash components without additional decoding. For all designs in this document, CE_1 and CE_2 are tied to ground. CE_0 is used as the only signal to enable the device. Chip enable signals must remain in an active state during any read or write access. When the CE pins disable the 3 Volt Intel StrataFlash memory, the device is deselected and power consumption is reduced to standby levels. For more information on typical CE configurations see the *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet.

RP#: Reset/Power Down is an active low signal. It resets internal automation and puts the device in power-down mode. Exit from reset sets the device in read array mode with page-mode disabled. After exiting from reset or powering on the 3 Volt Intel StrataFlash memory, bit 16 of the read control register must be set to enable page-mode timings.

BYTE#: Byte enable is an active low signal. Byte enable low places the 3 Volt Intel StrataFlash memory in x8 mode. Byte enable high places the 3 Volt Intel StrataFlash memory in x16 mode.

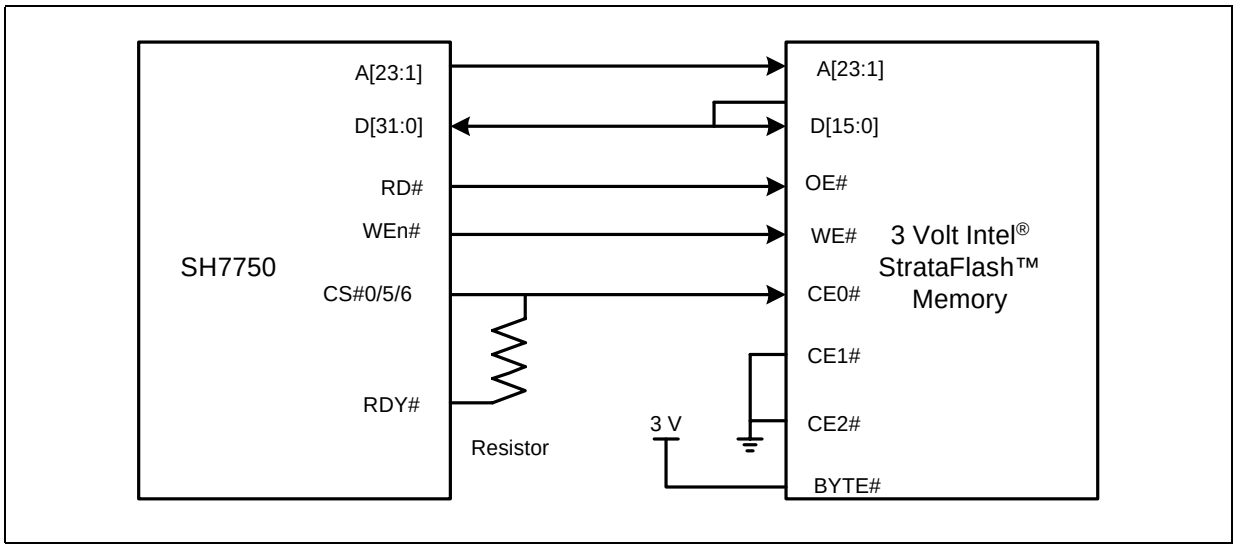
This document assumes all other pins (e.g., Address, Data, etc.) are connected in such a way as to insure proper device functioning.

3.0 Interfacing the 3 Volt Intel® StrataFlash™ Memory to SH7750 at 66 MHz

The SH7750 embedded microprocessor produced by Hitachi employs a 32-bit RISC architecture which features object code upward-compatible with the SH-1, SH-2, and SH-3 microprocessors. The SH-4 uses a 16-bit fixed-length instruction set, which enables program code size to be reduced by about 50%. Figure 1 illustrates the block diagram of the 3 Volt Intel StrataFlash memory interfaces to the SH7750.

The SH7750 allows the designer to choose the bus clock that 1/3 of the main clock (200_MHz).

Figure 1. The 3 Volt Intel® StrataFlash™ Memory Interfaces to the SH7750 Microprocessor



3.1 Interface Considerations

This sample interface uses two 3 Volt Intel StrataFlash memory devices in 16-bit mode. Timing diagrams were made with the 128-Mbit 3 Volt Intel StrataFlash components with the memory bus running at 66 MHz. There is no other required logic between the processor and the 3 Volt Intel StrataFlash memory. The bus width setting of the processor should be set at area 0, 5 or 6 for high-speed read access. A pull-down resistor is required in this interface to control the Ready (RDY#) pin of the CPU. RDY# needs to be pulled low by CE# during flash accesses to indicate the use of the CPU's internal programmable wait states.

This reference interface in this document uses page-mode timings. Before 3 Volt Intel StrataFlash memory's page-mode timings can be used, Read Configuration Register bit 16 (RCR.16) must be set to b'1 to enable the page-mode.

3.2 Processor Interface Signals

The sample reference uses the following main signals provided by the SH7750:

A_{23}–A_0: The address bus signals the memory which piece of information is to be accessed.

D_{31}–D_0: The data bus contains bi-directional data paths to transfer data between the processor and the flash memory.

CSn#: The Chip Select signal indicates which memory bank the processor is accessing.

RD#/WEn#: Read/Write indicates the direction of the current data transfer.

RDY#: The Ready pin is driven by external devices to insert external wait-states.

3.3 Control Signal Generation

Figure 2 shows a four-word page-mode read timing diagram. The wait-states are generated internally by programming the CPU's Wait Control Registers (WCR).These registers should be set to 9 for the first page-mode read cycle to insert wait-states. The subsequenct Burst Pitch is one wait-state. If the designer selects area 6, bits 31:29 of the WCR2 should be set to b'101. If the designer selects area 5, bits 25:23 should be set to b'101. Similarly, bits 5:3 should be set to b'101 for the area 0.

Figure 3 shows a write timing diagram. The designer needs to have four wait-states inserted. A pull-down register is connected between CSn# and RDY# to pull RDY# low during flash accesses and to allow other devices to drive RDY# low during flash accesses and to allow other devices to drive RDY# during other memory accesses. The specific value of the resistor will depend on the specific system design.

In the Bus Control Register 1 (BCR1), bits 13:11 should be set b'001 for the four consecutive accesses if the designer selects the area 0. The bits 10:8 of the BCR1 should be set to b'001 if the designer selects area 5. Similarly, bits 7:5 should be set b'001 to enable area 6.

In register BCR2, if the designer selects area 5, bit 11 (bit: 2n+1 = 2*5+1 = 11) should be set to b'1 and bit 10 (2*n = 2*5 = 10) should be set to b'1. If the designer selects area 6, bit 13 (2*n+1 = 2*6+1 = 13) should be set b'1 and bit 12 (2*n = 2*6 = 12) should be set to b'1.

The following signal can be found in the Hitachi *SH-4 Hardware Manual*: t_{AD}, t_{CSD}, t_{RSD}, t_{WED1}, t_{RDS}, t_{RDH}.

The following signal can be located in *3 Volt Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet: R2, R3, R15.

Read all appropriate documentation before attempting this interface.

Figure 2. The 3 Volt Intel® StrataFlash™ Memory/SH7750 Four Word Page-Mode Read Cycle at 66 MHz

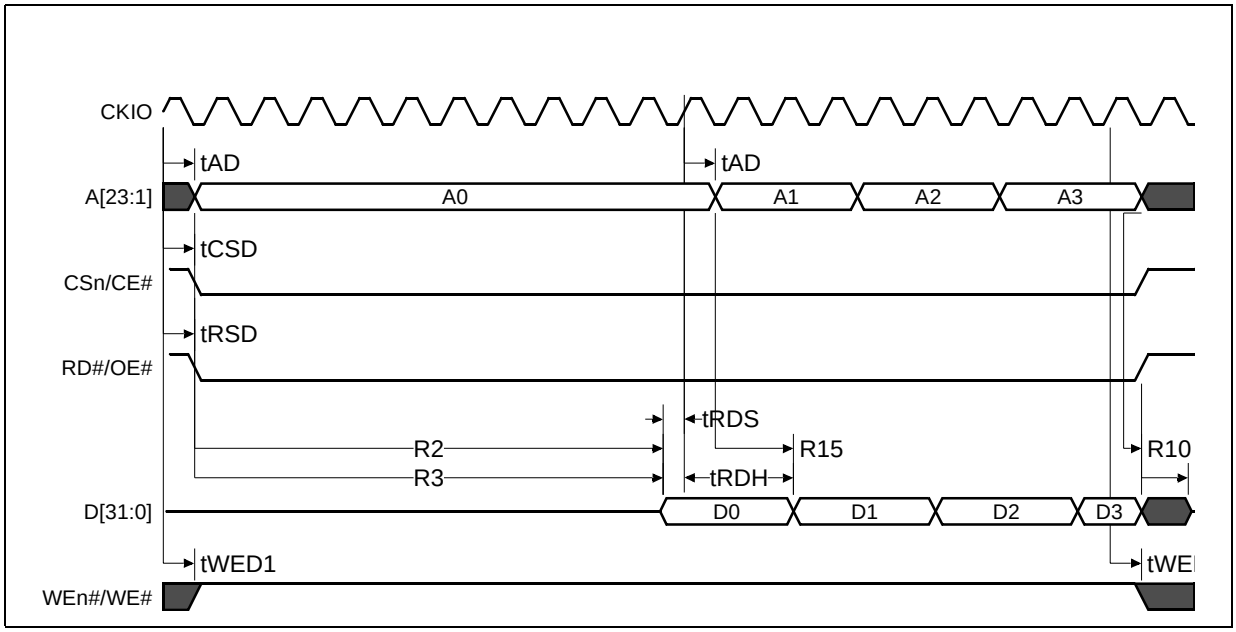
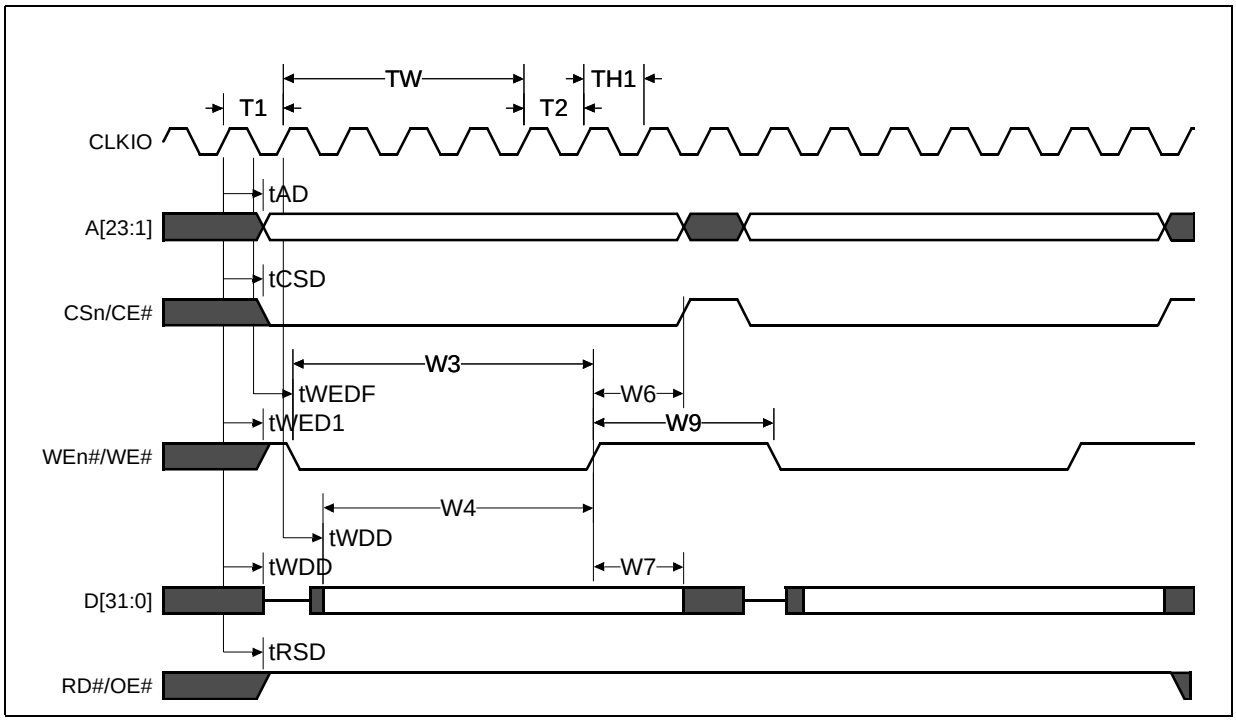


Figure 3. The 3 Volt Intel® StrataFlash™ Memory/SH7750 Write Cycle at 66 MHz



4.0 Summary

The 3 Volt Intel StrataFlash memory devices provide 2X the bits in 1X the space. These devices provide reliable two-bit-per-cell storage technology. Faster performance can be enabled by setting RCR bit 16 to enable page-mode reads. The 3 Volt Intel StrataFlash memory devices are able to have different I/O voltages by using different V_{CCQ} voltages. The 3 Volt Intel StrataFlash memory components come in a variety of different packages and densities for increased flexibility. This “glueless” interface reduce power consumption. It is an excellent option for code and data applications where high density and low cost are required.

Appendix A Additional Information

Order Number	Document/Tool
290667	*Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A* datasheet
298130	*Intel® StrataFlash™ Memory: 28F128J3A, 28F640J3A, 28F320J3A Specification Update*
297859	*AP-677 Intel® StrataFlash™ Memory Technology*
292222	*AP-664 Designing Intel® StrataFlash™ Memory into Intel® Architecture*
292221	*AP-663 Using the Intel® StrataFlash™ Memory Write Buffer*
292218	*AP-660 Migration Guide to 3 Volt Intel® StrataFlash™ Memory*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292172	*AP-617 Additional Flash Data Protection Using V_{PP} RP#, and WP#*
Note 4	*SH-4 Hardware Manual, v1.1*

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. For the most current information on Intel StrataFlash memory, visit our website at http://developer.intel.com/design/flash/isf.
4. This manual can be located at the following URL:http://semiconductor.hitachi.com/products/h_micon/1_sh/4_sh4_/H14TH002D2/pdf/h1402.pdf.