APPLICATION
NOTE

Using the Intel® StrataFlash™ Memory Write Buffer

July 1998

Order Number: 292221-001

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 80217-9808

or call 1-800-879-4683
or visit Intel's Website at http://www.intel.com

CG-041493

CONTENTS

PAGE

TABLES

REVISION HISTORY

Date of Revision	Version	Description
07/10/98	-001	Original version

1.0 INTRODUCTION

Each Intel® StrataFlash™ memory device includes a 16-word (32-byte) write buffer. Using the write buffer can improve programming performance up to 20 times over non-Write Buffer writes. This application note explains how to use the write buffer on Intel StrataFlash memory devices.

1.1. Common Flash Interface

Intel StrataFlash memory supports the Common Flash Interface (CFI). CFI is a published, standardized data structure. It includes a standard set of commands and allows system software to query the device for information about functions supported by the device, various electrical and timing characteristics, and to determine configurations. More information about Common Flash Interface is available in the application note *Common Flash Interface (CFI) and Command Sets*, order number 292204.

It is recommended to incorporate CFI into designs using Intel StrataFlash memory. This allows for easier upgrades between CFI-compliant products. CFI reference code is available from Intel’s developer‘s website at “http://developer.intel.com.” This CFI reference code already utilizes the Write to Buffer algorithm and commands. This reference code allows the host system’s software to communicates with Intel StrataFlash memory. Thus, the software engineer can simply integrate this software into their application code instead of having to write device drivers from scratch.

2.0 USING THE WRITE TO BUFFER COMMAND

Writing to the buffer is initiated with the Write to Buffer command, along with an address in a block. All addresses written to the flash in a single Write to Buffer sequence must be in the same erase block. After the command is issued, the eXtended Status Register (XSR) can be read by lowering OE#. Status register bit 7 (DQ_7) indicates if the Write Buffer is available. If the buffer is available, the number of bytes or words to be programmed is written to the device. Next, the first byte or word to be programmed should be written to the device, followed by the other bytes/words for programming. These bytes/words are written to the buffer at the read/write cycle time of t_{AVAV}. After the last piece of data is written to the buffer, a Program Buffer to Flash Confirm command must be issued. While the buffer is being programmed to the device, the status register may be accessed by lowering OE#. The time it takes to program one byte or word from the buffer to the flash is the write buffer program time t_{WHQV1}/t_{EHQV1} or t_{WHQV2}/t_{EHQV2}. After the buffer has been programmed to the device, read array mode can be resumed by issuing the Read Array command. Table 1 shows the general steps for programming with the write buffer.

Table 1. General Write Buffer Bus Cycles

Bus Cycle Type	Cycle Purpose	Address Bus	Data Bus
Write	Initiate Write to Buffer command	Block Address	E8H–Write to Buffer command
Read[1]	Get eXtended status register value Verify if write buffer is available XSR.7 = 1 write buffer is available XSR.7 = 0 write buffer is not available	Does not matter	XSR
Write	Tell flash how many bytes/words will be written	Block Address	Number of bytes/words to be written
Write	Write data to flash	Address to be written	Data to be written
	Repeat writing data to flash		
Write	Program Buffer to Flash Confirm Command	Block Address	D0H
Read[1]	Read Status Register, check Write State Machine status, check for errors	Block Address	Status register

NOTE:

1. The status register and the XSR may be accessed by lowering OE#.

If the write buffer is not available after the first Write to Buffer command is issued, reissue the Write to Buffer command and reread the XSR until it is.

For better performance and lower power, the starting address of the data should be aligned with the beginning of a write buffer boundary (A_4–A_0 of the start address = 0). This allows for maximum programming performance and lower power consumption. The fastest per-byte programming occurs when the buffer is filled completely.

When writing the number of words to be programmed, 00H to 0FH indicates that 1 to 16 words will be written when in x16 mode. Likewise, 00H to 1FH indicates that 1 to 32 bytes will be written when in x8 mode. All addresses to be programmed must be between the start address and the start address plus the number of words or bytes to be written.

The status register indicates errors that occur during buffered writes. Table 2 is a summary of status register-indicated errors during the programming process. When SR.7 goes high after the programming is completed, then other status register bits should be checked for errors. Any time SR.4 or SR.5 is set, the device will not accept more Write to Buffer commands. If an error occurs when writing, SR.4 will be set to “1” to indicate a program failure. Only “1”s that do not successfully program to “0”s are detected by the internal WSM. If a command other than Program Buffer to Flash Confirm is given when it is expected, or if the user attempts to program past an erase block boundary, SR.4 and SR.5 will be set to “1” to indicate an “Invalid Command/ Sequence” error. If a write is attempted when $V_{PEN} \leq V_{PENLK}$ status register bits SR.4 and SR.3 are set to “1.” SR.1 and SR.4 are set to “1” when a write is attempted when the corresponding Block Lock-Bit is set and RP# = V_{IH}. The status register should be cleared after an error is detected.

Table 2. Status Register States during the Programming Process

SR.7 = 0	WSM busy, all other bits in High Z
SR.7 = 1	WSM ready
SR.4 = 1	Program error

SR.4 = 1
SR.5 = 1
	Invalid command/sequence

SR.4 = 1
SR.3 = 1
	$V_{PEN} \leq V_{PENLK}$[1]

SR.4 = 1
SR.1 = 1
	Block is locked, RP# = V_{IH}[2]

NOTES:

1. Buffered writes with invalid V_{PEN} and V_{CC} voltages produce spurious results and should not be attempted.
2. Buffered writes with V_{IH}<RP#<V_{HH} produce spurious results and should not be attempted.

3.0 WRITING FOUR WORDS USING THE WRITE TO BUFFER COMMAND

This is an example of writing four words of data in x16 mode using the write to buffer command. Table 3 is a listing of bus activity for programming these four words. The data will be written at a starting address of 015600H. This address is at a page buffer boundary. The four words to be written are represented with “XX.”

The commands follow the same sequence as shown in Table 1. The Write to Buffer command is issued normally, followed by reading the extended status register and checking XSR.7 for write buffer status. Four is then written to tell the device the number of words to be written. Next, the four words of data are written, followed by the Program Buffer to Flash Confirm command. Finally, the status register should be monitored to make certain that programming completes successfully.

Table 3. Writing Four Words Using the Write Buffer

	Bus Cycle Type	Address Bus[1,2]	Data Bus	Comment
1	Write	010000H	E8H	Write to Buffer command
2	Read[3]	010000H	XSR	Read XSR, check XSR.7 1 = write buffer is available 0 = write buffer busy
3	Write	010000H	03H	Writing 03H means four words will be programmed
4	Write	015600H	XX	Data to be programmed.
5	Write	015602H	XX	Data to be programmed.
6	Write	015601H	XX	Data to be programmed.
7	Write	015603H	XX	Data to be programmed.
8	Write	010000H	DOH	Program Buffer to Flash Confirm command

9	Read[3]	010000H	Status Register	Read Status Register, check SR.7
				SR.7 = 1 ⇒ WSM Ready
				SR.7 = 0 ⇒ WSM Busy
				(See Table 2 for error checking.)

NOTES:

1. Addresses listed assume the flash device address is at 000000H.
2. In this example when address 010000H is shown any address in the block may be used.
3. The status register and the XSR may be accessed by lowering OE#.

The total time to program these four words can be found by using the specifications in the *Intel® StrataFlash™ Memory Technology, 32 and 64 Mbit* datasheet, order number 290606. The Read/Write cycle time t_{AVAV} is used for each write cycle to the flash, including each word written and issuing the Write to Buffer command, writing the number of words to be programmed, and writing Program Buffer to Flash Confirm command. For each word programmed, the time t_{WHQV2}/t_{EHQV2} should be added as well. Finally, for every time the SR or XSR is read by lowering OE#, the time t_{GLQV} should be added. For this example, the total time for programming four words is:

$(3*t_{AVAV})+(2*t_{GLQV})+(4*t_{AVAV})+(4*t_{WHQV2}/t_{EHQV2})$.

A more general form for Write to Buffer sequence time is:

$(3*t_{AVAV})+(2*t_{GLQV})+(N*t_{AVAV})+(N*t_{WHQV2}/t_{EHQV2})$

where N is the number of words programmed ($N \le 16$).

4.0 WRITING 32 WORDS WITH THE WRITE TO BUFFER COMMAND IN X16 MODE

Writing more bytes/words than can be contained in the write buffer requires multiple Write to Buffer commands. Table 4 shows two consecutive Write to Buffer commands with successive addresses starting at 179C0H. The words to be programmed are represented by “XX.” After the first Write to Buffer command has been confirmed, the system must wait while the write buffer data is programmed into the array. When SR.7 goes high after the programming is completed, then other status register bits should be checked for errors. If there are no errors, the next write to buffer sequence can be used to fill the buffer with the next set of data. If an error is indicated by the status register, the condition causing the error should be fixed, and the status register should be cleared before another write to buffer command is attempted. For instance, if status register bits 4 and 3 are set, this indicates that $V_{PEN} \le V_{PENLK}$.

In this case, V_{PEN} should be raised to V_{PENH}, the status register cleared, and then the Write to Buffer command attempted again. The time taken to program all the data in this example is:

$$(3*t_{AVAV})+(2*t_{GLQV})+(16*t_{AVAV})+(16*t_{WHQV2}/t_{EHQV2})$$
$$+$$
$$(3*t_{AVAV})+(2*t_{GLQV})+(16*t_{AVAV})+(16*t_{WHQV2}/t_{EHQV2})$$

for the 32 words to be written.

5.0 CONCLUSION

The Intel StrataFlash memory write buffer is intended to substantially improve programming performance of single byte/word writes. Proper use of the write buffer can result in a 20X improvement over single byte/word writes. One of the functions of the CFI reference code is to provide a means to easily integrate the write buffer functionality into an application.

Table 4. Writing 32 Words Using the Write Buffer

Bus Cycle Type	Address Bus(1,2)	Data Bus	Comment
Write	010000H	E8H	Write to Buffer command
Read[3]	010000H	XSR	Read XSR, check XSR.7 1 = write buffer is available 0 = write buffer busy
Write	010000H	0FH	Writing 0FH means 16 words to be programmed
Write	0179C0H	XX	First data to be programmed
			Write the next 14 Words
Write	0179CFH	XX	Last data to be programmed
Write	010000H	D0H	Program Buffer to Flash Confirm command

Read(3)	010000H	Status Register	Read Status Register, check SR.7
			SR.7=1⇒WSM Ready
			SR.7=0⇒WSM Busy
			(See Table 2 for error checking.)

Write	010000H	E8H	Write to Buffer Command
Read(3)	010000H	XSR	Read XSR, check XSR.7 1=write buffer is available 0=write buffer busy
Write	010000H	0FH	Write 0FH means 16 words to be programmed
Write	0179D0H	XX	First data to be programmed
			Write the next 14 words
Write	0179FFH	XX	Last data to be programmed
Write	010000H	D0H	Program Buffer to Flash Confirm command

Read(3)	010000H	Status Register	Read Status Register, check SR.7
			SR.7 = 1 ⇒WSM Ready
			SR.7 = 0 ⇒WSM Busy
			(See Table 2 for error checking.)

NOTES:

1. Addresses listed assume the flash device address is at 000000H.
2. In this example when address 010000H is shown any address in the block may be used.
3. The status register and the XSR may be accessed here by lowering OE#.

APPENDIX A
ADDITIONAL INFORMATION

Order Number	Document/Tool
210830	*Flash Memory Databook*
290606	*Intel® StrataFlash™ Memory Technology 32 and 64 Mbit* datasheet
292204	*Common Flash Interface (CFI) and Command Sets*

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.