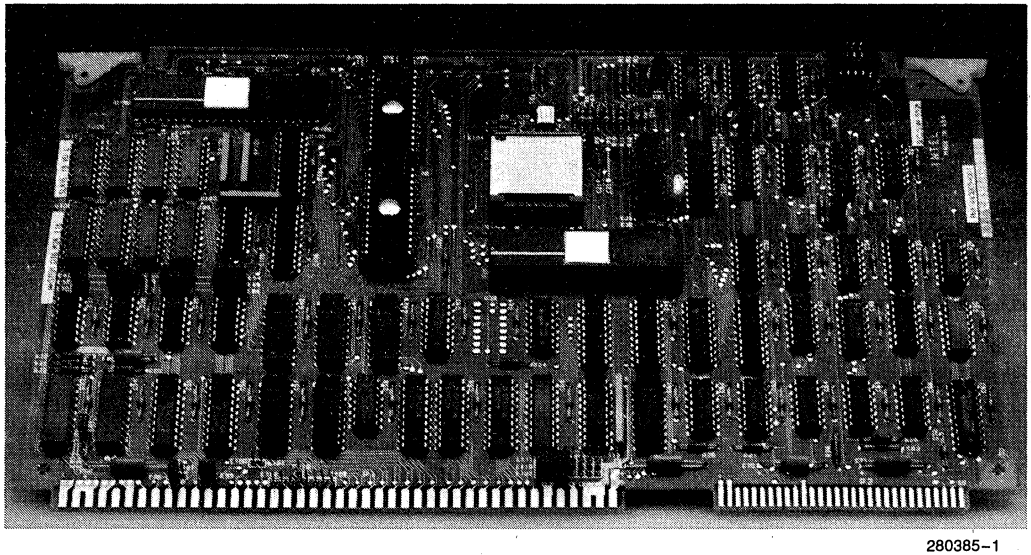
iSBC® 552A AND iSXM™ 552A IEEE 802.3 COMPATIBLE COMMUNICATIONS ENGINE PRODUCTS MEMBER OF THE OpenNET™ PRODUCT FAMILY

- **Provides High-Performance Network Front-End Processing for All MULTIBUS® I Systems Regardless of the Operating System of the Host**
  - **— Intelligent Controller with an 8 MHz 80186 Processor and 256K of DRAM Memory**
  - **— IEEE 802.3 Network Port Driven by the 82586 LAN Coprocessor**
- **Can Execute On-Board the Intel iNA 960/961 Software, an Implementation of Industry Standard ISO 8073 Transport and ISO 8473 Network Protocols**
- **Resident Network Software Can be Down-Loaded Over the Bus or the LAN**
- **On-Board Diagnostic and Boot Firmware**
- **Supported by XNX-NET and RMX-NET Network File Service Software Products**
- **Available in Two Versions**
  - **— iSBC 552A is a Flexible, Intelligent Communications Controller for IEEE 802.3 LANs**
  - **— iSXM™ 552A is a Preconfigured Controller for Executing iNA 961 Transport and Network Software as a Fully Qualified System Extension Module for the System 310 Family Products**

The iSBC 552A and iSXM 552A COMMengine products are designed for communications front end processor applications connecting MULTIBUS I systems onto IEEE 802.3 compatible LANs. COMMengines are dedicated to the communications tasks within a system allowing the host to spend more time processing user applications. A major advantage of COMMengines is that they can be used to network existing systems and established designs without forcing the redesign of the entire system architecture.

The iSBC and iSXM 552A boards can be used with any operating system because they require only a high level interface to communicate with the host (eg. transport commands in the case of the iSXM 552A board). The result is a powerful system building block which enables the OEM to network MULTIBUS I based systems with different operating systems. Applications for the 552A products include networked multiuser XENIX 286 based systems for the office and laboratory, iRMX-based systems for real-time applications, or many other system applications.



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THE iSBC® BOARD vs THE iSXM™ BOARD

The iSBC 552A version is a board that offers the hardware necessary for the user to construct an IEEE 802.3 front-end processor for custom requirements. The Intel iNA 960 ISO standard transport and network software can be configured and optimized to run on the iSBC 552A board.

The iSXM 552A version is a product that is preconfigured for Intel's family of System 310 products, includes the necessary internal system cabling, and is fully qualified to run in System 310 products. The iSXM 552A board supports the iNA 961 ISO standard transport and network software with no configuration activities required of the customer. iSXM 552A board customers receive the iNA 961 software through a separate purchase of a software license.

ARCHITECTURE DESCRIPTION

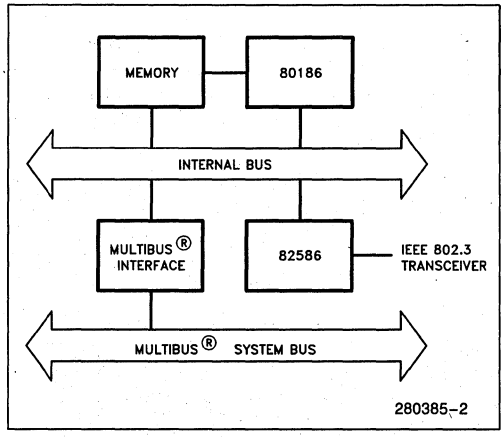


Figure 1. iSBC®/iSXM™ 552A Architecture

The iSBC and iSXM 552A boards consist of the following major architectural blocks (see Figure 1): an 80186 processor running at 8 MHz, the IEEE 802.3 I/O channel based on the 82586 LAN coprocessor, the on-board memory consisting of ROMs and 256K of zero wait state dynamic RAM, and the MULTIBUS I interface.

Processor

The iSBC 552A board contains an 80186 processor operating at 8 MHz. It is responsible for implement ing the intelligent interface between the iSBC 552A board and a host processor. The 80186 processor runs the iNA 960/961 transport software and delivers data between user buffers in MULTIBUS I memory and iNA 960/961 buffers on the iSBC and iSXM 552A boards. iNA 960/961 software is responsible for the reliable transfer of information across the IEEE 802.3 compatible network.

The 80186 and 82586 use both synchronous and asynchronous ready logic. The 80186 chip select lines are used to select memory mapped I/O locations.

The 80186 supplies the timers and the interrupt controller on the iSBC 552A board. The interrupt controller is used in the fully nested mode. The inputs and the outputs of the 80186 timers are not connected to external sources and destinations. Timer clocking and timer interrupts are generated internally in the 80186.

Memory

The iSBC/iSXM 552A board is equipped with 256K Bytes of zero wait state dynamic RAM and 16K Bytes of EPROM. The EPROM parts (Type 2764) are in two 28-pin sockets (JEDEC 27256 or 27572). The user can substitute parts (Type 27512) to provide 128K Bytes of EPROM.

The one megabyte address space of the 80186 is divided into four quadrants (see Figure 2). The first quadrant (0–256K Byte) is reserved for local EPROM memory and the last quadrant (768–1000K Byte) is reserved for local DRAM memory. The second quadrant (256–512K Byte) is used for memory mapped I/O. The iSBC/iSXM 552A board is totally memory mapped. The third quadrant (512–768K Byte) maps into a 256K Byte MULTIBUS I window. This window allows the iSBC/iSXM 552A board to access a total of 16M Byte of MULTIBUS I memory in 256K Byte segments. The iSBC/iSXM 552A board does not contain any memory which is accessible by other boards over the MULTIBUS I system bus.

The 256K Byte MULTIBUS I window starts on 64K Byte boundaries anywhere in the 16M Byte MULTIBUS I memory. The starting location of this window is determined by a memory mapped I/O latch described in the "iSBC 552A User Interface" section.

Memory mapped I/O locations are selected by the PCS and the MCS control lines of the 80186 processor. Functions controlled by memory mapped I/O are discussed in the "iSBC 552A User Interface" section.

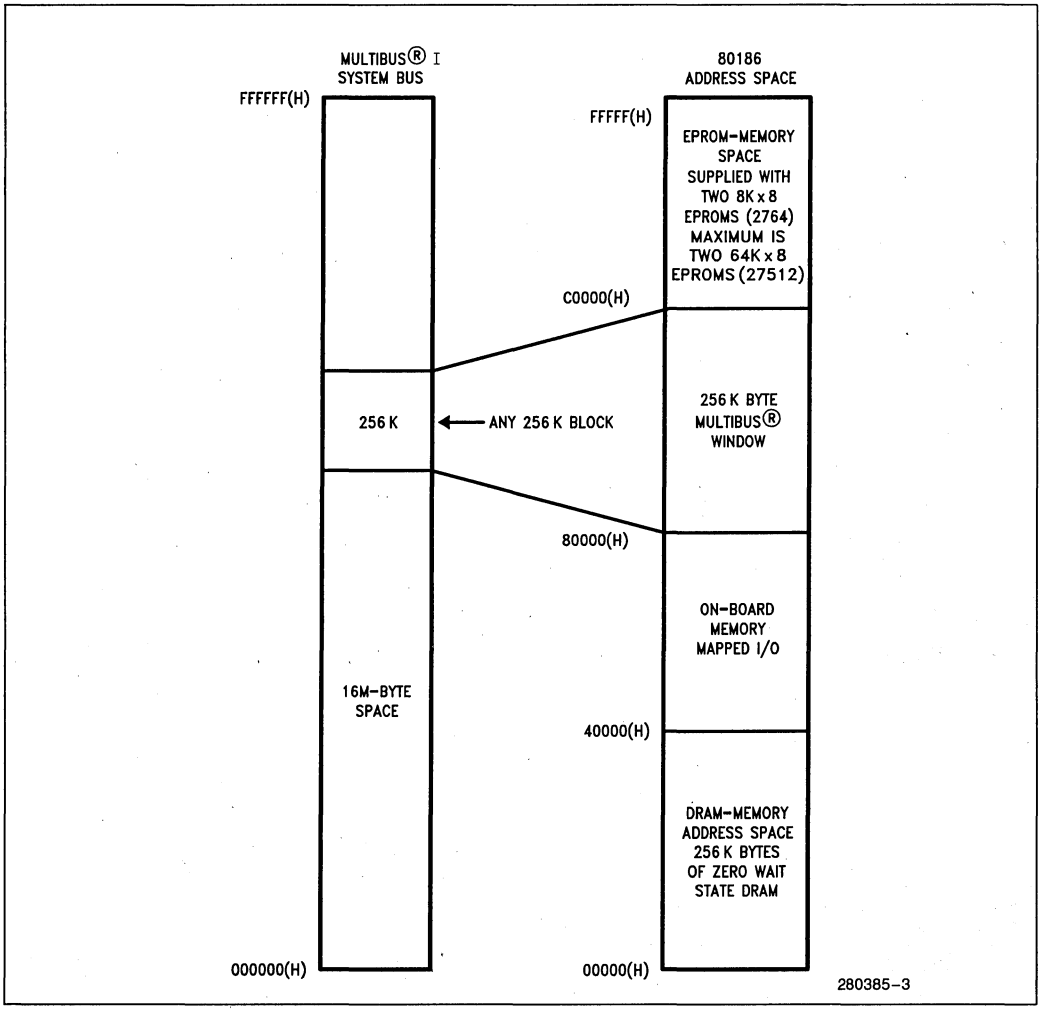


Figure 2. iSBC® iSXM™ 552A Memory Configuration

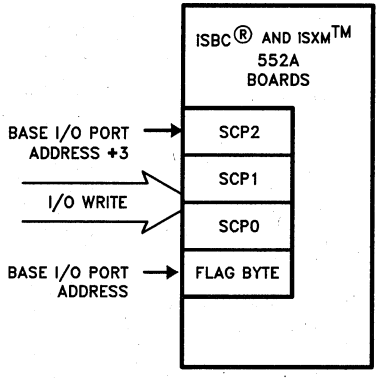
IEEE 802.3 Interface

The IEEE 802.3 Interface on the iSBC/iSXM 552A board is based on the 82586 LAN controller. Data is transferred between the on-board memory of the iSBC/iSXM 552A board and the 82586 controller by 82586 initiated DMA. The 82586 initiates the DMA cycles by activating the HOLD signal to the 80186 processor. The DMA cycle begins when the 80186 processor activates the HOLD ACKNOWLEDGE signal.

Each iSBC/iSXM 552A board is manufactured with a unique default 48-bit IEEE 802.3/Ethernet network address stored in an address PROM. This address PROM is protected by checksum and can be read by utilizing the on-board memory mapped I/O. The 82586 can be programmed to have this or any other Ethernet address.

MULTIBUS® I Interface

The iSBC/iSXM 552A board can access the MULTIBUS I with an 8- or 16- bit data path and can support up to 24-address bits. An I/O operation by the 80186 on the iSBC/iSXM 552A board normally accesses the I/O ports on the 80186 that controls the processor's interrupt controller and timers. MULTIBUS I/O is disabled in this normal operation. iSBC/iSXM 552A MULTIBUS I/O operations can be enabled or disabled by writing to memory mapped I/O control locations (Table 2). When the MULTIBUS I/O is enabled, the iSBC/iSXM 552A board can write or read the complete 64K Bytes of I/O space locations.



Base I/O port address = configurable. If 8-bit I/O is used, base port address is configurable from 0-OFCH. If 16-bit I/O is used, base port address is configurable from 0-OFFFCH.
Flag byte: see Table 1.
SCP0–SCP2: I/O written by host processor and read by 80186 on iSBC and iSXM 552A SCP0 can be jumper preset.

Figure 3. iSBC® 552A MULTIBUS® I Communication Interface

Table 1

Value Written to Flag Byte Port	Action
1	Resets iSBC 552A Board
2	Interrupts 80186 on Interrupt Level 1
4	Clears a MULTIBUS Interrupt Previously Generated by the iSBC 552A Board

A host processor in a system communicates with the iSBC/iSXM 552A board via a flag byte port and three other byte registers in the MULTIBUS interface. These registers are called the "System Configuration Pointer" registers (SCP0–SCP2). The flag byte port and the SCP registers are presented as 4 consecutive MULTIBUS I/O ports to the host processor. The locations of these I/O ports on the MULTIBUS are configurable on the iSBC 552A (Figure 3). To the 80186 processor on the iSBC/iSXM 552A board, the three SCP registers are memory mapped locations.

The flag byte port is used by the host processor to reset the iSBC/iSXM 552A board, to interrupt the 80186 processor, and to reset a MULTIBUS I interrupt generated by the iSBC/iSXM 552A board (Table 1). SCP0–SCP2 are general purpose registers that the host processor can I/O write to and the iSBC/iSXM 552A board can read from. SCP0 can also be preset by hardware jumpers.

iSBC® 552A FUNCTIONAL DESCRIPTION

The iSBC 552A board is a high performance general purpose IEEE 802.3 compatible COMMengine designed to offload a host processor in a system from transport layer and network layer communication processing. The board supports user written communications software for unique applications or it can run Intel's iNA 960/961 transport and network software in standard applications. When running iNA 960 software, the iSBC 552A board provides the host processor with reliable process to process message delivery. User messages to be sent are copied by iNA 960 software into iSBC 552A board local memory for transmission. Packets received from the network are first buffered and reassembled into messages on the iSBC 552A board. These received messages are then delivered to the user.

The iSBC 552A board makes use of the functions on the 82586 controller to implement a number of network functions. These functions include reprogramming the iSBC 552A station address, Multicast packet reception filtering, and loopback diagnostics. The 82586 also records a set of network statistics information. Information stored includes the number of CRC and alignment errors, the number of occurrences of no receive buffer resources and the number of DMA overruns/underruns.

The iSBC 552A can be configured to have a range of EPROM memory configurations up to 128K Bytes using 27512's.

The iSBC 552A board and iNA 960 software combination offers a flexible and configurable transport

COMMengine, and allows a user to optimally configure the system for highest performance. The iSXM 552A and iNA 961 combination offers a preconfigured turn-key solution. In both cases, iNA 960/961 software and the 552A significantly reduce the design cycle involved in designing and implementing a transport COMMengine.

For additional information about iNA 960/961, please refer to the iNA 960/961 data sheet.

iSBC® 552A User Interface

The iSBC 552A board communicates with a host processor through a handshake of interrupts. The host processor can generate flag byte interrupts to the 80186 on the iSBC 552A and the iSBC 552A can generate MULTIBUS I interrupts to the host processor. The host processor and the iSBC 552A board can also communicate through shared MULTIBUS I system memory. None of the on-board buffer on the iSBC 552A board is accessible to the host processor but the iSBC 552A can read and write all of the 16M Byte of MULTIBUS I system memory.

The host processor and the iSBC 552A board further communicate through the SCP registers. These byte registers can be I/O written by the host and can be read through memory mapped I/O by the iSBC 552A processor.

The 80186 processor controls the iSBC 552A through memory mapped I/O. Functions that are controlled are listed in Table 2.

OPERATING ENVIRONMENTS

The iSBC/iSXM 552A is designed to function in any MULTIBUS I system as a communications processor. It can function as both a MULTIBUS I bus master or a slave. As a MULTIBUS I master, it can access up to 16M Byte of host memory and 64K Byte of I/O address. As a MULTIBUS I slave, it occupies four consecutive I/O locations on the MULTIBUS I system memory. These locations are reserved for the flag byte and the three SCP registers.

iSXM™ 552A FUNCTIONAL DESCRIPTION

The iSXM 552A board is offered to operate specifically with the iNA 961 transport and network layer software. The iSXM 552A firmware provides the capabilities to load iNA 961 onto the 552A from either a buffer in the local host or remotely from another IEEE 802.3 network station. It also performs a variety of IEEE 802.3 and on-board diagnostics (see sections on iNA 961 User Interfaces and Operating Systems Environment).

iNA 961 software and the iSXM 552A board together provide the functionality of a preconfigured operating system independent transport engine. In addition to transport services, iNA 961 software also includes extensive data link, internetworking, and network management services. Figure 4 shows the distribution of network seven layer functions between iNA 961/iSXM 552A and the host processor. Table 3 shows some examples of functions provided by iNA 961. Refer to the iNA 960/961 data sheet for more iNA 961 information.

Table 2. iSBC® 552A Memory Mapped Functions

80186 Chip Select Lines	Read/Write by 80186	Functions
MCS	R	MULTIBUS I Interface registers (System Configuration Pointer Registers, see "MULTIBUS Interface" Section)
PCS	W	Channel Attention to 82586
	R	Reading iSBC 552A Ethernet Address PROMS
	W	Controlling Loopback of the Serial Interface
	W	Disabling and Enabling MULTIBUS I/O
	W	Generating and Clearing iSBC 552A Interrupts to the MULTIBUS System Bus
	W	Controlling the On-Board LED
	W	Latches the MULTIBUS Window Segment (8 most Significant Bits of 24-Bit Address)

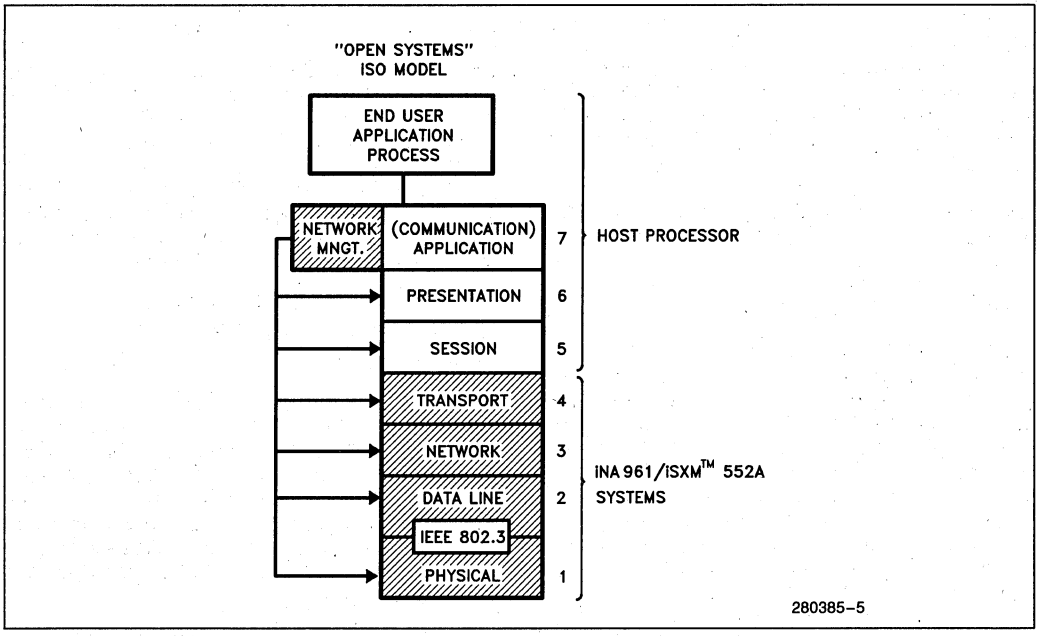


Figure 4. iNA 961 Configuration on iSXM™ 552A Board

Table 3. iNA 961 Services

Transport	Virtual Circuit Open: Establish a Virtual Circuit Database Send Connect: Actively Try to Establish a Virtual Connection Await Connect: Passively Awaits the Arrival of a Connection Request Send: Send a Message Receive: Post a Buffer to Receive a Message Close: Close a Virtual Circuit Datagram Send: Send a Datagram Message Receive: Post a Buffer to Receive a Datagram Message
Data Link	Transmit: Transmit a Data Link Packet Receive: Post a Buffer to Receive a Data Link Packet Connect: Make a Data Link Logical Connection (Link Service Access Point, IEEE802.3/802.2) Disconnect: Disconnect a Data Link Logical Connection Change Ethernet Address: Change the Ethernet Address Add Multicast Address: Add a Multicast Address Delete Multicast Address: Remove a Multicast Address Configure 82586: Configure the 82586 Controller
Network Management	Read/Clear/Set Network Objects (Local/Remote): Read/Clear/Set Local or Remote iNA 960 Network Parameters Read/Set Network Memory (Local/Remote) Read/Set Memory of the Local or a Remote Station Useful in Network Debug Process. Boot Consumer: Requests a Network Boot Server to Load a Boot File into this Station Echo: Echo a Packet between this Station and Another Remote Station on the Network

iSBC®/iSXM™ 552A Boot Firmware User Interface

The iSBC/iSXM 552A boot firmware is used to load iNA 961 or other software onto the 552A board from either local MULTIBUS I memory or a remote network station. The firmware performs a number of local and network diagnostics. Table 4 describes the functions of the boot firmware.

The iSBC/iSXM 552A boot firmware interfaces with the host processor through a configurable command buffer location in MULTIBUS I memory. This location can be either jumper or program configured. The host processor updates the command byte in the command buffer and expects the firmware to update the response byte when the command is done. The host processor signals to the firmware to examine this command buffer by writing a 2 to the flag byte port. The firmware will update the response byte when the command is completed.

The iSBC/iSXM 552A boot firmware commands fully support the initialization of the MIP interface. The MIP interface is used by the host processor to communicate with the iNA 961 once it is loaded and started. See section "iNA 961 User Interfaces" for details.

iNA 961 User Interfaces

User programs give iNA 960 commands to the iNA 961 software on the iSBC/iSXM 552A board via the MULTIBUS I Interface Protocol (MIP). MIP is an Intel reliable message delivery protocol between MULTIBUS I processors. Figure 5 illustrates how this message delivery functions. Commands are passed between the iSBC/iSXM 552A board and the host processor in the form of request blocks. A request block is a buffer that contains a command specification and the command parameters. Each request block (or equivalently, each command) is reliably delivered from the host processor to iNA 961 via the MIP facility. iNA 961 will extract the command information and carry out the command. After the command is done, iNA 961 will use the MIP facility to return the command result to the user program.

Table 4. iSXM™ 552A Boot Firmware Commands

Command	Function
Presence	This command will indicate that the boot firmware is functional by returning the version number of the firmware, the power on diagnostic result, and the default Ethernet address of the iSXM 552A board.
Load	Load a program from MULTIBUS memory into a designated location in the iSBC 552A memory.
Load and Go	Load a program from MULTIBUS bus memory into a designated location in the iSXM 552A memory. Proceed to start this program once it is loaded. This command also initializes the MIP interface on the iSXM 552A board.
Echo	Echo a packet between this iSXM 552A board and another station on the network.
Remote Boot	This command requests a remote boot server station to download software onto the iSXM 552A board.
MIP Initialize and Start	Used after a remote boot. This command initializes the MIP interface on the iSXM552A board and then start the software loaded by the remote boot command.

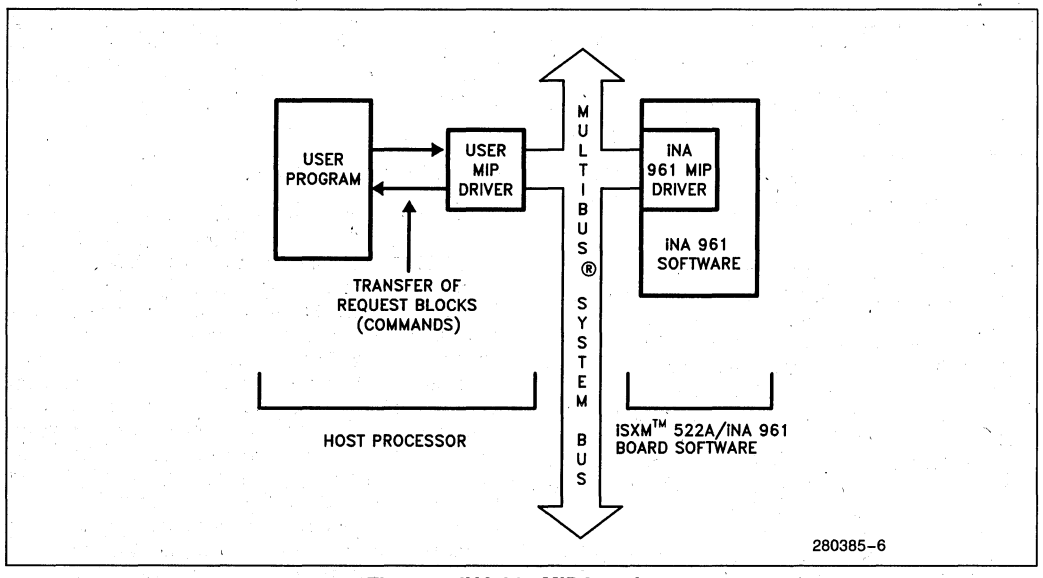


Figure 5. iNA 961 MIP Interface

iNA 961 request blocks are in the same formats as iNA 960 commands. Refer to the iNA 960/961 data sheet and reference manuals for more details on iNA 960/961 software.

Operating Systems Environment

The iSBC/iSXM 552A board and iNA 960/961 software can function in any MULTIBUS I environment. The communication between the iSBC/iSXM 552A and the host processor is entirely independent of any host operating systems. iNA 960/961 uses the MIP protocol to interface with the host processor. The MIP is a reliable, host operating system independent, process to process communication scheme between any processors on the MULTIBUS I System Bus. iNA 960/961 can service multiple processes utilizing its services at the same time.

A host processor passes iNA 960/961 commands and buffers in the MULTIBUS I system memory to the iNA 960/961 software. This software is responsible for updating the response fields of these commands. It is responsible for copying the user send buffer in MULTIBUS I system memory into its onboard buffers for transmission and for copying received messages to user buffers in MULTIBUS I system memory.

Diagnostics

The iSBC/iSXM 552A board offers a range of power up diagnostics designed to ensure that the 80186 processor, the memory, and the IEEE 802.3 interface are functioning properly. Table 5 describes these diagnostics.

Table 5. Functions Checked by iSXM™ 552A Diagnostics

1. Insufficient RAM
2. RAM March Pattern Test
3. Ram Ripple Data Test
4. Boot Firmware PROM Checksum
5. Address PROM Checksum
6. 80186 Interrupt Controller
7. 80186 Timer Controller
8. 82586 Initialization
9. 82586 CRC Check
10. 82586 Broadcast Packet Recognition
11. 82586 External Loopback
12. 82586 Individual Address Recognition
13. 82586 Multicast Address Recognition
14. 82586 Reset
15. 82586 Diagnose Check

DEVELOPMENT ENVIRONMENT

The iSXM 552A board is a complete system product that allows a user to emphasize the development of high level software, such as a network file server. The iSXM 552A board and the iNA 961 software together form a transport COMMengine that integrates into any MULTIBUS I system. iNA 961 is supplied in a boot loadable file format. This file can be loaded into the iSXM 552A by a host processor or through a remote boot server network node. The boot firmware on the iSXM 552A supports both functions. In order to remote boot the host system, appropriate host processor firmware and software is required.

The iSBC 552A allows a user to fine tune iNA 960 and to put the software on the board. Both iNA 960 and the iSBC 552A can be flexibly configured to best meet the users' requirements. An Intel development system, together with the Intel I2ICE™ system or equivalent product can be used if the user desires to do extensive development work on the iSBC 552A. Intel also supplies a wide range of host processor boards and systems (such as the iSBC 286/12 and system 310) that will function well both with the iSBC 552A or the iSXM 552A board.

SPECIFICATIONS

Data Transfer: 8 or 16 bits

Average Raw MULTIBUS I Transfer Rate:

8.7M bits/second (450 ns., 16-bit system memory and no MULTIBUS I contention)

Transceiver Interface

Transmit Data Rate: 10M bits/second

Signal Levels: Series 10,000 ECL-compatible

Host Interrupts: One MULTIBUS I non-vector interrupt for use in system/host handshaking

MULTIBUS Interface: The iSBC/iSXM 552A board conforms to all AC and DC requirements outlined in Intel MULTIBUS I Specification. Order Number 142686-022m except for the following signals:

Signal DAT0–DAT7

Signal Specification:
IIL = 180 μA IIH = 125 μA

DC Power Required: All voltages supplied by the MULTIBUS I interface

+5.0V ±5%, 6.2A maximum

+12.0V ±5%, 0.5A maximum

Environmental

Temperature: 0°C to +55°C Operating
−40°C to −65°C Non-Operating

Humidity: 5% to 90% Operating
5% to 95% Non-Operating

ORDERING INFORMATION

Part Number	Description
SBC552A	IEEE 802.3 COMMengine
SXM552A	IEEE 802.3 Transport Engine for iNA961 and SYP310 systems
iNA960	Configurable transport software usable with the SBC552A
iNA961	Preconfigured transport software for the SXM552A