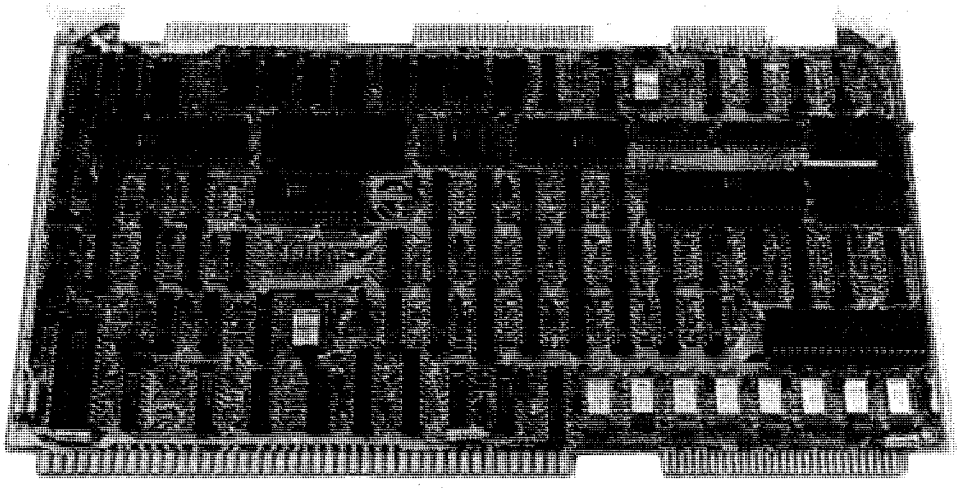
iSBC® 80/30
SINGLE BOARD COMPUTER

- 8085A CPU Used as Central Processing Unit
- 16K Bytes of Dual Port Dynamic Read/Write Memory with On-Board Refresh
- Sockets for up to 8K Bytes of Read Only Memory
- Sockets for 8041A/8741A Universal Peripheral Interface and Interchangeable Line Drivers and Line Terminators
- 24 Programmable Parallel I/O Lines with Sockets for Interchangeable Line Drivers and Terminators
- Full MULTIBUS® Control Logic Allowing up to 16 Masters to Share the System
- Programmable Synchronous/Asynchronous RS232C Compatible Serial Interface with Fully Software Selectable Baud Rate Generation
- 12 Levels of Programmable Interrupt Control
- Two Programmable 16-Bit BCD or Binary Counters
- Auxiliary Power Bus, Memory Protect, and Power-Fail Interrupt Control Logic for RAM Battery Backup
- Compatible with Optional iSBC® 80 CPU, Memory, and I/O Expansion Boards

The iSBC 80/30 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical self-contained computer-based solutions for OEM applications. The iSBC 80/30 is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, universal peripheral interface capability, I/O ports and drivers, serial communications interface, priority interrupt logic, programmable timers, MULTIBUS control logic, and bus expansion drivers all reside on the board.



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FUNCTIONAL DESCRIPTION

Central Processing Unit

Intel's powerful 8-bit n-channel 8085A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/30. The 8085A CPU is directly software compatible with the Intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. The minimum instruction execution time is 1.45 microseconds. The 8085A CPU has a 16-bit program counter. An external stack, located within any portion of iSBC 80/30 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this eternal stack. This stack provides subroutine nesting bounded only by memory size.

Bus Structure

The iSBC 80/30 has an internal bus for all on-board memory and I/O operations and a system bus (i.e., the MULTIBUS) for all external memory and I/O operations. Hence, local (on-board) operations do not tie up the system bus, and allow true parallel processing when several bus masters (i.e., DMA devices, other single board computers) are used in a multimaster scheme. A block diagram of the iSBC 80/30 functional components is shown in Figure 1.

RAM Capacity

The iSBC 80/30 contains 16K bytes of dynamic read/write memory using Intel 2117 RAMs. All RAM read and write operations are performed at maximum processor speed. Power for the on-board RAM may be provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. The iSBC 80/30 contains a dual port controller, which provides dual port capability for the on-board RAM memory. RAM accesses may occur from either the iSBC 80/30 or from any other bus master interfaced via the MULTIBUS. Since on-board RAM accesses do not require the MULTIBUS, the bus is available for any other concurrent operations (e.g., DMA data transfers) requiring the use of the MULTIBUS. Dynamic RAM refresh is accomplished automatically by the iSBC 80/30 for accesses originating from either the CPU or via the MULTIBUS. Memory space assignment can be selected independently for on-board and MULTIBUS RAM accesses. The on-board RAM, as seen by the 8085A CPU, may be placed anywhere within the 0- to 64K-address space. The iSBC 80/30 provides extended addressing jumpers to allow the on-board RAM to reside within a one megabyte address space when accessed via the MULTIBUS. In addition, jumper options are provided which allow the user to reserve 8K- and 16K-byte segments of on-board RAM for use by the 8085A CPU only. This reserved RAM space is not accessible via the MULTIBUS and does not occupy any system address space.

EPROM/ROM Capacity

Sockets for up to 8K bytes of nonvolatile read only memory and provided on the iSBC 80/30 board. Read only memory may be added in 1 K-byte increments up to a maximum of 2 K-bytes using Intel 2708 or 2758 erasable and electrically reprogrammable ROMs (EPROMs); in 2 K-byte increments up to a maximum of 4 K-bytes using Intel 2716 EPROMs; or in 4 K-byte increments up to 8K-bytes maximum using Intel 2732 EPROMs. All on-board EPROM/ROM operations are performed at maximum processor speed.

Parallel I/O Interface

The iSBC 80/30 contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripharal Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable.

Universal Peripheral Interface (UPI)

The iSBC 80/30 provides sockets for a user supplied Intel 8041A/8741A Universal Peripheral Interface (UPI) chip and the associated line drivers and terminators for the UPI's I/O ports. The 8041A/8741A is a single chip microcomputer containing a CPU, 1K bytes of ROM (8041A) or EPROM (8741A), 64 bytes of RAM, 18 programmable I/O lines, and an 8-bit timer. Special interface registers included in the chip allow the 8041A to function as a

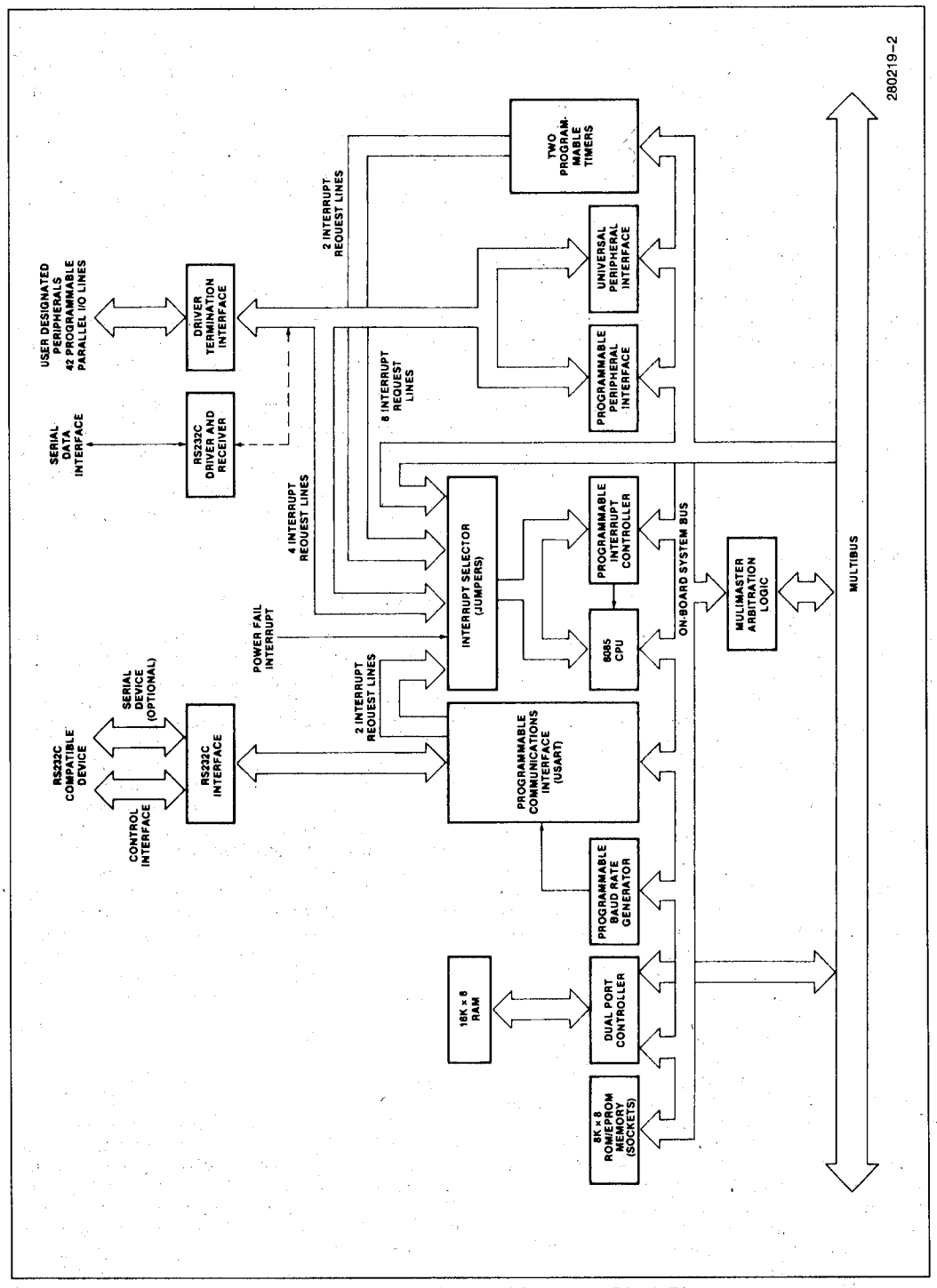


Figure 1. iSBC® 80/30 Single Board Computer Block Diagram

slave processor to the iSBC 80/30's 8085A CPU. The UPI allows the user to specifiy algorithms for controlling user peripherals directly in the chip, thereby relieving the 8085A for other system functions. The iSBC 80/30 provides an RS232C driver and an RS232C receiver for optional connection to the 8041A/8741A in applications where the UPI is programmed to handle simple serial interfaces. For additional information, including 8041A/8741A instructions, refer to the UPI-41A User's Manual and application note AP-41.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 80/30. A software selectable baud rate generator provides the USART with all common communication frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM By-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable.

Multimaster Capability

The iSBC 80/30 is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the iSBC 80/30 provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 80/30's or other bus masters to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters to share the MULTIBUS with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the iSBC 80/30 or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and transfer via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct memory access (DMA) operations, and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

The iSBC 80/30 provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable Interval Timer. Each counter is capabile of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Program-

Port	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

mable Interrupt Controller, to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, and to the 8041A/8741A Universal Programmable Interface, or may be routed as inputs to the 8255A and 8041A/8741A chips. The gate/trigger inputs may be routed to I/O terminators associated with the 8255A or as output connections from the 8255A. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 80/30 RS232C USART serial port. In utilizing the iSBC 80/30, the systems designer simply configures, via software, each timer independently to meet system requirements.

Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be read "on the fly".

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Interrupt Capability

The iSBC 80/30 provides vectoring for 12 interrupt levels. Four of these levels are handled directly by the interrupt processing capability of the 8085A CPU and represent the four highest priority interrupts of the iSBC 80/30. Requests are routed to the 8085A interrupt inputs, TRAP, RST 7.5, RST 6.5, and RST 5.5 (in decreasing order of priority) and each input generates a unique memory address (TRAP: 24H; RST 7.5: 3CH; RST 6.5: 34H; and RST 5.5: 2CH). An 8085A jump instruction at each of these addresses then provides linkage to interrupt service routines located independently anywhere in memory. All interrupt inputs with the exception of the trap interrupt may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085A CPU. The Intel 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer for use in designing request processing configurations to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8085A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt Request Generation—Interrupt requests may originate from 18 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when

a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers and by the universal peripheral interface, eight additional interrupt request lines are available to the user for direct interface to user designated peripheral devices via the system bus, and two interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific Priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 Power Supply or equivalent.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added by using Intel MULTIBUS compatible expansion boards. High speed integer and floating point arithmetic capabilities may be added by using the iSBC 310A High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as sub-systems. Modular expandable backplanes and cardcages are available to support multi-board systems.

SPECIFICATIONS

Word Size

Instruction: 8, 16, or 24 bits
Data: 8 bits

Cycle Time

Basic Instruction Cycle: 1.45 μs

NOTE:
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM: 0-07FF (using 2708 or 2758 EPROMs); 0-0FFF (using 2716 EPROMs); 0-1FFF (using 2716 EPROMs; 0-1FFF (using 2732 EPROMs).

On-Board RAM: 16K bytes of dual port RAM starting on a 16K boundary. One or two 8 K-byte segments may be reserved for CPU use only.

Memory Capacity

On-Board Read Only Memory: 8K bytes (sockets only)
On-Board RAM: 16K bytes
Off-Board Expansion: Up to 65,536 bytes in user specified combinations of RAM, ROM, and EPROM

NOTE:
Read only memory may be added in 1K, 2K, or 4K byte increments.

I/O Addressing

On-Board Programmable: I/O (see Table 1)

Port	8255A				8041A/8741A		USART	
	1	2	3	Control	Data	Control	Data	Control
Address	E8	E9	EA	EB	E4 or E6	E5 or E7	EC	ED

I/O Capacity

Parallel: 42 programmable lines using one 8255A (24 I/O lines) and an optional 8041A/8741A (18 I/O lines)

Serial: 2 programmable lines using one 8251A and an optional 8041A/8741A programmed for serial operation

NOTE:
For additional information on the 8041A/8741A refer to the UPI-41 User's Manual (Publication 9800504).

Serial Communications Characteristics

Synchronous: 5–8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous: 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Interrupts

Addresses for 8259A Registers (Hex notation, I/O address space)

DA Interrupt request register

DA In-service register

DB Mask register

DA Command register

DB Block address register

DA Status (polling register)

NOTE:
Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Interrupt Levels routed to 8085A CPU automatically vector the processor to unique memory locations:

Interrupt Input	Memory Address	Priority	Type
TRAP	24	Highest	Non-maskable
RST 7.5	3C	↑	Maskable
RST 6.5	34	↓	Maskable
RST 5.5	2C	Lowest	Maskable

Timers

Register Addresses (Hex notation, I/O address space)

DF Control register

DC Timer 0

DD Timer 1

DE Timer 2

NOTE:
Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference: 2.46 MHz ±0.1% (0.041 μs period, nominal); 1.23 MHz ±0.1% (0.81 μs period, nominal); or 153.60 kHz ±0.1% (6.51 μs period nominal).

NOTE:
Above frequencies are user selectable

Event Rate: 2.46 MHz max

NOTE:
Maximum rate for external events in event counter function.

Interfaces

MULTIBUS: All signals TTL compatible

Parallel I/O: All signals TTL compatible

Interrupt Requests: All TTL compatible

Timer: All signals TTL compatible

Serial I/O: RS232C compatible, data set configuration

System Clock (8085A CPU)

2.76 MHz ±0.1%

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 2KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000
Serial I/O	26	0.1	3M 3462-000

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Line Drivers and Terminators

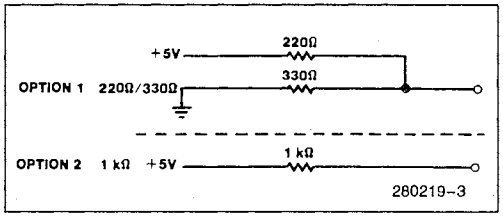
I/O Drivers: The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/30.

Driver	Characteristics	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

NOTE:
I = inverting; NI = non-inverting; OC = open collector

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 kΩ terminators.

I/O Terminators: 220Ω/330Ω divider or 1 kΩ pullup



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Address	Tri-State	50
Commands	Tri-State	32

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 18 oz. (509.6 gm)

Output Frequencies/Timing Intervals

Function	Single Timer/ Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.63 μs	427.1 ms	3.26 μs	466.50 min
Programmable One-Shot	1.63 μs	427.1 ms	3.26 μs	466.50 min
Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-Wave Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software Triggered Strobe	1.63 μs	427.1 ms	3.26 μs	466.50 min
Hardware Triggered Strobe	1.63 μs	427.1 ms	3.26 μs	466.50 min

Electrical Characteristics

DC POWER REQUIREMENTS

Configuration	Current Requirements			
	V_{CC} = +5V ±5% (max)	V_{DD} = +12V ±5% (max)	V_{BB} = −5V ±5% (max)	V_{AA} = −12V ±5% (max)
Without EPROM(1)	I_{CC} = 3.5A	I_{DD} = 220 mA	I_{BB} = —	I_{AA} = 50 mA
With 8041/8741(2)	3.6A	220 mA	—	50 mA
RAM only(3)	350 mA	20 mA	2.5 mA	—
With iSBC 530(4)	3.5A	320 mA	—	150 mA
With 2K EPROM(5) (using 8708)	4.4A	350 mA	95 mA	40 mA
With 2K EPROM(5) (using 2758)	4.6A	220 mA	—	50 mA
With 4K EPROM(5) (using 2716)	4.6A	220 mA	—	50 mA
With 8K EPROM(5) (using 2332)	4.6A	220 mA	—	50 mA

NOTES:
1. Does not include power required for optional EPROM/ROM, 8041A/8741A I/O drivers, and I/O terminators.
2. Does not include power required for optional EPROM/ROM. I/O drivers and I/O terminators.
3. RAM chips powered via auxiliary power bus.
4. Does not include power required for optional EPROM/ROM, 8041A/8741A I/O drivers, and I/O terminators. Power for iSBC 530 is supplied through the serial port connector.
5. Includes power reqiured for two EPROM/ROM chips, 8041A/8741A and 220Ω/330Ω input terminators installed for 34 I/O lines; all terminator inputs low.

Environmental Characteristics

Operating Temperature: 0°C to 55°C

Reference Manual

9800611B— iSBC 80/30 Single Board Computer Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED. Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/30	Single Board Computer with 16K bytes RAM