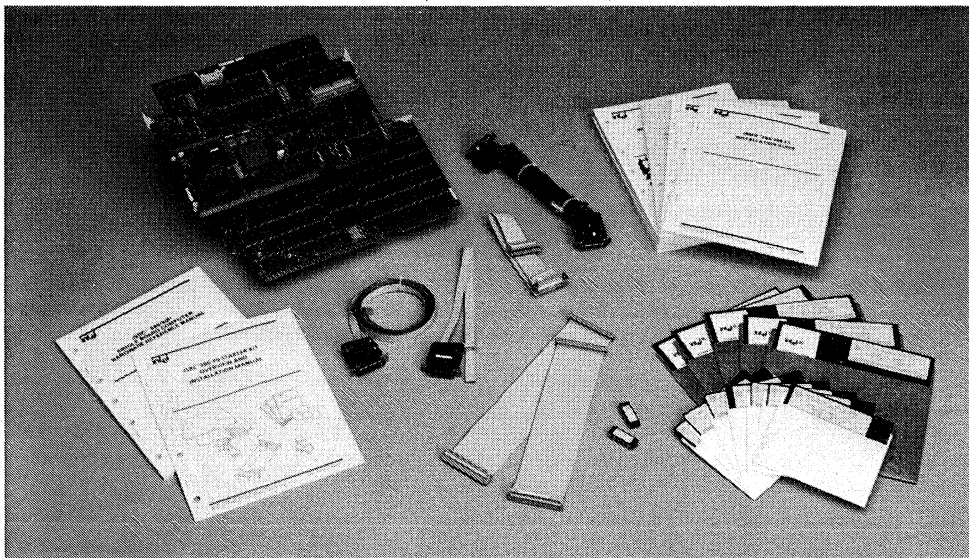


iSBC® 386/20 SINGLE BOARD COMPUTER STARTER KITS

- Starter Kit Includes iSBC® 386/20P CPU Board, 2 or 4MB Memory Board, and P-MON386ES Monitor or iRMX® 286/386 ES Software
- High Performance 32-bit Processor System Using the 80386 Microprocessor
- High Speed Numerics Coprocessor
- Cache Memory Provides 0 Wait-state Memory Reads
- High Speed 32-bit Memory Interface
- iSBX™ Interface Supports I/O Expansion Using iSBX MULTIMODULE™ Boards
- Up to 128KB of EPROM Local Memory
- MULTIBUS® Interface for Multimaster Configurations and System Expansion

The Starter Kits include an iSBC 386/20P CPU board, a 2 or 4 megabyte memory board, the choice of the P-MON386ES monitor or the iRMX 286/386 ES operating system/monitor software, interconnecting cables, and documentation. This kit allows the board or system level designer to quickly assemble an 80386-based MULTIBUS I System and evaluate the iSBC 386/20P board and 80386 microprocessor and begin system design and software development. All of the hardware pieces are provided, preconfigured to speed start-up time.

The iSBC 386/20P Single Board Computer, included in the kit, is Intel's highest performance MULTIBUS I CPU board. The iSBC 386/20P board features an 80386 32-bit microprocessor, a 16 kilobyte cache memory, and a high speed, dual-port memory interface that supports up to 16 megabytes of physical memory. The board also features a math coprocessor to offload the CPU and greatly enhance system performance in floating point, math-intensive applications. To take advantage of the 80386 32-bit architecture, all data transfers between the microprocessor and the dual-port memory are 32 bits wide.



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FUNCTIONAL DESCRIPTION

Overview—iSBC® 386/20 Starter Kit

The iSBC 386/20 Starter Kits are a set of hardware and software products designed to allow the user to easily evaluate the iSBC 386/20P CPU board and 80386 microprocessor, and to begin system design and software development. The kits include an iSBC 386/20P CPU board, either an iSBC 402P 2-megabyte or iSBC 404P 4-megabyte memory board, the choice of P-MON386ES debug monitor or iRMX 286/386 ES software, interconnecting cables and user documentation. Each of these kits is described below.

iRMX® 286/386 ES-Based iSBC® 386/20P Starter Kit

The iRMX Starter Kit is designed to support 16-bit iRMX-based applications and enables a new or an existing iRMX 286 Release 1 application to run on the iSBC 386/20P board. The starter kit also includes a 16-bit debug monitor that supports 16-bit application software development either in an on-target development environment using an Intel 286/310 system or in a host-target development environment using a Series III/IV system. These two development environments are shown in Figure 1.

The starter kit contains diskettes, two 27256 EPROMs, serial cables for connection to the host Series III/IV development system or separate console terminal, and installation/operating instructions.

The diskettes provide Update 3 of the iRMX 286 Release 1 Operating System, modified iRMX 286 software ported to run on the iSBC 386/20P board, and 16-bit 80286/80386 ES monitor software. Both 8" ISIS format and 5-1/4" iRMX format diskette media are provided. The EPROMs, which the user installs on the iSBC 386/20P board, contain the bootloader, device initialization code, and the debug monitor. The user must separately provide and license the iRMX 286 Release 1 operating system software. The iRMX 286/310 system or Intellec® Series III/IV development system are also user provided.

The 80286/80386 monitor allows the designer to debug both real mode and protected mode applications that run on the iSBC 386/20P board.

The monitor provides commands that perform the following functions:

- Bootstrap load the program of your choice
- Examine and modify the contents of the 80386 registers and board memory
- Display the contents of memory and descriptor tables
- Load and execute relocatable and absolute object files
- Move blocks of memory from one location to another
- Perform I/O to a specified port
- Disassemble and execute instructions
- Single-step execution of instructions
- Define and examine symbols in a program

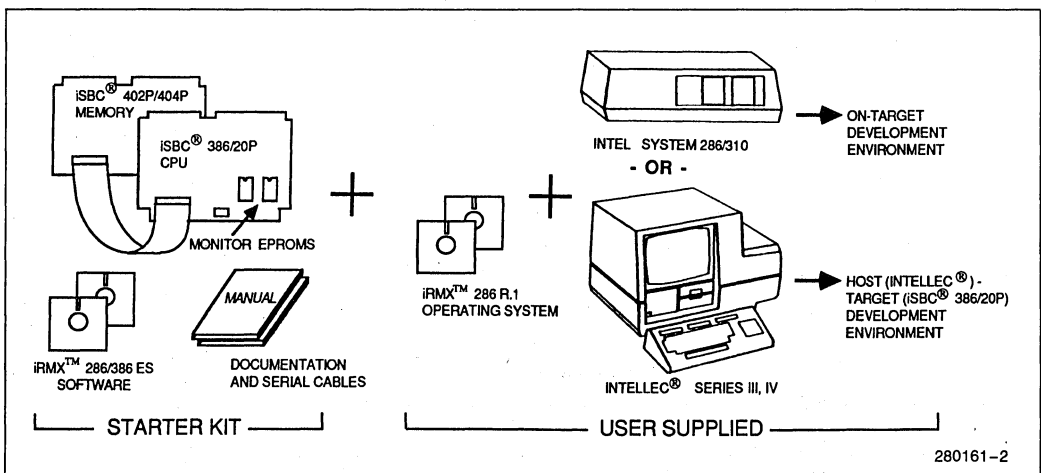


Figure 1. iRMX® Starter Kit Development Environments

Using the starter kit, designers can generate and debug 16-bit application software either on the host Intellec system or on the ISBC 386/20P-based system. The iRMX 286 Operating System together with the 80286/80386 ES monitor support the use of iRMX 286 16-bit languages and tools including ASM 86, ASM 286, PL/M 286, BIND 286, BUILD 286, and AEDIT text editor. Thirty-two-bit languages are not supported.

The starter kit also allows designers to download all or part of an existing iRMX 286-based application to the ISBC 386/20P board for execution. In some cases, software timing loops may need to be readjusted to compensate for the increased clock rate of the 80386 microprocessor. Furthermore, I/O address references may also need changing to match the I/O map of the ISBC 386/20P board.

iRMX 86-based 8086 applications will also run on the ISBC 386/20P board. The code is first recompiled to run under iRMX 286 operating system using 286 compilers. The code is then downloaded to the ISBC 386/20P board using the iRMX 286/386 ES software. As with other code, the iRMX 86 application code may have to be modified to adjust software timing loops and I/O address references.

Configuring the On-Target Development Environment

If the designer chooses to configure an on-target development environment using an Intel 286/310 system, either a standard SYS 310-40(A), -41(A), or -17(A) system may be used.

In addition to the iSBC 386/20P board and memory, other boards that the iRMX 286/386 ES software supports may be installed in the system. These boards include the iSBC 214/215G/217/218A series of disk controller boards, the iSBC 188/48 and iSBC 544A 8- and 4-channel communications boards, the iSBC 350 line printer board, the iSBX 351 2-channel communications MULTIMODULE™ and a RAM (disk) driver.

P-MON386-based iSBC® 386/20 Starter Kit

The P-MON-based starter kit uses the XENIX hosted P-MON386ES debug monitor and is intended for non-iRMX-based and component-based applications. The monitor, when used with an existing XENIX 286/310 system as shown in Figure 2, enables the designer to develop software on the host system, then download the code to the target ISBC 386/20P board for execution. Code from an existing 16-bit application may also be downloaded to the ISBC 386/20P board from the host system. Using the P-MON386ES monitor, designers can access and control all of the 80386 visible user-hardware resources without any assistance from an operating system.

The starter kit includes 5-1/4" diskettes that contain the host portion of the monitor software, two 27512 EPROMS, two cables for connection to either a DCE or DTE RS232C interface at the host system and installation/operation instructions. The EPROMS, which the user installs on the ISBC 386/20P board, contain the bootloader, device initialization code, and the target resident portion of the monitor soft-

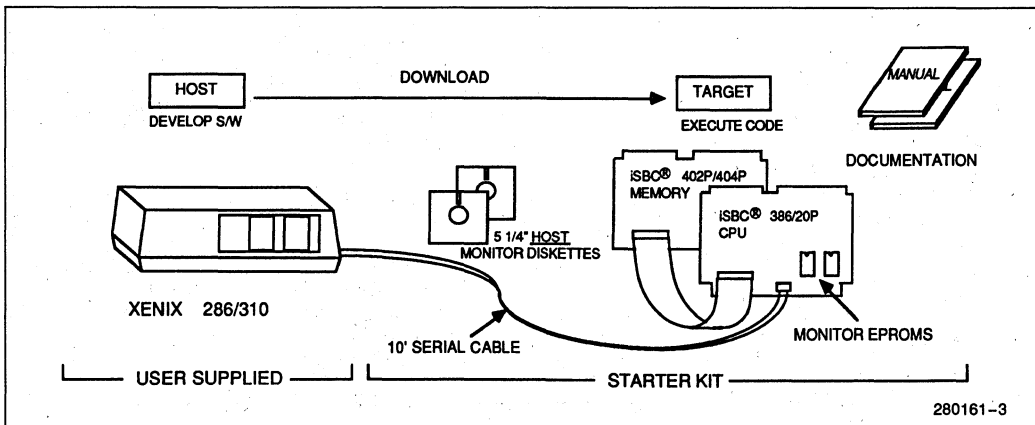


Figure 2. P-MON386ES Host-Target Development Environment

ware. The XENIX* 286/310 system is not part of the kit and may be ordered separately from Intel.

The P-MON386ES monitor provides the following user assistance programming tools and system debug capabilities:

- Download Intel 8086, 80286, and 80386 object module formats (with no symbolics)
- Examine/modify memory, I/O ports, processor registers, descriptor tables, and the task state segment
- Convert addresses from virtual to linear, linear to physical, and virtual to physical
- Evaluate expressions
- Control execution both in real and protected mode
- Set software breakpoints on execution addresses
- Set hardware breakpoints on execution and data addresses
- Disassemble memory

Both 16-bit and 32-bit XENIX hosted languages and tools are supported, including COBOL, FORTRAN,

*Xenix is a trademark of Microsoft Corporation

BASIC, 80386 Assembler, C386 Compiler, PL/M 386 Compiler, and 80386 Relocation/Linkage/Library tools.

The monitor software also allows the designer to download all or part of an existing 8086 or 80286-based 16-bit application to the iSBC 386/20P board for execution. The P-MON386ES-based starter kit does not provide operating system (O.S.) support. If the application software uses an O.S. interface, the O.S. must be ported to run with the 80386 microprocessor, the 8251A Serial Controller, and the 80287 math coprocessor (if used).

Overview—iSBC® 386/20P CPU Board

The iSBC 386/20P board is Intel's first 32-bit MULTIBUS I single board computer using the 80386 microprocessor. The board employs a dual-bus structure: a 32-bit CPU bus for data transfers between the CPU and memory; and a 16-bit bus for data transfers over the MULTIBUS, iSBX, local memory, and 8-bit I/O interfaces. In this manner, the board takes advantage of the 80386 CPU's 32-bit wide data bus while maintaining full compatibility with the MULTIBUS interface and iSBX MULTIMODULE boards. A block diagram of the board is shown in Figure 3.

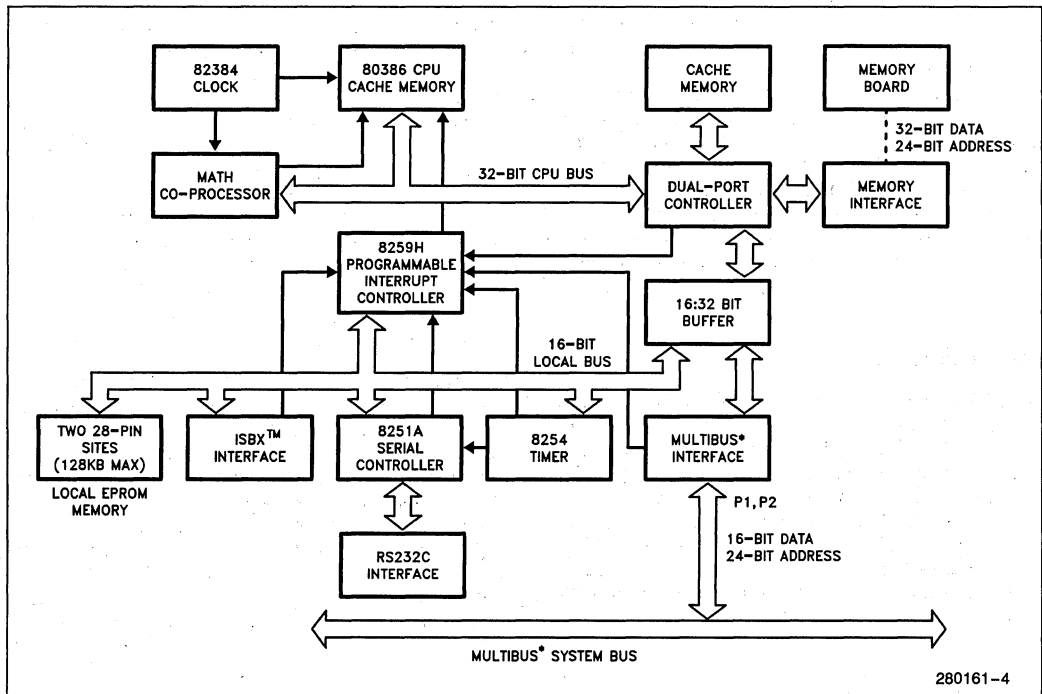


Figure 3. iSBC® 386/20P CPU Board Block Diagram

The iSBC 386/20P board can be used in many applications originally designed for Intel's 16-bit microcomputers, such as the iSBC 286/10A and iSBC 286/12, 8 MHz, 80286-based, single board computers. In this way, performance can be easily upgraded without requiring major hardware or software changes.

The iSBC 386/20P CPU board, which is in the starter kit, is an early release version of the iSBC 386/20 production board.

Central Processor Unit

The heart of the iSBC 386/20P board is an 80386 microprocessor. This device utilizes address pipelining, a high speed execution unit, and on-chip memory management/protection to provide the highest level of system performance. The 80386 microprocessor also features an Address Translation Unit that supports up to 64 terabytes of virtual memory.

The 80386 CPU is upwardly compatible with Intel's 8088, 8086, 80186, and 80286 CPUs. Application software written for these other 8 and 16 bit microprocessor families can be easily recompiled to run on the 80386 microprocessor.

The 80386 microprocessor resides on the 32-bit wide CPU bus which interconnects the CPU with the math coprocessor and dual-port memory. This arrangement tightly couples the CPU to the memory to form a high performance processor/memory 'engine'. A separate 16-bit bus couples the CPU and dual-port memory to the MULTIBUS and iSBX interfaces, local EPROM memory, and other on-board I/O resources. With this arrangement, the iSBC 386/20P board can take full advantage of the 80386 microprocessor's 32-bit architecture while maintaining full compatibility with the MULTIBUS and iSBX interfaces.

Instruction Set

The 80386 instruction set includes variable length instruction format (including double operand instructions), 8-, 16-, and 32-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions. All existing instructions have been extended to support 32-bit addresses and operands. New bit manipulation and other instructions have been added for extra flexibility in designing complex software.

Numeric Data Processor

For enhanced numerics processing compatibility, the iSBC 386/20 Starter Kit includes an 80287-based math module which is installed on the iSBC 386/20P board. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The numeric data processor meets the IEEE P754 (Draft 7) standard for numeric data processing and maintains compatibility with 8087-based systems. Data transfers to/from the on-board CPU bus are 16-bits wide. On future iSBC 386/20 boards, this module will be replaced by an 80387 numeric coprocessor. This device will provide higher performance through a 32-bit data path to the CPU bus, added numeric instructions, and a faster clock.

Architectural Features

The 8086, 8088, 80186, 80188, 80286, and 80386 microprocessor family contains the same basic sets of registers, instructions, and addressing modes. The 80386 processor is upward compatible with the 8086, 8088, 80186, 80188, and 80286 CPUs.

The 80386 operates in two modes: protected virtual address mode, and 8086 real address mode. In protected virtual address mode (also called protected mode), programs use virtual addresses. In this mode, the 80386 CPU automatically translates logical addresses to physical addresses. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. In 8086 real address mode, programs use real address with up to one megabyte of address space. Both modes provide the same base instruction set, registers, and addressing mode.

Interrupt Control

Incoming interrupts are handled by two cascaded on-board 8259A programmable interrupt controllers and by the 80386's NMI line. Twenty potential interrupt sources are routed to the programmable controllers and the interrupt jumper matrix. Using this jumper matrix, the user can connect the desired interrupt sources to specific interrupt levels. Interrupts originating from up to 15 sources are then prioritized and sent to the CPU. A sixteenth interrupt source may be connected to the 80386 NMI line. Table 1 includes a list of devices and functions supported by interrupts.

Table 1. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface	Requests from MULTIBUS resident peripherals or other CPU boards	8
8251A Serial Controller	Indicates status of transmit and receive buffers and Ring Indicator lead of the RS232C interface	3
8254 Timers	Timer 0, 1 outputs; function determined by timer mode (hardwired to interrupt controller)	2
iSBX Connector	Function determined by iSBX MULTIMODULE board	4
Bus Timeout	Indicates addressed MULTIBUS or iSBX resident device has not responded to command within 10 msec	1
Power Fail Interrupt	Indicates AC power is not within tolerance. Signal generated by system power supply	1
Parity Interrupt	Indicates on-board parity error	1

Memory Capabilities

The iSBC 386/20P board supports both EPROM local memory located on board and DRAM dual-port memory which connects to the iSBC 386/20P board. The dual-port memory is supported by a high speed on-board cache memory.

The cache memory supports 4K entries, with each entry comprised of a 32-bit data field and an 8-bit tag field. The tag field is used to determine which actual memory word currently resides in a cache entry. The cache memory size and effective replacement algorithm are designed to optimize both the probability of cache 'hits' and local bus utilization.

DUAL-PORT MEMORY INTERFACE

The iSBC 386/20P preproduction board supports a high-speed, 32-bit memory interface that connects to the iSBC 402P 2 megabyte or iSBC 404P 4 megabyte memory expansion board using a pair of ribbon cables supplied in the kit. The iSBC 402P/404P board is a standard MULTIBUS I form-factor board. Production iSBC 385/20 CPU boards will use low-profile memory modules that plug directly onto the iSBC 386/20 board. The modules use surface mount technology devices and will be available in 1, 2, 4, and 8 megabyte sizes. Two modules may be used together to provide up to 16MB of system memory. Both the board and modules support byte-parity error detection and have 32-bit wide data paths to the 80386 CPU and 16-bit wide data path, to the MULTIBUS interface.

LOCAL MEMORY

The local memory consists of two 28-pin JEDEC sites that support EPROM devices, and are intended for boot-up and system diagnostic/monitor routines. Maximum local memory capacity is 128KB using high capacity Intel 27512 EPROM devices. The iSBC 386/20P board provided in the starter kit includes two EPROM devices which are programmed with monitor software.

The local memory resides at the upper end of the 80386 device's memory space for both real and protected mode operation. Local memory access time is selectable at from three to six wait-state and is a function of the speed of the device used.

CACHE MEMORY

A 16KB cache memory on the iSBC 386/20P board by the 80386 provides 0 wait-state reads by the 80386 for data and program code resident in the cache memory. The cache memory is updated whenever data is written into the dual-port memory or when the CPU executes a read cycle and the data or program code is not already present in cache memory. This process is controlled by the cache replacement algorithm.

Programmable Timer

Three 16-bit, programmable interval timer/counters are provided using an 8254 device, with one timer dedicated to the serial port for use as a baud rate generator. The other two timers can be used to generate accurate time intervals under software control or to count external events and raise an interrupt to the CPU when a certain count is reached. The timers are not cascadable. Seven timer/counter modes are available as listed in Table 2. Each counter is capable of operating in either BCD or binary modes. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter 'window' has been enabled or an interrupt may be generated after N events occur in the system.

Serial I/O

The iSBC 386/20P board includes one RS232C serial channel, which is configured as an asynchronous, DTE interface. Data rates up to 19.2 kilobaud may be selected. The serial channel can connect either to a host system for software development or to a standalone terminal for field diagnostic support. For standalone use, unhosted monitor software needs to be programmed by the user into the local EPROM memory. The physical interface is a 10-pin ribbon-style connector located on the front edge of the board. Included in the starter kit are mating serial cables to connect to a terminal or host system.

iSBX™ Interface

For iSBX MULTIMODULE support, the iSBC 386/20P CPU board provides a 16-bit iSBX connector which may be configured for use with either 8- or 16-bit, single or double-wide iSBX MULTIMODULE boards. Using the iSBX interface, a wide variety of specialized I/O functions can be easily and inexpensively added to the iSBC 386/20P board.

Reset Functions

The iSBC 386/20P board is designed to accept an AUX (auxiliary) reset signal via the board's P2 interface. In this way, system designs which require front panel reset switches are supported. The iSBC 386/20P board uses the AUX reset signal to reset all on-board logic (excluding DRAM refresh circuitry). The iSBC 386/230P board will also respond to an INIT Reset Signal generated by another board in the system.

LED Status Indicators

Mounted on the top edge of the iSBC 386/20P board are four LED indicators that indicate the operating status of the board and system. One indicator is used to show that an on-board parity error or a MULTIBUS bus parity error has occurred. A second LED indicates that a MULTIBUS or iSBX bus access timeout has occurred. The third LED is triggered by the start of an 80386 bus cycle and will go off if the 80386 CPU stops executing bus cycles. The fourth LED can be set under program control to illuminate by writing to a specific I/O location.

MULTIBUS® SYSTEM ARCHITECTURE

Overview

The MULTIBUS system architecture includes three bus structures: the system bus, the local bus extension and the iSBX MULTIMODULE expansion bus. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The MULTIBUS System architecture also includes the iLBX™ memory interface which is not supported by the iSBC 386/20P board.

System Bus—IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations using multiple processors, I/O boards, and peripheral boards. The MULTIBUS system bus is supported with a broad array of board level products, VLSI interface components, detailed published specifications and application notes.

System Bus—Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatibility expansion boards. Memory may be expanded by adding user specified combinations of EPROM boards, DRAM boards, or bubble memory boards. Input/Output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

System Bus—Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the iSBC 386/20P board provides full system bus arbitration control logic. This control logic allows up to four bus masters to share the system bus using a serial (daisy chain) priority scheme. By using an external parallel priority decoder, this may be extended to 16 bus masters. In addition to multiprocessing, the multimaster capability also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

iSBX™ Bus MULTIMODULE® On-Board Expansion

One 8-, 16-bit iSBX MULTIMODULE connector is provided on the iSBC 386/20P microcomputer board. Through this connector, additional on-board I/O functions may be added. The iSBX MULTIMOD-

ULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., floppy disks), BITBUS™ Control, and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX interface connector on the iSBC 386/20P board provides all the signals necessary to interface to the local on-board bus, including 16 data lines. The iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 386/20P microcomputer board. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX modules may also be designed. An iSBX bus interface specification is available from Intel.

SOFTWARE SUPPORT

Operating Systems

The iRMX 286/386 ES software (available in the iRMX-based starter kit), together with the iRMX 286 Release 1 Operating System, currently provides operating system support for the iSBC 386/20P board.

The production iSBC 386/20 board will be supported both by the iRMX 286 Release 2 operating system and the System V/386™ UNIX*-based operating system.

The iRMX 286 Release 2 operating system is a real-time multi-tasking and multi-programming software system capable of executing all the configurable layers of the iRMX 286 operating system on the 80386 microprocessor and the iSBC 386/20 single board computer. The operating system is designed to support time-critical applications such as factory automation, industrial control, and communications networks.

For multiple user, interactive systems, Intel will offer the System V/386 operating system, which is designed to support a broad range of applications in business, science, and engineering. Typical applications include distributed data processing, business data and word processing, software development, scientific and engineering applications, and graphics.

*UNIX is a trademark of Bell Labs

LANGUAGES AND TOOLS

Intel will be offering several languages supported by the iRMX and System V/386 operating systems. For the iRMX 286/386 Software System and the iRMX 286 Release 2 operating system, this includes ASM 286, Pascal 286, PL/M 286, C 286, and FORTRAN 286. For the System V/386 Operating System, languages will include ASM 386, C 386, PL/M 386, and FORTRAN 386. Software development tools will include PSCOPE Monitor 386, and an ICETM 386 in-circuit emulator.

System Compatibility

The iSBC 386/20P Single Board Computer is complemented by a wide range of MULTIBUS hardware and software products from over 200 manufacturers worldwide. This enables the designer to easily and quickly incorporate the iSBC 386/20P board into his system design to satisfy a wide range of high performance applications.

Applications that use other 16-bit MULTIBUS single board computers (such as Intel's iSBC 286/10A and iSBC 286/12 8 MHz, 80286 based single board computers) can be easily upgraded to use the iSBC 386/20P board. Only minor changes to hardware and systems software (for speed and I/O configuration dependent code) may be required.

BOARD SPECIFICATIONS

Word Size

Instruction—8, 16, 24, 32 or 40 bits
Data—8, 16, 32 bits

System Clock

CPU—16 MHz
Numeric Processor—80287 module—8 MHz

Cycle Time

Basic Instruction—16 MHz—125 ns (assumes instruction in queue)

NOTE:

Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles)

Dual-Port Memory

Capacity—One memory board
Maximum Physical Memory—
4 Megabytes (protected mode)
1 Megabyte (real mode)
Compatible DRAM Memory—
iSBC 402P 2MB or
iSBC 404P 4MB parity memory board (supplied with starter kit)

Local Memory

Number of sockets—Two 28-pin JEDEC Sites
Maximum size—128KB with 27512 EPROMS

I/O Capability

Serial Channel
Type—One RS232C DTE Asynchronous channel using an 8251A device.
Max speed—19.2 kilobaud
Leads supports—TD, RD, RTS, CTS, DSR, RI, CD, SG
Connector Type—10 pin ribbon
Expansion—One 8/16-bit iSBX interface connector for single or double wide iSBX MULTIMODULE board.

Interrupt Capacity

Potential Interrupt Sources—20 (2 fixed, 18 jumper selectable)
Interrupt Levels—16 using two 8259A devices and 80386 microprocessors NMI line.

Timers

Quantity—Two programmable timers using one 8274 device.
Input Frequency—1.23 MHz \pm 0.1%

Interfaces

MULTIBUS Bus—All signals TTL compatible
iSBX Bus—All signals TTL compatible
Serial I/O—RS232C, DTE
Timer—All signals TTL compatible
Interrupt Requests—All TTL compatible

MEMORY MAP (DEFAULT CONFIGURATION)

MEMORY TYPE	PVAM ADDRESS	MEMORY TYPE	REAL MODE ADDRESS
LOCAL EPROM (EPROM IN U32/U33) 27256 EPROMs	FFFFFFFFH	LOCAL EPROM (EPROM IN U32/U33) 27256 EPROMs	FFFFFFH
	(64K BYTES)		(64K BYTES)
UNUSED MEMORY	FFF0000H	MULTIBUS MEMORY	F0000H
	FFFEFFFFH		FFFFFFH
MULTIBUS MEMORY	01000000H	DUAL-PORT DRAM	(64K BYTES)
	00FFFFFFH		E0000H
DUAL-PORT DRAM	00200000H		DFFFFH
	001FFFFFFH		(896K BYTES)
	00000000H		000000H

Memory as seen from the on-board 80386

MEMORY TYPE	MULTIBUS® ADDRESS	MEMORY TYPE	MULTIBUS® ADDRESS
DUAL-PORT DRAM	1FFFFFFH	DUAL-PORT DRAM	DFFFFH
	(2M BYTES)		(896K BYTES)
	0000000H		000000H

Memory as seen from the MULTIBUS® interface
Note:

The ISBC 386/20P board is default configured for PVAM operation. To operate the board in real mode, the dual-port DRAM ending address must be set to DFFFFH, as shown.

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Counter	
	Min	Max
Real-time interrupt	667 ns	53.3 ms
Programmable one-shot	667 ns	53.3 ms
Rate generator	18.8 Hz	1.50 MHz
Square-wave rate generator	18.8 Hz	1.50 MHz
Software triggered strobe	667 ns	53.3 ms
Hardware triggered strobe	667 ns	53.3 ms
Event counter	—	8.0 MHz

Physical Characteristics
DIMENSIONS:

iSBC 386/20P CPU Board—
Width—12.00 in. (30.48 cm)
Height—8.75 in. (22.22 cm)

iSBC 402P/404P Memory Board—
Width—12.00 in. (30.48 cm)
Height—6.75 in. (17.15 cm)

RECOMMENDED MINIMUM CARDCAGE SLOT SPACING:

iSBC 386/20P CPU Board—1.2 in. (3.0 cm) (with or without iSBX MULTIMODULE)
iSBC 402P/404P Memory Board — 0.8 in. (2.0 cm)

MULTIBUS® DRIVERS

Function	Type	Sink Current (ma)
Data	Tri-State	64
Address	Tri-State	24
Commands	Tri-State	32
Bus Control	Open Collector	16/32

Mating Connectors

Function	# of Pins	Centers (in)	Connector Type	Vendor*	Vendor Part* Vendor* Number
iSBX Bus Connector	44	0.1	Soldered	Viking	000293-0001
Serial RS232C Connector	10	0.1	Flat Crimp	3M	3399-6010
Front Panel Connector	14	0.5	Flat Crimp	3M	3385-6014
P2 Interface Edge Connector	60	0.1	Flat Crimp T&B Ansley	KEL-AM	RF30-2803-5 A3020

* Or equivalent

APPROXIMATE WEIGHT:

iSBX 386/20P CPU Board—26 oz. (731 gm)
 iSBX 402P/404P Memory Board—18 oz. (510 gm)

Starter Kit System Requirements

IRMX®-BASED KIT

Intellec Series III/IV Development System (host)
 Intel 286/310 System (target)
 Models Sys 310-17, -17A, -40, -40A, -41, or -41A

PMON-BASED KIT

XENIX 286/310 System (host)
 Models Sys 310-40, -40A, -41, -41A, or -APXX.

NOTE:

System must be configured with XENIX Release 3, Update 3 (or higher) and a minimum of 2 MB of DRAM memory.

DC POWER REQUIREMENTS

Board	Voltage	Current (Approx.)
iSBX 386/20P CPU Board*	+5V	11A(max) 9A (typ)
	±12V	35mA (max) 20mA (typ)
iSBX 402P/404P Memory Board	+5	5.5A (max) 3.9A (typ)

***Notes:**

1. Includes power for local EPROM Memory
2. Does not include power for iSBX MULTIMODULE

ORDERING INFORMATION

Part Number	Description
SBC38620SPKGR	iRMX 286/386 ES-Based iSBX 386/20 Starter Kit. Supplied: iSBX 386/20P CPU board; iSBX 402P 2MB memory board; one set of CPU/memory ribbon cable assemblies; four serial cables for connection to Intellec Series III/IV system or console terminal; two 27256 EPROMs; 8" ISIS media and 5-1/4" iRMX media host/target diskettes; user documentation.
SBC38620SPKG2R	Same as above except with iSBX 404P 4MB memory board.
SBC38620SPKG	P-MON386ES-Based iSBX 386/20 Starter Kit. Supplied: iSBX 386/20P CPU board; iSBX 402P 2MB memory board; one set of CPU/memory ribbon cable assemblies; two serial cables for connection to DCE or DTE RS232C host interface; two 27512 EPROMs; 5-1/4" host diskettes; user documentation.
SBC38620SPKG2	Same as above except with iSBX 404P 4MB memory board.