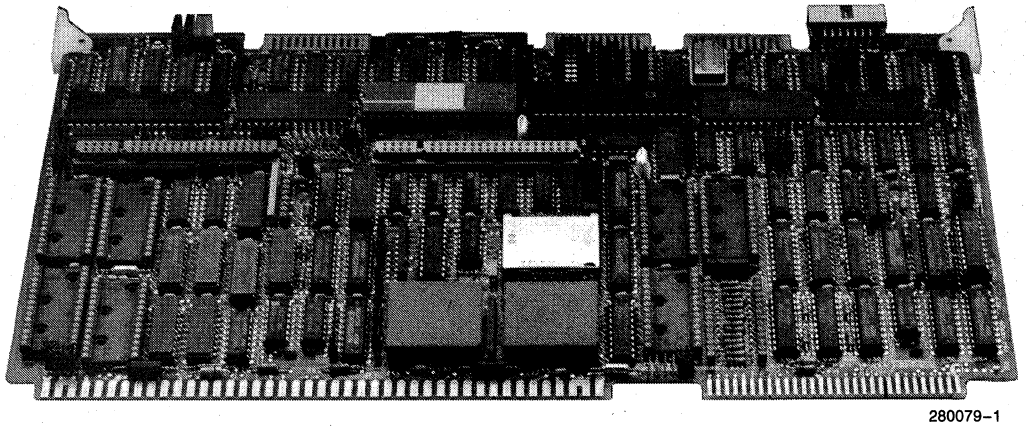
iSBC® 286/10A SINGLE BOARD COMPUTER

- 8 MHz 80286 Microprocessor
- Supports User Installed 80287 Numeric Data Processor
- iLBX™ Interface for iLBX Memory Board Expansion
- 0 Wait-State Synchronous Interface to EX Memory Expansion Boards
- Eight JEDEC 28-Pin Sites for Optional SRAM/iRAM/EPROM/E²PROM Components
- Optional Expansion to Sixteen JEDEC 28-Pin Sites with Two iSBE® 341 Boards
- Maximum On-Board Memory Capacity 384 KB
- Two iSBX™ Bus Interface Connectors for I/O Expansion
- 16 Levels of Vectored Interrupt Control
- Centronics-Compatible Parallel I/O Printer Interface
- Two Programmable Multiprotocol Synchronous/Asynchronous Serial Interfaces; One RS232C, the Other RS232C or RS422/449 Compatible

The iSBC® 286/10A Single Board Computer is a member of Intel's complete line of microcomputer modules and systems which take advantage of Intel's VLSI technology to provide economical, off-the-shelf, computer-based solutions for OEM applications. The board is a complete microcomputer system on a 6.75 x 12.0 inch printed circuit card. The CPU, system clock, memory sockets, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers all reside on the board. The iSBC 286/10A board offers both a standard iLBX interface for high-speed memory access to Intel's series of iLBX memory boards and a new, 0 wait-state, synchronous interface for use with Intels EX series of memory boards. The iSBC 286/10A Single Board Computer is fully compatible with its predecessor, the iSBC 286/10A board, and can be used in applications originally designed for the earlier model.



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* UNIX® is a registered trademark of BELL Labs.

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Order Number: 280079-005

FUNCTIONAL DESCRIPTION

Overview

The iSBC 286/10A board utilizes the powerful 80286 CPU within the MULTIBUS® system architecture, enhanced by the industry standard iLBX bus and a new, 0 wait-state, synchronous memory interface, to provide a high performance 16-bit solution. This board also includes on-board interrupt, memory and I/O features facilitating a complete signal board computer system. The iSBC 286/10A board is designed to be fully compatible with the iSBC 286/10 board, and only minor changes to software timing loops may be required.

Central Processing Unit

The central processor for the iSBC 286/10A board is the 80286 CPU operating at a 8.0 MHz clock rate. The 80286 CPU is upwardly compatible with Intel's 8088 and iAPX 86 CPUs. The 80286 CPU runs 8088 and 86 code at substantially higher speeds due to it's parallel chip architecture. In some cases, software timing loops may have to be adjusted to accommodate the faster CPU clock. In addition, the 80286 CPU provides on chip memory management and protection and virtual memory addressing of up to 1 gigabyte per task. Numeric processing power may be enhanced with the user installed 80287 numerics processor. The clock rates for the 80286 and the 80287 are independent with the 80287 rate jumper selectable at either 5.3 or 8.0 MHz.

Instruction Set

The 80286 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the 80287 Numeric Data Processor extends the 80286 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The 80287 meets the proposed IEEE P754 standard for numeric data processing and maintains compatibility with 8087-based systems.

Architectural Features

The 8086, 8088, 80186 and the 80286 microprocessor family contains the same basic set of registers, instructions, and addressing modes. The 80286 processor is upward compatible with the 8086, 8088, and 80186 CPUs.

The 80286 operates in two modes: 8086 real address mode, and protected virtual address mode. In 8086 real address mode, programs use real address with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. Both modes provide the same base instruction set, registers, and addressing modes.

VECTORED INTERRUPT CONTROL

Incoming interrupts are handled by two on-board 8259A programmable interrupt controllers and by the 80286's NMI line. Interrupts originating from up to 16 sources are prioritized and then sent to the CPU as a vector address. Further interrupt capability is available through bus vectored interrupts where slave 8259 interrupt controllers are resident on separate iSBC boards and are then cascaded into the on-board interrupt control.

INTERRUPT SOURCES

Twenty-three potential interrupt sources are routed to the interrupt jumper matrix where the user can connect the desired interrupt sources to specific interrupt levels. Table 1 includes a list of devices and functions supported by interrupts.

MEMORY CAPABILITIES

There are a total of eight 28-pin JEDEC sites on board. Four sites are for local memory and can contain up to 256K bytes of EPROM devices. The four other sites are known as the dual-port memory and may be addressed by the MULTIBUS interface and the on-board CPU bus. Up to 128K bytes of either iRAM, SRAM, EPROM, or E^2PROM can reside in these sites. Both the local and dual-port memory can be expanded to eight sites each by using two iSBC 341 JEDEC expansion modules. In this way, smaller size memory devices can be used up to the 256KB (local) and 128KB (dual-port) memory capacities.

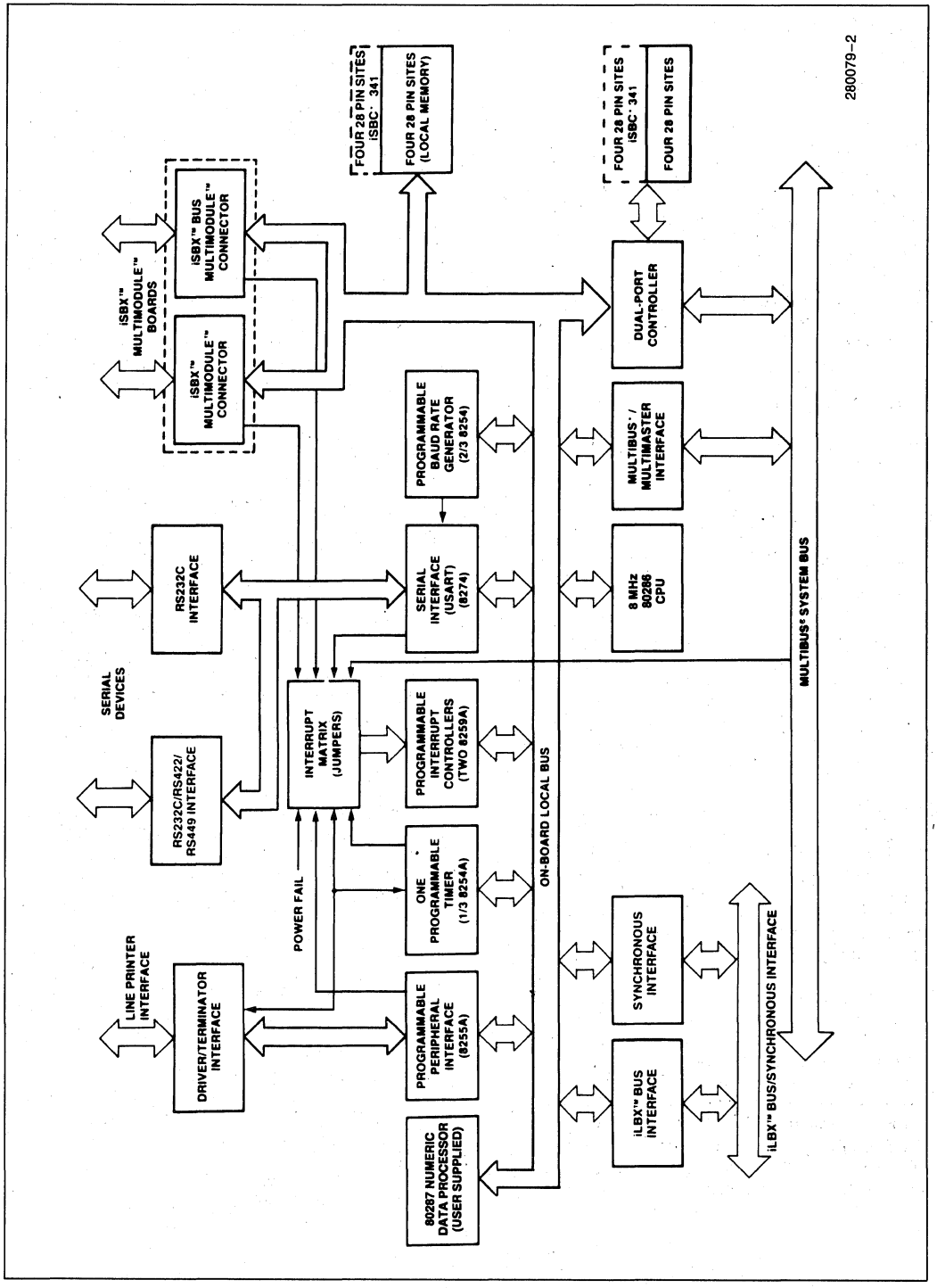

Figure 1. iSBC® 286/10A Block Diagram

Table 1. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface	Requests from MULTIBUS Resident Peripherals or Other CPU Boards	8*
8259A Programmable Interrupt Conroller	8 Level Vectored Interrupt Request Cascaded to Master 8259A	1
8274 Serial Controller	8 Level Vectored Interrupt Request Cascaded to Master 8259A	1
8255A Line Printer Interface	Signals Output Buffer Empty	1
8254 Timers	Timer 0, 1 Outputs; Function Determined by Timer Mode	2
iSBX Connectors	Function Determined by iSBX MULTIMODULE Board	4 (2 per iSBX™ Connector)
Bus Fail Safe Timer	Indicates Addressed MULTIBUS Resident Device Has not Responded to Command within 6 ms	1
Power Fail Interrupt	Indicates AC Power Is not within Tolerance	1
External Interrupt	General Purpose Interrupt from Auxiliary Connector, Commonly Used as Front Panel Interrupt	1
On-Board Logic	Conditioned Interrupt Source from Edge Sense Latch, Inverter, or OR Gate	3

* May be expanded to 56 with slave 8259A PICs on MULTIBUS* boards

SERIAL I/O

A two channel serial communications interface using Intel's 8274 Multi-Protocol Serial Controller (MPSC) is contained on the iSBC 286/10 board. Two independent software selectable baud rate generators provide the MPSC with all common communication frequencies. The protocol (i.e., asynchronous, IBM* bisync, or SDLC/HDLC), data format, control character format, parity and baud rate are all under program control. Software interfacing to the MPSC can be via either a polled or interrupt driven routine. One channel may be configured for an RS232C or RS422/RS449 interface with the other channel RS232C only. The data, command and signal ground lines for each channel are brought out to two 26-pin edge connectors.

PROGRAMMABLE TIMERS

The iSBC 286/10A board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller or to the 8274 MPSC to count external events or provide baud rate generation. The third interval timer in the 8254 is dedicated to providing a clock for the programmable baud rate generator in the iSBC 286/10A board's MPSC serial controller. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

LINE PRINTER INTERFACE

An 8255A Programmable Peripheral Interface (PPI) provides a line printer interface, several on-board functions, and four non-dedicated input bits. Drivers are provided for a complete Centronics compatible line printer interface. The on-board functions implemented with the PPI are power fail sense, override, NMI mask, non-volatile RAM enable, clear timeout interrupt, LED 0 and 1, clear edge sense flop, MULTIBUS interrupt, and serial channel A loopback. The PPI's I/O lines are divided into three eight bit ports: A, B, and C. Four non-dedicated input bits allow the state of four user-configured jumper connections to be input. The PPI must be programmed for mode 0 with ports A and C used as outputs and port B as input. A 16-bit write to Port B is used to set the iSBC 286/10A board into 24-bit address mode. The parallel port assignment is shown in Table 3.

Table 2. Programmable Time Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Even Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

Table 3. Parallel Port Bit Assignment

Port A—Output	
Bit	**Function**
0	Line Printer Data Bit 0
1	Line Printer Data Bit 1
2	Line Printer Data Bit 2
3	Line Printer Data Bit 3
4	Line Printer Data Bit 4
5	Line Printer Data Bit 5
6	Line Printer Data Bit 6
7	Line Printer Data Bit 7
Port B—Input	
Bit	**Function**
0	General Purpose Input 0
1	General Purpose Input 1
2	General Purpose Input 2
3	General Purpose Input 3
4	Line Printer ACK/ (Active Low)
5	Power Fail Sense/ (Active Low)
6	Line Printer Error (Active Hi)
7	Line Printer Busy (Active Hi)
Port C—Output	
Bit	**Function**
0	Line Printer Data Strobe (Active Hi)
1	Override/ (Active Low)
2	NMI Mask (0 = NMI Enabled)
3	Non-Volatile RAM Enable; Clear Timeout Interrupt/
4	LED 0 (1 = On); Clear Edge Sense Flop/
5	MULTIBUS Interrupt (1 = Active)
6	Serial CHA Loopback (0 = Online, 1 = Loopback)
7	LED 1 (1 = 0n); Clear Line Printer Ack Flop/

MULTIBUS® SYSTEM ARCHITECTURE

Overview

The MULTIBUS system architecture includes three bus structures: the system bus, the local bus extension and the MULTIMODULE expansion bus as shown in Figure 2. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The local bus extension allows large amounts of high performance memory to be accessed from a CPU board over a private bus. The MULTIMODULE extension bus is a means of adding inexpensive I/O functions to a base CPU board.

Each of these three bus structures are implemented on the iSBC 286/10A board providing a total system architecture solution.

SYSTEM BUS—IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations using multiple processors, I/O boards, and peripheral boards. The MULTIBUS system bus is supported with a board array of board level products. VLSI interface components, detailed published specifications and application notes.

SYSTEM BUS—EXPANSION CAPABILITIES

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, bubble memory boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

SYSTEM BUS—MULTIMASTER CAPABILITIES

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 286/10A board provides full system bus arbitration control logic. This control logic allows up to three iSBC 286/10A board or other bus masters, including the iSBC 80 board family of MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to multiprocessing configuration made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

HIGH SPEED OFF-BOARD MEMORY

The iSBC 286/10A board can access off-board memory either over the MULTIBUS (P1) interface, or over the P2 interface as shown in Figure 3. Memory transfers over the P2 interface are faster because the CPU board doesn't have to arbitrate for access to the MULTIBUS interface.

Using the P2 interface, the iSBC 286/10A Board can be configured to operate with either a standard iLBX interface or with a high-performance, synchronous interface.

The iSBC 286/10A Board as supplied is configured to operate with a synchronous, P2 interface. This high-performance interface is designed to connect to Intel's new EX series of memory expansion boards to yield a CPU to memory read/write time of 0 wait-states. The EX memory expansion boards are available in sizes ranging from 512K bytes up to 4M

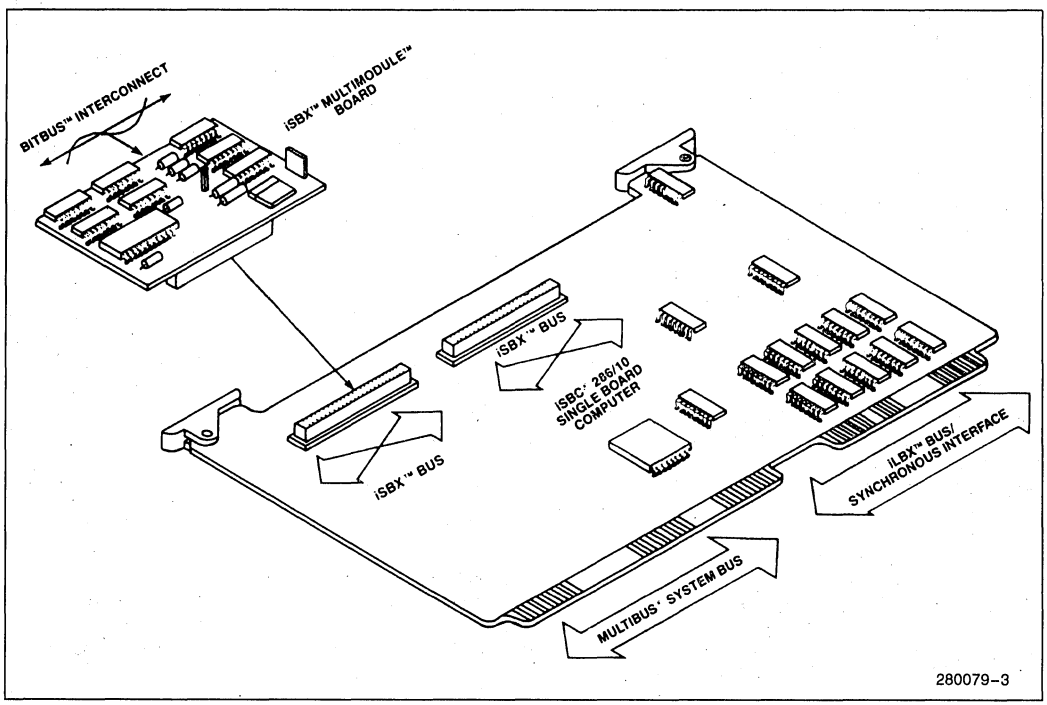

Figure 2. MULTIBUS® System Architecture

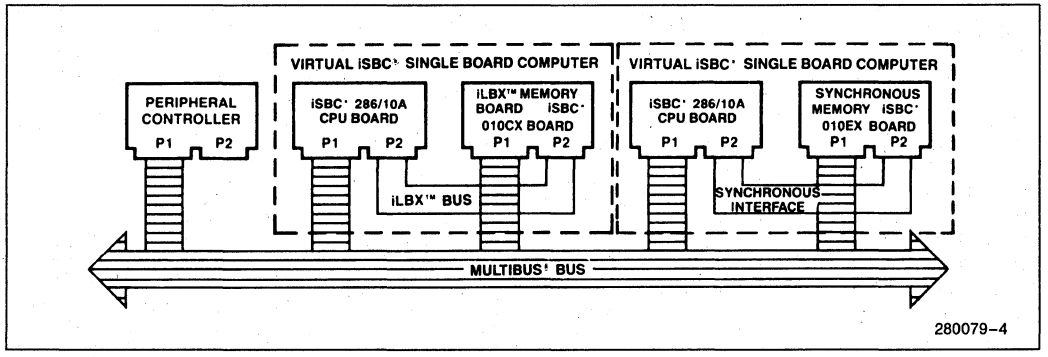

Figure 3. MULTIBUS®/iLBX™/Synchronous Interface Configurations

bytes and available in sizes ranging from 512K bytes up to 2M bytes. Memory expansion boards from other manufacturers that meet the iLBX standard may also be used. CPU to memory access time is usually 1 or more wait-states depending on the speed of the memory used.

A total of four memory boards can be placed on the iLBX or synchronous interface bus. With 4M byte memory boards, this results in a total of 16M bytes on the memory expansion bus.

iSBX™ BUS MULTIMODULE™ ON-BOARD EXPANSION

Two 8/16-bit iSBX MULTIMODULE connectors are provided on the iSBC 286/10A microcomputer board. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULEs optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., bubble cassettes and floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS Board form factor compatible boards. The iSBX interface connectors on the iSBC 286/10A provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 286/10A microcomputer board. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX modules may also be designed. An iSBX bus interface specification and iSBX connectors are available from Intel.

Software Support

Software support from Intel includes the iRMX 86, iRMX 286, and XENIX* operating systems, assembly and high level languages, development systems, in-circuit emulators, and various other hardware and software tools.

For those applications needing a real-time, multitasking operating system, Intel offers the iRMX 86 and iRMX 286 operating systems. The iRMX operating systems are particularly well suited for industrial or commercial applications where the processor is simultaneously controlling multiple, real-time, interrupt intensive processes. Typical applications include machine and process control, data aquisition, signal processing, front-end processing, and digital PABX control. The iRMX operating systems employ a highly configurable, modular structure that allows easy system configuration and expansion.

The iRMX 86 operating system enables the iSBC 286/10A board to address up to 1MB of memory in real address mode. Using the iRMX 286 operating system, this address range is extended to 16 MB in native mode. The iRMX 286 operating system also allows the user to take advantage of the hardware traps built into the 80286 processor that provide expanded debug capabilities and increased code reliability.

Application code written for the iRMX 86 operating system can be compiled using 286 compilers to run under the iRMX 286 operating system. Application code will require only minor changes.

Assembly and many high level languages are supported by the iRMX operating systems and Intellec® Series IV development systems. Language support for the iSBC 286/10A board in real address board

includes Intel's ASM 86, PL/M 86, PASCAL 86, FORTRAN 86, and C86, as well as many third party 8086 languages. Language support for native address mode include ASM 286, PL/M 286, PASCAL 286 and FORTRAN 286. Programs developed in these languages can be downloaded from an Intel System 310 or Series IV Development System to the iSBC 286/10A board via the iSDM System Debug Monitor. The iSDM monitor also provides on-target program debugging support including breakpoint and memory examination features.

Intel also offers the XENIX operating system which is designed for those applications needing an interactive, multiple user system. Typical applications include small business systems, software development/engineering workstations, distributed data processing, communications, and graphics.

Intel's XENIX operating system is a fully licensed derivative of UNIX*, enhanced by Intel to provide device driver support for Intel board and component products plus other features that yield greater flexibility, increased reliability, and easier configurability. Intel's XENIX operating system has been optimized for use with the 80286 microprocessor and supports such features as on-chip memory management and protection which provide ease of portability and higher performance.

Applications software can be written in either Intel's FORTRAN, COBOL, or BASIC languages using a XENIX-based, Intel 286/310 or 286/380 system, or by using an Intel iDIS™ Database Information System. The user can also select from a wide variety of existing third party languages and applications software.

SPECIFICATIONS

Word Size

Instruction—8, 16, 24, 32 or 40 bits
Data—8 or 16 bits

System Clock

CPU—8.0 MHz
Numeric Processor—5.3 or 8.0 MHz (Jumper Selectable)

Cycle Time

Basic Instruction—8.0 MHz—375 ns; 250 ns (assumes instruction in queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles)

Local Memory

Number of sockets—Four 28-pin JEDEC sites, expandable to 8 sites using iSBC 341 JEDEC Expansion Module

Maximum Size—256 KB

Compatible Devices—EPROM, up to 64K x 8 (Intel 27512)

Dual-Port Memory

Number of sockets—Four 28-pin JEDEC sites, expandable to 8 sites using iSBC 341 JEDEC Expansion Module

Maximum Size—128 KB

Compatible Devices—EPROM, up to 32K x 8 (Intel 27256)

SRAM
iRAM, up to 8K x 8 (Intel 2186)
E^2PROM, up to 2K x 8 (Intel 2817A)

Off-Board Physical Memory

Operating System	Address Mode	Size
iRMX 86 Rlse. 6	Real	1MB
iRMX 286 Rlse. 1	Native	16 MB
XENIX Rlse. 3	Native	16 MB

I/O Capability

Parallel—Line printer interface, on-board functions, and four non-dedicated input bits

Serial—Two programmable channels using one 8274 device

Timers—Three programmable timers using one 8254 device

Expansion—Two 8/16-bit iSBX MULTIMODULE connectors

BAUD RATES

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)				
	Synchronous	Asynchronous			
Reference: 1.23 MHz	÷1	÷1	÷16	÷32	÷64
615.	615,000	615,000	38,400	19,200	9,600
307.	307,000	307,000	19,200	9,600	4,800
154.	154,000	154,000	9.600	4,800	2,400
76.8	76,800	76,800	4,800	2,400	1,200
56.0	56,000	—	—	—	—
38.4	38,400	38,400	2,400	1,200	600
19.2	19,200	19,200	1,200	600	300
9.6	9,600	9.600	600	300	150
4.6	4,800	4,800	300	150	75
2.4	2,400	2,400	150	75	—
1.2	1,200	1,200	75	—	—
0.6	600	600	—	—	—

Serial Communications Characteristics

Synchronous—5–8 bit characters; internal or HDLC/SDLC character synchronization; automatic sync insertion; even or odd parity

Asynchronous—5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; even or odd parity

Interrupt Capacity

Potential Interrupt Sources—25, 5 fixed, 20 jumper selectable

Interrupt Levels—16 vectored requests using two 8259As and the 80286's NMI line.

Timers

Input Frequencies—1.23 MHz ±0.1% or 3.00 MHz ±0.1% (Jumper Selectable)

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	667 ns	53.3 ms	1.33 μs	58.2 min
Programmable One-Shot	667 ns	53.3 ms	1.33 μs	58.2 min
Rate Generator	18.8 Hz	1.50 MHz	0.000286 Hz	750 kHz
Square-Wave Rate Generator	18.8 Hz	1.50 MHz	0.000286 Hz	750 kHz
Software Triggered Strobe	667 ns	53.3 ms	1.33 μs	58.2 min
Hardware Triggered Strobe	667 ns	53.3 ms	1.33 μs	58.2 min
Event Counter	—	8.0 MHz	—	—

MATING CONNECTORS (OR EQUIVALENT PART)

Function	# of Pins	Centers (in)	Connector Type	Vendor	Vendor Part No.
iSBX Bus Connector 16-Bit (J5, J6)	44	0.1	Soldered	Viking	000293-001
I/O Connectors (J1–J3)	26	0.1	Flat Crimp	3M	3462-0001
Front Panel Connector (J4)	14	0.5	Flat Crimp	3M	3385-6014
iLBX/Synch. Interface Edge Connector (P2)	60	0.1	Flat Crimp	KEL-AM T & B Ansley	RF30-2803-5 A3020

INTERFACES

MULTIBUS Bus—All signals TTL compatible

iSBX Bus—All signals TTL compatible

iLBX Bus—All signals TTL compatible

Synchronous Interface—All signals TTL compatible

Serial I/O—Channel A: RS232C/RS422/RS449 compatible, DCE or DTE; Channel B; RS232C compatible, DCE only

NOTE:
User supplied 34487 line driver and SIP termination resistor need to be installed for RS422/RS499 operation.

Timer—All signals TTL compatible

Interrupt Requests—All TTL compatible

MULTIBUS® DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	16
Address	Tri-State	16
Commands	Tri-State	32
Bus Control	Open Collector	20

iLBX™ DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	9
Address	Tri-State	20
Commands	Tri-State	8
Bus Control	TTL	8

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.4 in. (1.0 cm)
Minimum Slot Spacing: 0.6 in. (1.5 cm)
Weight: 14 oz. (397 gm)

Electrical Characteristics

DC Power Requirements: +5V, 7.0A; ±12V, 50 mA (serial I/O)

NOTE:
Does not include power for optional EPROM, E^2PROM, or RAM memory devices, or installed MULTIMODULE boards

Environmental Characteristics

Operating Temperature: 0°C to 60°C with 7 CFM airflow across board

Relative Humidity: to 90% (without condensation)

Reference Manual

147532-001—iSBC® 286/10A Hardware Reference Manual (order separately)

ORDERING INFORMATION

Part Number	Description
SBC 286/10A	Single Board Computer