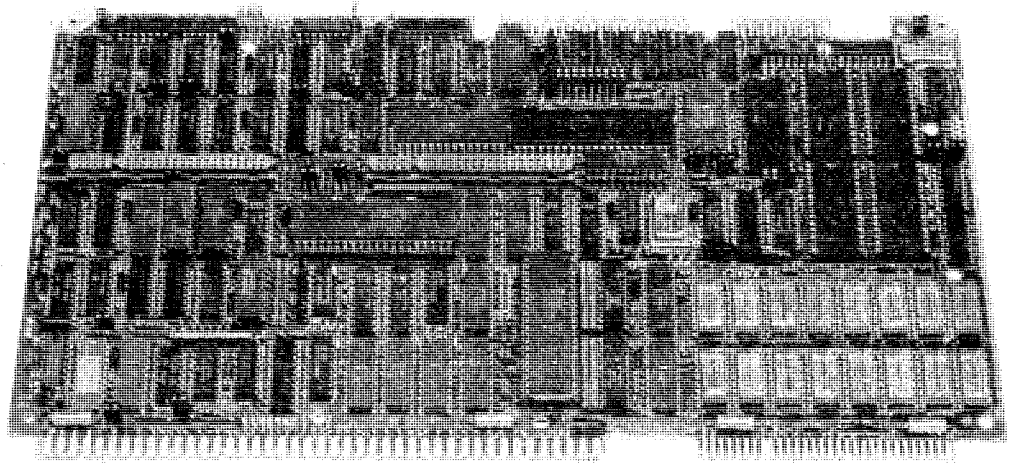
iSBC® 86/14 AND iSBC® 86/30 SINGLE BOARD COMPUTERS

- 8086 Microprocessor with 5 or 8 MHz CPU Clock
- Fully Software Compatible with iSBC® 86/12A Single Board Computer
- Optional 8086 Numeric Data Processor with iSBC® 337A MULTIMODULE™ Processor
- 32K/128K bytes of Dual-Port Read/Write Memory Expandable On-Board to 256K bytes with On-Board Refresh
- Sockets for up to 64K bytes of JEDEC 24/28-pin Standard Memory Devices
- Two iSBX™ Bus Connectors
- 24 Programmable Parallel I/O Lines
- Programmable Synchronous/Asynchronous RS232C Compatible Serial Interface with Software Selectable Baud Rates
- Two Programmable 16-Bit BCD or Binary Timers/Event Counters
- 9 Levels of Vectored Interrupt Control, Expandable to 65 Levels
- MULTIBUS® Interface for Multimaster Configurations and System Expansion
- Supported by a Complete Family of Single Board Computers, Memory, Digital and Analog I/O, Peripheral Controllers, Packaging and Software

The iSBC 86/14 and iSBC 86/30 Single Board Computers are members of Intel's complete line of OEM microcomputer systems which take full advantage of Intel's technology to provide economical, self-contained, computer-based solutions for OEM applications. Each board is a complete computer system on a single 6.75 x 12.00-in. printed circuit card distinguished by RAM memory content with 32K bytes and 128K bytes provided on the iSBC 86/14 and iSBC 86/30 board, respectively. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the boards.



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FUNCTIONAL DESCRIPTION

Central Processing Unit

The central processor for the iSBC 86/XX* boards is Intel's iAPX 86/10 (8086-2) CPU. A clock rate of 8 MHz is supported with a jumper selectable option of 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers and two 16-bit index registers, all accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for support of the data structures required for today's structured, high level languages as well as assembly language.

NOTE:
iSBC 86/XX designates both the iSBC 86/14 and iSBC 86/30 CPU boards.

Instruction Set

The 8086 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the iSBC 337A MULTIMODULE Numeric Data Processor extends the 8086/10 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32, and 64-bit integer, and 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary.

Architectural Features

A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 750 nsec minimum instruction cycle to 250 nsec for queued instructions. The stack-oriented architecture readily supports modular programming by facilitating fast, simple, inter-module communication, and other programming constructs needed for asynchronous real-time systems. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K bytes at a time and activation of a specific register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions.

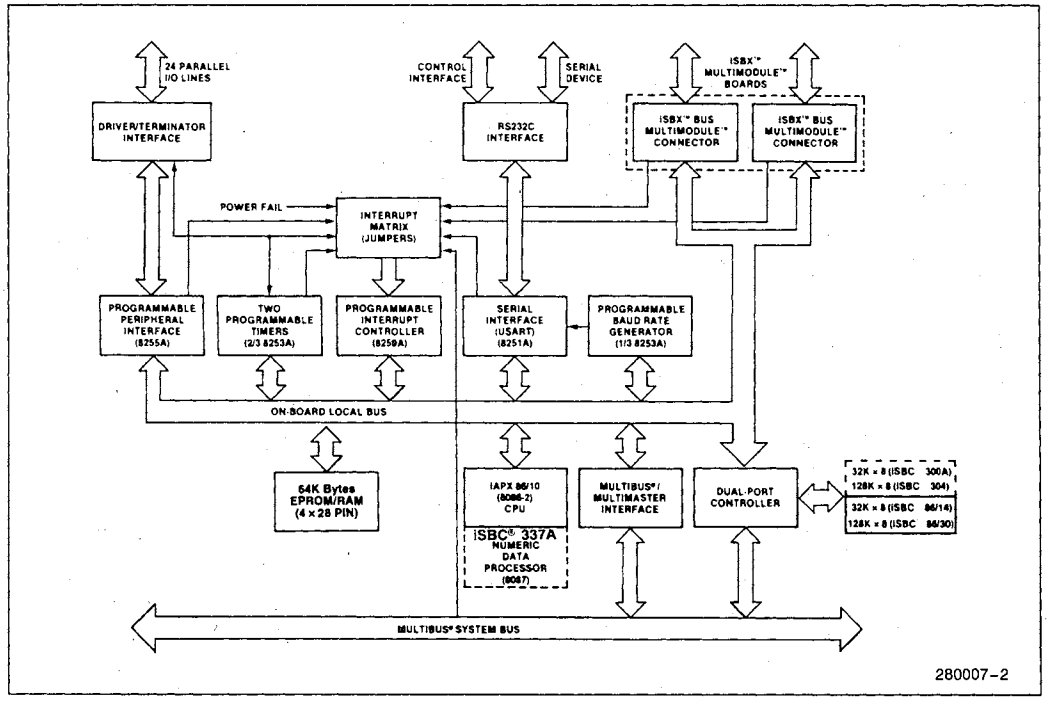


Figure 1. iSBC® 86/XX Block Diagram

RAM Capabilities

The iSBC 86/14 and iSBC 86/30 microcomputers contain 32K bytes and 128K bytes of dual-port dynamic RAM, respectively. In addition, on-board RAM may be doubled on each microcomputer by optionally adding RAM MULTIMODULE boards. The on-board RAM may be expanded to 256K bytes with the iSBC 304 MULTIMODULE Board mounted onto the iSBC 86/30 board. Likewise, the iSBC 86/14 microcomputer may be expanded to 64K bytes with the iSBC 300A MULTIMODULE option. The dual-port controller allows access to the on-board RAM (including RAM MULTIMODULE options) from the iSBC 86/XX boards and from any other MULTIBUS master via the system bus. Segments of on-board RAM may be configured as a private resource, protected from MULTIBUS system access. The amount of memory allocated as a private resource may be configured in increments of 25% of the total on-board memory ranging from 0% to 100% (optional RAM MULTIMODULE boards double the increment size). These features allow the multiprocessor systems to establish local memory for each processor and shared system memory configurations where the total system memory size (including local on-board memory) can exceed one megabyte without addressing conflicts.

EPROM Capabilities

Four 28-pin sockets are provided for the use of Intel 2716s, 2732As, 2764s, 27128s, and their respective ROMs. When using 27128s, the on-board EPROM capacity is 64K bytes. Other JEDEC standard pinout devices are also supported, including byte-wide static RAMs.

Parallel I/O Interface

The iSBC 86/XX Single Board Computers contain 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. In order to take advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators, allowing the selection of the appropriate combination of optional line drivers and terminators with the required drive/termination characteristics. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 86/XX boards. A software selectable baud rate generator provides the USART with all common communication frequencies. The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C command lines, serial data lines and signal ground line are brought out to a 26-pin edge connector.

Programmable Timers

The iSBC 86/XX boards provide three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable In-

Table 1. Input/Output Port Modes of Operation

Port	Lines (Qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X(1)
	4	X		X			X(1)

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

terval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O terminators associated with the 8255A to allow external devices or an 8255A port to gate the timer or to count external events. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 86/XX boards' RS232C USART serial port. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation or real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an internal trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

iSBX™ MULTIMODULE™ On-Board Expansion

Two 8/16-bit iSBX MULTIMODULE connectors are provided on the iSBC 86/XX microcomputers. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., cassettes and floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 86/XX boards provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 86/XX microcomputers. A broad range of iSBX MULTIMODULE options are available in this family from Intel. Custom iSBX modules may also be designed for use on the iSBC 86/XX boards. An iSBX bus interface specification and iSBX connectors are available from Intel.

MULTIBUS® SYSTEM BUS AND MULTIMASTER CAPABILITIES

Overview

The MULTIBUS system bus is Intel's industry standard microcomputer bus structure. Both 8 and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In its simplest application, the MULTIBUS system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the MULTIBUS structure also allows very powerful distributed processing configurations with multiple processors and intelligent slave I/O, and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. On-

board EPROM capacity may be expanded to 128K by user reprogramming of a PAL device to support 27256 EPROM devices. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 86/XX boards provide full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 86/XX boards or other bus masters, including iSBC 80 family MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

Interrupt Capability

The iSBC 86/XX boards provide 9 vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 8086 CPU. This interrupt is typically used for signaling catastrophic events (e.g., power failure). The Intel 8259A Programmable Interrupt Controller (PIC) provides control and vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available for use in designing

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-Rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific Priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

request processing configurations to match system requirements for efficient interrupt servicing with minimal latencies. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from all on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves requests according to the selected mode and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked via software, by storing a single byte in the interrupt mask register of the PIC. In systems requiring additional interrupt levels, slave 8259A PICs may be interfaced via the MULTIBUS system bus, to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Interrupt Request Generation

Interrupt requests to be serviced by the iSBC 86/XX boards may originate from 28 sources. Table 4 includes a list of devices and functions supported by interrupts. All interrupt signals are brought to the interrupt jumper matrix where any combination of interrupt sources may be strapped to the desired interrupt request level on the 8259A PIC or the NMI input to the CPU directly.

Power-Fail Control and Auxiliary Power

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 and iSBC 640 Power Supply or equivalent, to initiate an orderly shut down of the system in the event of a power failure. Additionally, an active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences. An auxiliary power bus is also provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

System Development Capabilities

The development cycle of iSBC 86/XX products can be significantly reduced and simplified by using either the System 86/310 or the Intellec Series IV Microcomputer Development System or the IBM PC.

IN-CIRCUIT EMULATOR

The I²ICE In-Circuit Emulator provides the necessary link between the software development environment and the "target" iSBC 86/XX execution system. In addition to providing the mechanism for loading executable code and data into the iSBC 86/XX boards, the I²ICE In-Circuit Emulator provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software.

PL/M-86

Intel's system's implementation language, PL/M-86, is standard in the System 86/310 and is also available for the Series IV and the IBM PC. PL/M-86 provides the capability to program in algorithmic language and eliminates the need to manage register usage or allocate memory while still allowing explicit control of the system's resources when needed. FORTRAN 86, PASCAL 86 and C86 are also available the Intellec Series IV, 86/310 systems and the IBM PC.

SPECIFICATIONS

Word Size

Instruction: 8, 16, 24, or 32 bits

Data: 8, 16 bits

System Clock

5.00 MHz or 8.00 MHz ±0.1% (jumper selectable)

Cycle Time

BASIC INSTRUCTION CYCLE

8 MHz: 750 ns
250 ns (assumes instruction in the queue)

5 MHz: 1.2 μs
400 ns (assumes instruction in the queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles).

Table 4. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface	Requests from MULTIBUS resident peripherals or other CPU boards.	8; may be Expanded to 64 with Slave 8259A PICs on MULTIBUS Boards
8255A Programmable Peripheral Interface	Signals input buffer full or output buffer empty; also BUS INTR OUT general purpose interrupt from driver/terminator sockets.	3
8251A USART	Transmit buffer empty and receive buffer full.	2
8253 Timers	Timer 0, 1 outputs; function determined by timer mode.	2
iSBX Connectors	Function determined by iSBX MULTIMODULE board.	4 (2 per iSBX Connector)
Bus Fail Safe Timer	Indicates addressed MULTIBUS resident device has not responded to command within 6 ms.	1
Power Fail Interrupt	Indicates AC power is not within tolerance.	1
Power Line Clock	Source of 120 Hz signal from power supply.	1
External Interrupt	General purpose interrupt from auxiliary (P2) connector on backplane.	1
iSBC 337A MULTIMODULE Numeric Data Processor	Indicates error or exception condition.	1
Parity Error	Indicates on-board RAM parity error from iSBC 303 parity MULTIMODULE board (iSBC 86/14 option).	1
Edge-Level Conversion	Converts edge triggered interrupt request to level interrupt.	1
OR-Gate Matrix	Outputs of OR-gates on-board for multiple interrupts.	2

Memory Cycle Time

RAM: 750 ns

EPROM: Jumper selectable from 500 ns to 875 ns

Memory Capacity/Addressing

ON-BOARD EPROM

Device	Total Capacity	Address Range
2716	8K bytes	FE000–FFFFF$_H$
2732A	16K bytes	FC000–FFFFF$_H$
2764	32K bytes	F8000–FFFFF$_H$
27128	64K bytes	F0000–FFFFF$_H$

NOTE:
iSBC 86/XX EPROM sockets support JEDEC 24/28-pin standard EPROMs and RAMs. Total EPROM capacity may be increased to 128 bytes by the user reprogramming an on-board PAL.

ON-BOARD RAM

Board	Total Capacity	Address Range
iSBC 86/14	32K bytes	0–07FFF$_H$
iSBC 86/30	128K bytes	0–1FFFF$_H$

WITH MULTIMODULE™ RAM

Board	Total Capacity	Address Range
iSBC 300A (with iSBC 86/14)	64K bytes	0–0FFFF$_H$
iSBC 304 (with iSBC 86/30)	256K bytes	0–3FFFF$_H$

I/O Capacity

Parallel: 24 programmable lines using one 8255A

Serial: 1 programmable line using one 8251A

iSBX MULTIMODULE: 2 iSBX boards

Serial Communications Characteristics

Synchronous: 5–8 bits characters; internal or external character synchronization; automatic sync insertion

Asynchronous: 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit direction

BAUD RATES

Frequency (kHz) (Software Selectable	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Timers

INPUT FREQUENCIES

Reference: 2.46 MHz ±0.1% (0.041 μsec period, nominal); or 153.60 kHz ±0.1% (6.51 μsec period, nominal)

NOTE:
Above frequencies are user selectable.

Event Rate: 2.46 MHz max

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/counter (Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.63μs	427.1 ms	3.26s	466.50 min
Programmable One-Shot	1.63 μs	427.1 ms	3.26s	466.50 min
Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-Wave Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software Triggered Strobe	1.63μs	427.1 ms	3.26s	466.50 min
Hardware Triggered Strobe	1.63 μs	427.1 ms	3.26s	466.50 min
Event Counter	—	2.46 MHz	—	—

Interfaces

MULTIBUS: All signals TTL compatible

iSBX Bus: All signals TTL compatible

Parallel I/O: All signals TTL compatible

Serial I/O: RS232C compatible, configurable as a data set or data terminal

Timer: All signals TTL compatible

Interrupt Requests: All TTL compatible

Connectors

Interface	Double-Sided Pins	Centers (in.)	Mating Connectors
MUILTIBUS System	86	0.156	Viking 3KH43/9AMK12 Wire Wrap
iSBX Bus 8-Bit Data	36	0.1	iSBX 960-5
Parallel I/O (2)	50	0.1	3M 3415-000 Flat or TI H312125 Pins
Serial I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat

Line Drivers and Terminators

I/O DRIVERS

The following line drivers are all compatible with the I/O driver sockets on the iSBC 86/05 board.

Driver	Characteristics	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

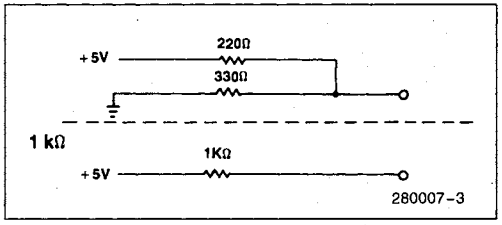
NOTE:
I = inverting; NI = non-inverting; OC = open collector.

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 KΩ terminators

I/O TERMINATORS

220Ω/330Ω divider or 1 kΩ pullup

220Ω/330Ω



MULTIBUS® Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	32
Address	Tri-State	32
Commands	Tri-State	32
Bus Control	Open Collector	20

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.70 in. (1.78 cm)
Weight: 14 oz (388 gm)

Environmental Characteristics

Operating Temperature: 0°C to 55°C
Relative Humidity: to 90% (without condensation)

Electrical Characteristics

DC POWER REQUIREMENTS

Configuration	Current Requirements (All Voltages ±5%)		
	+5V	+12V	−12V
Without EPROM[1]	5.1A	25 mA	23 mA
RAM only[2]	600 mA	—	—
With 8K EPROM[3] (using 2716)	5.4A	25 mA	23 mA
With 16K EPROM[3] (using 2732A)	5.5A	25 mA	23 mA
With 32K EPROM[3] (using 2764)	5.6A	25 mA	23 mA

NOTES:
1. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators.
2. RAM chips powered via auxiliary power bus in power-down mode.
3. Includes power required for 4 ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

Environmental Characteristics

Operating Temperature: 0°C to 55°C
Relative Humidity: to 90% (without condensation)

Reference Manual

144044-002: iSBC 86/14 and iSBC 86/30 Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 86/14	Single Board Computer
SBC 86/30	Single Board Computer