External Interrupt Controller Using Intel® 80310 I/O Processor Chipset

Application Note

July 2001

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Contents

Figures

Tables

Revision History

Date	Revision	Description
July 2001	001	Initial Release.

1.0 Introduction

This document provides information to implement an external interrupt controller when using the Intel® 80310 I/O processor chipset (80310), which is composed of the Intel® 80200 processor based on Intel® XScale™ Microarchitecture (ARM* architecture compliant) and the Intel® 80312 I/O companion chip (80312). The 80312 does not provide status and mask registers for the four external interrupt signals (**XINT[3:0]#** and **S_INT[D:A]#**), therefore this document discusses some alternative methods that need to be implemented in order to properly handle these interrupts.

The 80200 processor (80200) is scalable by software up to 733 MHz, with a bus frequency independently controlled running up to 100 MHz. 80200 low power consumption makes it ideal for power conscious applications.

The 80312 integrates a PCI-to-PCI bridge supporting both 64-bit and 32-bit modes running at 66 MHz. The PCI Bridge can also run at 33 MHz. The 80312 contains an integrated memory controller that supports Flash and SDRAM interface. The memory controller runs at a frequency up to 100 MHz.

This document leverages the Complex Programmable Logic Device (CPLD) implementation for interrupt handling from the Intel® IQ80310 Evaluation Platform (IQ80310). Further information can be found on Intel's web site located at:

http://developer.intel.com/design/iio/docs/dvtl_iq80310.htm

Information provided at this location provides all necessary information and source code necessary to implement an interrupt controller.

1.1 Technical Support, Schematics, and CPLD Equations

For technical assistance contact the Intel® Technical Support Hotline (1-800-628-8686).

Manuals are updated online and available in softcopy form. Up-to-date product and technical information including the *Intel® IQ80310 Evaluation Platform Manual* and useful links for developers are available at:

http://developer.intel.com/design/iio/

To order manuals from Intel, contact your local sales representative or Intel® Literature Sales (1-800-548-4725).

1.2 Related Documentation

Table 1. Related Documents and Websites

Document Title	Document #
Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Developer's Manual	273411
Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Datasheet	273414
Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Specification Update	273415
Intel® 80310 I/O Processor Chipset with Intel® XScale™ Microarchitecture Design Guide	273354
Intel® 80312 I/O Companion Chip Developer's Manual	273410
Intel® 80312 I/O Companion Chip Datasheet	273425
Intel® 80312 I/O Companion Chip Specification Update	273416
Intel® *82559 Fast Ethernet Multifunction PCI/Card Bus Controller*	743892
Intel® 80310 I/O Processor Chipset with Intel® XScale™ Microarchitecture Initialization	273438
Intel® XScale™ Microarchitecture, Programmers Reference Manual	273436
Redhat GNUPro* Toolkit, Getting Started Guide, GNUPro* 2000 for Intel® XScale™ Microarchitecture*	
Redhat User's Guide for Intel® XScale™ Microarchitecture, GNUPro* Toolkit*	
Redhat Redboot* User's Guide*	
Lattice Semiconductor Corporation MACH 4 CPLD Family	17466
GNUPro* Toolkit Documentation http://www.redhat.com/support/manuals/gnupro.html	
PCI Local Bus Specification, Revision 2.2 • PCI Special Interest Group • 1-800-433-5177 • http://www.pcisig.com	
UART PN# TL16C550C Documentation: Texas Instrument http://focus.ti.com/docs/prod/productfolder.jhtml?genericPartNumber=TL16C550C	
Intel® I/O Processors - Comprehensive Documentation http://developer.intel.com/design/iio	
ADI Engineering, Inc 80200EVB Evaluation Platform http://www.adiengineering.com	

2.0 Intel® IQ80310 Evaluation Platform Interrupt Handling Implementation

This section leverages the CPLD implementation for interrupt handling from the IQ80310. Further information can be found on Intel's web site located at

http://developer.intel.com/design/iio/docs/dvtl_iq80310.htm.

Information provided at this location provides all necessary information and source code necessary to implement an interrupt controller.

2.1 External Interrupts

External interrupts can include an external timer interrupt, i82559 Ethernet interrupt, two UART interrupts, and PCI interrupts INTA, INTB, INTC, and INTD. For this example interrupts are routed through the 80312 to the FIQ# interrupt pin on the 80312.

Figure 1 shows how interrupts are routed through the 80312. Figure 2 shows interrupt steering between the 80200 processor and the 80312. Some instances require the FIQ# and IRQ# pins of the 80312 to be swapped around, this is shown by the "switch" input to the CPLD shown in Figure 2. This interrupt line swapping is application and operating system dependant, verify which interrupt source/s is supported by the operating system. Figure 3 shows the interrupt steering within the CPLD that is present on the IQ80310 evaluation platform.

2.2 Handling External Interrupts

The global IRQ dispatcher in the code provided at:

http://developer.intel.com/design/iio/docs/dvtl_iq80310.htm

reads the status register to determine which sources are interrupting and calls appropriate handlers. Interrupt handler connecting routines are supplied to allow users to connect their handlers into this dispatcher, refer to same URL as global IRQ dispatcher above for further information. The global IRQ dispatcher is called by the assembly IRQ handler, which saves the current register set to the stack and disables further IRQ interrupts before calling the IRQ dispatcher. This dispatcher then checks the interrupt status register to determine which external interrupt is generating IRQ, and then calls the appropriate user handler. User interrupt handlers should clear the source of the interrupt before returning. The IRQ handler also checks the FIQ1 and FIQ2 status registers in the 80312 for other possible interrupt sources.

Figure 1. Interrupt Steering inside the Intel® 80312 I/O Companion Chip

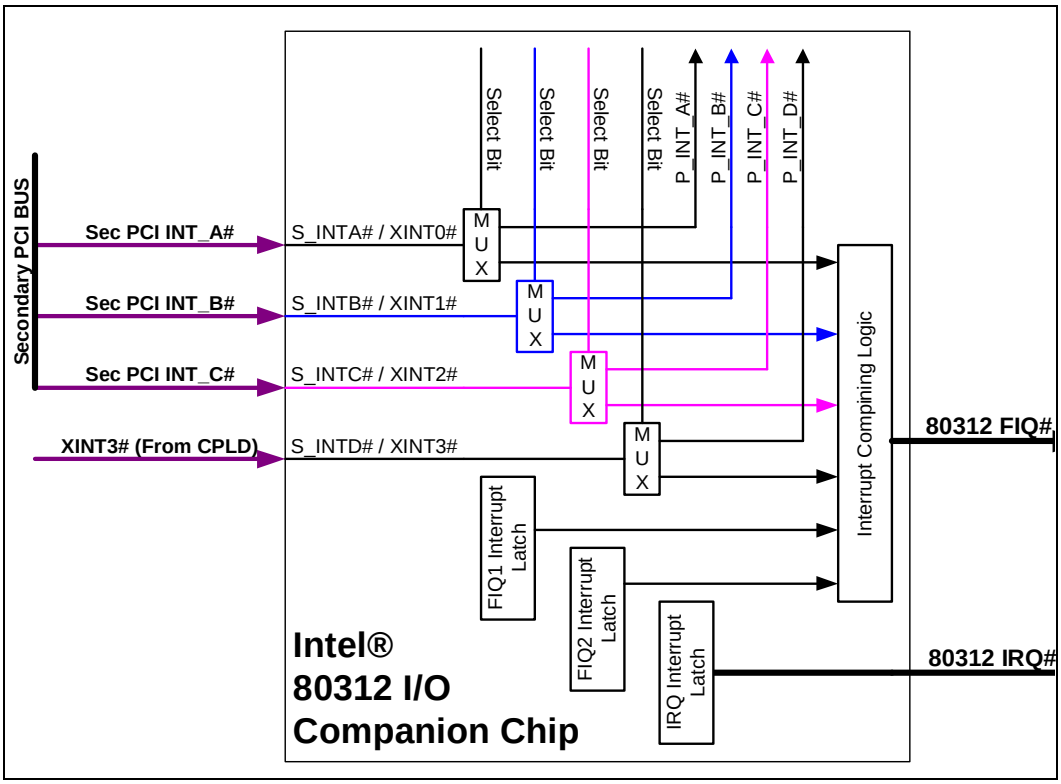


Figure 2. Interrupt Steering between Intel® 80200 Processor and Intel® 80312 I/O Companion Chip

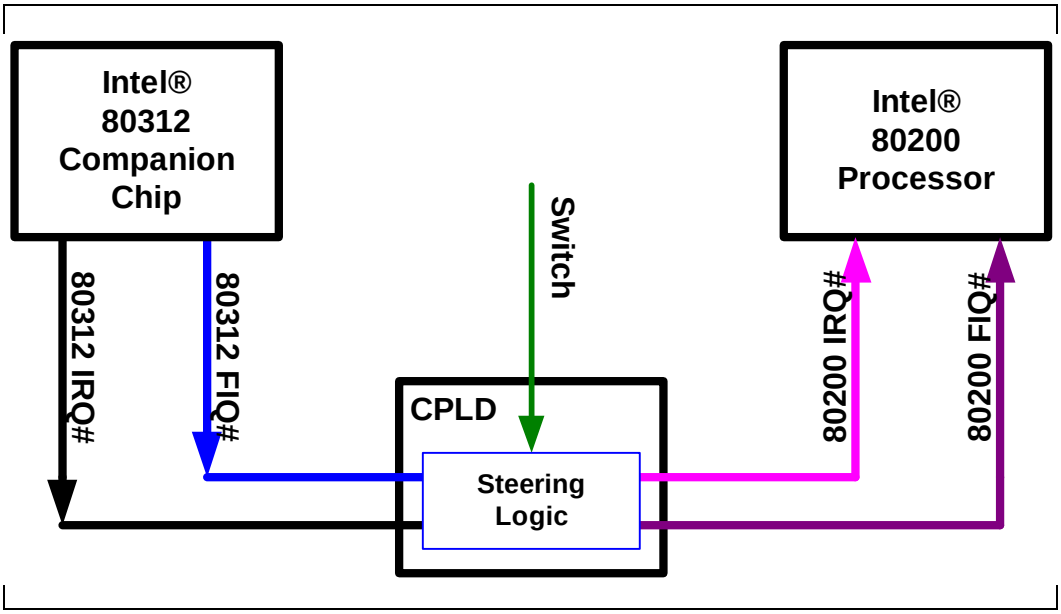
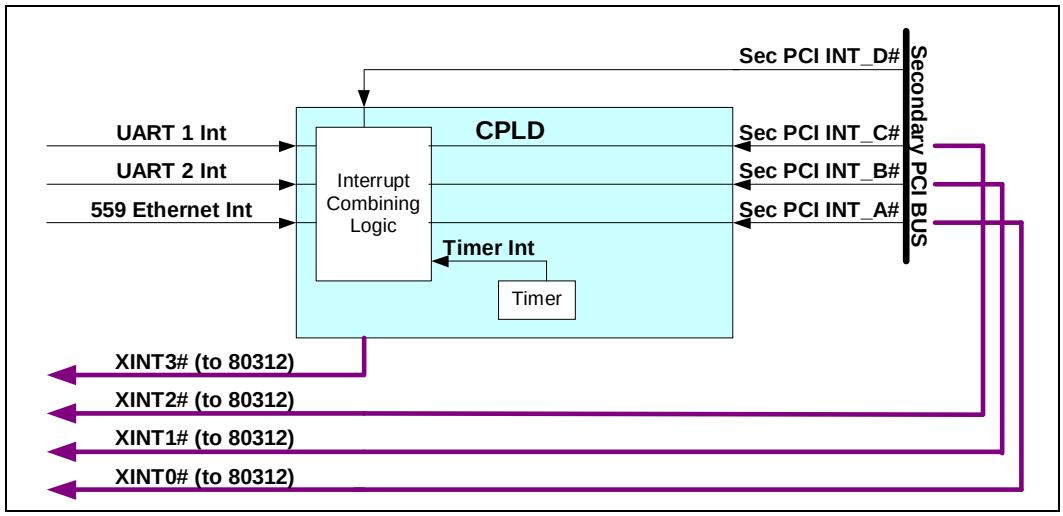


Figure 3. Interrupt Steering inside the CPLD on the Intel® IQ80310 Evaluation Platform



2.3 Interrupt Status Registers

The interrupt status registers, in the CPLD, are used to determine which external interrupt is generating an interrupt. The definition of these registers is shown in Table 2 and Table 3. These registers are checked to determine which device(s) is causing the interrupt. The appropriate interrupt handler(s) is called by the dispatcher. Figure 4 shows the interrupt routing of the status register inside the CPLD.

Table 2. Interrupt Status Register 0, 0xFE820000 (read only)

Bit #	Interrupt Source
BIT 0	External Timer Interrupt
BIT 1	I82559 Ethernet Interrupt
BIT 2	UART1 Interrupt
BIT 3	UART2 Interrupt
BIT 4	Secondary PCI INTD

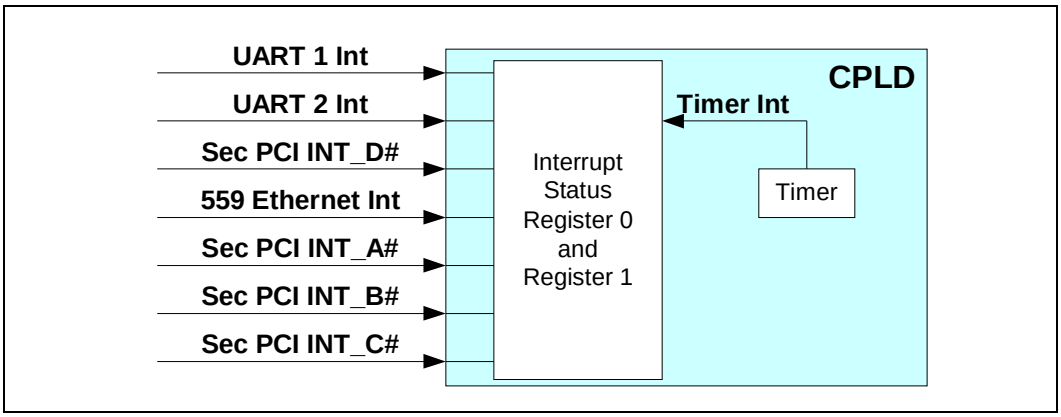
NOTES:
1. Read = 1, Interrupt Occurred.
2. Read = 0, No interrupt (Default State).

Table 3. Interrupt Status Register 1, 0xFE850000 (read only)

Bit #	Interrupt Source
BIT 0	SPCI INTA
BIT 1	SPCI INTB
BIT 2	SPCI INTC

NOTE: Read = 0, No interrupt (Default State).

Figure 4. Interrupt Status Register Inside the CPLD



2.4 Interrupt Mask Register

The interrupt mask register is used to turn off or on individual external interrupts. Table 4 shows the definition for the interrupt mask register.

Table 4. Interrupt Mask Register, 0xFE860000

BIT #	INTERRUPT SOURCE
BIT 0	External Timer Interrupt
BIT 1	I82559 Ethernet Interrupt
BIT 2	UART1 Interrupt
BIT 3	UART2 Interrupt
BIT 4	PCI INTD

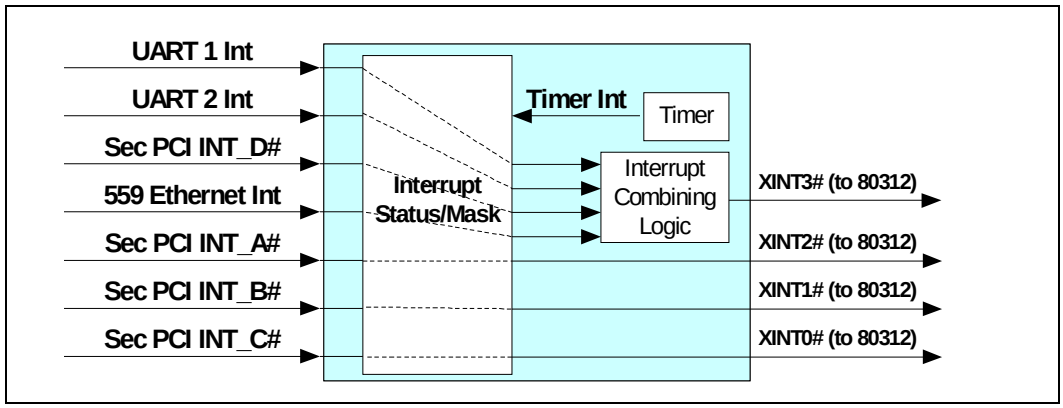
NOTE: Read = 1, Interrupt is MASKED = Disable (Default State)
Write = 1, MASK interrupt

2.5 Other Possible Interrupt Handling Options

Other possible interrupt options could include the addition of the PCI INTA, INTB and INTC to be included in the Interrupt status/mask register shown in Figure 5 as well as the Interrupt steering inside the CPLD. These other possible interrupt handling options are not part of the CPLD source code being supplied at:

http://developer.intel.com/design/iio/docs/dvtl_iq80310.htm

Figure 5. Example Interrupt Status/Mask Register Using the CPLD



3.0 Implementing Interrupt Status and Mask Register without a CPLD

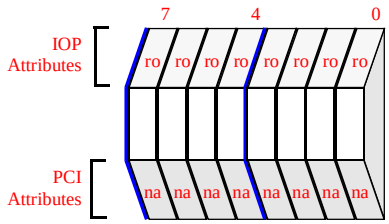
3.1 General Purpose Input Output Support

Eight pins are provided on the 80312 as General Purpose Input Output (GPIO) pins. The eight pins are GPIO[7:0]. These pins can be used by the 80200 to control or monitor external devices in the I/O subsystem.

3.1.1 General Purpose Inputs

The current state of the eight GPIO pins can be read by software and acted upon accordingly. The data contained in this register reflects the current state of the pin. Table 5 shows the configuration of the register. The GPIO data register is initialized to 00H upon assertion of **P_RST#.**

Table 5. GPIO Input Data Register - GPID



Intel® 80200 Processor Local Bus Address
0000 1720H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
07	0_2	GPIO7 Input Data -- This bit reflects the state of the **GPIO[7]** pin following the deassertion of **P_RST#**.
06	0_2	GPIO6 Input Data -- This bit reflects the state of the **GPIO[6]** pin following the deassertion of **P_RST#**.
05	0_2	GPIO5 Input Data -- This bit reflects the state of the **GPIO[5]** pin following the deassertion of **P_RST#**.
04	0_2	GPIO4 Input Data -- This bit reflects the state of the **GPIO[4]** pin following the deassertion of **P_RST#**.
03	0_2	GPIO3 Input Data -- This bit reflects the state of the **GPIO[3]** pin following the deassertion of **P_RST#**.
02	0_2	GPIO2 Input Data -- This bit reflects the state of the **GPIO[2]** pin following the deassertion of **P_RST#**.
01	0_2	GPIO1 Input Data -- This bit reflects the state of the **GPIO[1]** pin following the deassertion of **P_RST#**.
00	0_2	GPIO0 Input Data -- This bit reflects the state of the **GPIO[0]** pin following the deassertion of **P_RST#**.

3.2 Routing Interrupts to GPIO Port of Intel® 80312 I/O Companion Chip

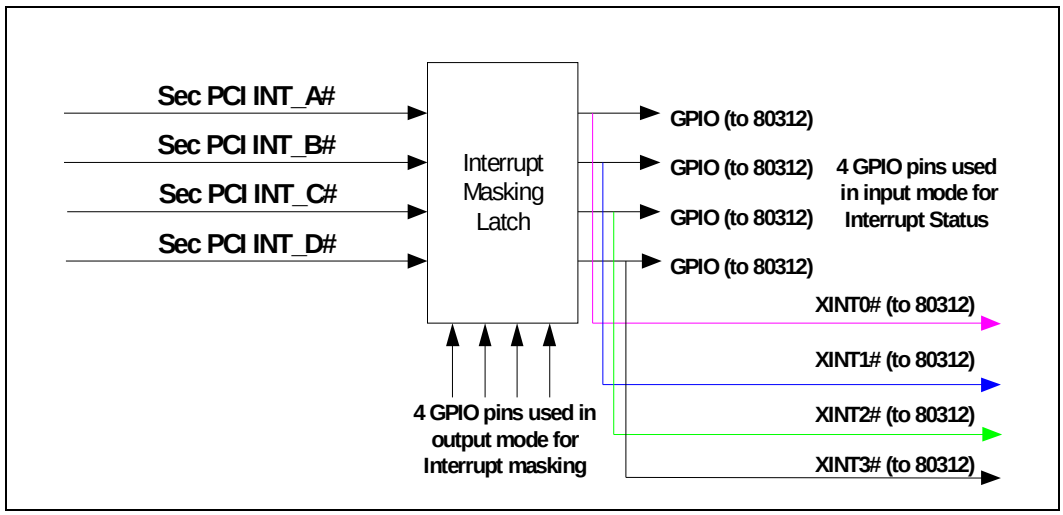
3.2.1 Possible Interrupt Routing Options for GPIO

Figure 6 shows a possible way to route the interrupt sources to the 80312.

The 80312 has four possible sources for external interrupts. These four interrupt sources can be routed in parallel to the GPIO port to monitor interrupt status and the remaining four GPIO ports can be used as outputs for interrupt masking, Figure 6 shows how to make these connections. Since there are four interrupt sources, using the GPIO port for interrupt status and mask will consume all eight pins of the GPIO port.

Further information on configuring the GPIO port as outputs can be found in the *Intel® 80312 I/O Companion Chip Developer's Manual*, order number 273410.

Figure 6. Interrupt Routing using the GPIO Port



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