

Power Management Features on the Embedded Ultra Low-Power Intel486™ Processor

by Samar Al-Khairi
APCD Design Engineering

Abstract

Power management features are becoming essential in the embedded market segment. The ultra low-power Intel486™ embedded processor contains all the power saving features offered by the Intel486 SL enhanced processors plus additional ones. These power saving features include SMM mode, Stop Clock mode, Auto Halt Power down mode, and enhanced auto clock freeze mode. The enhanced auto clock freeze control are completely transparent to external chip set and are designed to not affect CPU operation in any way. Auto clock freeze consists of two parts: Global clock freeze (clock throttle) control and local clock freeze control. This paper discusses all the power saving features offered by the ultra low-power embedded Intel486 processor with emphasis on the auto freeze features providing timing diagrams and illustrations when applicable.

Introduction

With the push towards low power applications, power consumption has become an important consideration in the design of embedded processors. As the complexity of processors and the target frequency grows, power management features start to play an important role. Low power is essential for embedded applications since battery life is directly related to the power consumed. The Intel486 embedded processor offers aggressive power saving techniques to dynamically manage the power consumption on the chip. These techniques can be classified into two major categories: macro level software and system controlled power management methods and micro level dynamic software and system transparent methods.

In the first category, the embedded Intel486 processor provides software and hardware controllability to the operating system and system hardware allowing them to power down the processor when needed. One of the means by which this is achieved is by a hardware interrupt pin, STPCLK#, that allows system hardware to control the power consumption of the processor by adjusting the CLK input in a controlled sequence. Another way of achieving the low power state is by executing the HALT instruction. Upon execution of HALT, the processor will automatically enter a low power state called auto halt powerdown state. In the second category, the embedded Intel486 processor provides dynamic local

power management features where idle parts of the processor shut down their clocks to save power. For example the Kcache Unit freezes the clocks if the processor determines that no cache access cycle will run.

Enhanced Auto Clock Freeze Mode

The Auto Clock freeze feature on the embedded Intel486 processor consists of two parts: local clock freeze control and global clock freeze control. Local clock freeze controls the clocks used by the local unit (Bunit, Cunit,..) while global clock freeze "Clock Throttle" controls the global clock distribution ph1 and ph2. The Auto clock freeze control features are designed not to decline the processor performance and are completely transparent to the external system.

Figure 1 shows the clock distribution on the embedded Intel486 processor. The global clock freeze is controlled by circuitry within the clock unit. The circuitry checks for several internal pipeline status and based on that it gates the clock output from the clock generator unit. If the internal pipeline is not empty or not stalled then the clocks are not frozen. During memory or I/O wait cycles, HOLD/HLDA cycles, AHOLD cycles and BOFF# cycles, the clocks are frozen out of the clock unit causing significant power savings. The freeze break conditions such as RDY#, INTR, or BOFF# will restart the clocks when asserted. The total power to consumption that can be saved from the global clock freeze feature is on the order of 10mA at 3.3V 33 MHz.

Local clock freeze relies on control signals within the embedded processor to indicate the clocks to a particular block can be frozen. These control signals gate the clocks to the local units and once activated the clocks to the local blocks are frozen causing significant power savings. The total power consumption that can be saved from the local clock freeze is on the order of 25mA at 3.3V 33 MHz.

STPCLK# and Auto Halt Powerdown

The Intel486 embedded processor implements software and system power management strategies in the form of STPCLK# pin and HALT instruction. The STPCLK# is implemented as a low priority level interrupt. Upon recognition of the interrupt, the embedded processor executes a microcode sequence which stops execution on the next instruction boundary, stops the prefetch unit, empties all the internal pipelines and write buffers, generates a Stop Grant bus cycle, and stops the internal clock. The processor will

acknowledge the Stop Grant state when RDY# or BRDY# has been returned active. During the Stop Grant state the processor power consumption drops to 15-25 ma (depending on the CLK input frequency). If the CLK input is completely stopped, the processors enters into the Stop Clock state where the power consumption drops to 35-45 ua.

Power management using the HALT instruction is essentially similar to the Stop Clock mechanism. Upon the execution of the HALT instruction, the processor will automatically enter a low power state called Auto Halt

Powerdown State. The processor will issue a normal HALT bus cycle when entering this state. The system can generate a STPCLK# while the processor is in the Auto Halt powerdown state. If this occurs, the processor will generate a Stop Grant bus cycle and enter the Stop Grant State from the Auto Halt Powerdown state. Upon de-asserting STPCLK# the processor returns to the Auto Halt powerdown state. Figure 1 illustrates the state transitions between Stop Clock and Auto Halt Power down states.

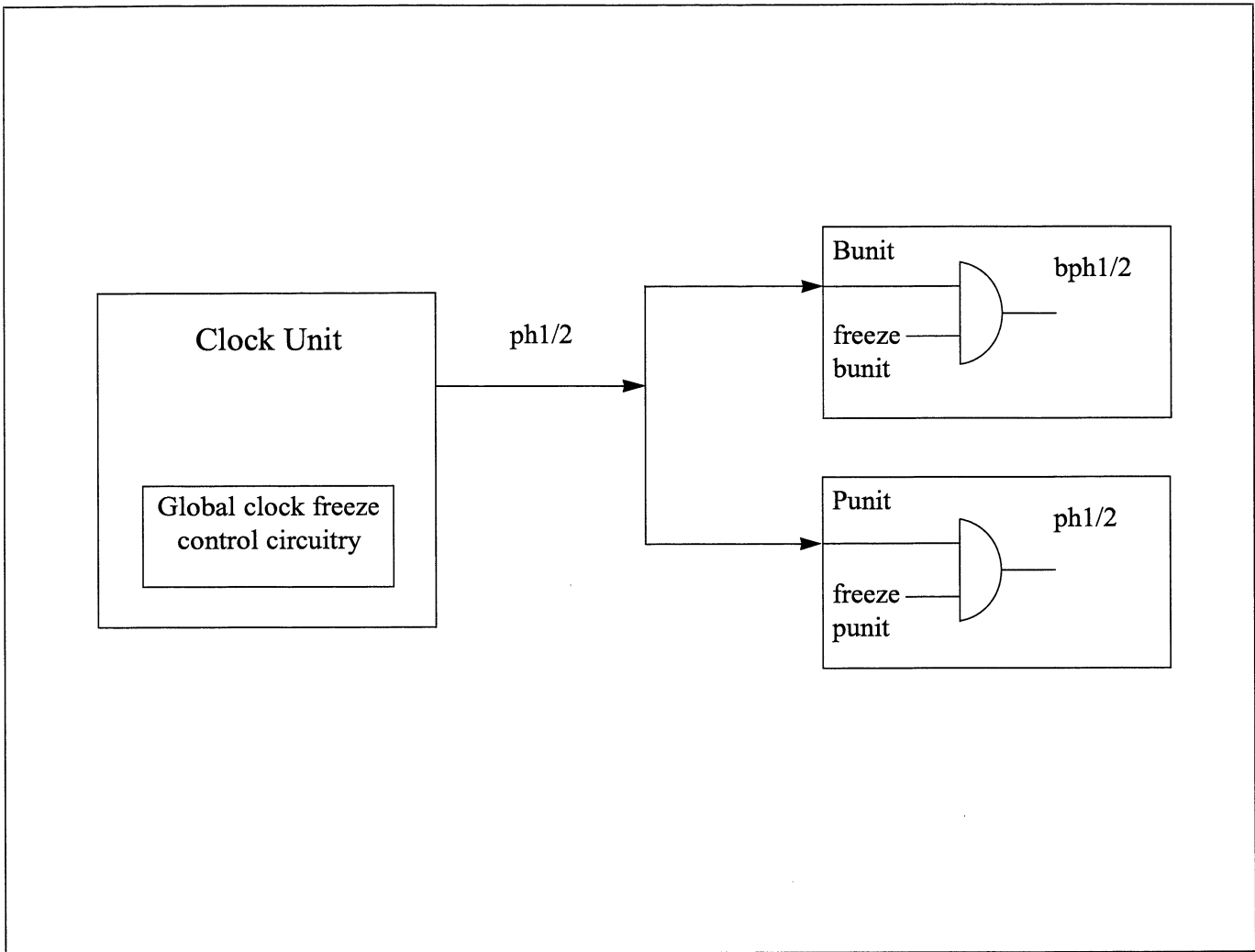


Figure 1. Clock Distribution Diagram

System Management Mode (SMM)

This mode is composed of a special purpose interrupt (SMI#) that serves as the hardware interface and a secure memory address space that stores processor status and SMI handlers. The SMI handlers are special software routines that perform various system management functions including system power control. When SMI# is asserted the Intel486 embedded processor will respond to the interrupt

by asserting SMIACT#. The processor then saves its state into SMRAM area and will start executing the SMI handlers. The last instruction in an SMI handler is RSM instruction which will restore the processor state from SMRAM, de-assert SMIACT#, and return control to the interrupted program. The processor is the most active component in a system. Therefore, clock control in SMM mode allows saving a lot of processor power.

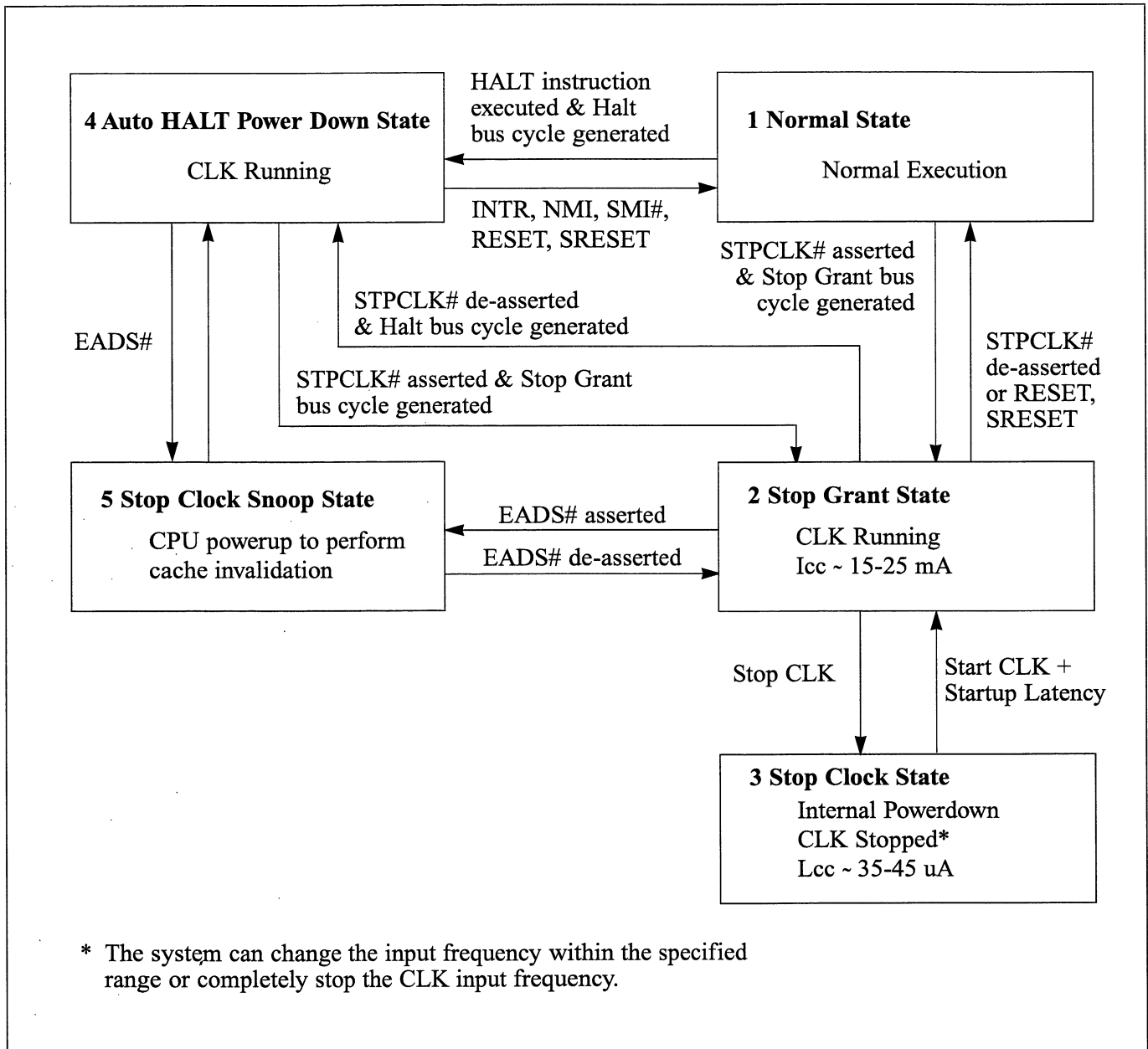


Figure 2. Intel486™ Processor Stop Clock State Diagram

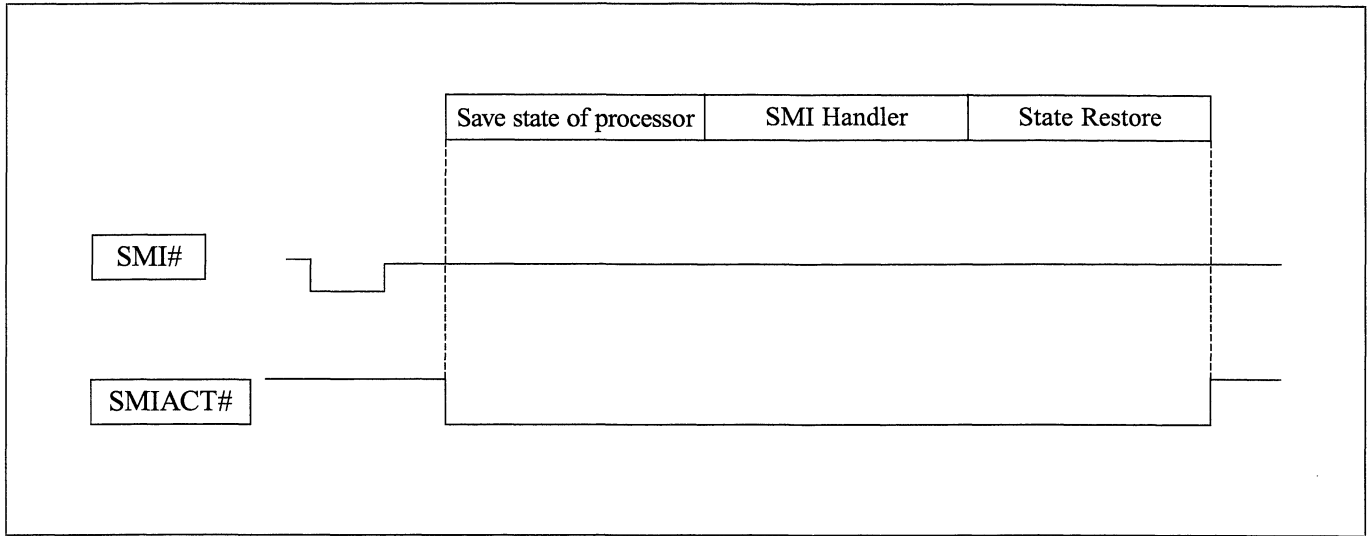


Figure 3. Basic SMI# Interrupt Service

Conclusion

As technology advances and faster processor operation is required, efficient power management techniques become crucial for meeting low-power high speed computing demands. Power management has to be done at both the system level and the processor level. The Intel486 embedded processor implements aggressive techniques for

achieving this goal. The operating system and system hardware are provided with hooks to allow them to control the power activity of the processor. In addition, the auto clock freeze feature allows significant power savings without significant degradation to the processor performance.

References

1. Intel486™ Microprocessors and Related Products, Intel Corporation, Santa Clara, California, 1995.
2. P24D Processor External Design Specification, Intel Corporation, 1994.
3. Embedded Ultra Low-Power Intel486™ SX Processor EDS, Intel Corporation, 1995.
4. Desmond Yuen, "Intel's SL Architecture", McGraw-Hill series, 1993.
5. Masaru Ishigami, "Pentium® Processor Design Consideration for Mobile Systems", Intel Corporation, 1994.

Intel Reference Numbers

World Wide Web Address:	http://www.intel.com
FaxBack System:	1 (800) 525-3019 or (503) 264-6835
Application Bulletin Board System:	1 (503) 264-7999
Intel Literature Center:	1 (800) 548-4725 7 a.m. to 7 p.m. CST
Retail PC and Network Products:	1 (800) 538-3373 or (503) 629-7000 7 a.m. to 7 p.m. PST
General Information Hotline:	1 (800) 628-8686 & (916) 356-3104 5 a.m. to 5 p.m. PST

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supercedes previously published specifications on these devices from Intel. *Other brands and names are the property of their respective owners. ©Intel Corporation 1996

UNITED STATES	JAPAN	FRANCE	UNITED KINGDOM	GERMANY	HONG KONG	CANADA
Intel Corporation 2200 Mission College Blvd. Santa Clara, CA 95052-8119	Intel Japan, K.K. 5-6 Tokodai, Tsukuba-shi Ibaraki-ken, 300-26	Intel Corporation S.A.R.L. 1, Quai De Grenelle, BP543 75725 Paris Cedex	Intel Corporation (U.K.) Ltd. Pipers Way Swindon SN3 1RJ Wiltshire, England	Intel GmbH Dornacher Strasse 1 D-85622 Felkirchen Muenchen	Intel Semiconductor Ltd. 32/F Two Pacific Place 88 Queensway, Central	Intel Semiconductor of Canada, Ltd. 190 Attwell Drive, Suite 500 Rexdale, Ontario M9W 6H8