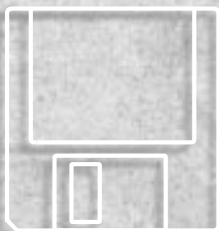


Ultra-Low Power Intel486™ SX Processor Evaluation Board Manual

**K E E P I N G
Y O U O N E
D E S I G N
A H E A D**



February, 1996
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Ultra-Low Power Intel486™ SX Processor Evaluation Board Manual

February 1996

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CHAPTER 1
ABOUT THIS MANUAL

1.1	CONTENT OVERVIEW	1-1
1.2	NOTATION CONVENTIONS	1-2
1.3	RELATED DOCUMENTS	1-3
1.4	ELECTRONIC SUPPORT SYSTEMS	1-4
1.4.1	FaxBack Service	1-4
1.4.2	Bulletin Board System (BBS)	1-4
1.4.3	CompuServe Forums	1-4
1.4.4	World Wide Web	1-4
1.5	TECHNICAL SUPPORT	1-5

CHAPTER 2
GETTING STARTED

2.1	OVERVIEW	2-1
2.2	BEFORE YOU BEGIN	2-4
2.3	SETTING UP THE BOARD	2-4
2.4	CONFIGURING THE BIOS	2-8
2.4.1	Using an IDE Hard Disk Drive	2-8
2.4.2	Using a Floppy Drive	2-9
2.4.3	Using the Resident Flash Array or a PC Card	2-10
2.4.3.1	Formatting After Booting from a Floppy Drive	2-10
2.4.3.2	Formatting After Booting from an IDE Hard Disk Drive	2-12
2.5	CHANGING THE DEFAULT VGA DRIVERS	2-14
2.6	PROGRAMMING FLASH MEMORY	2-14

CHAPTER 3
THEORY OF OPERATION

3.1	BLOCK DIAGRAM	3-1
3.2	ULTRA-LOW POWER Intel486™ SX PROCESSOR CIRCUITRY	3-2
3.2.1	Measuring Processor Current	3-2
3.2.2	In-circuit Emulator Connectors	3-2
3.3	MISCELLANEOUS POWER SIGNALS	3-3
3.4	PICOPOWER CHIPSET REGISTERS AND OPTIONS	3-3
3.4.1	Clock and Reset Interface Signals	3-4
3.4.2	Bus Control Interface	3-4
3.4.3	Power Management Features of the PicoPower Chipset	3-4
3.5	MEMORY	3-5
3.5.1	DRAM SIMM	3-6
3.5.2	Flash SIMM	3-6
3.5.2.1	DRAM Socket Address Scheme	3-7
3.5.2.2	Flash SIMM Address Scheme	3-7
3.5.3	Resident Flash Array (RFA)	3-8

3.5.4	Flash Boot Device	3-10
3.5.5	Cyber Quest Flash Loader Utilities	3-10
3.6	VIDEO CONTROLLER	3-13
3.7	SERIAL PORTS (COM1, COM2)	3-13
3.8	PARALLEL PORT	3-15
3.9	INFRARED PORT	3-16
3.10	PCMCIA CONTROLLER	3-16
3.11	MOUSE/KEYBOARD CONTROLLER	3-17
3.12	IDE CONTROLLER	3-18
3.13	PORT80H OUTPUT DISPLAY	3-18
3.14	POWER SUPPLY SUPPORT	3-19
3.14.1	Real-Time Clock Battery	3-19
3.15	SPEAKER	3-19
3.16	RESET CIRCUITRY	3-20

CHAPTER 4

HARDWARE REFERENCE

4.1	SPECIFICATIONS	4-1
4.2	JUMPERS	4-1
4.2.1	JP1: Flat-Panel Select Jumpers	4-3
4.2.2	JP3: HBBF Jumper	4-4
4.2.3	JP4 & JP8: Setting Processor Core Voltage Jumpers	4-5
4.2.4	JP5: Clock Speed Jumpers	4-6
4.2.5	JP6: Force Update Jumper	4-7
4.2.6	JP7: 5 V Power Jumper	4-7
4.2.7	JP9: Power Supply Jumper	4-7
4.2.8	JP10: Flash Boot Device (FBD) Control Jumper	4-7
4.2.9	JP11: 12 V Power Jumper	4-8
4.3	CONNECTORS	4-9
4.3.1	J1-J4: 40-pin ICE Headers	4-9
4.3.2	J5: Misc Header	4-13
4.3.3	J6: LCD Connector Header	4-14
4.3.4	J7: Portable Power Connector	4-15
4.3.5	J8: IDE Connector	4-16
4.3.6	J9: PC Power Connector	4-17
4.3.7	J10: 26-pin LPT1 Header	4-18
4.3.8	J11: Infrared Header	4-19
4.3.9	VGA Connector	4-20
4.3.10	P1: PCMCIA Connector	4-21
4.3.11	P2: Keyboard	4-22
4.3.12	P3: Mouse	4-22
4.3.13	COM1	4-23
4.3.14	COM2	4-24

4.3.15	AT-bus Connector Pinouts	4-25
4.4	CHIPSET REFERENCE	4-27
4.4.1	Memory Map	4-27
4.4.2	PicoPower Chipset Register Decodes	4-28
4.4.2.1	Keyboard and Mouse Controller	4-28
4.4.2.2	Serial Port 1 (COM1:)	4-29
4.4.2.3	Serial Port 2 (COM2:)	4-29
4.4.2.4	Parallel Port (LPT1:)	4-30
4.4.2.5	IDE Hard Disk Drive	4-30
4.4.2.6	VGA/LCD Controller Cirrus Logic* CL-GD6245	4-31
4.4.2.7	PCMCIA Controller (CL-PD6710)	4-31
4.4.3	IRQ map	4-32
4.4.4	DMA Channels	4-33
4.5	SCHEMATICS	4-34

CHAPTER 5
BIOS SOFTWARE REFERENCE

5.1	POWER-ON SCREEN DISPLAY	5-1
5.2	BIOS SETUP SCREENS	5-1
5.3	BIOS SETUP MAIN MENU	5-3
5.3.1	System Time:/System Date	5-3
5.3.2	Diskette A/Diskette B	5-3
5.3.3	IDE Adapter 0 Master/Slave Sub-Menus	5-4
5.3.4	Video System	5-4
5.3.5	Boot Options Sub-Menu	5-4
5.3.6	Keyboard Features (Numlock) Sub-Menu	5-4
5.3.7	IDE Adapter Sub-Menus	5-4
5.3.7.1	Autotype Fixed Disk	5-5
5.3.7.2	Type	5-5
5.3.7.3	LBA Mode Control	5-6
5.3.8	Memory Shadow Sub-Menu	5-6
5.3.8.1	Using Shadow Memory Regions	5-6
5.3.9	Boot Options Sub-menu	5-7
5.3.9.1	Boot Sequence	5-7
5.3.9.2	SETUP Prompt	5-8
5.3.9.3	POST Errors	5-8
5.3.9.4	Floppy Check	5-8
5.3.9.5	Summary Screen	5-8
5.3.10	Keyboard Features Sub-menu	5-9
5.3.10.1	Numlock	5-9
5.3.10.2	Key Click	5-9
5.3.10.3	Keyboard Auto-Repeat Rate	5-9
5.3.10.4	Keyboard Auto-Repeat Delay	5-9
5.4	BIOS SETUP ADVANCED MENU	5-10
5.4.1	Integrated Peripherals Sub-Menu	5-10

- 5.4.2 Large Disk Access Mode5-10
- 5.4.3 BIOS Boot Medium5-11
- 5.4.4 Built-in BIOS Extension Configuration5-11
 - 5.4.4.1 M-Systems TFFS BIOS Base Address5-11
- 5.4.5 Integrated Peripherals Sub-Menu5-12
 - 5.4.5.1 COM Port/COM Port5-12
 - 5.4.5.2 LPT Port5-12
 - 5.4.5.3 LPT Mode5-13
 - 5.4.5.4 Diskette Controller5-13
 - 5.4.5.5 IDE Controller5-13
 - 5.4.5.6 UART2 Mode5-13
- 5.5 BIOS SETUP EXIT MENU 5-14
 - 5.5.1 Save Values & Exit5-14
 - 5.5.2 Discard Values & Exit5-14
 - 5.5.3 Get Default Values5-14
 - 5.5.4 Load Previous Values5-15
 - 5.5.5 Save Current Values5-15

CHAPTER 6

INSTALLING VGA DRIVERS AND UTILITIES

- 6.1 DISPLAY DRIVERS AND UTILITIES SOFTWARE 6-1
 - 6.1.1 Before You Begin6-1
 - 6.1.2 Contacting Cirrus Logic6-1
- 6.2 DOS INSTALLATION 6-2
- 6.3 CLMODE 6-3
 - 6.3.1 Using CLMode's Menu-driven Interface6-3
 - 6.3.2 Configuring the Attached Monitor6-3
 - 6.3.3 Using CLMODE's Command Line Options6-4
 - 6.3.4 Other Utilities6-5
- 6.4 WINDOWS INSTALLATION 6-6
- 6.5 WINMODE 6-6
- 6.6 WINDOWS DISPLAY DRIVERS 6-8
 - 6.6.1 Before Upgrading From a Previous Release6-8
 - 6.6.2 Installing Windows 3.1 Display Drivers6-9
- 6.7 WINDOWS 95 AND OTHER OPERATING SYSTEMS 6-10

CHAPTER 7

USING FLASH DISKS

- 7.1 AN OVERVIEW OF TRUEFFS 7-1
 - 7.1.1 What if there is no drive letter?7-2
- 7.2 USING TFFS 7-3
 - 7.2.1 Installing the TFFS Driver Software7-3
 - 7.2.2 Formatting the RFA or PC Card7-4
 - 7.2.3 Booting From the RFA or PC Card7-4

CHAPTER 8
PROGRAMMING FLASH MEMORY

8.1	USING THE FLASHLDR UTILITY	8-1
8.1.1	Before You Begin	8-2
8.1.2	Installation on the Host PC	8-2
8.1.2.1	Host Setup	8-2
8.1.2.2	Evaluation Board Setup	8-3
8.1.3	Running the Confidence Test Program	8-3
8.1.4	Entering FLASHLDR Commands	8-5
8.1.4.1	Using Flash Command Files (.FLC)	8-6
8.1.4.2	Flash Programming Utility Command Summary	8-7
8.1.4.3	Flash Programming Utility Options Summary	8-8
8.1.4.4	Loading a Program	8-10
8.1.4.5	Loading a Program to Execute at System Start-up	8-11
8.1.4.6	Executing a User Loaded Program or Target Program at System Startup	8-11
8.1.5	LED Diagnostic Codes	8-12
8.1.5.1	Updating the BIOS	8-13
8.1.6	Support	8-13
8.2	SELF-HOSTED REFLASHING	8-14
8.2.1	Installation	8-14
8.2.2	Before You Begin	8-14
8.2.3	Operation	8-15
8.2.3.1	Examples	8-15

CHAPTER 9
USING POWER MANAGEMENT

9.1	INTRODUCTION	9-1
9.2	INSTALLATION	9-1
9.3	POWER MANAGEMENT MODES	9-2
9.3.1	Conserve Mode	9-2
9.3.2	Doze Mode	9-2
9.3.3	Sleep Mode	9-2
9.3.4	Primary Events	9-2
9.3.5	Secondary Activity Events	9-3
9.4	COMMAND LINE OPTIONS	9-4
9.5	CONSERVE MODE OPTIONS	9-5
9.6	DOZE MODE OPTIONS	9-6
9.7	SLEEP MODE OPTIONS	9-7
9.8	PRIMARY EVENT OPTIONS	9-8
9.9	SECONDARY EVENT OPTIONS	9-9
9.10	DOS-PM MISCELLANEOUS OPTIONS	9-10



APPENDIX A

ERROR MESSAGES

A.1 INTRODUCTION A-1

A.2 COMMON ERROR MESSAGES A-1

 A.2.1 BIOS Error Messages A-1

 A.2.2 MS-DOS Operating System Error Messages A-4

APPENDIX B

PORTABLE POWER SUPPLY

B.1 INTRODUCTION B-1

B.2 AC INPUT B-1

B.3 HIGH VOLTAGE DC B-1

B.4 BATTERY CHARGE/CONTROL CIRCUIT B-1

B.5 +5 V B-2

B.6 +3.3 V B-2

APPENDIX C

FLAT-PANEL DISPLAY

C.1 CONNECTOR CABLING C-1

 C.1.1 LM64C08P Dual Scan Color STN Cabling C-2

 C.1.2 LM64P80 Dual Scan Monochrome C-3

 C.1.3 LQ9DO21 Color TFT C-4

FIGURES

Figure	Page
2-1 Ultra-Low Power Intel486™ Processor Evaluation Board Layout	2-3
3-1 Ultra-Low Power Intel486™ Processor Evaluation Board Functional Block Diagram	3-1
3-2 Page Control/Boot Block Register	3-9
3-3 Boot Block Flash Memory Selection	3-12
3-4 MISC Control Register	3-14
4-1 Location of Jumpers and Connectors	4-2
5-1 POST Display with Error	5-1
5-2 BIOS Setup Main Menu	5-3
5-3 IDE Adapter Sub-menu	5-5
5-4 Memory Shadow Sub-menu	5-6
5-5 Boot Options Sub-menu	5-7
5-6 Keyboard Features Sub-menu	5-9
5-7 Advanced Menu	5-10
5-8 Integrated Peripherals Sub-menu	5-12
5-9 Exit Menu	5-14
6-1 WinMode Screen Display	6-7
8-1 Flash Boot Device Memory Map	8-16
B-1 Portable Power Supply Block Diagram	B-3

TABLES

Table	Page
3-1	Chipset Clock and Reset Interface Signals 3-4
3-2	Power Saving Hardware Registers 3-5
3-3	Hardware Power Control Pins 3-5
3-4	RAS (10 Bit Column Address Mode) 3-7
3-5	CAS (10 Bit Column Address Mode) 3-7
3-6	RAS (10 Bit Column Address Mode) 3-7
3-7	CAS (10 Bit Column Address Mode) 3-7
3-8	Serial Port Control 3-15
3-9	LED Control 3-18
4-1	Environmental and Electrical Specifications 4-1
4-2	Jumper Summary 4-3
4-3	LCD Flat-Panel Jumper Selection 4-4
4-4	Processor Core Voltage Jumper Selection 4-5
4-5	CPU Frequency Jumper Selection 4-6
4-6	Processor Voltage Selections 4-6
4-7	ICE Header (J1) Pinout 4-9
4-8	ICE Header (J2) Pinout 4-10
4-9	ICE Header (J3) Pinout 4-11
4-10	ICE Header (J4) Pinout 4-12
4-11	Misc. Header (J5) Pinout 4-13
4-12	LCD Connector (J6) Pinout 4-14
4-13	Power Connector (J7) Pinout 4-15
4-14	IDE Connector (J8) Pinout 4-16
4-15	Power Connector (J9) Pinout 4-17
4-16	LPT1 Header (J10) Pinout 4-18
4-17	Infrared Header (J11) Pinout 4-19
4-18	VGA Connector (JP2) Pinout 4-20
4-19	PCMCIA Connector (P1) Pinout 4-21
4-20	Keyboard Connector (P2) Pinout 4-22
4-21	Mouse Connector (P3) Pinout 4-22
4-22	COM1 Connector (P5) Pinout 4-23
4-23	COM2 Connector (P4) Pinout 4-24
4-24	AT-bus Connector (G2) Pinout 4-25
4-25	AT-bus Connector (G1) Pinout 4-26
4-26	Memory Map 4-27
4-27	PicoPower Chipset Registers 4-28
4-28	Keyboard Controller 4-28
4-29	Serial I/O (COM1:) Port 4-29
4-30	Serial I/O (COM2:) Port 4-29
4-31	Parallel I/O (LPT1:) Port 4-30
4-32	IDE Hard Disk Drive 4-30
4-33	SVGA Controller 4-31
4-34	PCMCIA Controller Registers 4-31
4-35	Interrupt Map 4-32

TABLES

Table		Page
4-36	DMA Usage	4-33
4-37	Schematics	4-34
8-1	Flash Command File	8-6
8-2	Flash Loader Commands	8-7
8-3	FLASHCMD Options	8-9
8-4	Terms Used in FLASHCMD Commands	8-10
8-5	Flash Loader Status	8-12
C-1	Tested Flat Panel Displays	C-1
C-2	LM64C08P Dual Scan Color STN Cabling	C-2
C-3	LM64P80 Dual Scan Monochrome Cabling	C-3
C-4	LQ9DO21 Color TFT Cabling	C-4



1

About This Manual



This manual tells you how to set up and use the Ultra-Low Power Intel486™ Processor Evaluation Board.

1.1 CONTENT OVERVIEW

Chapter 1, About This Manual — Contains an overview of this manual.

Chapter 2, Getting Started — Provides complete instructions on how get to an operating system prompt by setting jumpers, providing power, connecting peripherals, mounting or installing the board, and configuring the BIOS.

Chapter 3, Theory of Operation — Provides information on the system design.

Chapter 4, Hardware Reference — Provides a description of jumper settings and functions, pinout information for each connector, and describes the chipset's registers, I/O map, IRQs, and DMA channels.

Chapter 5, BIOS Software Reference — Describes the BIOS setup options.

Chapter 6, Installing VGA Drivers and Utilities — Describes the VGA software supplied with the Ultra-Low Power Intel486 Processor Evaluation Board.

Chapter 7, Using Flash Disks — Describes how to format and use PCMCIA-compatible PC Cards and the Resident Flash Array (RFA).

Chapter 8, Programming Flash Memory — Describes how to use the Cyber Quest, Inc.* flash loader software to update the BIOS via a serial port connected to a host PC. This chapter also describes how to reflash the BIOS without using the serial port.

Chapter 9, Using Power Management — Describes the DOS utility that controls power management features.

Appendix A, Error Messages — Contains recovery information for setup and configuration errors.

Appendix B, Portable Power Supply — Provides complete reference design information for the battery charger power supply.

Appendix C, Flat-Panel Display — Describes flat panel displays tested to work with the evaluation board.

1.2 NOTATION CONVENTIONS

The following notation conventions are used in this manual.

#	Pound symbol (#) appended to a signal name indicates signal is active low.
<i>italics</i>	Italics identify variables and indicate new terms.
bold sans-serif	In text, identifies commands (instructions).
typewriter font	This font is used for code examples. All characters are equal width; this is useful for maintaining accurate character spacing.
UPPERCASE	In text, signal names are shown in uppercase. When several signals share a common name, each signal is represented by the signal name followed by a number; the group is represented by the signal name followed by a variable (<i>n</i>). In code examples, signal names are shown in the case required by the software development tool in use.

Designations for hexadecimal and binary numbers Hexadecimal numbers are represented by a string of hex digits followed by the letter *H*. A zero prefix is added to numbers that begin with *A* through *F*. (*FF* is shown as *OFFH*.) For binary numbers, the letter *B* may be appended for clarity.

Units of Measure	mA	milliamps, milliamperes
	A	amps, amperes
	Kbit, Kbyte	kilobits, kilobytes
	KΩ	kilo-ohms
	Mbit, Mbyte	megabits, megabytes
	KHz, MHz	kilohertz, megahertz
	ms	milliseconds
	μs	microseconds
	ns	nanoseconds
	μF	microfarads
	W	watts
V	volts	

NOTE:
Units listed are frequently used; other units and symbols are used as necessary.

1.3 RELATED DOCUMENTS

You can order Intel product literature from the following Intel literature centers.

1-800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

These documents that may help you understand and use your Ultra-Low Power Intel486 Processor Evaluation Board:

Intel Documents:

Intel486™ Processor Programmer's Reference Manual, order number 240486.

Embedded Ultra-Low Power Intel486™ SX Processor datasheet, order number 272731.

Flash Memory Products Data Manual, order number 210830.

Intel 82C42PE, Keyboard & Mouse Controller, Multikey/42 Version 1.1, May 12, 1993.

Intel UPI-C42, Universal Peripheral Interface CHMOS 8-Bit Slave Microcontroller datasheet, 1991.

Other documents:

Advanced Power Management (APM) BIOS Interface Specification, Revision 1.1, Intel and Microsoft, September 1993.

BIOScope Technical Reference, Version 1.0, 2/16/95.

Cirrus Logic CL-PD6710 PCMCIA Host Adapters Data Sheet*, Version 2.5, July 1994.

Cirrus Logic, CL-GD6245 Advanced Data Book, Version 1.1, September 1994.

Cirrus Logic, CL-GD624X, Applications Book, Revision 1.0, June 17, 1994.

NoteBIOS 4.0 Power Management System Developer's Reference, 6/6/95.

The PCMCIA Developer's Guide, Sycard Technology, 1994.

PhoenixBIOS™ 4.04 Developer's Reference, Phoenix Technologies, Ltd., Sept. 8, 1994.

PhoenixBIOS™ 4.0 Technical Reference, Phoenix Technologies, Ltd., March 15, 1994.

PicoPower Redwood Technical Reference Manual (PT86C768 & PT86C718), Databook Version 3.0P, July 8, 1994.

Standard Microsystems SMC FDC37C665IR, Super I/O Chip Data Sheet. Revision 11/2/94.

IEEE 1284 Extended Capabilities Port Protocol and ISA Standard.

1.4 ELECTRONIC SUPPORT SYSTEMS

Intel's FaxBack* service and application BBS provide up-to-date technical information. Intel also maintains forums on CompuServe* and offers a variety of information on the World Wide Web. These systems are available 24 hours a day, 7 days a week, providing technical information whenever you need it.

1.4.1 FaxBack Service

FaxBack is an on-demand publishing system that sends documents to your fax machine. You can get product announcements, change notifications, product literature, device characteristics, design recommendations, and quality and reliability information.

1-800-525-3019 (US or Canada)
+44-1793-432509 (Europe)
+65-256-5350 (Singapore)
+852-2-844-4448 (Hong Kong)
+886-2-514-0815 (Taiwan)
+822-767-2594 (Korea)
+61-2-975-3922 (Australia)
1-503-264-6835 (Worldwide)

1.4.2 Bulletin Board System (BBS)

The application BBS has software updates, hypertext manuals and datasheets, software drivers, firmware upgrades, code examples, application notes and utilities, and quality and reliability data.

To access the BBS, use a terminal program to dial the telephone number given below for your area; once you are connected, respond to the system prompts.

503-264-7999	U.S., Canada, Japan, Asia Pacific
44(0)1793-432955	Europe

1.4.3 CompuServe Forums

The CompuServe forums provide a means for you to gather information, share discoveries, and debate issues. Type "go intel" for access. For information about CompuServe access and service fees, call CompuServe at 1-800-848-8199 (U.S.) or 614-529-1340 (outside the U.S.).

1.4.4 World Wide Web

Intel offers a variety of information through the World Wide Web (<http://www.intel.com/>). Select "Embedded Design Products" from the Intel home page.

1.5 TECHNICAL SUPPORT

If you need help with your evaluation board, contact Intel's Embedded Computing Operation Help Line. The telephone number is 602-554-1172. The Help Line is open from 8:00 a.m. to 5:00 p.m., Mountain Standard time.

1

Follow these guidelines when calling to request support:

- Be ready to provide the serial number of your Ultra-Low Power Intel486 Processor Evaluation Board, the system and video BIOS name and version (if they are different from the factory installed versions), the version number of the FFS software, operating system and version, and peripheral configuration.
- Write down any error messages that you encountered.
- Be ready to attempt to duplicate the problem.
- If possible, make the call from near the area where you were working with the evaluation board.



2

Getting Started



This chapter identifies the Ultra-Low Power Intel486™ Processor Evaluation Board's key components, features and specifications. Step-by-step instructions tell you how to set up the evaluation board, and install the software needed for your configuration.

2.1 OVERVIEW

The evaluation board is an embedded-application development board, based on the Ultra-Low Power Intel486™ SX processor and the PicoPower* chipset. It is especially suited for low-power application development.

The Ultra-Low Power Intel486™ Processor Evaluation Board has these features:

- Meets stringent safety and low EMI standards (UL-1950)
- Provides connectors for in-circuit emulation (ICE)
- Has jumper selectable frequency and voltage options
 - Supports processor core voltages (V_{CC}) of 3.3 V, 2.7 V, and 2.4 V. The processor interface voltage (V_{CCP}) is always set at 3.3 V to interface correctly with other system components
 - Separate supply-voltage input for operating the processor core at a lower voltage
 - Supports operating frequencies from 4 MHz to 33 MHz.
- Uses PicoPower chipset (PT86C768 and PT86C718)
- Flash memory device with system software
 - System and video BIOS
 - BIOS setup utility
 - Flash file system software
 - Flash loader software

The system memory feature set includes:

- Supports up to 8 Mbyte of DRAM (4 Mbytes provided)
- Processor and memory devices do not use parity

The peripherals feature set includes:

- Power-control signals to turn off peripherals
- Intel FlashFile™ component, 1Mx8, E28F008SA (or equivalent) Resident Flash Array (RFA) with M-Systems* TrueFFS* software to configure it as a Resident Flash Disk (RFD)
- 512Kx8, 28F004-B Flash Boot Device (FBD) memory, containing the PhoenixBIOS*, LCD/VGA display BIOS, and Cyber Quest* flash loader
- Support for flash memory SIMM featuring Intel 28F016XD (or equivalent), 72-pin devices

User-accessible on-board connectors include:

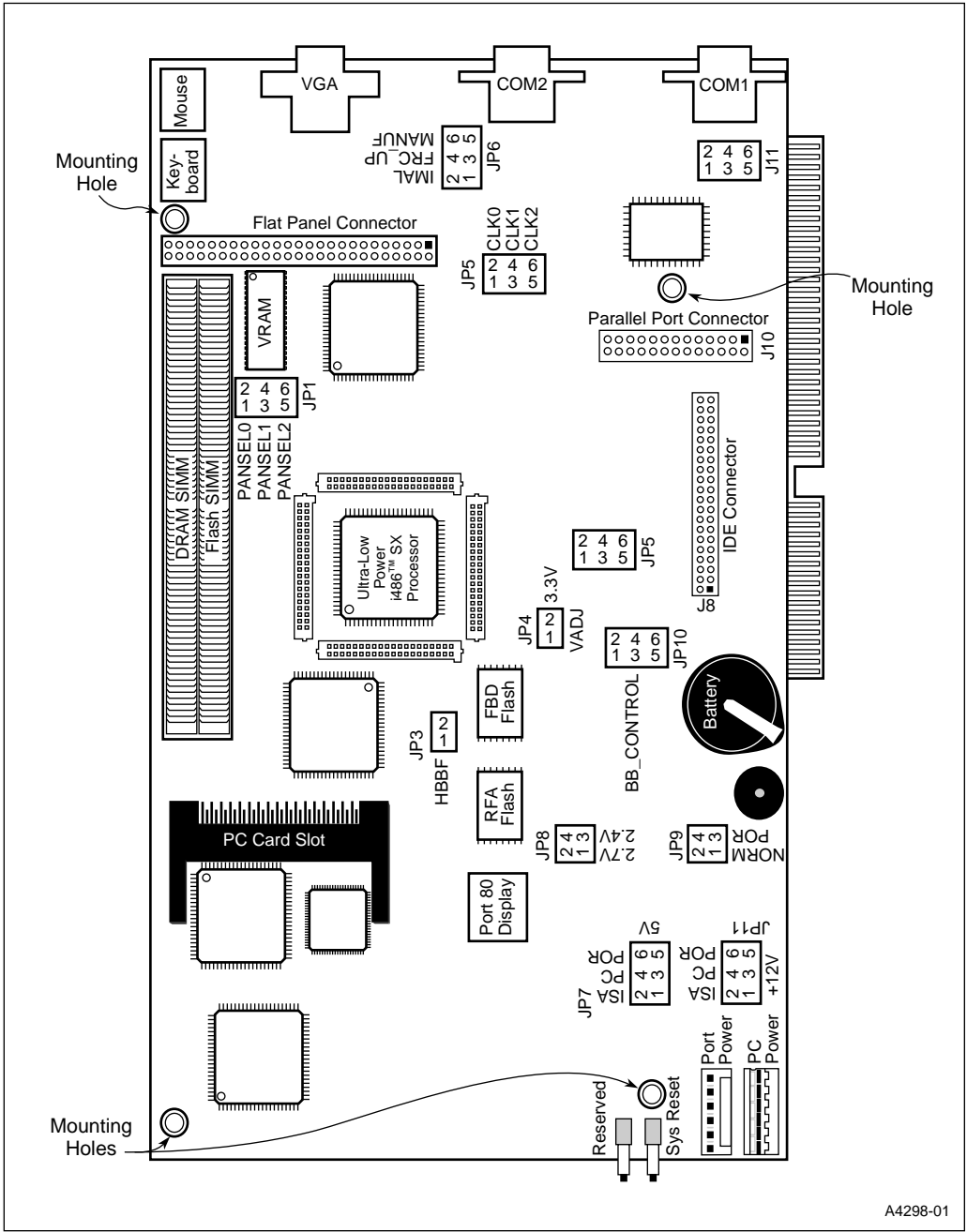
- Two serial RS-232 ports; COM1 is DCE and COM2 is DTE
- Infrared serial port shared with COM2 DTE Port. Infrared port is a 6-pin, 0.1" dual-in-line header
- One EPP/ECP parallel port accessed through a 0.1" dual-in-line header
- PCMCIA socket supporting one Type I or Type II PCMCIA card
- PS/2* keyboard and PS/2 mouse (6-pin mini-DIN)
- VGA display connector (15-pin HD DShell)
- LCD display connector (dual-in-line 2 mm header)
- ISA edge board connector
- Standard PC power supply connector (only +5 V and +12 V used)
- External power supply connector for battery operated portable power supply; portable power supply must provide +3.3 V, +5 V, +12 V

Miscellaneous features include:

- Super-VGA/flat-panel display controller on the Intel486™ SX processor local bus, with 512 Kbyte (DRAM) display memory.
- Reset push button, Resume/Suspend push button
- Stand-off feet for table-top operation

These software utilities and drivers are included in your kit:

- Cyber Quest flash loader utility
- M-Systems TrueFFS flash formatting software for RFA and PC Cards
- Cirrus Logic* VGA utilities and drivers
- Power management DOS driver software for Sleep, Doze and Suspend modes



A4298-01

Figure 2-1. Ultra-Low Power Intel486™ Processor Evaluation Board Layout

2.2 BEFORE YOU BEGIN

Before you set up and configure your evaluation board, you need to gather some additional hardware and software.

VGA Monitor	You can use any standard VGA or multi-resolution monitor or a flat-panel display. The setup instructions in this chapter assume that you are using a standard VGA monitor.
Power Supply	You can use a standard PC/AT power supply, a portable power supply or an ISA-bus, passive backplane to supply power.
Keyboard	You need a PS/2 keyboard to use the BIOS setup software.
Backplane	You can use an ISA-bus, passive backplane to mount the evaluation board. This is the recommended setup method.
Mouse	Optional. You can use a PS/2 mouse.
Storage Device	You must choose a storage device to load the operating system, or to load software onto another disk (including the Resident Flash Disk). You can use a preformatted and pre-loaded IDE hard disk drive, PC Card formatted with M-Systems TrueFFS* software, or floppy diskette. To use a floppy drive, you must use an ISA-bus, passive backplane, and a separate floppy controller card.
Host PC	Optional (required if you use the Cyber Quest flash loader software). You can transfer files from a host PC to the evaluation board. To transfer DOS files, you need DOS and a file transfer program on both the host PC and the evaluation board.

2.3 SETTING UP THE BOARD

Once you have gathered the hardware described in the last section, follow the steps below to set up your evaluation board. Refer to Figure 2-1 for jumper locations.

1. Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electro-static discharge damage; such damage may cause product failure or unpredictable operation.
2. Inspect the contents of your kit. Make sure that all items are included. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

CAUTION

Many of the connectors on the evaluation board provide power through non-standard pins. Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Use extreme caution when preparing to connect cables to this product.

3. Remove the jumper from pins 3 and 4 (VADJ) of JP4. Place a jumper on pins 1 and 2 (3.3 V) of JP4. See Figure 2-1 for jumper locations. This sets the processor core voltage to 3.3 V. Use this setting until you have verified that your evaluation board is set up properly. Instructions for changing this setting appear on page 4-5.
4. Make sure there is a jumper on pins 3 and 4 (CLK1) of JP5 (only). This sets the processor clock frequency to 33 MHz. Use this setting until you have verified that your evaluation board is set up properly. Instructions for changing this setting appear on page 4-6.
5. Select a power supply option (this step configures jumpers only, you connect the power cables later in the procedure):
 - **ISA-bus, passive backplane:** Remove the jumper from pins 3 and 4 (PC) of JP7 *and* JP11. Place a jumper on pins 1 and 2 (ISA) of JP7 *and* JP11. For common installations, *both* JP7 and JP11 should have the same setting. Do not mount your evaluation board in the backplane yet. This is the recommended method for installing the evaluation board.
 - **Standard PC power supply:** Make sure there is a jumper on pins 3 and 4 (PC) of JP7 *and* JP11. For common installations, *both* JP7 and JP11 should have the same setting.
 - **Portable Power Supply:** Move the jumper from pins 3 and 4 (PC) of JP7 *and* JP11 to pins 5 and 6 (POR) of JP7 *and* JP11. Move the jumper from Pins 1 and 2 (NORM) of JP9 to pins 3 and 4 (POR) of JP9.
6. Connect a VGA monitor to the 15-pin D-type connector labeled JP2.
7. Connect a PS/2 style keyboard (6-pin mini DIN connector) or compatible to P2. Make sure the power is OFF when you connect or disconnect the keyboard. Disconnecting the keyboard with the power on may destroy the port.
8. OPTIONAL - Connect a PS/2 mouse (6-pin mini DIN connector) or compatible to P3. Make sure the power is OFF when you connect or disconnect the mouse. Disconnecting the mouse with the power on may destroy the port.

9. Connect a storage device to the evaluation board:

You can use the storage device as a bootable disk, or as a means to transfer operating system or other software to a PC Card or to the resident flash array on the evaluation board. *Before* you install a hard disk or PC Card in the evaluation board, you must format the drive or card, and install the desired software onto the drive or card. (Instructions for using the evaluation board to format a PC Card begin on page 2-10.)

- IDE hard disk drive:
 - Connect the hard drive to a computer, and format the drive. Follow the instructions that came with the drive.
 - Install operating system files to the drive.
 - Turn off the power. Disconnect the drive from the computer.
 - Connect the hard drive's IDE connector to the J8 connector on the evaluation board. Pin 1 is next to the asterisk printed on the board.

CAUTION

Make sure the tracer on the ribbon cable aligns to pin 1 on both the hard disk and the header. Connecting the cable backwards can damage the evaluation board.

- Connect the hard drive to the power supply.
- You may have to make changes to the system BIOS to enable this hard disk.
- PC Card: Insert a pre-formatted, bootable PC Card into the PCMCIA slot (labeled P1). You must make changes to the system BIOS to enable this disk. This is explained later in this chapter.
- Floppy drive: A floppy drive connected to the evaluation board is the most direct method for loading software.
 - This option requires that you use an ISA bus passive backplane. You also need a floppy controller card and cables.
 - Install the floppy controller card in the backplane, and connect the floppy cable to J10 on the evaluation board.
 - Connect a power cable to the floppy drive.
 - To avoid conflicts, disable the hard drive port, parallel port(s) and COM port(s) on the floppy controller.
 - You have to make changes to the system BIOS to enable this floppy disk. This is explained later in this chapter.

10. Mount or install the evaluation board:
 - **ISA-bus, passive backplane:** Mechanically, the evaluation board conforms to all outline requirements of an ISA-bus add-in card. Use a passive backplane with no termination resistors; the evaluation board provides the termination for the passive ISA backplane.
 - Make sure system power is off. Do not insert the evaluation board into (or remove it from) a live backplane.
 - While supporting the backplane, firmly press the evaluation board down until it is seated in the backplane.
 - **Surface mount:** The evaluation board has four mounting holes. Be sure to mount the evaluation board in a location where you have access to all available header pins and connectors. Mounting holes on the evaluation board are 1/8" (0.125") in diameter, or 3.175 mm.
 - **Table-top Operation:** The evaluation board is shipped with four plastic standoff "feet" for use in a table-top environment. These feet are shipped in a plastic bag with eight screws. Install the feet so that the chip side of the board is showing.
11. Make sure the DRAM SIMM is installed in the socket labeled DRAM.
12. Connect the power supply:
 - **ISA-bus, passive backplane:**
 - For a backplane with a power connector: with the power supply turned off, connect the power supply cable (labeled P1 or P8) to the six-pin power header on your backplane.
 - For an unpowered backplane: with the power supply turned off, connect the power supply cable (labeled P1 or P8) to the six-pin power header (J9, labeled PC) on the evaluation board. Place a jumper on pins 1 and 2 (ISA) *and* 2 and 3 (PC) of jumpers JP7 and JP11. In this configuration, not all voltages supported on a standard bus are available.
 - **Standard PC power supply:** With the power supply turned off, connect the power supply cable (labeled P1 or P8) to the six-pin power header, (J9, labeled PC).
 - **Portable Power Supply:** With the portable power supply turned off, connect the power supply cable to the six-pin power header (J7, labeled PORT). Reference information for creating a portable power supply is located in Appendix B, "Portable Power Supply."
13. Depending on your configuration, you may have to enable certain options in the BIOS. This is described in the next section.

2.4 CONFIGURING THE BIOS

This section describes how to configure the BIOS for your drive configuration, and reach an operating system prompt. This section assumes that you have already followed the installation and configuration steps listed in the previous section.

The following sections provide step by step instructions for these three drive configuration options:

- IDE hard disk drive
- Floppy drive
- PC Card or Resident Flash Array (RFA)

2.4.1 Using an IDE Hard Disk Drive

1. Turn on the power to your evaluation board and peripherals. When prompted, press F2 to enter Setup.
2. In the Main menu, highlight Diskette A. Press the + key until Not Installed appears.
3. Highlight Diskette B. Press the + key until Not Installed appears.
4. Highlight IDE Adapter 0 Master and press Enter.
5. Highlight Autotype Fixed Disk and press Enter.

Existing (formatted) disks must use the same parameters that were used when the disk was originally formatted. Most disks have a factory-attached label which specifies cylinder, head, and sector information. Make sure the BIOS settings match these initial settings.

- For IDE disks which comply to ANSI specifications, BIOS reads the information (cylinder, head, and sector) from the new disk and sets the configuration accordingly.
- For IDE disks which do not comply with the ANSI specifications, use the Type field to manually enter device characteristics.

When an IDE drive is specified in the BIOS setup, it becomes the C: drive.

6. Press Esc to return to the Main menu.
7. Select Advanced from the options at the top of the screen.
8. From the Advanced menu, highlight BIOS Boot Medium option. Press the + key until IDE appears.
9. Highlight Integrated Peripherals and press Enter.
10. Highlight IDE Adapter. Press the + key until Enabled appears.
11. Press Esc.

12. Select Exit from the options at the top of the screen.
13. Highlight Save Changes and Exit and press Enter.
14. The system reboots with the new BIOS settings. The system performs a power on self test (POST). If errors occur during the POST, the BIOS displays the error on your monitor. If error messages appear on your monitor during the POST, refer to Appendix A, “Error Messages.”

2.4.2 Using a Floppy Drive

1. Turn on the power to your evaluation board and peripherals. When prompted, press F2 to enter Setup.
2. In the Main menu, highlight Diskette A. Press the + key until the correct type of floppy appears.
3. Highlight Diskette B. Press the + key until Not Installed appears.
4. Select Advanced from the options at the top of the screen.
5. From the Advanced menu, highlight BIOS Boot Medium option. Press the + key until IDE appears.
6. Select Integrated Peripherals and press Enter.
7. Highlight Diskette Controller. Press the + key until Disabled appears.
8. Press Esc.
9. From the Main menu, highlight Boot Options and press Enter.
10. Highlight Boot Sequence and press the + key until A: then C: appears.
11. Press Esc.
12. Insert a bootable system diskette in the floppy drive. (Steps 2 and 3 in the next section tell you how to create a bootable floppy.)
13. Select Exit from the options at the top of the screen.
14. Highlight Save Changes and Exit and press Enter.

The system reboots with the new BIOS settings. The system performs a power on self test (POST). If errors occur during the POST, the BIOS displays the error on your monitor. If error messages appear on your monitor during the POST, refer to Appendix A, “Error Messages.”

2.4.3 Using the Resident Flash Array or a PC Card

You can use the Resident Flash Array (RFA) or a PC Card as your boot drive and storage device. As with the IDE hard disk drive, you must first format an RFA or PC Card. Two methods for formatting an RFA or PC Card for the first time are described in this section:

- Formatting after booting from a floppy drive (requires a floppy drive attached to the evaluation board)
- Formatting after booting from an IDE hard disk drive

2.4.3.1 Formatting After Booting from a Floppy Drive

In order to use this method to format the RFA or PC Card for the *first* time, you need a floppy drive attached to the evaluation board. Follow the steps given earlier in this chapter to set up the floppy drive *before* you follow the steps below. If you cannot attach a floppy, use a hard disk as described in “Formatting After Booting from an IDE Hard Disk Drive” on page 2-12.

Your computer must have the same type of floppy drive as the one attached to the evaluation board. You will use this computer and drive to format a floppy diskette, and place DOS files and other program files onto this diskette.

1. Follow the steps in “Setting up the Board” on page 2-4 to set up the evaluation board in a backplane with a floppy drive and controller card.
2. At the *computer*, insert a diskette in the floppy drive and format it using the DOS FORMAT command. For example, **FORMAT A: /S** (where A: is the floppy drive).
3. Create or copy a CONFIG.SYS file on the floppy. You can use the sample file included on the M-Systems diskette (in the SS subdirectory). The file must contain the following commands.

FILES=30

BUFFERS=30

STACKS=9,256

DEVICE=A:\PCICSS.COM

DEVICE=A:\TFFS.COM /SIZE=8192

4. Copy to the floppy diskette the DOS files SYS.COM and LABEL.COM. From the M-Systems disk included in your evaluation board kit, copy TFFS.COM, TFORMAT.COM and PCICSS.COM (located in the SS subdirectory). Set this disk aside, you will need it again in a few minutes.
5. Turn on the power to the evaluation board. Press F2 to enter Setup.
6. In the Main menu, highlight Diskette A. Press the + key until the correct type of floppy appears.
7. Highlight IDE Adapter 0 Master. Press Enter.

8. Highlight Type and press the +key until (none) appears. Press Esc.
9. From the Advanced menu, highlight BIOS Extension Base Address. Press the + key until Not Installed appears. Press Esc.
10. Insert the bootable floppy you created into the floppy drive attached to the evaluation board, then select Exit from the options at the top of the screen.
11. Highlight Save Changes and Exit and press Enter.
12. The system reboots with the new BIOS settings. The RFA appears as the C: drive; a PC Card appears as the D: drive. If you are formatting a PC Card, insert it now.
13. Format the RFA or PC Card (or both) using the TFORMAT command. For example,
A:>TFORMAT C:
14. Use the DOS LABEL command to give volume names to the RFA and PC Card. For example,
A:>LABEL C: RFA
15. Delete the CONFIG.SYS file from the floppy. For example,
A:>DEL CONFIG.SYS
16. Turn off the power to the evaluation board, then turn it back on. Press F2 to enter Setup.
17. Select Advanced from the options at the top of the screen.
18. From the Advanced menu, highlight BIOS Extension Base Address. Press the + key until C800-CFFFH appears.
19. Select Exit from the options at the top of the screen.
20. Highlight Save Changes and Exit and press Enter. The system reboots with the new BIOS settings.
21. From the A: prompt, enter **SYS C:** to make the RFA a bootable disk, or enter **SYS D:** to make a PC Card bootable.
22. Turn off the power to the evaluation board, then turn it back on. Press F2 to enter Setup.
23. Select Advanced from the options at the top of the screen.
24. From the Advanced menu, highlight BIOS Boot Medium option. Press the + key until RFA (to boot from the RFA) or PCMCIA (to boot from a PC Card) appears.
25. From the Main menu, highlight Diskette A. Press the + key until Not Installed appears.
26. Select Exit from the options at the top of the screen.
27. Highlight Save Changes and Exit and press Enter.

The system reboots with the new BIOS settings. The system performs a power on self test (POST). If errors occur during the POST, the BIOS displays the error on your monitor. If error messages appear on your monitor during the POST, refer to Appendix A, “Error Messages.”

2.4.3.2 Formatting After Booting from an IDE Hard Disk Drive

Use this procedure if it is not possible to attach a floppy drive to your evaluation board. In order to format the RFA or PC Card for the very first time, you need an IDE Hard Disk drive attached to the evaluation board. Follow the steps given in the last section to set up the IDE Hard Disk drive before you follow the steps below.

You need a computer and access to its hard drive connector. You will use this computer to install the M-Systems files and place DOS files onto a hard drive.

1. At the *computer*, install the DOS bootable IDE hard drive.
2. Insert the M-Systems diskette in the floppy drive of the computer and enter **INSTALL** from the floppy drive. Follow the installation instructions to install the TFFS files onto the hard drive (for more information refer to Chapter 7, “Using Flash Disks”). Make sure your hard disk drive has the DOS files SYS.COM and LABEL.COM.
3. Follow the steps in “Setting up the Board” on page 2-4 to set up the evaluation board with an IDE hard drive.
4. Turn on the power to the evaluation board. Press F2 to enter Setup.
5. Highlight BIOS Extension Base Address. Press the + key until Not Installed appears.
6. Select Exit from the options at the top of the screen.
7. Highlight Save Changes and Exit and press Enter.
8. The system reboots with the new BIOS settings. The IDE hard drive appears as the C: drive; The RFA appears as the D: drive; a PC Card appears as the E: drive. If formatting a flash PC Card, insert it now.
9. Format the RFA or PC Card (or both) using the TFORMAT command. For example,
C:\>TFORMAT D:
10. Use the DOS LABEL command to give volume names to the RFA and PC Card. For example,
C:\>LABEL D: RFA
11. Delete the CONFIG.SYS file from the hard drive.
C:\>DEL CONFIG.SYS
12. Turn off the power to the evaluation board, then turn it back on. Press F2 to enter Setup.
13. Select Advanced from the options at the top of the screen.

14. From the Advanced menu, highlight BIOS Extension Base Address. Press the + key until C800-CFFFH appears.
15. Select Exit from the options at the top of the screen.
16. Highlight Save Changes and Exit and press Enter. The system reboots with the new BIOS settings.
17. From the C: prompt, enter **SYS D:** to make the RFA a bootable disk, or enter **SYS E:** to make a PC Card bootable.
18. Turn off the power to the evaluation board, then turn it back on. Press F2 to enter Setup.
19. Select Advanced from the options at the top of the screen.
20. From the Advanced menu, highlight BIOS Boot Medium option. Press the + key until RFA (to boot from the RFA) or PCMCIA (to boot from a PC Card) appears.
21. From the Main menu, highlight IDE Adapter 0 Master. Press enter. Highlight Type and press the + key until (none) appears. Press Esc.
22. Select Exit from the options at the top of the screen.
23. Highlight Save Changes and Exit and press Enter.

The system reboots with the new BIOS settings. The system performs a power on self test (POST). If errors occur during the POST, the BIOS displays the error on your monitor. If error messages appear on your monitor during the POST, refer to Appendix A, "Error Messages."

When an IDE drive, RFA, and PC Card are all active drives in the system, there is up to a 45 second delay during the boot sequence.

The BIOS Boot Medium option on the Advanced Menu of the BIOS Setups affects drive letter assignments for the Flash media (PC Card or RFA). When you have configured more than one type of drive, the IDE drive is always the C: drive.

WARNING

The TFFS.COM and PCICSS.COM device drivers are provided for first time flash media formatting only. Once formatted, the BIOS extension controls access to the RFA and PC Cards. When using the device drivers, set the BIOS Extension Base Address to Not Installed. Doing so prevents data loss.

2.5 CHANGING THE DEFAULT VGA DRIVERS

After you have set up your evaluation board using the instructions in this chapter, you may want to change the default video drivers. For instructions on how to do this, see Chapter 6, “Installing VGA Drivers and Utilities.”

2.6 PROGRAMMING FLASH MEMORY

After you have set up your evaluation board, you may want to program the evaluation board's flash memory, or download application programs into the boot block flash device. For instructions on how to do this, see Chapter 8, “Programming Flash Memory.”



3

Theory of Operation



CHAPTER 3 THEORY OF OPERATION

3.1 BLOCK DIAGRAM

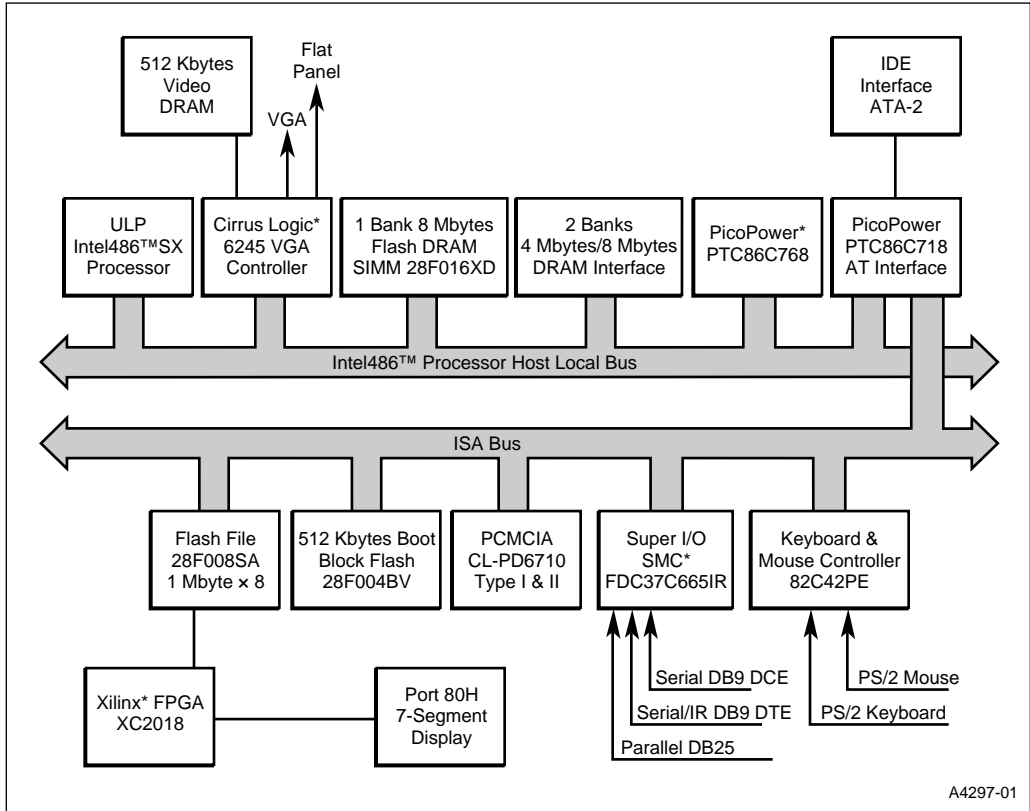


Figure 3-1. Ultra-Low Power Intel486™ Processor Evaluation Board Functional Block Diagram

3.2 ULTRA-LOW POWER Intel486™ SX PROCESSOR CIRCUITRY

The Ultra-Low Power Intel486™ SX processor is capable of running at various frequencies and core voltage settings to reduce power consumption. The jumper used to set the processor frequency is JP5, and the jumpers used to set the processor voltage are JP4 and JP8. A complete description of each jumper appears in “Jumpers” on page 4-1.

3.2.1 Measuring Processor Current

The processor current can be measured independently of the board’s current by replacing the jumper at JP4 with a milli-ammeter. (Be sure to use a low voltage drop milli-ammeter; the voltage drop directly subtracts from the processor’s working voltage.) Note that this measures only the current of the core processor input (V_{CC}) of the processor. The component’s I/O pad circuitry (V_{CCP}) is not isolated from the rest of the 3.3 V plane.

- To measure the current for the 3.3 V setting, place the milli-ammeter between pins 1 and 2 (3.3 V) on the JP4 connector.
- To measure the current for the 2.7 V or 2.4 V, select the voltage with the JP8 jumper, and place the milli-ammeter between pins 3 and 4 (VADJ) on the JP4 connector.

The maximum current expected for the Ultra-Low Power Intel486 SX processor is 350 mA. The typical current is about 180 mA (processor idle, 3.3 V, 33 MHz).

3.2.2 In-circuit Emulator Connectors

Four connectors surrounding the processor allow you to make a local bus connection to an in-circuit emulator (ICE) or logic analyzer. These connectors contain the signals to easily set up the processor for diagnostic purposes. Header information is shown in Chapter 4, “Hardware Reference.”

The TCK, TDO, TMS and TDI signals are all used for boundary scan diagnostic testing of the processor. The RESVD signal is unique to the Ultra-Low Power Intel486 SX processor. It must be connected to a 10 K Ω pull-up resistor for correct processor operation.

3.3 MISCELLANEOUS POWER SIGNALS

The ACPWR, Low Battery and Very Low Battery signals are inputs to the PicoPower chipset's power management circuitry. You must program the PicoPower chipset to use these inputs. The relevant registers internal to the PicoPower which deal with these multi-functional pins are:

Low Battery	Index Register 110H, Bit 4 set high enables this input for power management controller.
Very Low Battery	Index Register 110H, Bit 4 set high enables this input for power management controller.
ACPWR	Index Register 110H, Bit 4 set high enables this input for power management controller.

3.4 PICOPOWER CHIPSET REGISTERS AND OPTIONS

The PicoPower chipset consists of two 176-pin TQFP packages. The PT86C768 is the interface between the local address bus and DRAM. It contains a DRAM controller which can support up to 16 MBytes of memory per bank. (Because of power supply limitations, 8 Mbytes is the largest SIMM you can use on the evaluation board.) The PT86C768 also supplies the FLASH ROM chip select, power management interface registers and controls Input/Output signals.

Several registers can be used to set up shadowing, configure unique or broad ranged general purpose chip selects, and select timers. Listed below are some of the main registers and control signals which are associated with the PT86C768.

3.4.1 Clock and Reset Interface Signals

Table 3-1. Chipset Clock and Reset Interface Signals

Signal	Description
CLK_IN	This is the clock from the programmable PLL oscillator.
CLK_CPU	This control signal is the actual clock sent to the processor. It is under the control of the chipset since during a Power Management Suspend Mode the clock is shut off.
PWRGOOD	This control signal is the reset signal for the chipset. When this signal is in the low state the system is held in reset. The Maxim* 696 chip is the source for this signal which has a timed length of approximately 425 ms. This signal pulses low for at least 425 ms after a power on reset or after pushing the reset button. This signal occurs after the clocks are asserted as the LLINEOUT signal from the Maxim chip enables the clock circuitry before the reset is de-asserted. This enables the Xilinx* chip to attain its programming before the processor starts its code fetch from the Flash Boot Device (FBD).
RSTCPU	This is the reset signal to the CPU. This signal is asserted during power up.
RESETDRV#	This is the reset signal to the ISA BUS. This signal is controlled by the PicoPower chipset and is under control of the internal registers. Asserting this signal resets any of the devices located on the ISA bus.

3.4.2 Bus Control Interface

The PT86C718 is the interface chip to the ISA bus control signals. It includes the circuitry for handling interrupts, DMA transfers and standard ISA bus signals. The source and sink capability of its I/O pins matches that of a standard ISA bus driver. The AT SYSCLK is derived from the CPUCLK and is divided down to produce a slower speed < 8 MHz clock for the ISA bus. At 33 MHz this divisor is 4 and at 25 MHz this divisor is 3. No smaller divisor exists in the chipset and hence any processor frequency less than 25 MHz is divided by 3 and output on the AT SYSCLK. For example a 16 MHz CPUCLK produces a 5.3 MHz AT SYSCLK. This slowing of the AT clock helps to reduce the overall power consumption when running at slower speeds.

3.4.3 Power Management Features of the PicoPower Chipset

The PicoPower chipset provides many features for reducing power. Some of these features can be either controlled by hardware or software depending upon the level of power savings desired. Timers exist within the chipset for determining how long a specific power state is held before issuing a power management interrupt (PMI) or automatically transitioning to the next power saving state.

Four registers control the external output lines to the on-board hardware. Each register has a bit location for PC0 - PC9 and can be set high or low for any of the ten possible outputs.

Other registers internal to the chipset determine which hardware control pins are active during power up or used by other functions. (Refer to the *PicoPower Redwood Technical Reference Manual* for more information about programming the power management functions).

Table 3-2. Power Saving Hardware Registers

Index Register	Description
009H	Fully-ON Mode Power Control Register
00AH	Doze Mode Power Control Register
00BH	Sleep Mode Power Control Register
00CH	Suspend Mode Power Control Register

Although each register can control ten possible output lines, the evaluation board only provides six items to be controlled due to the multiplexed capability of these pins. Many of these pins are used as inputs to other functions when not needed for controlling power management peripherals.

Table 3-3. Hardware Power Control Pins

Pin	Device Controlled	Pin	Device Controlled
PC0	(SER_DREN1) High True Serial Port Driver Enable for COM1	PC5	(VGA.OSCEN) Enables the VGA chips oscillator. High True.
PC1	(PWRSABV_SER#) Low true IR Suspend mode. Shuts down the Serial Port Chip	PC6	(SER_DREN2) High True Serial Port Driver Enable for COM2
PC2	Not Available; used by another function	PC7	Not available; used by another function
PC3	Not available; used by another function	PC8	(VGAENBL) Used to place the VGA chip in Suspend mode. High True
PC4	Not available; used by another function	PC9	(PORT80_DIS#) PORT 80 LED disable. Low True Signal

The Ultra-Low Power Intel486™ Processor Evaluation Board includes a DOS program to demonstrate the effectiveness of using the chipset registers to reduce system power. Refer to Chapter 9, “Using Power Management,” for more information.

3.5 MEMORY

The evaluation board memory can consist of DRAM and FLASH SIMM Modules, Resident Flash Array (RFA) and Boot Block Flash. The PhoenixBIOS* is capable of searching for the size of DRAM using the appropriate protocols for reading and writing to DRAM locations. The board supports two SIMM sockets; one for DRAM SIMMs and the other for Flash SIMMs. The Flash SIMM socket can be populated with DRAM if desired. The maximum amount of memory allowed is 8 Mbytes. This limitation is due to power requirements of the 3.3 V power supply.

3.5.1 DRAM SIMM

The maximum amount of SIMM type memory which can be installed on the board is limited to the current capability of the evaluation board's 3.3 V power supply. The maximum suggested output current for the 3.3 V power supply (due to transformer core limitation) is 1.35 A. This limits the maximum amount of memory which can be added to the board, since, depending upon the types and number of chips used on the SIMM modules, a 16 Mbyte SIMM module could take as much as 1 A to run.

The current being used by the 3.3 V supply can be measured by connecting a milli-ammeter between the JP9 connector pins 1 & 2. These are the pins closest to the D8 diode.

The PhoenixBIOS uses the PicoPower chipset DRAM controller in a 3 RAS mode. There is a limit of three banks of memory. The maximum amount of memory which can be accessed per bank is limited to 16 Mbytes. The DRAM socket contains two banks and the FLASH socket contains one bank. When a double sided DRAM SIMM is placed in the FLASH socket only the front side of the SIMM is accessed; the back side has its RAS control line tied high and is not enabled.

The PicoPower chipset provides registers for setting up the access modes for the DRAM. The PhoenixBIOS initializes this for a 4-2-2 timing for the DRAM running at 33 MHz. Changing the timing is not recommended. The suggested type of DRAM SIMMs to use are 3.3 V, 70 ns SIMMS. The standard board has a 4 Mbyte, 3.3 V, 70 ns SIMM.

3.5.2 Flash SIMM

The Flash SIMM socket has its address lines wired differently than the DRAM SIMM socket. The DRAM socket follows the normal convention of address lines from the PicoPower chipset which does not place the memory in a linear addressing mode. High order address lines are interspersed with the lower address lines, depending on the number of CAS address lines being used.

To correctly use the Flash SIMM, the memory must be addressed in 32 Kbyte blocks. This is performed in hardware by inserting the MA0 line between MA9 and MA10 and shifting the MA address lines down by one. This is shown in the following tables.

3.5.2.1 DRAM Socket Address Scheme

Table 3-4. RAS (10 Bit Column Address Mode)

MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A21

Table 3-5. CAS (10 Bit Column Address Mode)

MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
X	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2

Address order presented to the FLASH SIMM:

A22, A20, A19, A18, A17, A16, A15, A14, A13, A12, **A21**, A11, A10, A9, A8 A7, A6, A5, A4, **A3**, A2.

The above method of addressing produces a contiguous block with A11 as the highest address bit. The maximum contiguous block size is 4 Kbytes. By inserting MA0 between MA10 and MA9 and moving the MA9 - MA1 multiplexed address lines down by one, you produce a contiguous block of memory which can be from 8 Kbytes to 8 Mbytes in size.

Within the block the addresses are not linear, but they do all fall within the same block. With the Intel Flash DRAM memory (28F016XD), which requires a 32 Kbytes contiguous block, all addresses fall within a block. Without this modification to the Flash SIMM socket, the programmer must add a driver which produces contiguous blocks of memory within the Flash SIMM device. This could be quite time consuming and would impact memory performance.

3.5.2.2 Flash SIMM Address Scheme

Table 3-6. RAS (10 Bit Column Address Mode)

MA10	MA0	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12

Table 3-7. CAS (10 Bit Column Address Mode)

MA10	MA0	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
X	A3	A11	A10	A9	A8	A7	A6	A5	A4	A2

Address order presented to the Flash SIMM:

A22, A21, A20, A19, A18, A17, A16, A15, A14, A13, A12, **A3**, A11, A10, A9, A8, A7, A6, A5, A4, A2

The addresses are linear above the A12 address bit, which implies the contiguous block size ranges from 8 Kbytes to 8 Mbytes. The READID command for the XD flash SIMMs should also work correctly, since the bottom three address bits are also linear.

While a DRAM SIMM could be installed in the Flash SIMM socket, the re-ordering of the address lines requires that the SIMM be 1 Mbyte x 32 (4 Mbyte total) or larger for the DRAM to be refreshed properly.

3.5.3 Resident Flash Array (RFA)

The evaluation board contains a 1Meg X 8 bit (1 Mbyte) Flash File Device (28F008) which is configured on board as a Resident Flash Array (RFA). The RFA may be formatted as a disk by the M-Systems* TFFS* software. The RFA is accessed through a 16 Kbyte window in the upper memory region (D0000 - EFFFFH) of the system. The M-Systems code creates this window at DC000H. A Xilinx XC2018 part is used to enable the RFA, set the page size and store the page register. This is all handled transparently by the M-Systems code.

The interface to the RFA is implemented through a variable size memory window in the ISA bus memory space. This memory window is programmed using a range comparator function of the PicoPower chipset. The upper address bits which select the variable size pages (8 Kbyte - 64 Kbyte) within the flash disk is provided by a register at I/O port 1096H. This register provides the upper 4-7 bits of the Flash address.

The second register (Page Control/Boot Block) is multipurpose and contains both the Page Register control and also the Boot Block flip bit controls (discussed later in this chapter).

Page Control/Boot Block Register (Read/Write)				Address: 2096H			
7							0
FBSEL	SBBF	HBBF	—	—	FLEN	WIN1	WIN0
Bit Number	Bit Mnemonic	Function					
7	FBSEL	Flip Bit Select. Selects either the SBBF or HBBF bit as the control for the Flash boot address SA18 bit. 0 = Selects the HBBF as the active boot block control bit. 1 = Enables SBBF control of the SA18 address bit on the Boot Flash.					
6	SBBF	Software Boot Block flip bit. This bit powers up in a default state of low. This bit is used in conjunction with the FBSEL bit to control the SA18 address line on the Flash Boot device. 0 = When the FBSEL bit is set to a one and the SBBF is low the SA18 bit is not inverted. This causes the top half (Cyber Quest* portion) of the Flash Boot Device to be used as the BIOS code source (Normal State). 1 = When FBSEL is high and SBBF is high the lower half (PhoenixBIOS portion) of the Flash Boot Device is used as the BIOS code source (SA.18 inverted). The SBBF bit is readable and writeable.					
5	HBBF	Hardware Boot Block Flip Bit control. A read of this bit shows the current setting of the hardware Boot Block Flip bit (JP3). 0 = (JP3 jumper is on) SA.18 address bit is not inverted. The upper half of the 512 Kbyte Boot Flash is used for the 256 Kbytes of BIOS. 1 = (JP3 jumper is off) The SA.18 bit is inverted and the lower half of the 512 Kbyte Boot Flash is used for the 256 Kbytes of BIOS. The HBBF bit is set by an external hardware jumper and reflects the state of this jumper to the processor. The HBBF is used during power up, since the FBSEL bit's default is to enable the HBBF as the active Boot Block Flip input. This bit is read only.					
4-3	NA	Reserved.					
2	FLEN	Power up state is flash disabled. This bit is readable and writeable. 0 = Flash is disabled when low. 1 = Enables the RFA when in the high state.					
1	WIN1	The settings of the WIN0 and WIN1 data bits are shown below for selecting the window size of the Flash Memory. The default window size is 64 Kbytes. The location of the memory window is selected by a register internal to the PicoPower chipset.					
0	WIN0						
		WIN1	WIN0	Window Size (Kbytes)			
		0	0	64			
		0	1	32			
		1	0	16			
		1	1	8			

Figure 3-2. Page Control/Boot Block Register

3.5.4 Flash Boot Device

The PhoenixBIOS, Cyber Quest Flash Loader Utilities and Cirrus Logic* video BIOS all reside in a single 512 Kbyte x 8 TQFP flash boot device (Intel 28F004BV-T or equivalent.)

The flash boot device allows BIOS changes and upgrades to be loaded and programmed after the board leaves the factory. This feature may be required to support different flat-panel displays, for development of a different BIOS, etc.

To allow an update of the BIOS, place a jumper on pins 4 and 6 (FRC_UP) of JP6 and make sure that boot block control is enabled on JP3. When pins 4 and 6 are jumpered, the Cyber Quest code initiates a reflash of the onboard flash boot device. This jumper is connected to an input pin of the keyboard controller and is used in cases where the BIOS is corrupted and the operating system does not boot.

The flash boot device is protected using two jumpers. These jumpers are located at connector JP10 (BB_CONTROL). By placing a jumper on pins 1 and 3 all blocks other than the boot block can be written. By placing an additional shunt on pins 2 and 6, (requires a wire with square pin connectors) the 16 Kbyte boot block can be reprogrammed.

The Flash Boot Device is memory addressed and resides in the last 512 Kbytes of system memory at address FFF80000H to FFFFFFFFH.

3.5.5 Cyber Quest Flash Loader Utilities

To support the Flash Loader Utilities from Cyber Quest, the evaluation board has a hardware jumper, JP3 (HBBF) which symmetrically “flips” the addresses of the device. When JP3 is jumpered, the location addressed as 00000H is flipped with 40000H in the boot device and the address at 3FFFFH in the boot device is flipped with 7FFFFH. This allows the system to boot to code in the Boot Block, or in the first 128 Kbyte main block with the simple change of a jumper.

Address bit A18 separates the 512 Kbyte boot device into two 256 Kbyte address blocks.

- When A18 is high, the top portion of the boot block device is selected. (the protected boot block is located at the top of the device).
- When A18 is low the bottom portion of the boot device is selected and the BIOS located at 3FFFFH and below is selected.

The selection of the A18 address is performed using a programmable device (XC2018) which reads the jumper and inverts BB.SA18 when a jumper is in place. This programmable register is I/O addressed at 2096H. This register is described in Figure 3-2.

Bit 5 (HBBF) of the Page Control/Boot Block Register shows the current status of the Hardware Boot Block Flip bit (HBBF) as set by the hardware.

- When HBBF=1 (no jumper on JP3) the BIOS is inverted and the PhoenixBIOS is at the boot address.
- When HBBF=0, (jumper on pins 1 and 2 of JP3) then the Cyber Quest Flash Loader utility is at the boot address (Normal Linear Mode).

The software can also flip the FBD address map while the system is running by writing to the SW Boot Block Flip Bit (SBBF) in bit 6 of I/O address 2096H.

- When SBBF=1 the FBD is inverted and PhoenixBIOS is at the boot address.
- When SBBF=0 then Cyber Quest is at the boot address. Software can read the status of the Software Boot Block Flip bit (SBBF) by examining bit 1 of this address.

The FBSEL bit (bit 7) controls whether the SBBF or HBBF is used to determine the BB.SA18 address bit. At power up, only the HBBF bit affects the BIOS location. The FBSEL powers up in default mode (low), selecting the HBBF bit to determine the inversion of BB.SA18. When FBSEL is high, SBBF determines the inversion. The SBBF and FBSEL are reset to zero at power up. In order to enable the SBBF bit to control BB.SA18 the FBSEL bit must be set to a one.

The HBBF bit is default valid at power-up.

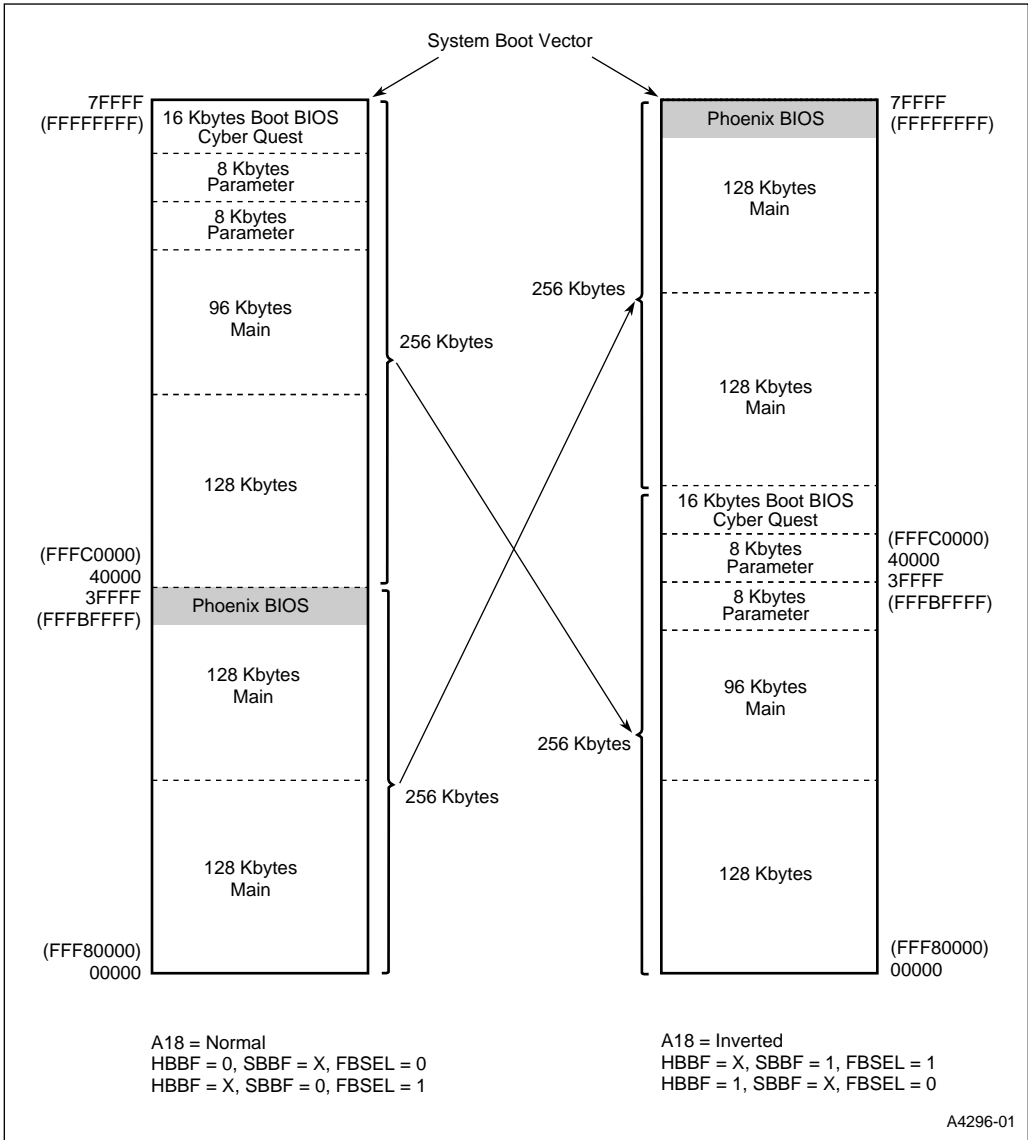


Figure 3-3. Boot Block Flash Memory Selection

3.6 VIDEO CONTROLLER

The evaluation board has a Cirrus Logic CL-GD6245 VGA-compatible video and flat-panel display controller. The controller supports flat-panel displays, including single and dual scan monochrome LCD's, STN and TFT color LCD displays.

The VGA controller resides on the processor local bus. The device is a mixed logic type, enabling both 3.3 V and 5 V operation. This allows it to operate directly off the local bus in a much higher throughput environment.

The CL-GD6245 provides simultaneous CRT and LCD operation (SimulSCAN*) for single and dual-scan color and monochrome LCDs, as well as fixed and multi-frequency analog CRTs. Using a single DRAM for display memory, the CL-GD6245 optimizes the memory and LCD interfaces to provide 640x480, 256 color SimulSCAN operation on dual-scan color STN LCDS.

The VGA controller supports Standby and Suspend power-management modes for reduced power consumption when the system is not active. The internal Standby Counter can initiate Standby mode without software intervention. During this reduced power mode, the LCD is turned off, while the display memory can be accessed and modified.

In Suspend mode, all I/O pins, except a dedicated Suspend-mode pin, are deactivated to further reduce power consumption. In this mode, the display-memory data is preserved but cannot be accessed. The Suspend mode can be initiated by the Power Management control register inside of the PicoPower chipset by use of an external control pin. The Suspend mode of the VGA controller can then be set by the power conservation mode of the PicoPower chipset (Sleep, Doze, Suspend). The power conservation capabilities of the VGA controller can also be activated by video BIOS software control if desired. The power management program PM.EXE demonstrates the use of this method of VGA suspend. See Chapter 9, "Using Power Management."

3.7 SERIAL PORTS (COM1, COM2)

The SMC* Super I/O chip (FDC37C665IR) provides two high-speed NS16C550A-compatible UARTs with send and receive data through 16-Byte FIFOs. The SMC has a programmable baud rate generator capable of sending data at 115.2 Kbaud maximum. The two serial ports have a 9-pin serial connector with COM1 configured as a null terminal (DCE) and COM2 as a standard serial port (DTE).

COM2 is also used as a Infrared Port and multiplexed by a control bit located in the Miscellaneous Control Register (Figure 3-4). The LEDCON selects between software or hardware power-down of the COM2 serial port driver chip. When LEDCON is set low (default), the COM2 serial port is under the control of the INFRD# bit. When LEDCON is high, the PC6 power management pin from the PicoPower chipset controls the serial port driver.

MISC Control Register (Read/Write)				Address: 3096H			
				Reset State: 010xxxx0B			
7				0			
LEDDIS	INFRD#	LEDCON	—	—	—	—	SFRC
Bit Number	Bit Mnemonic	Function					
7	LEDDIS	LED Disable. Read/Write. Controls Port 80 Display LED when LEDCON is set low. 0 = Enables the LED 1 = Shuts off the LED.					
6	INFRD#	Controls the COM2 serial port when LEDCON is set low. 0 = Enables the infrared input and shuts down the COM2 serial port driver. 1 = Enables the COM2 serial port driver.					
5	LEDCON	LED Control. This bit enables either software or hardware control of the LED and COM2 serial port. 0 = Enables the LEDDIS and INFRD# signals to control the LED and COM2 serial ports, respectively. 1 = Port80_DIS and SERA_COM2 signals from the PicoPower chipset control the LED and COM2 serial port, respectively.					
4-1		Reserved.					
0	SFRC	Software Forced Recovery Bit. This RAM bit is preserved across keyboard resets.					

Figure 3-4. MISC Control Register

When INFRD# (bit 6) is in the low state, and LEDCON (bit 5) is low, the serial port driver chip (SN75LCB187) is disabled, which allows the Infrared Port to drive the serial inputs of the FDC37C665IR. When INFRD# is in the high state and LEDCON is low, the serial drive chip is enabled and the receive input to the FDC37C665IR is controlled by the SN75LCB187.

Table 3-8. Serial Port Control

LEDCON	INFRD#	SER.DREN2 (PC6)	PWRSAV.SER# (PC1)	Description
0 (default)	1 (default)	X	X	COM2 Serial Port Driver Enabled
0 (default)	0 (default)	X	X	COM2 Serial Port Driver Disabled, Infrared Enabled
1	X	1	1	COM2 Serial Port Driver Enabled
1	X	1	0	COM2 Shutdown, COM2 Serial Port Driver Enabled
1	X	0	1	COM2 Serial Port Driver Disabled, Infrared Enabled
1	X	0	0	COM2 Shutdown, COM2 Serial Port Driver Disabled

3

For power-down operations, the PWRGD control pin is pulled low. This signal is sourced from the PicoPower chipset’s power management pins. When PWRGD is pulled low, all inputs to the FDC37C665IR are disconnected, the device is put in a low power mode, and all outputs are floated. The contents of all registers are preserved as long as V_{CC} is valid.

Provisions are made for waking up the PicoPower chipset by use of activity input lines to the power management controller. The COM1 serial port provides two power management activity inputs to the PicoPower chipset. This is the SERA.COM1 line which goes to the EXTACT2 input and also to the WAKE1 input of the PicoPower Chipset. The EXTACT2 input can be used to bring the evaluation board out of Idle or Standby power management mode. The WAKE1 input is used to bring the evaluation board out of a Suspend power management mode.

The COM2 serial port has two signals which allow it to bring the evaluation board out of a power management state. These two signals are SERA.COM2 and COM2A.RI which respectively go to the EXTACT1 and the RING inputs of the PicoPower chipset. The EXTACT1 signal can be used to bring the evaluation board out of the Idle or Standby power management mode. The RING input is used to bring the evaluation board out of a Suspend power management mode.

3.8 PARALLEL PORT

The parallel port is incorporated within the SMC FDC37C665IR Super I/O chip. The chip supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port mode. The FDC37C665IR contains protection circuitry which prevents possible damage to the parallel port due to printer power-up. The port is available on a dual-in-line 0.1” header. The header’s pin-out allows the use of a DB-25 connector.

3.9 INFRARED PORT

The FDC37C665IR infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Two infrared implementations are provided, IrDA and Amplitude Shift Keyed IR.

IrDA allows serial communication at baud rates up to 115 Kbaud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a single infrared pulse at the beginning of the serial bit time. A one is signaled by sending no infrared pulse during the bit time.

This port is fused with a user-replaceable 2 A (type OMF63V) fuse.

The Amplitude Shift Keyed IR allows serial communication at baud rates up to 19.2 Kbaud. Each word is sent serially beginning with a zero value start bit. A zero is signaled by sending a 500 KHz waveform for the duration of the serial bit time. A one is signaled by sending no transmission during the bit time.

The infrared port is enabled by setting the INFRD# bit in the Miscellaneous Control Register to a low state (3096H, Bit D6). This bit disables the serial port driver chip (SN75LBC187) and allows the receive driver from the Infrared port to send data to the Super I/O serial port.

Two other external activity inputs are made available at the six-pin infrared port. These can be used to cause a PMI interrupt to the chipset causing the system to awaken from a power savings mode. The MUX_FP6 input is used to wake the system from the Sleep or Doze mode. The MUX_FP5 is used to wake the system from a Suspend mode.

3.10 PCMCIA CONTROLLER

The PC Card interface uses a Cirrus Logic CL-PD6710 and is located on the ISA bus. This device is compliant with PCMCIA 2.1 and JEIDA 4.1 specifications and has an 82365SL-compatible register set. The CL-PD6710 employs energy-efficient mixed-voltage technology that can reduce system power consumption. The chip provides a Suspend mode, which stops the internal clock and an automatic low-power dynamic mode, which stops transactions on the PCMCIA bus, stops internal clock distribution and turns off much of the internal circuitry.

The voltages supported on the connector are +3.3 V, 5 V and +12 V for Flash cards. Physically, only PC Card types I and II are supported. Type III PC Card are not supported. Although the only software support provided is for Flash PC Cards, standard Card and Socket Services drivers could be used to support other PCMCIA compatible cards.

The chips' control registers are located on the ISA bus at address locations 3E0H - 3E1H.

The CL-PD6710 incorporates energy savings modes such as low power dynamic mode, Suspend mode and control of the PCMCIA socket power.

When in low power dynamic mode, periods of inactivity cause the CL-PD6710 to enter a low power state where the clock is turned off to most of the chip, and the PCMCIA address and data lines are set to a static value. The chip powers up in this state and it can be disabled by writing to an on-board control register. When activity occurs on the PCMCIA bus, or system accesses to chip registers or inserted cards begin, the chip returns from this low power state to normal operating mode. It returns to this low power mode when there is no activity on the PCMCIA bus, or no system accesses to chip registers or no card changes.

Suspend Mode can also be programmed, which is the chip's second lowest power mode. (2 mW). The CL-PD6710 is put into Suspend mode by writing to the MISC Control 2 register. In Suspend mode all the internal clocks are turned off and only accesses to the MISC Control 2 register are supported.

All accesses to the PC Cards are ignored when in Suspend mode. V_{CC} and V_{PP} power to the card is left unchanged. Interrupts are passed through to the processor when in Suspend mode. To disable this mode the processor writes to the MISC Control 2 register again and clears the appropriate bit. The CL-PD6710's internal clock synthesizer requires 50 ms to restart after coming out of the Suspend mode.

Further power management can be achieved by software control of the PCMCIA socket's V_{CC} and V_{PP} power supplies. The CL-PD6710 provides six power control pins for controlling external logic to switch V_{CC} and V_{PP} voltage on and off. Cards can be turned off when not in use to reduce power consumption.

3.11 MOUSE/KEYBOARD CONTROLLER

A PC-compatible keyboard controller (82C42PE) is provided on the board. Connection is made with a 6-pin mini-DIN connector, the type used in PS/2*-compatible designs and elsewhere. Power to the keyboard is fused to meet safety agency requirements (e.g., UL1950). The fuse is not user-replaceable.

A PS/2 style mouse and keyboard interface is provided using the 82C42PC chip and the Phoenix MultiKey/42 firmware. Mouse and keyboard support are located at I/O address 60H to 64H.

CAUTION

Make sure the power is OFF when you connect or disconnect the keyboard.
Disconnecting the keyboard with the power on will destroy the port.

3.12 IDE CONTROLLER

The IDE hard disk drive interface is provided by the PicoPower chipset. The IDE hard disk is mapped to I/O addresses 1F0H - 1F7H, 3F6H, and 3F7H. Note that I/O address 3F7H is shared with the floppy disk controller as required for PC compatibility. The IDE hard disk uses AT-bus interrupt IRQ14. Connection to an IDE hard disk is made through a 40-pin 0.1” dual-in-line header mounted on the PCB. As part of the CPU chipset, this interface exists on the Ultra-Low Power Intel486 SX processor local bus and can therefore support the higher throughput requirements of the Fast-ATA specification (Modes 0-2). Special drivers would need to be written to implement this on the evaluation board, however, because the PhoenixBIOS does not support it. Up to two drives are supported by the IDE interface.

3.13 PORT80H OUTPUT DISPLAY

This output is located in I/O space at address 80H and is used for a seven-segment output device. A hexadecimal latch is used which allows the bottom eight bits of binary data to select the 256 possible values for the seven-segment display. This output port is only used for system BIOS diagnostic purposes, although other test programs could use it as well.

The display is enabled through either the hardware or software. If under hardware control the LEDCON bit (bit 6) in the Miscellaneous Control Register (Figure 3-4) is set high. In this mode the LED is controlled by the polarity of the PORT80_DIS (PC9) signal from the PicoPower Chipsets Power Management Signals. When PORT80_DIS is set high, the LED is off; when PORT80_DIS is low, the LED is on.

To control the LED from software set the LEDCON bit to a low state. In this mode the LED is controlled by the LEDDIS bit (bit 7) in the Miscellaneous Control Register (3096H). When LEDDIS is set high, the LED is disabled. When LEDDIS is set low the LED is enabled. The power on default is with the LED enabled and hence LEDDIS is set low with LEDCON set low.

Table 3-9. LED Control

LEDCON	LEDDIS	PORT80_DIS (PC9)	Description
0	0	X	LED Enabled
0	1	X	LED Disabled
1	X	0	LED Enabled
1	X	1	LED Disabled

3.14 POWER SUPPLY SUPPORT

The board supports multiple power supply options. Power to the board is supplied either through the ISA edge board connector, the standard PC power supply connector, or a special portable external power supply connector.

To decrease power supply drop, all jumpers are in series with the appropriate power supply pins. When active switches are used, part of the voltage is dropped due to switch resistance.

When your portable power supply provides +5 V, an on-board switching regulator provides +3.3 V. For longer battery life it may be more efficient to use a switching +3.3 V supply on the portable power supply than the on-board +3.3 V switching regulator.

The processor's power supply is derived from a separate linear voltage regulator which is variable by selecting the appropriate taps. Three voltages are selectable using the jumpers supplied on the board: 2.4 V, 2.7 V and 3.3 V.

3.14.1 Real-Time Clock Battery

A built-in socketed coin cell is provided for backup of the real-time clock and CMOS RAM. This cell is installed at the factory, and is user-replaceable. The battery cell used is a 3 V lithium coin cell, Panasonic* part number BR200 or equivalent. The expected lifetime of the battery is expected to be two years, with no power source applied. When power is applied to the evaluation board, the drain on the battery is zero.

Diode and/or resistor protection is employed in accordance with UL1950/EN0950 requirements to prevent reverse current from flowing to the internal battery.

3.15 SPEAKER

A very small piezo-electric speaker (0.5" [12.7 mm diameter] maximum) is connected to the PicoPower chips' output. It is buffered from the PicoPower chips' output to increase the signal amplitude.

3.16 RESET CIRCUITRY

The upper push-button reset switch (SW1) is provided to reset the system. It is connected to the input of a system reset controller. When asserted the reset controller debounces the switch and outputs a reset pulse to the system lasting approximately 425 ms.

The system reset controller ensures the clock circuitry does not turn on before the power supply has reached at least 2.7 V, thus maintaining proper startup protocol. The Maxim chip also holds the processor and chipset in reset until the Xilinx has been programmed. This ensures that the Flash Boot Device is addressed correctly and the diagnostic LEDs operate during BIOS setup.

A second push-button reset switch (SW2) is reserved for future use.



4

Hardware Reference



CHAPTER 4 HARDWARE REFERENCE

4.1 SPECIFICATIONS

Table 4-1. Environmental and Electrical Specifications

Environmental		
Temperature	operating	0 - 60°C over 6600 ft. (2000m) derated 2°C per 1000 ft. (300 m)
	storage	-40 to 85°C
Humidity	operating	5 - 95% (non condensing)
	storage	5 - 95% (non condensing)
Altitude	operating	0 - 10,000 ft. (3000 m)
	storage	0 - 40,000 ft. (12,000 m)
Vibration	operating	2.5 g acceleration over 5-300 Hz sine wave (P-P), 1 oct/min sine sweep
	storage	5 g acceleration over 5-300 Hz sine wave (P-P), 1 oct/min sine sweep
Shock	operating	30 g, 11 ms duration, half-sine shock pulse
	storage	50 g, 11 ms duration, half-sine shock pulse
Electrical		
Current	typical	+5 V @ 1.2 A
		+12 V @ 120 mA for writing to Flash BIOS

NOTE: Specifications assume PCCard not installed.

4.2 JUMPERS

This section describes the function of each jumper on your evaluation board. The jumper locations and factory settings are shown in Figure 4-1.

CAUTION

In order to change jumper settings, turn off power to the evaluation board, change the jumper(s) and then reapply power. Never attempt to change *any* jumper while the board is powered up.

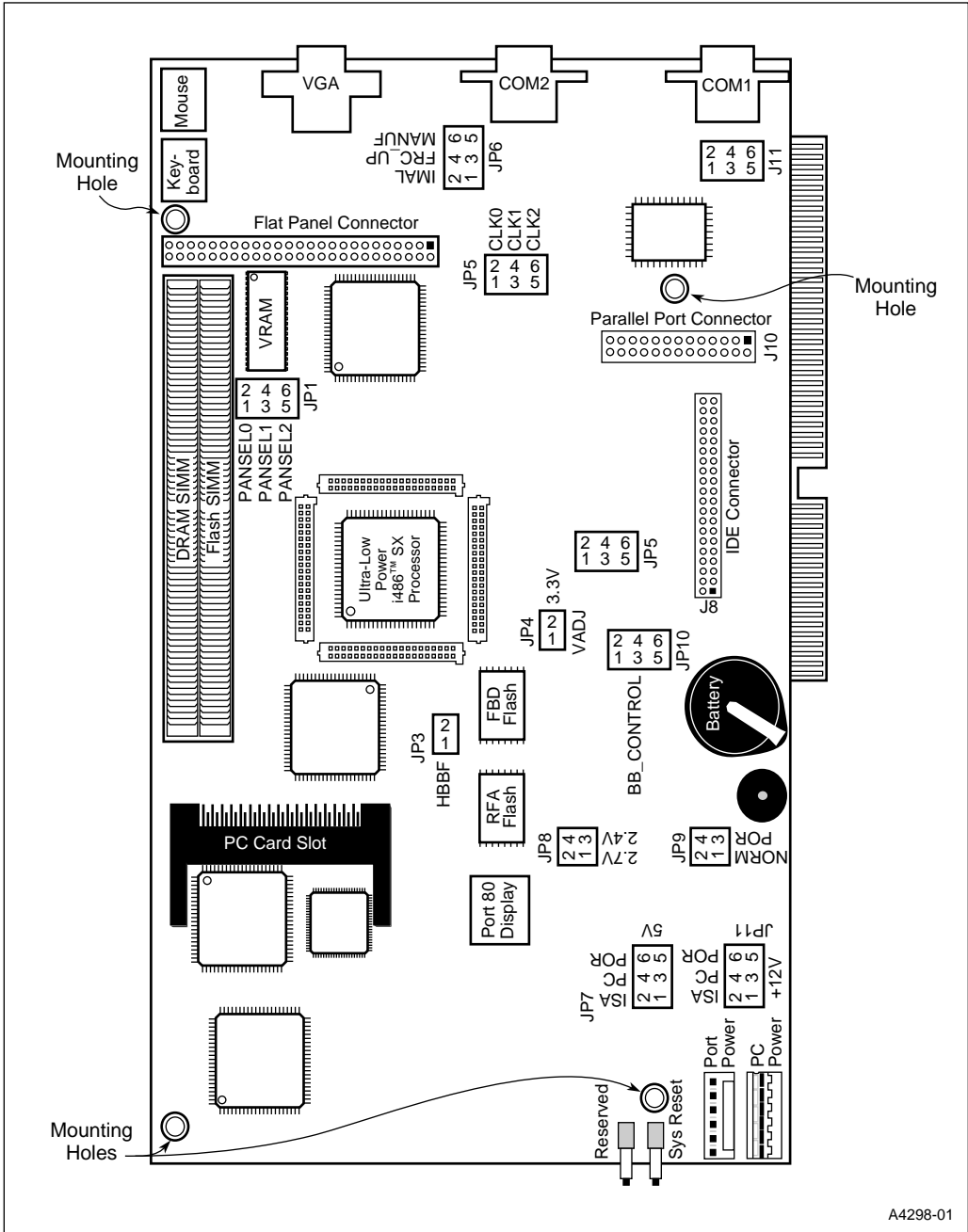


Figure 4-1. Location of Jumpers and Connectors

The evaluation board jumpers are summarized in the table below:

Table 4-2. Jumper Summary

Jumper	Title	Purpose	Default
JP1	PANSEL0, 1 & 2	Selects flat-panel display	All 3 installed
JP3	HBBF	Enables Cyber Quest* or PhoenixBIOS* startup code	Installed
JP4	3.3V, VADJ	Selects CPU core voltage: 3.3 V or VADJ	VADJ installed
JP5	CLK0, 1 & 2	Selects processor clock speed	CLK1 installed
JP6	IMAL, FRC_UP, MANUF	Forces flash update when used with JP3	n/a
JP7	5 V	Selects from three 5 V power options	PC installed
JP8	2.7V, 2.4V	Selects 2.4 V or 2.7 V VADJ	2.7 V
JP9	NORM, POR	Selects 3.3 V power supply source	NORM installed
JP10	BB_CONTROL	Controls reflashing the Flash Boot Device	n/a
JP11	+12V	Selects from three 12 V power options	PC installed

4.2.1 JP1: Flat-Panel Select Jumpers

When you are using a flat-panel display, you must set jumpers PANSEL0, PANSEL1, and PANSEL2 to configure the video BIOS for use with your particular flat-panel display. When you are not using a flat-panel display, the selections make no difference.

The BIOS extension for the VGA controller is included in the Flash Boot Device where the system BIOS resides. Since it is contained in a flash device, it is possible to upgrade (reflash) the video BIOS extension to include additional or different flat-panel displays after the board has left the factory. The video BIOS supplied with the evaluation board supports several different flat-panels, which are selected by the three jumpers. These jumpers are read by the video BIOS during power up to select the panel according to the following chart.

‘IN’ indicates that the jumper is installed. The default when the board leaves the factory is to include all three jumpers set to the ‘IN’ position.

Table 4-3. LCD Flat-Panel Jumper Selection

PANSEL2	PANSEL1	PANSEL0	Panel Selected
IN	IN	IN	Single Scan Color STN, 16-Bit Interface, 8 color (e.g., Sanyo* LCM-CK53 or LCM-5327) (Default)
IN	IN	OUT	Dual Scan STN, Monochrome 6.3 MHz, (e.g., Sharp* LM64P80)
IN	OUT	IN	Dual Scan Color STN, 16-Bit Interface (e.g., Sanyo LCM-CA53, or LCM-5331)
IN	OUT	OUT	Color TFT - 9-Bit Interface (e.g., Sharp LQ9D011)
OUT	IN	IN	Single Scan Color STN - 8-Bit Interface
OUT	IN	OUT	Single Scan Monochrome STN - 4 Bit Interface
OUT	OUT	IN	Unused
OUT	OUT	OUT	Color TFT - 18-Bit Interface (e.g., Sharp LQ10D3011)

NOTE: Part numbers listed above have been tested to work with the ULP Intel486 SX processor evaluation board.

Due to a lack of standards in the LCD industry, standard cables are not available for the flat-panels supported on the evaluation board. Pinouts for the cables are listed in “Connectors” on page 4-9.

4.2.2 JP3: HBBF Jumper

Normally this jumper is installed. When installed, after a system reset the Cyber Quest utility is executed. The jumper causes the Cyber Quest startup code to run before the PhoenixBIOS code. The Cyber Quest code performs a checksum on the PhoenixBIOS, and if the checksum is correct, the system boots from the PhoenixBIOS code. When an error is discovered in the checksum, the Cyber Quest flash loader utility looks at the COM1 serial port to attempt to download a new PhoenixBIOS.

When this jumper is not installed, the Cyber Quest flash loader utility is bypassed and the evaluation board begins executing the PhoenixBIOS startup. This is the default.

This jumper is used in conjunction with JP6, the Force Update jumper. Refer to Chapter 8, “Programming Flash Memory” for more information.

4.2.3 JP4 & JP8: Setting Processor Core Voltage Jumpers

The processor core voltage is determined by JP8 and JP4. The processor takes two voltage supplies: V_{CCP} and V_{CC} . The V_{CCP} voltage is the interface voltage to the rest of the system and is set at 3.3 V. The V_{CC} voltage for the processor is a variable core supply voltage and is equal to the evaluation board's VADJ supply.

To set the VADJ supply to 3.3 V, the JP4 jumper must be in the 3.3 V position (connect pins one and two). It does not matter what position the JP8 jumper is in when the VADJ supply is set to 3.3 V.

To set the VADJ supply to 2.7 V or 2.4 V the JP4 jumper must be placed in the VADJ position. JP8 is used to set the VADJ supply to either 2.4 V or 2.7 V. See below for a chart showing these selections. 'IN' indicates that the jumper is installed. The default selection is 2.7 V.

Table 4-4. Processor Core Voltage Jumper Selection

JP4		JP8		V_{CC}
VADJ	3.3 V	2.7 V	2.4 V	
IN	OUT	IN	OUT	2.7 V (Default)
IN	OUT	OUT	IN	2.4 V
OUT	IN	X	X	3.3 V

NOTES:

1. X= Don't Care
2. The processor clock must be 25MHz or less when V_{CC} is 2.4 V.

4.2.4 JP5: Clock Speed Jumpers

JP5 is used to determine the CPU’s clock frequency by placing jumpers using the matrix shown below. There are eight possible jumper combinations, but only six are valid. The highest specified frequency for the processor is 33 MHz. ‘IN’ indicates that the jumper is installed.

Table 4-5. Processor Frequency Jumper Selection

CLK2	CLK1	CLK0	Frequency
IN	IN	IN	4 MHz
IN	IN	OUT	8 MHz
IN	OUT	IN	16 MHz
IN	OUT	OUT	20 MHz
OUT	IN	IN	25 MHz
OUT	IN	OUT	33.3 Mhz (Default)
OUT	OUT	IN	(Invalid)
OUT	OUT	OUT	(Invalid)

In order to set a new frequency the board should first be shut off, the jumper(s) changed and the power then reapplied. Never attempt to change *any* jumper while the board is powered up. The new frequency can be verified by watching the diagnostic start up information, which displays during boot up.

The table below shows the processor voltage and frequency selections allowed. Note that the only selection that is not allowed is 2.4 V with a frequency of 33 MHz. The default selection is 33 MHz.

Table 4-6. Processor Voltage Selections

Processor Voltage	Frequency Range
3.3 V +/- .3 V	up to 33 MHz (Default)
2.7 V +/- .2 V	up to 33 MHz
2.4 V +/- .2 V	up to 25 MHz

4.2.5 JP6: Force Update Jumper

JP6 is not used during installation and configuration. The default is no jumper installed.

Jumper pins 4 and 6 of JP6 to force an update of the BIOS during the next boot. Forcing an update means to interrupt the normal boot process, causing the evaluation board to search for information on a serial port coming from a host PC that will update the BIOS.

NOTE

Use jumper JP3 in conjunction with jumper JP6. Refer to Chapter 8, “Programming Flash Memory” for more information.

4.2.6 JP7: 5 V Power Jumper

JP7 is used to select from three alternative 5 V power supplies. You can select an ISA-bus passive backplane, a standard PC power supply, or the portable battery power supply. This selection normally matches the selection for JP11: 12 V Power. The default for JP7 is a PC power supply.

For connector information, refer to “Connectors” on page 4-9.

4.2.7 JP9: Power Supply Jumper

JP9 is used to select the source of 3.3 V power. To use the normal 3.3 V power supply, jumper pins 1 and 2 of JP9 together. This is the default. To use an external 3.3 V power supply from the portable battery supply connector, jumper pins 3 and 4.

4.2.8 JP10: Flash Boot Device (FBD) Control Jumper

This jumper is not used during installation. The default is no jumper installed.

The flash boot device is protected using two jumpers at JP10. One enables the capability to write to the flash device to update internal blocks other than the boot block. The second jumper is used to enable reflashing of the entire chip.

By placing a jumper on pins 1 and 3, all blocks other than the boot block can be written.

By placing an additional jumper on pins 2 and 6, (requires an actual wire with square pin connectors) the 16 Kbyte boot block can be reprogrammed.

4.2.9 JP11: 12 V Power Jumper

JP11 is used to select from three separate 12 V power supplies. You can use an ISA passive backplane, a standard PC power supply, or the portable battery power supply.

The selection for JP11 normally matches JP7. The default for JP11 is to select a PC power supply.

4.3 CONNECTORS

This section specifies the pinouts of the connectors on the evaluation board. These connectors adhere to existing standards. Pins are labeled from the point of view of looking into the front of the connector on the evaluation board. Refer to Figure 4-1 for the board location of each connector.

The Ultra-Low Power Intel486 SX processor is a 3.3 V part. All signals are 3.3 V level.

4.3.1 J1-J4: 40-pin ICE Headers

J1-J4 are Samtec SFM-120-L3-5-0

Table 4-7. ICE Header (J1) Pinout

Pin	Signal	Pin	Signal
1	ADS#	2	A2
3	GND	4	3.3 V
5	GND	6	3.3 V
7	A3	8	A4
9	A5	10	RESVD
11	A6	12	A7
13	A8	14	GND
15	A9	16	A10
17	3.3 V	18	GND
19	A11	20	A12
21	A13	22	A14
23	3.3 V	24	GND
25	A15	26	A16
27	A17	28	GND
29	3.3 V	30	TDI
31	TMS	32	A18
33	A19	34	A20
35	3.3 V	36	3.3 V
37	A21	38	A22
39	A23	40	A24

Table 4-8. ICE Header (J2) Pinout

Pin	Signal	Pin	Signal
1	VADJ	2	3.3 V
3	PCD	4	PWT
5	D/C#	6	M/IO#
7	GND	8	VADJ
9	BE3#	10	BE2#
11	BE1#	12	BE0#
13	BREQ	14	3.3 V
15	GND	16	W/R#
17	HLDA	18	CLK_CPU
19	VADJ	20	GND
21	VADJ	22	TCK
23	AHOLD	24	HOLD
25	GND	26	VADJ
27	KEN#	28	RDY#
29	NC	30	VADJ
31	BS8#	32	BS16#
33	BOFF#	34	BRDY#
35	NC	36	3.3 V
37	GND	38	LOCK#
39	PLOCK#	40	BLAST#

Table 4-9. ICE Header (J3) Pinout

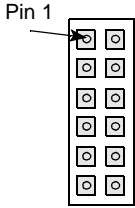
Pin	Signal	Pin	Signal
1	GND	2	GND
3	3.3 V	4	A25
5	A26	6	A27
7	A28	8	3.3 V
9	A29	10	A30
11	A31	12	GND
13	D0	14	D1
15	D2	16	D3
17	D4	18	VADJ
19	GND	20	VADJ
21	GND	22	GND
23	3.3 V	24	D5
25	D6	26	3.3
27	NC	28	D7
29	GND	30	D8
31	D9	32	GND
33	D10	34	D11
35	D12	36	D13
37	GND	38	3.3 V
39	D14	40	D15

Table 4-10. ICE Header (J4) Pinout

Pin	Signal	Pin	Signal
1	GND	2	D16
3	3.3 V	4	GND
5	GND	6	D17
7	D18	8	D19
9	D20	10	GND
11	3.3 V	12	D21
13	D22	14	D23
15	GND	16	3.3 V
17	D24	18	D25
19	D26	20	D27
21	GND	22	3.3 V
23	D28	24	S29
25	D30	26	D31
27	STPCLK#	28	TD0
29	SMI#	30	3.3 V
31	GND	32	SMIACT#
33	SRESET	34	NMI
35	INTR	36	FLUSH#
37	GND	38	RSTCPU
39	A20M#	40	EADS#

4.3.2 J5: Misc Header

Table 4-11. Misc. Header (J5) Pinout

Pin	Signal	Pin	Signal	Diagram
1	Processor Pin 20 (TCK)	2	Processor Pin 58 (TDO)	8x2, 0.100" [2.54 mm] pitch header; 3M 2514-6002UB 
3	Processor Pin 142 (TMS)	4	Processor pin 143 (TDI)	
5	Processor Pin 166 (RESVD)	6	PT86C768 Pin 124 (ACPWR)	
7	PT86C768 Pin 122 (Low Battery)	8	PT86C768 Pin 123 (Very Low Battery)	
9	GND	10	GND	

4.3.3 J6: LCD Connector Header

Table 4-12. LCD Connector (J6) Pinout

Pin	Signal	Pin	Signal	Diagram
1	V _{CC}	2	GND	25x2, 2 mm pitch header Samtec SMM-125-01-5-S-D
3	NC	4	P8	
5	NC	6	P9	
7	ENAVDD	8	GND	
9	ENAVEE	10	P10	
11	GND	12	P11	
13	M	14	GND	
15	FLM	16	P12	
17	GND	18	P13	
19	LP	20	GND	
21	SHCLKR#	22	P14	
23	GND	24	P15	
25	SHCLKR	26	GND	
27	GND	28	P16	
29	P0	30	P17	
31	P1	32	GND	
33	GND	34	NC	
35	P2	36	NC	
37	P3	38	GND	
39	GND	40	NC	
41	P4	42	NC	
43	P5	44	GND	
45	GND	46	NC	
47	P6	48	NC	
49	P7	50	GND	

4.3.4 J7: Portable Power Connector

Table 4-13. Power Connector (J7) Pinout

Pin	Signal	Diagram
1	GND	6 position, 0.098" [2.50 mm] pitch
2	+5 V	
3	+12 V	
4	NC	
5	+3.3 V	
6	GND	

4.3.5 J8: IDE Connector

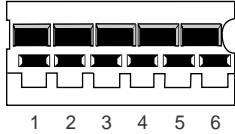
Table 4-14. IDE Connector (J8) Pinout

22x2, 0.1" pitch header
Samtec STMM-122-01-S-D-20

Pin	Signal	Pin	Signal
1	RESET#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	key
21	n/c	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IOCHRDY	28	n/c
29	n/c	30	GND
31	IRQ	32	IOCS16#
33	A1	34	PDIAG#
35	A0	36	A2
37	HCS0#	38	HCS1#
39	DASP#	40	GND

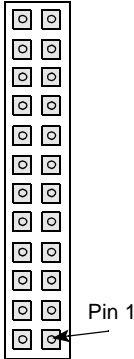
4.3.6 J9: PC Power Connector

Table 4-15. Power Connector (J9) Pinout

Pin	Signal	Diagram
1	OPEN	6 position, 0.098" [2.50 mm] pitch AMP #171825-6 
2	+5 V	
3	+12 V	
4	-12 V/NC	
5	GND	
6	GND	

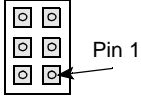
4.3.7 J10: 26-pin LPT1 Header

Table 4-16. LPT1 Header (J10) Pinout

Pin	Signal	Pin	Signal	Diagram
1	STROBE#	2	AF#	2x13, 0.1" square pin header 3M-89126-0013-TO 
3	DO	4	ERROR#	
5	D1	6	INIT#	
7	D2	8	SLCTIN#	
9	D3	10	GND	
11	D4	12	GND	
13	D5	14	GND	
15	D6	16	GND	
17	D7	18	GND	
19	ACK#	20	GND	
21	BUSY	22	GND	
23	PE	24	GND	
25	SLCT	26	GND	

4.3.8 J11: Infrared Header

Table 4-17. Infrared Header (J11) Pinout

Pin	Signal	Pin	Signal	Diagram
1	GND	2	RX	2 x 3, 0.1" square pin header 
3	V _{CC}	4	TX	
5	EXT Activity wakeup from Sleep and Doze mode	6	EXT Activity wakeup from Suspend Mode	

4.3.9 VGA Connector

Table 4-18. VGA Connector (JP2) Pinout

Pin	Signal	Diagram
1	RED	15-pin female high-density D-sub JST KSEY-15S-1A3F19-13 or equivalent
2	GREEN	
3	BLUE	
4	n/c	
5	GND	
6	ANALOG GND	
7	ANALOG GND	
8	ANALOG GND	
9	n/c	
10	GND	
11	n/c	
12	n/c	
13	H SYNC	
14	V SYNC	
15	n/c	

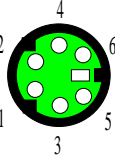
4.3.10 P1: PCMCIA Connector

Table 4-19. PCMCIA Connector (P1) Pinout

Pin	Signal	Pin	Signal
1	GND	35	GND
2	D3	36	/CD1
3	D4	37	D11
4	D5	38	D12
5	D6	39	D13
6	D7	40	D14
7	/CE1	41	D15
8	A10	42	/CE2
9	/OE	43	VS1
10	A11	44	/IORD
11	A9	45	/IOWR
12	A8	46	A17
13	A13	47	A18
14	A14	48	A19
15	/WE_PGM	49	A20
16	RDY/BSY	50	A21
17	V _{CC}	51	V _{CC}
18	VPP1	52	VPP2
19	A16	53	A22
20	A15	54	A23
21	A12	55	A24
22	A7	56	A25
23	A6	57	VS2
24	A5	58	/RESET
25	A4	59	WAIT
26	A3	60	/INPACK
27	A2	61	/REG
28	A1	62	BVD2/SPKR
29	A0	63	BVD1/STSCHD
30	D0	64	D8
31	D1	65	D9
32	D0	66	D10
33	WP/IOCS16	67	/CD2
34	GND	68	GND

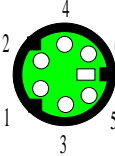
4.3.11 P2: Keyboard

Table 4-20. Keyboard Connector (P2) Pinout

Pin	Signal	Pin	Signal	Diagram
1	Keyboard Data	4	+5V	6-pin mini-DIN circular AMP 749266-1 or equivalent 
2	N/C	5	Clock	
3	GND	6	N/C	

4.3.12 P3: Mouse

Table 4-21. Mouse Connector (P3) Pinout

Pin	Signal	Pin	Signal	Diagram
1	Mouse Data	4	+5V	6-pin mini-DIN circular AMP 749266-1 or equivalent 
2	N/C	5	Mouse Clock	
3	GND	6	N/C	

4.3.13 COM1

- 9-pin female D-sub (DCE)
- Burndy ID09533E4GX00 or equivalent

Table 4-22. COM1 Connector (P5) Pinout

Pin	Signal
1	nc
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	nc

4.3.14 COM2

- 9-pin male D-sub (DTE)
- JST JSEY-9P-1A3F19-13 or equivalent

Table 4-23. COM2 Connector (P4) Pinout

Pin	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.3.15 AT-bus Connector Pinouts

- AT-bus (XT side) (G2)
- 31x2, 0.100" [2.54 mm] pitch card edge

Table 4-24. AT-bus Connector (G2) Pinout

Pin	Signal	Pin	Signal
A1	IOCHCK#	B1	GND
A2	SD7	B2	RESETDRV
A3	SD6	B3	V _{CC}
A4	SD5	B4	IRQ9
A5	SD4	B5	n/c
A6	SD3	B6	DRQ2
A7	SD2	B7	n/c
A8	SD1	B8	0WS#
A9	SD0	B9	+12 V
A10	IOCHRDY	B10	GND
A11	AEN	B11	SMEMW#
A12	SA19	B12	SMEMR#
A13	SA18	B13	IOW#
A14	SA17	B14	IOR#
A15	SA16	B15	DACK3#
A16	SA15	B16	DRQ3
A17	SA14	B17	DACK1#
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH#
A20	SA11	B20	SYSCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	DACK2#
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	V _{CC}
A30	SA1	B30	OSC
A31	SA0	B31	GND

- AT-bus (AT side) (G1)
- 18x2, 0.100" [2.54 mm] pitch card edge

Table 4-25. AT-bus Connector (G1) Pinout

Pin	Signal	Pin	Signal
C1	SBHE#	D1	MEMCS16#
C2	LA23	D2	IOCS16#
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	DACK0#
C9	MEMR#	D9	DRQ0
C10	MEMW#	D10	DACK5#
C11	SD8	D11	DRQ5
C12	SD9	D12	DACK6#
C13	SD10	D13	DRQ6
C14	SD11	D14	DACK7#
C15	SD12	D15	DRQ7
C16	SD13	D16	V _{CC}
C17	SD14	D17	MASTER#
C18	SD15	D18	GND

4.4 CHIPSET REFERENCE

This section describes the chipset’s registers, I/O map, IRQs, and DMA channels.

4.4.1 Memory Map

The PicoPower* PC/AT* chipset supports 25 bits of the 32-bit physical memory address. Memory at addresses between 0 and the theoretical maximum (32 Mbyte system plus 1 Mbyte video) of 20FFFFFFH is mapped as follows:

Table 4-26. Memory Map

Address Range	Region	Cached
00000000-0009FFFFH	640K system memory	yes
000A0000-000BFFFFH	VGA memory	yes
000C0000-000C7FFFFH	Shadowed VGA BIOS	yes
000C8000-000CFFFFH	BIOS Extensions	yes
000D0000-000D7FFFFH	Free	yes
000D8000-000DBFFFFH	PC Card Window	yes
000DC000-000DFFFFH	RFA Window	yes
000E0000-000EFFFFH		yes
000F0000-000FFFFFFH	Shadowed BIOS	yes
00000000-01FFFFFFFH	DRAM (1 Mbyte Standard) Bank 0/1 (8MB Max) Local Address Space	yes
03000000-04FFFFFFFH	Flash SIMM (4 Mbyte, min) Bank 2/3 (8 Mbyte) Local Address Space	yes

C8000 - 0DFFFFH may be used either as page frame, BIOS extension, Flash and PC Card windows, I/O buffer (i.e., for extended memory managers, Ethernet, etc.) or may be used by DOS as upper memory blocks if an extended memory manager driver is installed.

The PicoPower chipset contains configuration and non-configuration registers. The configuration registers are not enumerated here. These should only be manipulated by the BIOS. The non-configuration registers are shown in the following table.

4.4.2 PicoPower Chipset Register Decodes

Table 4-27. PicoPower Chipset Registers

I/O Addr	Functional group	Usage
0BH	8237 DMA Controller	Shadow Registers 1,2,3,4,5,
020H	8259 Interrupt Controller	Shadow Register 1, 5, 6
021H	8259 Interrupt Controller	Shadow Register 2, 3, 4
022H		
024H	Chipset Programming	Index Register
026H	Chipset Programming	Data Register
040H	8254 Timer	Counter 0, Shadow Register
041H	8254 Timer	Counter 1, Shadow Register
042H	8254 Timer	Counter 2, Shadow Register
043H	8254 Timer	Counter 3, Shadow Register
061H	Port B	Misc. functions
070H	Port 70	Real time clock/NMI control
071H	Port 71	RTC Data
092H	Port 92	Misc. functions
0A0H	8259 Interrupt Controller	Shadow Register 7, 11, 12,
0A1H	8259 Interrupt Controller	Shadow Register 8, 9, 10,
0D6H	8237 DMA Controller	Shadow Registers 6, 7, 8,

4.4.2.1 Keyboard and Mouse Controller

Table 4-28. Keyboard Controller

I/O Address	Functional group	Usage
060H	Keyboard & Mouse	Data port
064H	Keyboard & Mouse	Command/status port

4.4.2.2 Serial Port 1 (COM1:)

Table 4-29. Serial I/O (COM1:) Port

I/O Addr	Usage
3F8H	Receiver/transmitter buffer
	Baud rate divisor latch (LSB)
3F9H	Interrupt enable register
	Baud rate divisor latch (MSB)
3FAH	Interrupt ID register
3FBH	Line control register
3FCH	Modem control register
3FDH	Line status register
3FEH	Modem status register
3FFH	Scratch Register

4.4.2.3 Serial Port 2 (COM2:)

Table 4-30. Serial I/O (COM2:) Port

I/O Addr	Usage
2F8H	Receiver/transmitter buffer
	Baud rate divisor latch (LSB)
2F9H	Interrupt enable register
	Baud rate divisor latch (MSB)
2FAH	Interrupt ID register
2FBH	Line control register
2FCH	Modem control register
2FDH	Line status register
2FEH	Modem status register
2FFH	Scratch Register

4.4.2.4 Parallel Port (LPT1:)

Table 4-31. Parallel I/O (LPT1:) Port

I/O Addr	Usage
378H	Data port
379H	Status port
37AH	Control port
37BH–37FH	EPP Address Ports - EPP Mode Only
778H–77AH	ECP Registers

4.4.2.5 IDE Hard Disk Drive

Table 4-32. IDE Hard Disk Drive

I/O Addr	Usage
1F0H	Task file registers
1F1H	(HCS0# to drive active)
1F2H	
1F3H	
1F4H	
1F5H	
1F6H	
1F7H	
3F6H	Misc. AT registers
3F7H	(HCS1# to drive active)

4.4.2.6 VGA/LCD Controller Cirrus Logic* CL-GD6245

Table 4-33. SVGA Controller

I/O Addr	Usage
3B4/3D4H	CRT controller index
3B5/3D5H	CRT controller ports
3BA/3DAH	Input status register 1
3C0H	Attribute controller write port
3C1H	Attribute controller read port
3C2H	Misc. Output (write)
3C3H	Video Subsystem Enable (LB Only)
3C4H	Sequencer index
3C5H	Sequencer ports
3C6H, 83C6H	Color Palette Mask
3C7H, 83C7H	Color Palette Read Mode Index
3C8H, 83C8H	Color Palette Write Mode Index
3C9H, 83C9H	Color Palette Data
3CAH	Feature control
3CCH	Misc. Output (read)
3CEH	Graphics controller index
3CFH	Graphics controller ports

4.4.2.7 PCMCIA Controller (CL-PD6710)

Table 4-34. PCMCIA Controller Registers

I/O Addr	Usage
03E0H	PCMCIA Index Register
03E1H	PCMCIA Data Register

4.4.3 IRQ map

The following table lists the signals that are connected to the PicoPower chipset’s interrupts for 82C59 compatibility.

Table 4-35. Interrupt Map

IRQ	Function	Source
IRQ0	Timer	PicoPower Chipset
IRQ1	Keyboard	82C42PE KB Controller
IRQ2	Cascade IRQ8-IRQ15	PicoPower Chipset
IRQ3	Serial Port	Super I/O Chip COM2, PCMCIA IRQ3, ISA IRQ3
IRQ4	Serial Port	Super I/O Chip COM1, PCMCIA IRQ4, ISA IRQ4
IRQ5	Available	PCMCIA IRQ5, ISA IRQ5
IRQ6	Floppy Disk	ISA IRQ6
IRQ7	Parallel Port	PCMCIA IRQ7, Super I/O Chip IRQ7, ISA IRQ7
IRQ8	Real Time Clock	PicoPower Chipset
IRQ9	Available	PCMCIA IRQ9, ISA IRQ9
IRQ10	Available	PCMCIA IRQ10, ISA IRQ10
IRQ11	Available	PCMCIA IRQ11, ISA IRQ11
IRQ12	Mouse	82C42PE IRQ12, PCMCIA IRQ12, ISA IRQ12
IRQ13	Floating Point	Not Used
IRQ14	Hard Disk	PicoPower Chipset, ISA IRQ14, PCMCIA IRQ14
IRQ15	Available	PCMCIA IRQ15, ISA IRQ15
NMI	Parity Error, IOCHCHK	Not Used

4.4.4 DMA Channels

The PicoPower chipset supports two 8237 like DMA controllers. There are 7 sets of DMA registers supported within the PicoPower chipset. Note that DMA Channel 4 is not used.

Table 4-36. DMA Usage

DMA Channel		Function	Source
DRQ0	DACK0	(8Bit) Available	ISA
DRQ1	DACK1	(8Bit) Available	ISA
DRQ2	DACK2	(8Bit) Floppy Disk	ISA, Super I/O
DRQ3	DACK3	(8Bit) Parallel Port	ISA, Super I/O
DRQ5	DACK5	(16Bit) Available	ISA
DRQ6	DACK6	(16Bit) Available	ISA
DRQ7	DACK7	(16Bit) Available	ISA

4.5 SCHEMATICS

The floppy diskette labeled Schematics contains a self-extracting executable file called HUMBOARD.EXE. These files are OrCAD/SDT* II schematics and libraries, and postscript print files of each schematic sheet.

The following is a list of the schematic sheets, including the major integrated circuit items on each:

Table 4-37. Schematics

Sheet#	Filename	Major Components
1	HUMBIRD.SCH	ULP486SX
2	HUMREDW.SCH	PT86C718A2
	HUMREDW.SCH	PT86C768A2
3	HUMDRAM2.SCH	DRAM/FLASH SIMM Sockets
4	HUMSER.SCH	FDC37C6651R
5	HUMKB.SCH	S82C42PE
6	HUMVGA.SCH	CL-GD6245 VGA Controller
7	HUMCARD2.SCH	CL-PD6710-VC PCMCIA controller
8	HUMFFS.SCH	E28F008SA Flash File Device
	HUMFFS.SCH	XC2018-70TQ100C
9	HUMBB.SCH	E28F004BV-T120C Boot Block Flash device
10	HUMCLK.SCH	ICS9133-01CW20 Clock Synthesizer
	HUMCLK.SCH	MAX696CWE Reset controller
11	HUMISA2.SCH	ISAbus and power connectors



5

BIOS Software Reference



CHAPTER 5

BIOS SOFTWARE REFERENCE

5.1 POWER-ON SCREEN DISPLAY

When you turn on the power or reset the evaluation board, the system performs a power-on self-test (POST). The POST displays information showing the status of the BIOS self-test.

When errors occur during the power-on self-test, the BIOS displays the error on the appropriate line of the screen display and continues the boot process. It is important to watch the POST display to verify that no errors occur.

```
PhoenixBIOS Version 4.04
Copyright 1985-1995 Phoenix Technologies Ltd., All Rights Reserved
Copyright 1995 by RadiSys Corp. Version 1.00.00

CPU = INTELSX 25 MHz
0000640K System RAM Passed
0003072K Extended RAM Passed

System BIOS Shadowed
Video BIOS Shadowed
UMB upper limit segment address: F673
Diskette drive A error

Press <F1> to resume, <F2> to Setup
```

Figure 5-1. POST Display with Error

In the case above, floppy drive A: is not configured correctly. The screen image appears approximately as shown.

If error messages are displayed during or after the POST display, see Chapter 5, *Error Messages*.

5.2 BIOS SETUP SCREENS

The evaluation board's PhoenixBIOS* contains a BIOS Setup function to enable the user to display and alter the system configuration. This information is maintained in the evaluation board's nonvolatile CMOS RAM (located in the PicoPower* chipset) and is used by the BIOS to initialize the hardware.

This section describes the various menus and sub-menus that are used to configure the system. Your system may use the BIOS defaults and thus require very little intervention. This section is written as though you are encountering each field in sequence and for the first time.

During the setup and configuration of the evaluation board, a monitor and keyboard are required.

The BIOS Setup can only be entered following a power-up, CTRL-ALT-DEL, or equivalent. Press the F2 key when prompted to enter Setup.

NOTE

The prompt to press the F2 key to enter the BIOS setup can optionally be suppressed in the BIOS setup. However, you can still press the F2 key to enter the BIOS setup screens, even if the prompt is suppressed.

Use the up and down arrows to move from field to field. Use the right and left arrows to move from menu to menu, as noted in the menu bar at the top of the screen. When you use the arrow keys to leave a menu and then return, your active field is always at the beginning of the menu. When you select a sub-menu and then return to the Main Menu, you return to that sub-menu heading.

Fields with a triangle to the left are sub-menu headings. For most fields, position the cursor at the field and from the numeric keypad, press the + and - keys to scroll through the available choices. Certain numeric fields can also be entered via the keyboard. Once the entry has been changed to appear as desired, use the up and down arrow to move to the next field. When finished, move to the Exit Menu and use the options there to save changes and exit.

5.3 BIOS SETUP MAIN MENU

The BIOS Setup Main menu is shown below:

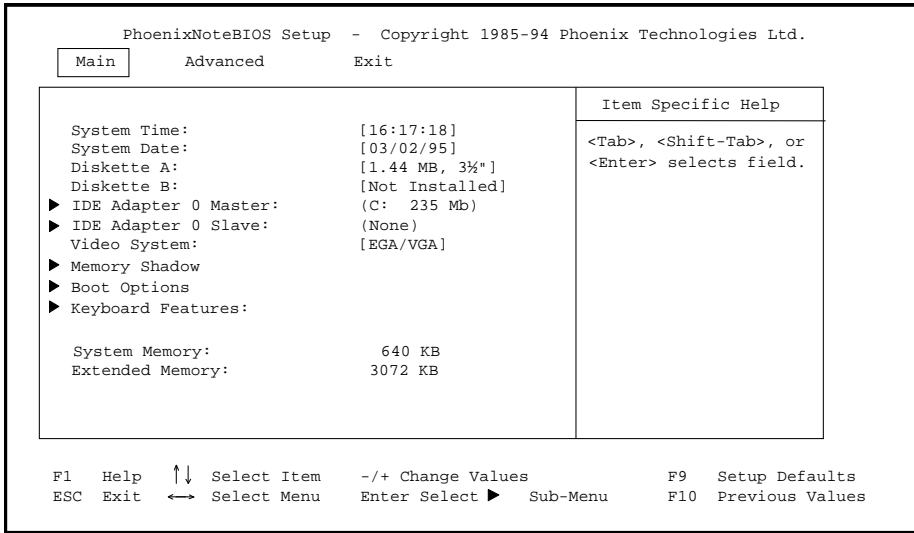


Figure 5-2. BIOS Setup Main Menu

The fields in each menu and sub-menu are explained below. Additional help information is available in the help area on each BIOS screen.

5.3.1 System Time:/System Date

These values are changed by moving to each field and typing in the desired entry. Use the tab key to move from hour to minute to second, or month to day to year.

5.3.2 Diskette A/Diskette B

This field identifies the type of floppy disk drive installed as the A: drive. An ISA-bus floppy drive controller card is required for this operation. When the evaluation board has a floppy drive installed, the proper setting is usually for a 1.44 MB floppy disk drive. Other options include 360K, 720K, 1.2 Mbytes, and 2.88 Mbytes. When no drive is installed, the proper setting is Not Installed.

5.3.3 IDE Adapter 0 Master/Slave Sub-Menus

These fields are headings for menus that allow you to enter complete disk drive information. Once the information is entered for the drive, the entry in the Main Menu shows the drive selected. For more information, turn to the section concerning the IDE Adapter Menus.

5.3.4 Video System

These fields are the three basic settings to use with your monitor: EGA/VGA, CGA 80x25, and Monochrome.

5.3.5 Boot Options Sub-Menu

The Boot Options Sub-menu allows you to change the boot delay, boot sequence, and disable several displays during the boot process, such as the SETUP prompt, POST errors, floppy drive check, and summary screen. Once you have set the boot sequence, your choice appears in this entry in the Main Menu. For more information, turn to the section concerning the Boot Options Sub-menu.

5.3.6 Keyboard Features (Numlock) Sub-Menu

Use this menu to enable or disable various keyboard features, including enabling the Numlock key, enabling the key click, and setting the keyboard auto-repeat rate and delay. The Numlock setting appears for this entry in the Main Menu. For more information, turn to the section concerning the Keyboard Features Sub-menu.

There are two more lines on the Main BIOS Setup Screen: “System Memory” and “Extended Memory.” These are display-only fields set by the BIOS.

5.3.7 IDE Adapter Sub-Menus

There are two IDE adapter sub-menus: one for the master drive and one for the slave drive. The master drive is the C: drive. To see the detailed characteristics of the device or to change the device, choose the IDE Adapter 0 Master Sub-menu to configure the fixed disk. The following screen appears:

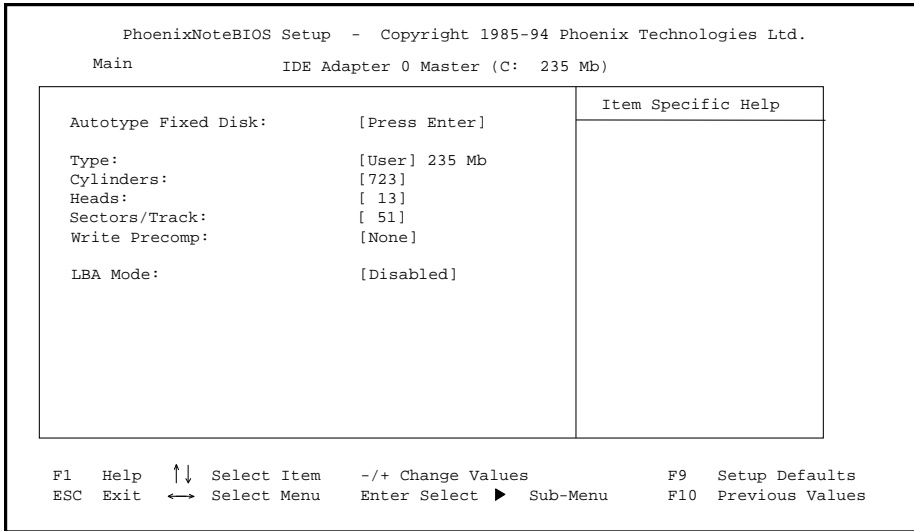


Figure 5-3. IDE Adapter Sub-menu

5.3.7.1 Autotype Fixed Disk

Use this option when setting up new disks. This option allows the BIOS to determine the proper settings of the disk based on information on the disk, which is detected by the BIOS for drives that comply with ANSI specifications.

Existing (formatted) disks must be set up using the same parameters that were used originally when the disk was formatted. You must enter the specific cylinder, head, and sector information as listed on the label attached to the disk drive at the factory. Note that if the disk drive was formatted incorrectly, the Autotyping function detects the disk drive’s correct parameters, NOT those used during the formatting. In that case, use the “User” type as described below.

5.3.7.2 Type

Select “None” when you are not using an IDE hard disk drive. When you have an IDE disk but cannot employ the “Autotype” feature, then select “User” for the Type and enter the correct drive values for cylinders, heads, and sectors/track from the disk’s documentation.

5.3.7.3 LBA Mode Control

You can enable or disable Logical Block Addressing (LBA) as needed. LBA is a method used by newer, larger hard disk drives that are configured in logical blocks as opposed to the old cylinders/heads/sectors method. Autotyping can override your selection here. The default is to use the standard mode, i.e., to leave LBA mode control disabled. Refer to your hard disk drive’s documentation for more details.

Once you have completed the setup for the IDE Master, you can choose the IDE Adapter 0 Slave Sub-menu to configure your second drive. The information required is similar to Master drive setup. When finished, press the Esc key to return to the Main Menu.

5.3.8 Memory Shadow Sub-Menu

The term “Memory Shadow” refers to the technique of copying information from ROM into RAM and accessing it in this alternate memory location. The Memory Shadow Sub-menu is discussed below.

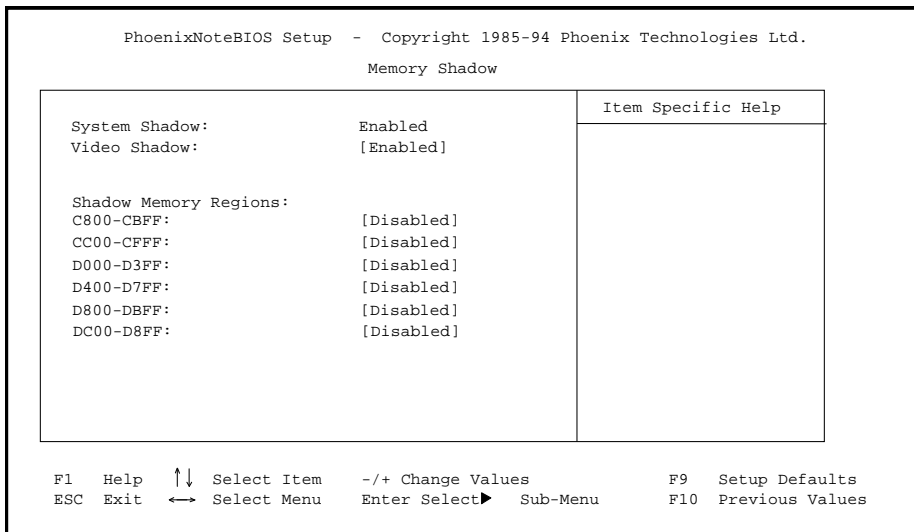


Figure 5-4. Memory Shadow Sub-menu

5.3.8.1 Using Shadow Memory Regions

The shadow regions should be used only when a module is installed in the system that contains a BIOS ROM. Enabling shadowing for the region occupied by the ROM increases system performance.

Do not enable shadowing for the same region specified for TFFS. When this ROM extension is installed, it is automatically shadowed. Do not enable shadowing for D800-DFFFH when the TFFS BIOS extension is enabled.

To exit this menu, press the Esc key. You return to the Main Menu.

5.3.9 Boot Options Sub-menu

The Boot Options Sub-menu allows you to change the boot sequence options. The following appears:

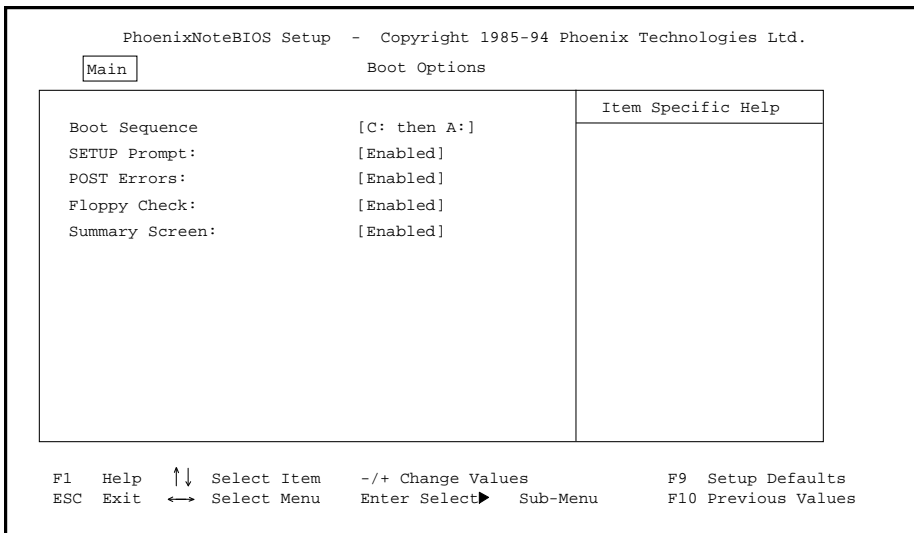


Figure 5-5. Boot Options Sub-menu

5.3.9.1 Boot Sequence

Use this option to define how the system treats floppy drive A: when booting. You can boot from a floppy in the A: drive or boot directly from the fixed disk drive. To reduce the amount of time required to boot, set the boot sequence to use the C: drive only. Note that the C: drive may be a formatted IDE drive, formatted RFD, or a formatted PC Card. The options are as follows:

- A: then C:** Used to boot from the floppy disk drive, or when no floppy is present in the A: drive, boot from the C: drive. This is the default setting.
- C: then A:** Used to boot from the C: drive, whether Flash or IDE, or when none is present, boot from the A: drive.
- C: only** Used to boot from the C: drive without searching for an A: drive.

5.3.9.2 SETUP Prompt

Use this option to enable or disable the message “Press F2 to enter Setup.” Even if the message is disabled, you can still press the F2 key to enter the Setup Menu. The default is to enable this prompt.

5.3.9.3 POST Errors

Use this option to stop during the boot if the system encounters error messages. Otherwise, the system continues to attempt to boot despite any startup error messages that display. The default is to enable this option, meaning the system stops on encountering errors during the POST process.

5.3.9.4 Floppy Check

Use this option to enable or disable the floppy drive search during the boot. To speed up booting, you can disable the floppy check. It is still possible to boot from the A: drive even with the floppy check disabled. The default is to disable the floppy check.

5.3.9.5 Summary Screen

Use this option to enable or disable a summary of the system configuration, which appears before the operating system starts to load. To save time, you can disable the summary screen. The default is to enable the summary screen display.

When you have completed the Boot Options Menu, exit back to the Main BIOS Setup Menu using the Esc key and complete the Keyboard Features Sub-menu.

5.3.10 Keyboard Features Sub-menu

Use this sub-menu to enable or disable various keyboard features.

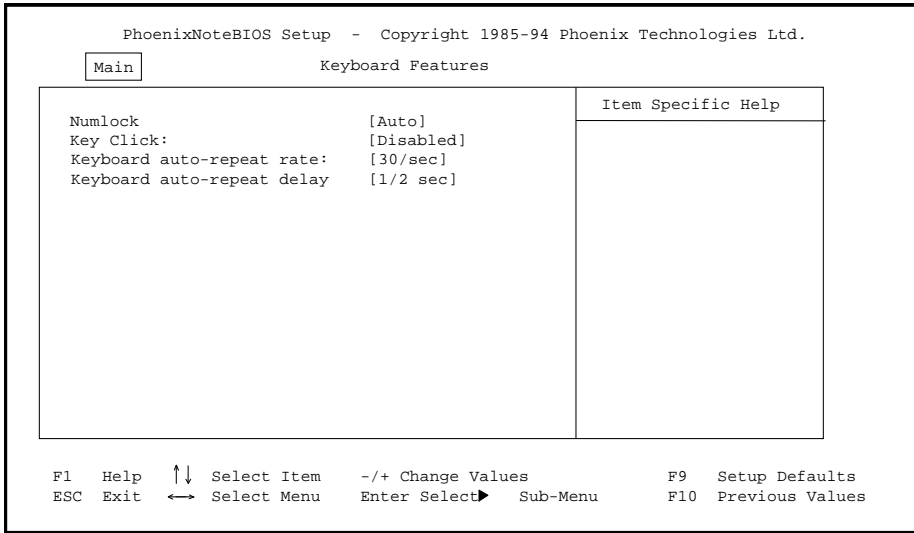


Figure 5-6. Keyboard Features Sub-menu

5.3.10.1 Numlock

Use this option to enable or disable the Numlock feature of the keyboard. This enables the use of the keypad numbers. The default is Numlock enabled.

5.3.10.2 Key Click

Use this option to enable or disable the key click feature on the keyboard. When enabled, the keyboard produces an audible click each time a key is pressed.

5.3.10.3 Keyboard Auto-Repeat Rate

Use this option to set the auto-repeat rate when holding a key down on the keyboard. The rates increment from two to 30 per second.

5.3.10.4 Keyboard Auto-Repeat Delay

Use this option to set the delay between when a key is pressed and when the auto-repeat feature begins. Options are 1/4, 1/2, 3/4, and one second.

5.4 BIOS SETUP ADVANCED MENU

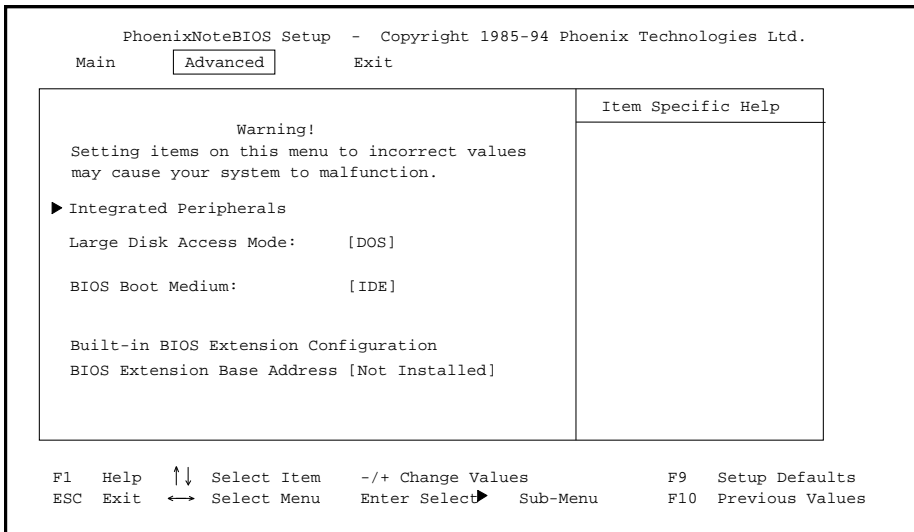


Figure 5-7. Advanced Menu

The Advanced Menu contains settings for integrated peripherals, memory shadow, large disk access mode, and setting the M-Systems* TFFS BIOS extension base addresses.

5.4.1 Integrated Peripherals Sub-Menu

Use this option to select the Integrated Peripherals sub-menu, in order to configure the COM ports, LPT port, IDE controller, and UART2 mode (IrDA mode). This sub-menu does not configure video, or Flash memory. For more information, turn to the section concerning the Integrated Peripherals Sub-menu.

5.4.2 Large Disk Access Mode

When using a drive larger than 528 MBytes, and using the DOS operating system, set this option to DOS in order to access the full size of the disk. Set this option to Other when using a different operating system, such as UNIX, Novell* Netware*, etc. Under DOS, when you do not set this feature you cannot access more than 528 MBytes on larger hard disks.

5.4.3 BIOS Boot Medium

Select from three different boot options: IDE, PCMCIA, or Resident Flash Array (RFA).

- Use IDE when you are booting normally from an IDE hard disk drive or a floppy disk connected to an IDE controller.
- Use PCMCIA when booting from a PC Card.
- Use RFA when booting from the Resident Flash Array.

A flash memory PCMCIA card and the evaluation board's onboard RFA can each be programmed to emulate a mass storage device. Either one can hold a bootable disk image. They must be formatted before they work as the boot medium. The IDE hard disk must be disabled to boot from a PC Card or from the RFA.

5.4.4 Built-in BIOS Extension Configuration

5.4.4.1 M-Systems TFFS BIOS Base Address

Use this option to enable and locate the M-Systems TrueFFS Boot BIOS extension program on the evaluation board. The BIOS extension must be enabled for the Flash memory to be used as a bootable drive. The base address defines the segment where the BIOS extension is installed. Be sure to exclude this area and the memory window at D800-DFFFH when using a memory manager such as EMM386.

Valid options are the following:

- C800-CFFFH (address C8000 - CFFFFH)
- D000-D7FFH (address D0000 - D7FFFH)
- Not Installed

5.4.5 Integrated Peripherals Sub-Menu

Use the options in this sub-menu to enable or disable the COM ports, the parallel port, the diskette controller, the IDE controller, and UART2 mode on the infrared port.

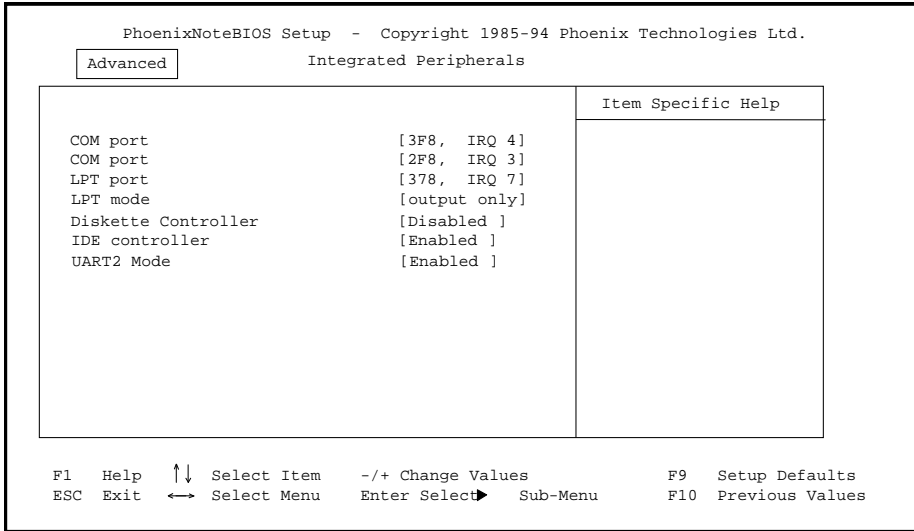


Figure 5-8. Integrated Peripherals Sub-menu

5.4.5.1 COM Port/COM Port

Use this option to enable and configure or disable the COM1 and COM2 ports present on the evaluation board. The COM ports are user-definable for their address range and interrupt.

The first entry in the menu refers to the COM1 port at P4, near the lower corner of the board. The second entry in the menu refers to the COM2 port at P5, next to the VGA connector. COM2 is also used for the infrared connector, or for a non-PS/2* style mouse.

5.4.5.2 LPT Port

Use this option to enable and configure or disable the LPT (parallel) port. The LPT port is user-definable for the address range. The default for LPT1 is 378. The IRQ is set to IRQ7.

COM and LPT ports not enabled on the evaluation board can be used on a user-supplied ISA-bus expansion card.

5.4.5.3 LPT Mode

Use this option to enable the onboard parallel port to operate as an Extended Capabilities parallel port (ECP). The ECP mode is for devices requiring higher data transfer rates; it also provides symmetric bi-directional communication.

5.4.5.4 Diskette Controller

Disable this option. There is no floppy controller header to connect to. Use a floppy disk drive controller card (which includes a hard disk controller) in your ISA-bus passive backplane to access a floppy drive.

5.4.5.5 IDE Controller

Use this option to enable or disable the onboard IDE controller. For example, when using an IDE controller card in the passive backplane to access a floppy drive, you may find it more convenient to use the card for both the floppy drive and the hard drive. In that case, disable the onboard IDE controller to prevent a conflict.

5.4.5.6 UART2 Mode

Use this option to select operating mode for the infrared port on COM2. There are three options:

Standard mode	Standard RS-232 type signalling
IrDA	Allows transfer rate up to 115 Kbaud
ASkIR	Amplitude Shift keyed Infrared. Allows baud rates of up to 19.2 Kbaud.

When you are finished, press Esc to exit back to the Advanced Menu.

5.5 BIOS SETUP EXIT MENU

Use the options in this menu to save your edit(s) as you go along or when you exit back to the boot process. You can also exit without saving the edits, or go back to the original default setups installed at the factory.

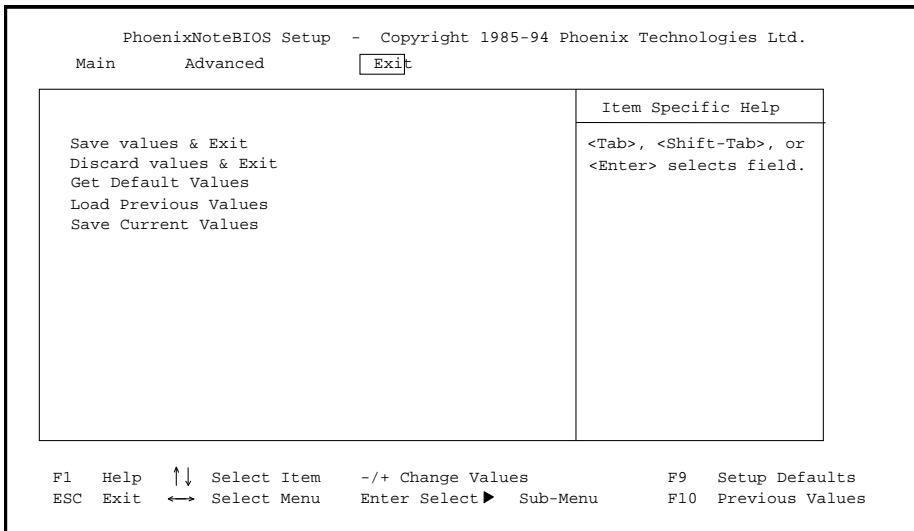


Figure 5-9. Exit Menu

5.5.1 Save Values & Exit

Use this option when you want to save the values you have just entered to battery-backed CMOS and then exit back to the boot process. The new values are loaded, and the system reboots using the new BIOS settings.

5.5.2 Discard Values & Exit

Use this option when you want to discard the changes you just made and set the system back to the BIOS as it was before you started making changes. The system boots with the old values.

5.5.3 Get Default Values

Use this option when you need to reset the BIOS values all the way back to the original, default values that were configured at the factory. You do not exit from the BIOS setups, so you can review the defaults and continue editing if you wish.

5.5.4 Load Previous Values

Use this option when you want to immediately re-load the system with the previous values before this editing session started. These are not the defaults loaded at the factory; these are the values present in the CMOS that were in use before the current editing session began. You do not exit, so you can review the changes made as a result of this selection. You can resume editing if necessary.

5.5.5 Save Current Values

Use this option to save the edits you have made during this session. You do not exit, and you can resume editing. This is useful for lengthy editing sessions involving several screens.



6

Installing VGA Drivers and Utilities



CHAPTER 6

INSTALLING VGA DRIVERS AND UTILITIES

The Ultra-Low Power Intel486™ Processor Evaluation Board contains a Super VGA (SVGA) graphics controller using the Cirrus Logic* SVGA CL-GD624X chip. The SVGA chip provides SVGA modes up to 800x600 on flat-panel displays, and CRT displays of 800x600 in 65,536 colors, and 1024x768 in 256 colors (non-interlaced). The controller is connected to the CPU local bus to give the best possible graphics performance.

While the VGA controller can use 1 Mbyte of video RAM, the evaluation board video RAM is limited to 512 Kbytes, implemented with one 256 Kbyte x 16 DRAM. This means that the VGA controller subsystem provides up to 256 colors for 800x600 and 640x480 displays. It provides up to 16 colors for 1024x768 displays.

6.1 DISPLAY DRIVERS AND UTILITIES SOFTWARE

The SVGA Driver and Utilities Software is supplied by Cirrus Logic. There are two diskettes: one for DOS and one for Microsoft* Windows* 3.1x. Be sure to check for READ.ME files on both diskettes before starting the installation. Portions of this Chapter are copyrighted by Cirrus Logic, Inc.*

For DOS users, the CLMODE VGA software utility program is used to configure flat-panel display options, define the type of monitor attached, and set the video modes supported by the Cirrus Logic chipset. CLMODE is supplied with your Cirrus Logic SVGA software. The following section describes these utilities and how to use them.

For Windows users, the WINMODE utility is used to configure Windows for use with the Cirrus Logic chipset, just as CLMODE works for DOS.

6.1.1 Before You Begin

The following instructions assume that you are familiar with DOS and certain DOS commands. Please review the associated DOS commands before performing the installation.

6.1.2 Contacting Cirrus Logic

If there are any newer versions of the software provided with your SVGA adapter, they are available on the Cirrus Logic BBS or their Web site.



The BBS phone number is (510) 440-9080. It can handle modems running up to 9600 baud. The modem should be set to NO parity, 8 data bits, 1 stop bit. Before you are able to download software, you must join the conference(s) for the product(s) that you are interested in.

The URL for the Cirrus Logic Web site is [HTTP://WWW.CIRRUS.COM](http://WWW.CIRRUS.COM).

6.2 DOS INSTALLATION

The installation utility is provided to facilitate the smooth installation of the display drivers and utility software. The installation program is menu-driven and allows you to select and install only those display drivers for software and applications currently in use.

It is important to note that some display drivers must have the associated vendor's application program already installed on the system prior to loading the Cirrus Logic SVGA display drivers. In other cases, the loading of the display driver may be an integral part of the vendor's product installation process. Please review the driver product section below for specific instructions prior to running the installation program.

This installation assumes that you have a floppy controller and floppy disk drive in your system. This requires that the evaluation board be installed in a passive ISA backplane with a floppy controller card or use some other workaround.

The DOS installation utility is located on the diskette labeled VGA Disk 1 of 2. To install the desired display drivers and utilities, insert the diskette into the A: drive, then type the following:

```
A:  
INSTALL
```

This begins the installation for the English version of the software. Follow the instructions on the screen to install the listed display drivers and Cirrus Logic software. The installation process asks you the destination directory, then gives you the option to install the Cirrus Logic GD624x Utilities, as well as several other application drivers. It is recommended that you only choose the Utilities. Press the space bar to toggle the selection field to a Yes. At any time you may press Esc to abort the installation process and go back to DOS.

6.3 CLMODE

The DOS utility CLMODE allows you to configure the panel options, define the type of monitor attached, and set the video modes supported by the Cirrus Logic chipset.

6.3.1 Using CLMode's Menu-driven Interface

At the DOS prompt type: **CLMODE**

The main popup window consists of a number of buttons. Each button represents a different option or menu. The underlined letter of a button name specifies the hot key combination for that item. For example, press the Alt key and the underlined letter keys simultaneously or just the underlined letter key to select an option. Note that to use a mouse, a mouse driver should be installed prior to running the CLMODE utility in order to use the mouse pointer for button selection.

6.3.2 Configuring the Attached Monitor

Selecting the proper monitor brand and model allows the Cirrus Logic chipset to display the highest quality output that it is capable of with the attached monitor. The monitor type determines what video modes are available to your system. It also determines the vertical refresh rates available. Generally, the higher the refresh, the better the screen looks.

Configuration	You can select from several options, including reverse video setup, bold fonts, panel expanded mode, panel power, black and white enhancement, CRT high refresh, display, graphics shading, text shading, and vertical position.
Monitor Type	There are eight possible choices for the type of monitor, ranging from straight VGA through to extended super multi-frequency monitors. You can test your selection using the Verify button.
Video Modes	Based on your monitor type selection, you can preview various video modes to determine which one your system can support. The evaluation board can support 800x600 in 256 colors, 640x480 in 256 colors, or 1024x768 in 16 colors.
About	Use this button to determine the CLMode Utility Program's version number.
Exit	When you exit the program, you can automatically install the settings you have chosen into the AUTOEXEC.BAT file, so that every time your system boots up the correct VGA modes are present.

Note that there is on-line help available in this screen for each of the three main choices: Configuration, Monitor Type, and Video Modes.

On many systems the monitor type is maintained from one session to the next. To test this, select a monitor type and exit the CLMODE program. Turn the computer off for ten seconds. After rebooting the computer, run CLMODE and verify whether or not the monitor that you selected is still enabled. If it is, it should not ever need to be set again in normal use.

If the monitor type was not kept then you should select the option to have CLMODE save the monitor type in your AUTOEXEC.BAT file. You are given this choice after selecting the Exit button.

6.3.3 Using CLMODE's Command Line Options

When command line options for CLMODE.EXE are given at the DOS prompt, the menu-driven windows are not displayed. Instead, configuration, monitor type, video mode and refresh rate are set at the DOS prompt. The command line options for CLMODE.EXE are listed below:

CLMODE {modenum} {m{montype} | {s n} }

Where:

- {modenum}** Mode number
- {montype}** Monitor type
- s** List status information.

Valid mode numbers:

- 0 VGA
- 1 8514
- 2 SVGA
- 3 Extended Super VGA
- 4 Multi-frequency
- 5 Extended Multi-frequency
- 6 Super Multi-frequency
- 7 Extended Super Multi-frequency

Valid monitor types:

t6=x(Hz)	640x480 @ (0 = 60, 1 = 72)
t8=x(Hz)	800x600 @ (0 = 56, 1 = 60, 2 = 72)
t1=x(Hz)	1024x768 @ (0 = 87i, 1 = 60, 2 = 70)
t2=x(Hz)	1280x1024 @ (0 = 87i, 1 = Not available)

For example, to set video mode 3:

CLMODE 3

For example, to select custom monitor timings with 640x480 at 60Hz and 800x600 at 72Hz refresh type:

CLMODE t6=0 t8=2

Typing an invalid option displays the command line help text.

Using [S] as a command line option displays the current CLMODE settings.

6.3.4 Other Utilities

There are six additional utility programs present on the Cirrus Logic Utilities diskette:

CRT.EXE	Resets CRT mode
PANEL.EXE	Starts PANEL mode
SIMUL.EXE	Simultaneous mode
SWITCHER.COM	Switches from CRT to PANEL
BOLD_DRV.COM	Uses bold font for driver
TSRFONT.COM	A TSR for font display

To learn more about these utilities, reference the README.TXT file on the diskette or contact Cirrus Logic.

6.4 WINDOWS INSTALLATION

The Windows installation utility is located on the diskette labeled VGA Disk 2 of 2. To install the desired Windows display drivers and utilities, you must be running Windows. Insert the diskette into the A: drive, then either use File Manager or the File/Run method to execute **A:\INSTALL.EXE**.

Follow the instructions on the screen to install the listed display drivers. A warning message displays informing you that you should be using the standard Windows VGA or SVGA driver to proceed. Users who are running Windows under OS/2 also receive additional instruction.

You can tailor the installation to your needs by selecting the destination drive and directory. Be sure to enter a directory so that the installation does not simply dump files into your root. Once the software is copied from the distribution diskette, the installation creates a VGAUTIL group and fills in icons for WinPanel, WinMode, and ChangeTo. Finally, the WINMODE application starts, seeking information about your current monitor and drivers.

6.5 WINMODE

The WINMODE utility runs under Windows 3.1 and allows you to change the screen resolution, number of available colors, and to select either large or normal size fonts and system resources.

This application assumes that the basic Windows VGA drivers are currently installed and configured using Windows Setup.

When you are unsure what resolutions and colors your video card can support, refer to the section of this manual on CLMode for information on how to determine available resolutions.

WINMODE is run by selecting the WINMODE icon. The first time that you run WINMODE, the settings for the current driver won't be correct; after you set them once, they are correct from then on.

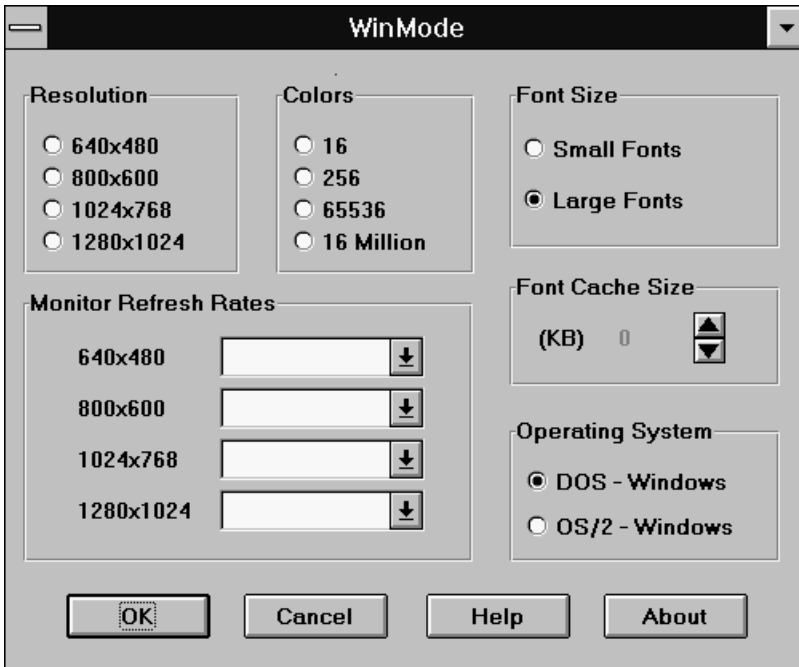


Figure 6-1. WinMode Screen Display

The following selections are made in WINMODE:

- Resolution** If you are unsure, select a safe setting to start, such as 800x600.
- Colors** If you are unsure, select a safe setting to start, such as 16 or 256.
- Font Size** You can choose between large and small fonts. With smaller monitors, the larger fonts are more readable. Small fonts are for large monitors with higher resolutions.
- Monitor Refresh Rates** Once the resolution and colors are selected, WINMODE displays several options for refresh rates at various settings. For some settings, there may be only one refresh rate option available. Note also that some of the higher resolutions may not be supported.
- Font Cache Size** You can increase or decrease the font cache size, depending on your needs. The font cache is memory available for saving bitmaps of frequently used fonts. WINMODE tries to set the optimum cache size for you, but you can make adjustments as necessary.
- Operating System** Choose between DOS-Windows and OS/2-Windows.

After new options have been selected, click the OK button. You are asked if you are ready to restart Windows in order for your changes to take effect. If you choose 'No', then the changes you made are discarded.

6.6 WINDOWS DISPLAY DRIVERS

The Cirrus Logic video controller is 100% VGA compatible. The display drivers described in this manual are supplied to improve the resolution for each supported software application package.

The installation instructions for each display driver follow the introduction section. Follow the instructions carefully to be sure that each display driver is correctly installed. All of the installation instructions assume that VGA Disk 2 of 2 is located in drive A:. If drive B: is used, the instructions should be changed appropriately.

NOTE

These instructions assume that you are familiar with DOS and DOS commands. Please review the installation instructions and the associated DOS commands before attempting the actual installation.

Not all video modes are available on the evaluation board. If an extended mode driver is installed for a video mode that is not available, the application program does not function properly. There are a number of things that determine the list of available video modes. Some of these include the current monitor type, the amount of installed memory, and the revision of the controller. To determine which modes are available before beginning the driver installation, run the CLMODE program and examine the list of available video modes.

6.6.1 Before Upgrading From a Previous Release

Before installing the new drivers, you should use Windows Setup to select the default VGA or SVGA video driver so that when you install the new drivers, there is no chance of overwriting the driver that Windows is using to control your screen. Next go to the system directory, and find a file that is named OEM?.INF where the question mark is a number. There may be more than one of these. These files are the different OEMSETUP.INF files that have been used to configure Windows for different devices. Using a text editor, such as Notepad or Edit, look at them until you find the one that is for the previous version of the Cirrus Logic video drivers and delete it. This is not completely necessary, but if you do not delete old files the drop down box for Setup becomes cluttered with different versions of the same files. In many cases, the old files have been overwritten by newer ones, and no longer exist.

6.6.2 Installing Windows 3.1 Display Drivers

If you have not already installed the WINMODE utility program, follow these instructions to install a single driver for a single resolution. If you want to be able to easily switch between different resolutions, you should install WINMODE before this procedure (refer to *Windows Installation*).

Windows 3.1 drivers can be installed from the DOS Windows Setup program or from the Windows Setup program. To install the Windows 3.1 drivers from the DOS prompt, proceed as follows:

1. Check that Windows 3.1 is already installed on your computer.
2. From your Windows directory, at the DOS prompt, type **SETUP** and press Enter. Follow the instructions on the screen. When you come to the screen which lists the hardware and software components such as display adapter (e.g. VGA, CGA, etc.), keyboard type, mouse type, etc., go to the Display selection by using cursor keys to move the highlighted bar and press Enter.
3. From the next menu listing of display options, scroll to the bottom of the list, and highlight the following text:

Other (Requires disk provided by a hardware manufacturer)

Press Enter, and when prompted, insert the Windows Display Driver diskette into drive A:\ and type:

A:

4. The list of drivers and their associated resolutions appears:

CIRRUS 624X V1.0, 1280X1024X16 **

CIRRUS 624X V1.0, 1024X768X16

CIRRUS 624X V1.0, 640X480X16

CIRRUS 624X V1.0, 640X480X256

CIRRUS 624X V1.0, 640X480X64K **

CIRRUS 624X V1.0, 800X600X16

CIRRUS 624X V1.0, 800X600X256

**** = not supported on the evaluation board**

5. Highlight the desired choice by moving the cursor to the correct display driver, and then press Enter.
6. Continue with the remainder of the setup procedure.

To install the Windows 3.1 drivers from the Windows Setup program, proceed as follows:

1. Ensure that Windows 3.1 is already installed on your computer and start Windows.
2. From the Main window of the Program Manager run the Windows 3.1 Setup program.
3. Select Change Systems Settings... from the Options menu of Setup.
4. Click on the down arrow at the right side of the Display: line. Scroll to the end of the list of available display drivers and select Other display (Requires disk from OEM)....
5. Insert the Windows display driver diskette into drive A: and type A:\ as the path name, then choose OK.
6. The list of available drivers and their associated resolutions appears:

CIRRUS 624X V1.0, 1280X1024X16 **

CIRRUS 624X V1.0, 1024X768X16

CIRRUS 624X V1.0, 640X480X16

CIRRUS 624X V1.0, 640X480X256

CIRRUS 624X V1.0, 640X480X64K **

CIRRUS 624X V1.0, 800X600X16

CIRRUS 624X V1.0, 800X600X256

**** = not supported on the evaluation board**

7. Highlight by moving the cursor to the desired display driver, and then choose OK.
8. Continue with the remainder of the setup procedure. The changes do not take effect until Windows is restarted.

6.7 WINDOWS 95 AND OTHER OPERATING SYSTEMS

If you are using Windows 95, the operating system will identify and install the required 32-bit drivers for the Cirrus Logic video controller using the operating system's installation software.

Contact Cirrus Logic for information about other operating systems compatible with the Cirrus Logic 624X video controller.



7

Using Flash Disks



CHAPTER 7 USING FLASH DISKS

This chapter contains information about formatting and using the RFA and PC Card disks. The M-Systems* software designed specifically for the Ultra-Low Power Intel486™ Processor Evaluation Board is shipped on a single diskette marked with the M-Systems label. Command line options for the device driver and syntax for the formatting command are included on the diskette in a file named TFFS32.DOC. This .DOC file is the TrueFFS* user's guide.

7.1 AN OVERVIEW OF TRUEFFS

TFFSBIOS is the TrueFFS module that enables BIOS disk emulation on Flash media.

The TrueFFS DOS device drivers included provide full read-write capability to Flash media like other DOS drives. In order to emulate fixed disks, provide the capability of booting from a Flash disk, and avoid the necessity for installing software drivers, it is necessary to use the TFFSBIOS module.

TFFSBIOS provides the same basic functionality provided by the TrueFFS device drivers: it reads and writes from Flash media. However, it occupies a very different position in the system which enables it to fully emulate fixed disks and provide true booting capability. For this reason, its installation is very different from the installation of a device driver.

TFFSBIOS is installed as a BIOS extension. A BIOS extension is a software module that resides in high memory (range C8000-EFFFH), and is automatically called by the system BIOS at boot time for initialization.

If the installation is successful you will see an opening announcement of TFFSBIOS briefly on your screen, and a new DOS drive letter will be available. TFFSBIOS installs the Flash medium as the last fixed disk in the system, so that if you previously had one fixed disk C:, the Flash medium will now appear as fixed disk number 2, drive D:.

You may now make the new fixed disk bootable using the DOS FORMAT or SYS command. For example,

```
SYS D:
```

or

```
FORMAT D: /s
```

DOS normally loads an operating system from the first fixed disk in the system (C:), so that your system will load DOS from the flash medium only when there is no IDE hard disk.

TFFSBIOS is installed as a server of BIOS interrupt 13 (disk system). This is a standard BIOS interface, which provides a standard interface to all disk controllers (IDE hard disk, floppy, RAM disk, etc.) in the system. The interrupt 13 servers for the IDE hard disk and floppy disks are embedded in the PhoenixBIOS. TFFS BIOS becomes an extension to this interface during initialization.

More than one fixed disk may be installed by the BIOS. The BIOS numbers disks starting at 80 hex, so that the first disk is 80H, the second 81H, etc. The first disk acts as the boot device.

By default TFFSBIOS installs as the last disk in the system, so that the drive letters for existing disks are not changed, and if there is a hard disk in the system, the system will still boot from it.

TFFSBIOS is resident at run-time in system RAM. It installs itself in the area below the 640 Kbyte DOS limit. To prevent itself from being over-written by DOS, it changes the DOS memory limit to a number below 640 Kbytes. Therefore after you install TFFSBIOS, it will appear that DOS has less than 640 Kbytes, by approximately 20 Kbytes.

7.1.1 What if there is no drive letter?

In the case where a media handled by TFFS BIOS is not properly formatted by TFORMAT, a problem will arise that there is no DOS drive letter that refers to the media. In this case it is not possible to use the utilities with a drive-letter, e.g., TCHECK D:, since there is no drive-letter D.

This situation occurs because DOS will only define a drive if the media contains a valid partition table in the master boot record (sector 0 of the media). This partition table is written by TFORMAT (and may be modified by FDISK) so if the partition table is missing because the media is unformatted, no drive letter exists. Refer to Chapter 2, “Getting Started” for instructions on how to format the RFA for the very first time.

7.2 USING TFFS

The evaluation board has two possible flash media:

- Resident Flash Array (RFA)
- PCMCIA socket with a Flash PC Card installed

The evaluation board is shipped with the RFA unformatted, and Flash PC Cards are also initially unformatted. The TFFS BIOS will only install flash media when it has been previously formatted. Therefore, the DOS device drivers must be used to initially format the media. Do not continue to use the DOS device drivers after you have formatted the RFA or PC Card. The BIOS extension should be used instead.

7.2.1 Installing the TFFS Driver Software

To install the TFFS driver software, you will need the following:

- The M-Systems Diskette
- A floppy drive attached to your evaluation board

Note that at this point, the TFFS BIOS must not be installed. You can verify this by entering the BIOS Setups and checking the BIOS extension base address in the Advanced Menu.

Follow these steps:

1. Insert the M-Systems diskette into the floppy drive and make that your current drive:

```
A:>
```

2. Start the install program and answer the questions on the screen.

```
A:>Install
```

When the installation is complete, you will return to the DOS prompt.

3. Edit the CONFIG.SYS file and do the following:
 - Remove the /Window=D000 parameter from TFFS.COM
 - If you are using EMM386 or a similar memory manager, exclude the region D800 to DFFFH with the parameter X=D800-DFFF.
4. Reboot to install the drivers.

7.2.2 Formatting the RFA or PC Card

To format the RFA or PC Card, follow these steps:

1. If a PC Card is to be used, install it into the PCMCIA socket.
2. Change to the directory with the TFFS drivers and utilities.

C:>CD TFFS

3. To format the RFA, type the following:

TFORMAT D:

4. To format the PC Card, type the following:

TFORMAT E:

When the evaluation board reboots, the RFA disk (RFD) and/or PC Card will be visible to the system. You can now use the DOS SYS command to transfer the system to a Flash disk.

7.2.3 Booting From the RFA or PC Card

To configure the evaluation board to boot to the RFA or PC Card, follow these steps.

1. Reboot the system and press F2 to enter the BIOS setups.
2. On the Main Menu, enter the IDE adapter sub menus and disable the IDE drives.
3. On the Advanced Menu, select either the RFA or PC Card as the BIOS boot medium.
4. Save and Exit.

NOTE

If an IDE drive, RFA and PC Card are all in the system, the following occurs: First, the TFFS BIOS extension will delay for up to 45 seconds during the boot sequence. Second, the BIOS boot medium entry on the Advanced Menu of the BIOS Setup will determine which Flash media will be installed first.



8

Programming Flash Memory



CHAPTER 8

PROGRAMMING FLASH MEMORY

This chapter describes the two ways to program the evaluation board's Flash Boot Device memory.

- The first section describes the FLASHLDR utility from Cyber Quest, Inc.*
- “Self-Hosted Reflashing” on page 8-14 describes the Self-Hosted REFLASH program.

8.1 USING THE FLASHLDR UTILITY

This section describes the installation, operation and commands used with the flash programming/loader utility, FLASHLDR. This utility allows you to download applications from a host PC system into the boot block flash device on the evaluation board. You can then run these applications from the boot block flash device. FLASHLDR may also be used to update the system BIOS and the BIOS extension programs which are pre-loaded in flash memory (see Figure 8-1 on page 8-16 for a map of flash memory).

The flash programming utility has two sections, the host software (FLASHLDR.EXE) that executes on a standard DOS based PC and communicates, through the serial port, with the target software (TARGET1.BIN). The evaluation board is shipped with TARGET1.BIN programmed into the 16Kbyte boot block of the flash. The target portion of the utility begins execution at processor start-up (power-up or reset) if a jumper is installed at JP3 (HBBF). Otherwise, control is passed directly to the Phoenix BIOS startup code.

NOTE

If a new flash device is installed, the target program TARGET1.BIN must be programmed into the device using an external programmer to be able to use the FLASHLDR utility.

With the jumper at JP3 installed, and pins 4-6 jumpered at JP6 (FRC_UP,MANUF), the target software will wait for commands from the host software. If the jumper at JP6 is removed, the target software will vector to a loaded boot program (set by the setboot command). If no boot program is defined, the target program will abort the boot sequence and wait for commands from the host (as if JP6 is installed). While waiting for commands from the host, the target program sends repeated 'A' characters to the COM port on the evaluation board. JP10 must be installed to program the flash boot device.

8.1.1 Before You Begin

Before using the FLASHLDR utility, assemble the following items:

- Ultra-Low Power Intel486™ Processor Evaluation Board
- Evaluation board Flash Utilities diskette
- Serial cable (6' Monitor Extension)
- Host PC
- Jumpers

8.1.2 Installation on the Host PC

To install files necessary for communicating with the Cyber Quest software on the evaluation board, the FLASHLDR program must be installed onto the Host PC. To do this, run the INSTALL program from the Flash Utilities diskette. For example, you would type the following:

INSTALL CQ C:

CQ specifies which software utility to install (CQ=CyberQuest FLASHLDR). C:\ specifies the destination drive and directory to install the files into. This command will install the FLASHLDR files onto the root directory of the C: drive. You may specify a subdirectory (INSTALL CQ C:\FLASH), but you must create the subdirectory before running the install program.

To manually install the Cyber Quest files, copy all the files from the FLASHLDR subdirectory on the Utilities diskette into a directory on your hard drive. You can use File Manager under Windows or use the COPY command from DOS. There is no installation program specifically for the FLASHLDR software. Note also that not all files on the diskette pertain to the FLASHLDR software.

8.1.2.1 Host Setup

In order to use the FLASHLDR software, you need to make sure that the COM port and baud rate options are correct for your host PC. Use a text editor to modify the COM port and baud options in FLASHLDR.FLC. Enter the following command:

EDIT FLASHLDR.FLC

Cursor down and make changes as necessary.

8.1.2.2 Evaluation Board Setup

1. Turn off power to the evaluation board. Connect one end of the serial cable provided to a COM port on the Host PC. Connect the other end to the COM1 connector on the evaluation board.
2. Place a jumper on pins 1 and 2 of JP3 (HBBF). Refer to Figure 4-1 on page 4-2 for jumper locations.
3. Place a jumper on pins 4 (FRC_UP) and 6 (MANUF) of JP6.
4. Place a jumper on pins 1 and 3 of JP10 (BB_CONTROL).
5. Turn on power to the evaluation board and host PC.
6. The LED port 80 will display the value A0 (see table 8-5 for other status values).

8.1.3 Running the Confidence Test Program

The HELLO test program may be used to perform an overall confidence test of the board and flash loader. The HELLO program is not dependent on the BIOS.

Running the HELLO test gives you a chance to see how the flash memory is programmed. It also acquaints you with some of the commands and options associated with the software and gives you a chance to use and manipulate them. We will first load the HELLO program into flash memory and then execute the program from the host PC.

First set up the host PC and the Evaluation board as described in the previous sections. From the DOS prompt of the host PC, change to the FLASHLDR directory and start the FLASHLDR utility:

```
C:\FLASH>FLASHLDR
```

To load the HELLO program, perform the following steps:

1. Connect to target:
FLASH CMD: conn
2. Program HELLO as boot program:
FLASH CMD: PrHello
3. Update tables and shutdown host/target communications link:
FLASH CMD: shutdown

To execute the HELLO program from system startup, perform the following steps:

1. Remove jumper at JP6. (OK to remove with power on)
2. Reset Evaluation board. (observe F8 on LED's)
3. Enter virtual terminal mode:

FLASH CMD: vt

4. Observe repeating hello message

Hello from 486SX board

Hello from 486SX board

5. Press **r** while the message is being displayed to display target loader sign-on message

CQi Flash Hello Program ...

To test the forced recovery mode, perform the following steps:

1. Install jumper at JP6. (You may install this jumper with the power on.)
2. Reset Evaluation board. (observe A0 on LED's)
3. Observe repeating As

To restore evaluation board to normal system boot, perform the following steps:

1. Press Esc to exit from vt mode.
2. Re-connect to target:

FLASH CMD: conn

3. Re-select LOADBIOS as boot program

FLASH CMD: setboot loadbios

4. Confirm LOADBIOS has JUMPER boot flag set

FLASH CMD: dir

5. (Optional) To remove the hello program

FLASH CMD: delete hello

6. (Optional) Confirm HELLO has been deleted

FLASH CMD: dir

7. Quit FLASHLDR program

FLASH CMD: exit

8. Remove jumper at JP6. (You may install this jumper with the power on.)
9. Reset the evaluation board.
10. Observe normal system boot up sequence.

8.1.4 Entering FLASHLDR Commands

Invoke the Flash loader on the host PC system by following these steps:

1. Set up the evaluation board as described in “Evaluation Board Setup” on page 8-3.
2. At the system prompt on the Host PC, in DOS, change to the flash directory.
To do this, enter:

CD FLASH

3. Start the flash loader by typing:

FLASHLDR

There are five ways to specify commands or options for processing by the flash programming utility. These are:

- Interactively from the flash loader prompt. At the flash programming utilities prompt, enter any command or option.

FLASH CMD: file=<filename>

- Automated from flash command files
- Passed on the invocation line of the flash programming utility. This can include flash command file commands.

C:\FLASH> FLASHLDR init;dir

- Using the standard DOS redirection of input to get commands from a file. When you use this method, input is redirected from a file and no additional commands can be entered from the keyboard; the input file should contain an exit or abort command.

C:\FLASH> FLASHLDR <filename>

- Using a pre-defined DOS environment variable, flashopt. Because of the way DOS processes commands that require the equal sign, substitute ‘+’ for ‘=’ in the normal syntax. For example:

```
C:\FLASH> set flashopt=port+com2;baud+38400
```

When FLASHLDR starts, the commands and options specified in the environment variable flashopt are executed first. If the file FLASHLDR.FLC is found in the current directory or in the directory where FLASHLDR.EXE was loaded from, the commands and options in the file are executed. This file usually contains configuration options such as port #, baud rate, etc. Last, parameters passed on the command line are executed. If an exit command is not encountered in any of the above, an interactive command session starts.

8.1.4.1 Using Flash Command Files (.FLC)

Flash command files are similar to DOS batch files without parameter passing. From the flash command line you can enter a single command to execute one or more different commands. Flash command files are identified by a .flc file extension. When a command is entered from the flash loader prompt and the command is not one of the pre-defined flash commands, the flash loader program will search multiple directories in the following order for a .flc file:

- Current directory
- Directories specified by the cmdpath option (e.g., cmdpath=..\cmd,..\bin,c:\flash)
- Directory where FLASHLDR.EXE was loaded from

If the file is found, the program executes the commands in the file until it reaches the end of the file. In addition, a full or partial path to a flash command file may be entered (e.g. c:\cmd\myboard.flc). The .flc extension is optional. Command files may invoke other command files. Following is an example:

Table 8-1. Flash Command File

```
// PRHELLO.FLC - Example cmd file to program hello program

echo *** Program hello program ***

delete! hello // Delete current copy of program
// The ! allows the flc to continue
// if hello is not found, without a !
// the flc will exit due to error

program hello.hex group=test ver=2.2 // Program into flash

setboot // Set hello as boot program

update // Update flash tables now
// Without this command, the flash
// tables will be updated on exit

dir // Display flash directory
```

You can now enter the newly created command the same way you enter the standard FLASHLDR commands. See “Entering FLASHLDR Commands” on page 8-5 for more detail. Text following the “/” symbol is a comment and is ignored for both the command files and the flash command line. This can be used to add information about your command or log file.

The full command set is presented in the next section.

8.1.4.2 Flash Programming Utility Command Summary

The following table lists the flash loader commands. Italicized text denotes terms listed previously. Text in square brackets denote optional parameters.

Table 8-2. Flash Loader Commands (Sheet 1 of 2)

Command	Abbrev/Options	Descriptions
abort	a	Abort program (tables not updated)
boot	b [<i>name</i>]	Allows you to immediately boot/start a program (boot flag not updated as in the setboot command)
checkhex	chk [<i>file</i>] [format=x] [addr=x]	Display hex file address
debug	-	Enable debug commands
delete	del [<i>name</i>]	Delete program from flash
dir	d	Display directory of programmed files
dos	[<i>str</i>]	Shell to DOS or execute command <i>str</i>
echo	[<i>str</i>]	Displays user messages in command files. Similar to the DOS echo command in batch files.
exit	e, x, quit, q	Performs a shutdown and exits program
<flash command>	-	Name of a flash command file minus the .flc extensions section “Using Flash Command Files (.FLC)”.
help	h, ?	Display command/option help
init	i [<i>port</i>] [baud=x]	Initializes link between host and target
map	m	Display flash address mapping (defined by board option)
noboot	nb	Clears boot program flag
options	opt	Display current options



Table 8-2. Flash Loader Commands (Sheet 2 of 2)

program	pr [<i>file</i>] [format=x] [addr=x] [name=x] [group=x] [version=x]	Programs specified file into flash memory using current options
reinitbls	rt [<i>board</i>] [system=x]	Reinitialize flash tables
setboot	sb [<i>name</i>]	Set boot program
shutdown	sh	Update flash information tables from RAM to the flash and closes communication link between target and host. User must shutdown to save changes.
term	vt [<i>port</i>] [vtbaud=x]	Emulate terminal (VT) (to the evaluation board COM1 port).
update	up	Immediately flushes changed tables to flash memory.
wait	w [x]	Pause processing of commands for x seconds.
!		Continue if an error occurs. Also inhibits any possible confirmation questions

8.1.4.3 Flash Programming Utility Options Summary

To see which options are currently set, enter this command:

opt

To make changes at the FLASH CMD: command line, type <option> = <yourvalue> and press the enter key. For example, to change the prompt from FLASH CMD to UPDATE, enter:

prompt=update

This table of options can be set at the FLASHCMD: prompt, or as command line parameters to other commands.

Table 8-3. FLASHCMD Options

Options	Possible Values	Default	Description
addr=	phys	0	Sets target flash address for programming binary files.
baud=	baud rate	9600	Set target communication baud rate. (Set the rate your application requires.)
board=	board	I386EX-EVAL	Set target system board. Effects memory map of the flash device to program. It is the programmers responsibility to program the chip selects to match the memory map.
cmdpath=	<i>dir</i> [, <i>dir</i> , ..]		Set search path for flash command files (.flc)
file=	file	-	Set program file.
format=	hex bin	-	Set program file type. Only required if extension is not .bin or .hex
group=	str	-	Set group name (user selectable)
log=	terse, normal, or verbose	NORMAL	Set logging level
memory=	none, ram, flash, or boot	flash	Set valid memory types for programming
name=	str	<i>file</i> minus director and extension	Set program name (user selectable)
port=	port	-	Set target com port. (Specify the port to which your serial cable is connected on the host PC from the evaluation board debug port.)
progpath=	<i>dir</i> [, <i>dir</i> , ..]		Set the program file search path
prompt=	str	FLASH CMD:	Set prompt
system=	str	TARGET	Set target system name (user selectable)
vector=	<i>b:0</i> <i>phys</i>	-	Set start vector
version=	str	-	Set program version (user selectable)
vtbaud	baud rate	9600	Set terminal emulator com baud rate
vtport=	port	-	Set terminal emulator com port
;			Command separator on single line
//			Anything entered after this symbol is a comment and will be ignored

The terms in square brackets are the options that can be specified with the command. These terms are defined in the following table.

Table 8-4. Terms Used in FLASHCMD Commands

Term	Definition
file	Valid DOS path with file name.
dir	Valid DOS directory path.
name	Symbolic name associated with programmed files.
port	Serial port name (<i>com1, com2, com3, com4</i>).
board	Valid board names are <i>i386ex-eval, i386ex-eval-dos, i386ex-Hummingboard1, i386ex-Hummingboard1-dos</i> . Previous names such as <i>exeval</i> and <i>dosexeval</i> are still accepted. Names that end with <i>-dos</i> represent memory maps <i>after</i> the loadbios program “flips” the flash device and changes the chip selects for DOS operation.
str	A string of ANSI characters.
b:o	Hex address in the form of base:offset (8000:0)
phys	Hex address in physical linear address form, (80000).
baud rate	A valid baud rate (300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200).

8.1.4.4 Loading a Program

The file to be programmed into the flash memory device must be either an Intel HEX file (.HEX by default) or a binary memory image file (.BIN by default). Once a file is loaded using the program command, you can set this file to be executed at system reset instead of the FLASHLDR target program. This is done by using the setboot command. Note that if the programmed file did not contain starting address information then the vector option must be set before the setboot command is used. This is required when using binary files. If the vector command is not used, you should verify that the start address set will work for your application.

8.1.4.5 Loading a Program to Execute at System Start-up

1. Set up the evaluation board as described in “Evaluation Board Setup” on page 8-3.
2. At the system prompt on the Host PC, in DOS, change to the flash directory.
For example, from the root on the C: drive enter:

CD FLASH

3. Create a flash command file (.FLC) for your application program. Use the PRHELLO.FLC as a template.
4. Start the flash loader by entering:

FLASHLDR

5. At the FLASH CMD: prompt, enter each of the appropriate commands

FLASH CMD: conn

FLASH CMD: pr<filename.flc>

FLASH CMD: shutdown

8.1.4.6 Executing a User Loaded Program or Target Program at System Startup

The jumpers at JP6/JP3 control which programs run at start-up:

- When the jumpers are removed, the flash target program immediately starts the selected user application program (if any). For example, the PhoenixBIOS startup code or the HELLO test program.
- When the jumpers are installed, the flash target program waits for commands from the PC host system to maintain the flash memory (program, delete, etc.).

8.1.5 LED Diagnostic Codes

The flash loader target uses the Port 80 display LEDs to provide feedback and diagnostic capability. The following table lists the LED value and the associated flash loader status.

In addition to the above, the flash loader will display the hex code of each command id as it is received from the host. After execution, the LED display will revert back to AA.

Table 8-5. Flash Loader Status

LED	Flash Loader Status
A0	Waiting for forced recovery (hardware jumper is installed)
A1	Waiting for forced recovery (software initiated)
A2	Waiting for forced recovery (flash tables corrupted)
A3	Waiting for forced recovery (no boot program in flash table)
AA	Ready and waiting for next command from host
F0 ⁽¹⁾	Board initialization started (set immediately after reset)
F1 ⁽¹⁾	Board initialization completed
F8 ⁽¹⁾	User boot program started (typically LOADBIOS)
F9 ⁽¹⁾	BIOS started (set by LOADBIOS)
0A ⁽²⁾	Read RAM (upload)
0B ⁽²⁾	Write RAM (download)
15 ⁽²⁾	Erase Flash Block
17 ⁽²⁾	Program Flash Block

NOTES:

1. LED values may appear temporarily (or all the time if an error has occurred)
2. LED values and commands that may appear for more than a second

8.1.5.1 Updating the BIOS

To update the PhoenixBIOS, Cirrus Logic* BIOS and M-Systems* BIOS, follow these steps.

1. Set up the evaluation board as described in “Evaluation Board Setup” on page 8-3.
2. Execute FLASHLDR.EXE on the PC host
3. Initialize and establish connection with the evaluation board:

FLASH CMD: conn

4. To update the Phoenix BIOS, enter the following command:

FLASH CMD: prbios

5. To update the Cirrus Logic Video BIOS, enter the following command:

FLASH CMD: prvid

6. To update the M-Systems TrueFFS BIOS, enter the following command:

FLASH CMD: prftl

7. To update tables and exit FLASHLDR, enter:

FLASH CMD: exit

8.1.6 Support

The Flash Loader software is distributed “as is” in binary form for use with Intel's evaluation boards. Source code examples of flash memory may be obtained by downloading IBOOTLDR.EXE (a self-extracting zip file) from the Intel Applications BBS. IBOOTLDR is a previous release of the flash utility utilized.

You may wish to contact the vendor responsible for developing the software if you desire a custom version of Flash Loader. Cyber Quest can be reached at:

Cyber Quest, Inc.
5667 Stone Rd., Suite 560
Centreville, VA 22020
(703) 631-8323
(703) 631-1669 (Fax)
75310.3637@compuserve.com

8.2 SELF-HOSTED REFLASHING

Self-hosted reflashing of the BIOS is intended for users who want to selectively reflash one part of the Flash Boot Device (FBD) at a time. It is not intended for use when reflashing the entire BIOS. Use the Cyber Quest utility explained in “Using the FLASHLDR Utility” on page 8-1, to replace a corrupt BIOS.

This section describes how to use the REFLASH.EXE program found on the Flash Utilities Plus Power Management diskette. The REFLASH.EXE program requires 2 Mbytes of DRAM to operate correctly.

8.2.1 Installation

To install the files necessary for a self-hosted reflash of the BIOS, run the INSTALL program found in the Flash Utilities diskette. Type INSTALL and press ENTER for more information. For example, you would type the following:

INSTALL REFLASH

This assumes the evaluation board is installed in a system with a passive backplane and a floppy controller.

To manually install the files, copy HEB.EXE and REFLASH.EXE from the REFLASH directory on the floppy disk into a directory you create.

Binary files used by REFLASH.EXE are the same files used by the Cyber Quest software. Some binary files can be found in the BIN directory on the floppy disk.

8.2.2 Before You Begin

To perform a self-hosted reflash of one segment of the evaluation board's flash boot device (FBD), note the following:

- You must be running under DOS. You *cannot* be running Windows.
- You must remove any programs from CONFIG.SYS and AUTOEXEC.BAT that make use of memory above one megabyte. DOS cannot be loaded high; you cannot install HIGHMEMSYS.
- You must set two jumpers at JP10. By placing a jumper on pins 1 and 3, all blocks other than the boot block can be written. By placing a jumper on pins 2 and 6, the 16 Kbyte boot block can be reprogrammed.

8.2.3 Operation

In order to successfully reflash the BIOS, follow these steps:

1. Run HEB.EXE (performs chipset and evaluation board-specific enabling operations)
2. Run REFLASH /F=62X5.bin /O=0 (This example reflashes only the video BIOS.)
3. When the DOS prompt appears, cycle the power.

8.2.3.1 Examples

To update the Cirrus Logic Video BIOS, enter:

```
heb  
reflash /F=62x5.bin /O=0
```

To update the M-Systems TrueFFS BIOS, enter:

```
heb  
reflash /F=ftlbioss.bin /O=8000
```

To update the PhoenixBIOS, enter:

```
heb  
reflash /F=bios.bin /O=20000
```

To update the Cyber Quest Target1 file, enter:

```
heb  
reflash /F=target1.bin /O=7C000
```

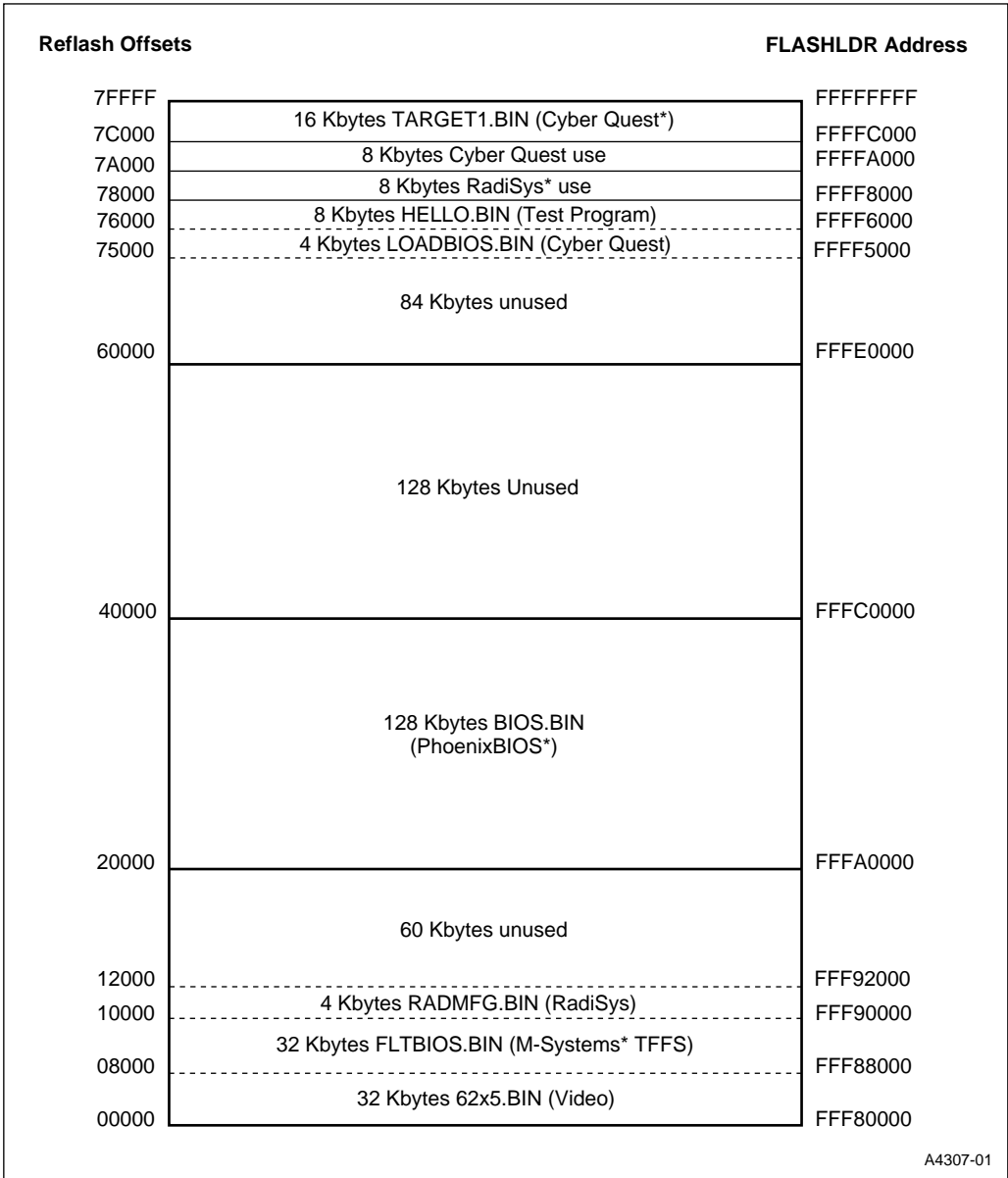
Depending on the size of the image to be flashed into the FBD, you may have to wait several minutes for reflash to complete.

WARNING

If the power fails or you otherwise interrupt REFLASH.EXE while it is attempting to reflash the boot block, you will corrupt the boot block and you will have to replace the boot block with one that has been programmed in an external programmer. If you damage the Cyber Quest boot block using TARGET1.BIN and using the Phoenix code BIOS.BIN -OR- the VGA BIOS 624X.BIN, the Intel Flash chip may be permanently damaged.

WARNING

If you specify the wrong file (and it exists) or the wrong offset, you will corrupt the Flash boot device.



A4307-01

Figure 8-1. Flash Boot Device Memory Map



9

Using Power Management



CHAPTER 9

USING POWER MANAGEMENT

9.1 INTRODUCTION

PM.EXE is a simple DOS program which initializes and enables power management timers in the PicoPower* chipset. With these timers, you can:

- Slow the CPU clock
- Turn off the Port 80 LED display
- Put the COM1 driver, SMC Super I/O chip, and the VGA controller into low power modes

All of these low-power modes can be disabled by various events, such as keystrokes, and then automatically re-entered after a specified time.

To set the evaluation board into a power management mode, use PM.EXE with various command line options, discussed later in this chapter.

Please note that due to chipset limitations, PM.EXE can only make changes to the clock speed when the evaluation board is operating at or below 25 MHz.

9.2 INSTALLATION

The PM.EXE file is found on the Flash Utilities Plus Power Management diskette in the PM subdirectory.

To install Power Management software, type `INSTALL PM C:\` to use the installation program on the diskette.

Manual installation is simple: copy the file into a directory you create on your hard disk drive. For example, you can put PM.EXE into a directory named `C:\PM`.

While setting up the PM.EXE command line it may be easier to include PM.EXE in a batch file, so that you don't have to enter the entire command line string each time you make changes. Once finished, you can include PM.EXE (or your customized batch file) into `AUTOEXEC.BAT`.

9.3 POWER MANAGEMENT MODES

There are three power management modes: Conserve, Doze, and Sleep.

9.3.1 Conserve Mode

PM.EXE can enable Conserve mode, disable Conserve mode, and set the Conserve Mode Clock Divisor.

Possible Conserve mode Clock Divisor settings are: 1, 2, 4, 8, 16, 32, and 64.

9.3.2 Doze Mode

PM.EXE can enable Doze mode, disable Doze mode, set the Doze mode timeout, and set the Slow-Clock Divisor. In addition, the user can specify whether the evaluation board's 7-segment display LED is enabled or disabled in Doze mode.

Possible Doze Mode Timeout settings are .125, .250, .500, 1, 4, 8, and 16 seconds.

Possible Slow-Clock Divisor settings are: 0, 2, 4, 8, 16, 32, and 64. A divisor of 0 indicates the Slow-Clock feature is disabled for Doze mode.

9.3.3 Sleep Mode

PM.EXE can enable Sleep mode, disable Sleep mode, set the Sleep Mode Timeout, and set the Slow-Clock Divisor. In addition, the user can configure the COM1, super-I/O chip, or VGA chip as enabled or disabled in Sleep mode.

Possible Sleep Mode Timeout settings are 1, 2, 4, 6, 8, 12, and 16 minutes.

Possible Slow-Clock Divisor settings are: 0, 2, 4, 8, 16, 32, and 64. A divisor of 0 indicates the Slow-Clock feature is disabled for Sleep mode.

9.3.4 Primary Events

PM.EXE allows the user to specify the events that will trigger the PicoPower chipset's Primary Idle Detector. When the Primary Idle Detector is triggered, the chipset will toggle from Doze mode or Sleep mode to Fully-On or Conserve mode.

When a Primary Event is masked, then that Primary Event will not trigger the Primary Idle Detector. When a Primary Event is unmasked, that Primary Event will trigger the Primary Idle Detector, forcing a chipset state change.

The following is the set of Primary Events that may be individually masked or unmasked:

- Keyboard activity
- Floppy Disk Drive activity
- Video activity
- Hard Disk Drive activity
- Serial Port activity
- Parallel Port activity

9.3.5 Secondary Activity Events

PM.EXE allows the user to specify the events that will trigger the PicoPower chipset's Secondary Activity Idle Detector, and to configure the Secondary Activity Timer. When the Secondary Activity Idle Detector is triggered, the chipset toggles from Doze or Sleep mode to the Revive state.

The hardware will remain in the Revive State for the period defined by the Secondary Activity Timer. When the Secondary Activity Timer expires, the hardware will return to its former state.

When a Secondary Event is masked, then that Secondary Event will not trigger the Secondary Activity Idle Detector. When a Secondary Event is unmasked, that Secondary Event will trigger the Secondary Activity Idle Detector, forcing a temporary transition to the Revive state.

The following is the set of Secondary Events that may be individually masked or unmasked:

- Interrupt activity
- Video activity
- Keyboard activity
- IRQ0 activity
- DMA activity
- ISA Bus Master activity

Possible Secondary Activity Timer settings are 125 μ s, 1 ms, 2 ms, 4 ms, 16 ms, 32 ms, and 64 ms.

9.4 COMMAND LINE OPTIONS

The PM.EXE command-line syntax is given below.

PM

```
{ /C [on | off] C[2 | 4 | 8 | 16 | 32 | 64 ] }
{ /DO [on|off] C[ 0 | 2 | 4 | 8 | 16 | 32 | 64 ] T[ .125 | .250 | .500 | 1 | 4 | 8 | 16 ]
/L[e]d }
```

```
{ /SL [on | off] C[ 0 | 2 | 4 | 8 | 16 | 32 | 64 ] T[ 1 | 2 | 4 | 6 | 8 | 12 | 16 ]
S1[e]d S2[e]d I[e]d V[e]d }
```

```
{ /P [ K[e]d H[e]d S[e]d P[e]d ] }
```

```
{ /SE T[ .125 | 1 | 2 | 4 | 16 | 32 | 64 ] [ S[e]d V[e]d K[e]d I[e]d
D[e]d M[e]d ] }
```

```
{ /DI [ O | S ] }
```

```
{ /V }
```

Any combination of these variables can be used at one time (up to the 128 character DOS limit). For example, the following is a valid command line:

```
PM /C ON C4 /DO ON C8 T4 LD /SL ON T2 S1D VD /P HD /SE DD /V
```

This would enable Conserve mode with a clock divisor of 4, enable Doze mode with a clock divisor of 8, a time-out of 4 seconds and turn off the LED, enable Sleep mode with a clock divisor of 8 and disable both the VGA controller and Serial port 1 while in Sleep mode. It also will mask hard-drive activity as a primary event trigger and DMA activity as a secondary event trigger and suppress output from the command line.

Another valid combination would be multiple occurrences of variations of the same argument. For example, the following is a valid command line:

PM /C ON C2 /DO ON C4 T4 /SL ON C4 T1 /DO LD C8

Note the two occurrences of the /DO argument. Doze mode would be enabled with a time-out of 4 seconds, the LED disabled, and a clock divisor of 8 since it appears on the command line last.

Once the modes are enabled, each feature of the particular mode may be manipulated individually. For example, if Sleep mode is enabled and you want to change the time-out, **PM /SL T2** would change the time-out to 2 without affecting the other settings or using a long command line again.

9.5 CONSERVE MODE OPTIONS

The Conserve mode option syntax is:

{ /C [on | off] C[2 | 4 | 8 | 16 | 32 | 64] }

- /C** Reconfigures Conserve mode
- ON** Places the hardware in Conserve mode. If no conserve clock divisor is specified on the command line, DOS-PM will default to a value of 2.
- OFF** Disables Conserve mode (returns to Fully-On mode)
- C2/4/8/16/32/64** Sets the conserve clock divisor

For example **PM /C ON C4** would set the Conserve mode to on with a clock division of 4. The Conserve mode is not a time delay mode. When enabled, the system goes directly into Conserve mode with whatever clock division set on the command line. Conserve mode can only be exited with a command line argument of OFF. Primary and secondary triggers have no effect on Conserve mode operation.

9.6 DOZE MODE OPTIONS

The Doze mode option syntax is:

```
{ /DO [on|off] C[ 0 | 2 | 4 | 8 | 16 | 32 | 64 ] T[ .125 | .250 | .500 | 1 | 4 | 8 | 16 ]
/L[e|d] }
```

/DO Reconfigures Doze mode

ON Places the hardware in Doze mode. If no slow-clock divisor is specified on the command line, DOS-PM uses the current conserve clock divisor setting. If no slow-clock divisor is specified on the command line, DOS-PM will leave the current slow-clock divisor setting. If no doze time-out setting is specified on the command line, DOS-PM will leave the current doze time-out setting. If no LED option is specified on the command line, DOS-PM will leave the current LED setting. If this is the initializing command line and no time-out, clock division or LED is specified, time-out will be set to 16 seconds, the clock division inactive and the LED will remain enabled.

OFF Disables Doze mode (returns to Fully-On mode)

Since Doze mode is a requirement before going into Sleep mode, Sleep mode must be turned off prior to or in conjunction with turning off Doze mode. If this is not done, PM.EXE will not turn off Doze mode. This can be accomplished by either issuing a **PM /SL OFF** command and then **PM /DO OFF** command or place both on the same command line, **PM /DO OFF /SL OFF**. Order of occurrence when both are included on the same command line is not important. Either of these methods will shut off Doze and Sleep modes.

If Doze mode is not enabled prior to issuing the command to enable Sleep mode, Doze mode will automatically be enabled with its initialization defaults of a 16 second time-out, LED enabled, and clock division inactive.

C0 Disables the slow-clock feature

C2/4/8/16/32/64 Sets the slow-clock divisor

The same slow clock is used by both the Doze mode and the Sleep modes. The last clock divisor for these two entries on the command line will be used by the system for their clock divisor. For example **/DO ON C4 /SL ON C8** would result in a clock divisor of 8 for both the DOZE and SLEEP clock divisor. However, a clock division of other than 0 must be used to enable the slow clock for a particular mode. Setting one slow clock on will not automatically turn the other slow clock on. For example, **/DO ON C4 /SL ON** would cause the slow clock for Doze mode to be enabled with a clock division of 4. When the system went into Sleep mode, however, the system would revert back to the original clock used before Doze mode, whether it be the fully on or the CONSERVE clock.

- T.125** Sets the doze time-out interval to 125 milliseconds
- T.250** Sets the doze time-out interval to 250 milliseconds
- T.500** Sets the doze time-out interval to 500 milliseconds
- T1/2/4/8/16** Sets the doze time-out interval (in seconds)
- Le** The 7-segment display LED remains enabled in Doze mode
- Ld** Disables the 7-segment display LED in Doze mode

For example **PM /DO ON T4 C4 LD** would set the Doze mode to on with a 4 second time-out with a clock division of 4 and disable the 7-segment display LED.

9.7 SLEEP MODE OPTIONS

The Sleep mode option syntax is:

```
{ /SL [on | off] C[ 0 | 2 | 4 | 8 | 16 | 32 | 64 ] T[ 1 | 2 | 4 | 6 | 8 | 12 | 16 ]
S1[e|d] S2[e|d] I[e|d]V[e|d] }
```

/SL Reconfigures Sleep mode

ON Places the hardware in Sleep mode. If no slow-clock divisor is specified on the command line, DOS-PM will use the current conserve clock divisor setting. If no sleep time-out setting is specified on the command line, DOS-PM will use the current sleep time-out setting. If no serial, super-I/O, or VGA settings are specified on the command line, DOS-PM will use the current settings. If the Sleep mode has not previously been initialized, then the defaults of a clock divisor of 2, a 16 minute time-out, and Serial1, Serial2, VGA and Super I/O are all enabled during Sleep mode.

The system will not go into Sleep mode if it is not already in Doze mode. Because of this requirement, Doze mode will be activated automatically if it is not already initialized when the command is given to enable Sleep mode. Doze mode will be started with its initialization defaults of a 16 second time-out, clock division inactive, and LED enabled

OFF Disables Sleep mode (returns to Fully-On mode)

C0 Disables the slow-clock feature

C2/4/8/16/32/64 Sets the slow-clock divisor

The same slow clock is used by both the Doze mode and the Sleep modes. The last clock divisor for these two entries on the command line will be used by the system for their clock divisor. For example **/DO ON C4 /SL ON C8** would result in a clock divisor of 8 for both the DOZE and SLEEP clock divisor. However, a clock division of other than 0 must be used to enable the slow clock for a particular mode. Setting one slow clock on will not automatically turn the other slow clock on.

For example, **/DO ON C4 /SL ON** would cause the slow clock for Doze mode to be enabled with a clock division of 4. When the system went into Sleep mode, however, the system would revert back to the original clock used before Doze mode, whether it be the fully on or the CONSERVE clock.

- T1/2/4/8/16** Sets the sleep time-out interval to (in minutes)
- S1e** Serial1 port remains powered in Sleep mode
- S1d** Serial1 port unpowered in Sleep mode
- S2e** Serial2 port remains powered in Sleep mode
- S2d** Serial2 port unpowered in Sleep mode
- Ie** Super-I/O chip remains powered in Sleep mode
- Id** Super-I/O chip unpowered in Sleep mode
- Ve** VGA chip remains powered in Sleep mode
- Vd** VGA chip unpowered in Sleep mode

For example **PM /SL ON T1 C4 VD S1D** would set the Sleep mode to on with a clock division of 4, a 1 minute time-out and disable both the VGA controller chip and serial port 1.

9.8 PRIMARY EVENT OPTIONS

The Primary event option syntax is:

{ /P [K[e|d] H[e|d] S[e|d] P[e|d]] }

- /P** Reconfigures the primary event mask
- Ke** Enables keyboard activity as a Primary Event trigger
- Kd** Disables keyboard activity as a Primary Event trigger

Since keyboard activity can be set to be a primary trigger and a secondary trigger, only one should be set at a time. PM.EXE will not allow you to set the keyboard activity to trigger both a primary event and a secondary event. By default, the trigger for Secondary Activity is disabled.

He	Enables hard disk activity as a primary event trigger
Hd	Disables hard disk activity as a primary event trigger
Se	Enables serial port activity as a primary event trigger
Sd	Disables serial port activity as a primary event trigger
Pe	Enables parallel port activity as a primary event trigger
Pd	Disables parallel port activity as a primary event trigger

9.9 SECONDARY EVENT OPTIONS

The Secondary Event option syntax is:

{ /SE T[.125 | 1 | 2 | 4 | 16 | 32 | 64] [S[e|d] K[e|d] I[e|d]

/SE	Reconfigures the Secondary Event Mask and Timer
T.125	Sets the secondary/event revive interval to 125 microseconds
T1/2/4/16/32/64	Sets the secondary event/revive interval (in milliseconds)
Se	Enables interrupt activity as a secondary event trigger
Sd	Disables interrupt activity as a secondary event trigger
Ke	Enables keyboard activity as a secondary event trigger
Kd	Disables keyboard activity as a secondary event trigger

Since keyboard activity can be set to be a primary trigger and a secondary trigger, only one should be set at a time. PM.EXE will not allow you to set the keyboard activity to trigger both a primary event and a secondary event. By default, the trigger for Secondary Activity is disabled.

Ie	Enables IRQ0 activity as a secondary event trigger
Id	Disables IRQ0 activity as a secondary event trigger
De	Enables DMA activity as a secondary event trigger
Dd	Disables DMA activity as a secondary event trigger
Me	Enables ISA bus master activity as a secondary event trigger
Md	Disables ISA bus master activity as a secondary event trigger

9.10 DOS-PM MISCELLANEOUS OPTIONS

- /DI O** Displays a list of the DOS-PM command-line options. Any invalid command line argument will also show a list of command line options as will typing PM by itself. At least one space must separate the command line arguments.
- /DI S** Displays the current power management settings. It will give detailed information for each of the available modes. It will only, however, show what system events are masked for both the primary and secondary activity detectors.
- /V** Suppresses output from the command line.



A

Error Messages

APPENDIX A ERROR MESSAGES

A.1 INTRODUCTION

This section deals with only the most common error messages encountered when booting up. Error messages can come from MS-DOS or from the PhoenixBIOS*. The Technical support phone number is listed in Chapter 1, "About This Manual."

A.2 COMMON ERROR MESSAGES

This section contains a summary of the most common error and warning messages alphabetized by message text. These are messages generated by the BIOS and MS-DOS that may be related to your hardware configuration.

A.2.1 BIOS Error Messages

DISKETTE DRIVE A (B) ERROR

Problem: Drive A: or B: is present but fails the BIOS POST diskette tests.

Solution(s): Check to see that the drive is defined with the proper diskette type in Setup and that the diskette drive is attached correctly.

EXTENDED RAM FAILED AT OFFSET: NNNN

Problem: Extended memory is not working properly.

Solution(s): Make sure the DRAM SIMM is installed properly. If the problem persists, contact Technical Support.

FAILING BITS: NNNN

Problem: The hex number nnnn is a map of the bits at the RAM address (in System, Extended, or Shadow memory) which failed the memory test. Each 1 (one) in the map indicates a failed bit.

Solution(s): Contact Technical Support.

FIXED DISK X FAILURE / FIXED DISK CONTROLLER FAILURE

Problem: The fixed disk is not working or is not configured properly.

Solution(s): Check to see if the fixed disk is attached properly.
Run Setup to ensure that the fixed disk type is correctly identified.

INCORRECT DRIVE A (B) TYPE

Problem: The floppy drive listed is not correctly identified in Setup.

Solution(s): Enter the BIOS Setup program and set the floppy drive size correctly.

INVALID NVRAM MEDIA TYPE

Problem: There is a problem with NVRAM access. There is a There

Solution(s): Contact Technical Support.

KEYBOARD CONTROLLER ERROR

Problem: The keyboard controller failed its POST test.

Solution(s): Try replacing the keyboard. Use a different make or model, if possible. If the problem persists, the onboard keyboard controller may be producing the error.

KEYBOARD ERROR

Problem: The keyboard is not working or is not connected.

Solution(s): Replace the keyboard. The error is in the keyboard, not the keyboard controller.

KEYBOARD ERROR NN

Problem: There is a stuck key on the keyboard.

Solution(s): The BIOS discovered a stuck key at scan code nn.

MONITOR TYPE DOES NOT MATCH CMOS - RUN SETUP

Problem: The monitor in use is not the same as the one recorded in the Setup.

Solution(s): Run Setup and check the video system identified in the Main Menu.

OPERATING SYSTEM NOT FOUND

Problem: An operating system is not present on either Drive A: or Drive C:.

Solution(s): Check the Setup and make sure the fixed disk and drive A: are properly identified.

PREVIOUS BOOT INCOMPLETE - DEFAULT CONFIGURATION USED

Problem: Previous POST did not complete successfully.

Solution(s): The POST loads the system's default values and offers to run Setup. If the failure was caused by incorrect values and they are not corrected, the next boot will likely fail. On systems with control of wait states, improper Setup settings can also terminate POST and cause this error on the next boot. Run Setup and verify that the wait-state configuration is correct. This error is cleared the next time the system is booted.

REAL TIME CLOCK ERROR

Problem: The real-time clock failed the BIOS test.

Solution(s): Remove the battery, wait 30 seconds, the reinstall the battery and power-up the system. If this is unsuccessful, contact Technical Support.

SHADOW RAM FAILED AT OFFSET:NNNN

Problem: Shadow RAM failed at the offset nnnn of the 64K block at which the error was detected.

Solution(s): Contact Technical Support.

SYSTEM BATTERY IS DEAD - REPLACE AND RUN SETUP

Problem: The CMOS clock battery indicator shows that the coin cell battery is dead.

Solution(s): Remove and replace the battery. Refer to Chapter 3, *Theory of Operations*, for more information. Run the Setups once the new battery is in place. Contact Technical Support if the system is going through batteries quickly.

SYSTEM CACHE ERROR - CACHE DISABLED

Problem: The RAM cache failed the BIOS test, so the BIOS disabled the cache.

Solution(s): Contact Technical Support.

SYSTEM CMOS CHECKSUM BAD - RUN SETUP

Problem: System CMOS has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Solution(s): Run Setup and reconfigure the system.

SYSTEM RAM FAILED AT OFFSET:NNNN

Problem: System RAM failed at offset nnnn in the 64K block at which the error was detected.

Solution(s): Contact Technical Support.

SYSTEM TIMER ERROR

Problem: The timer test failed.

Solution(s): Contact Technical Support.

A.2.2 MS-DOS Operating System Error Messages**BAD OR MISSING COMMAND INTERPRETER**

Problem: The DOS operating system cannot find the Command line interpreter.

Solution(s): Either COMMAND.COM is not present at the specified (or default) directory level of the boot disk or the "SHELL=" statement in your CONFIG.SYS lists the file incorrectly (wrong directory or misspelled).

GENERAL FAILURE READING DRIVE ...

Problem: This almost always indicates the presence of an unformatted hard disk partition or diskette.

Solution(s): Format the partition or diskette using the utilities supplied by your operating system.

INVALID DRIVE SPECIFICATION

Problem: You are trying to access a logical drive (e.g., A:, B:, ...) that is not known to the operating system.

Solution(s): Select a different logical drive. If you are trying to access a hard disk, you may need to create the logical partition.

NOT READY READING DRIVE ...

Problem: This is usually caused by not fully inserting a diskette into the floppy drive.

Solution(s): Eject the floppy diskette and reinsert, making sure that the diskette seats completely into the floppy drive.



B

Portable Power Supply



APPENDIX B

PORTABLE POWER SUPPLY

B.1 INTRODUCTION

The Ultra-Low Power Intel486™ Processor Evaluation Board can operate from a portable power supply. Although a portable power supply is not part of the evaluation board, this Appendix describes a portable power supply reference design that specifies an EMI filter, a bridge rectifier, a pre-regulator, a battery charge/control circuit, and a DC-DC controller.

One of the floppy diskettes shipped with the evaluation board is labeled Schematics. It contains a self-extracting executable file that is an archive of OrCAD*/SDT II schematics and libraries and postscript print files for each sheet.

B.2 AC INPUT

The supply accepts a AC voltage which can range from 85-265V RMS. This AC input is then filtered through a Electromagnetic filter, rectified and filtered through a bridge rectifier and capacitor.

B.3 HIGH VOLTAGE DC

This high voltage DC is then applied to the primary winding of the transformer. The other end of the transformer primary is driven by the integrated high voltage MOSFET within the TOP202 (3-terminal Pulse Width Modulated switch). The switching regulator circuit which is based on Power Integration's TOP-202YAI, generates a semi-regulated +15 V DC at the output winding which is supplied to the MAX783 DC-DC converter to generate the necessary board voltages. Line isolation is provided by the custom transformer mentioned above.

B.4 BATTERY CHARGE/CONTROL CIRCUIT

The battery charge/control circuit consists of several blocking diodes and a MOSFET. If AC voltage is providing the source, diode D3 is forward biased and current flows through the power switch to the DC-DC controller and also through the MOSFET which is turned on provided the gate is grounded and in this case it is shorted to ground) to the battery to provide a trickle charge at 20-30mA(25hrs for a full recharge) to the battery if connected. If battery only is applied, then the diode D4 is forward biased and current flows through the power switch to the DC-DC controller via the battery. The battery is a Ni-Cd 500 mA/h battery pack with the proper mating connector. This operates the system for approximately 35 minutes under battery @ 640 mA.

The MAX783 DC-DC controller converts the +15 V DC from the pre-regulator to +5 V, +3.3 V,

B

and +12 V using dual PWM (pulse width modulated) buck controllers for the +3.3 V @ 3 A and +5 V @ 3 A sources and dual VPP outputs (powered by an integral flyback winding controller) which in this case is tied together to provide one +12 V @ 120 mA.

B.5 +5 V

The +5 V supply is generated by a current-mode PWM step-down regulator using two N-channel MOSFETs, a rectifier, and a LC output filter. The two gate drives for the low-side and high-side MOSFETs switch the output to the inductor between the DC input voltage (+15 V DC) provided by the high-side MOSFET and ground provided by the low-side MOSFET. This is switched at a switching frequency of 300 KHz.

The feedback after the inductor determines the pulse width of the this switched pulse and the maximum current limit is set by an external low value sense resistor which prevents excessive inductor current during start-up and short circuit conditions. The voltage across this external shunt resistor is continuously monitored and the drive voltage to the high-side MOSFET is cut off if it exceeds 100 mV. This resistor is set for a 3 A load maximum.

B.6 +3.3 V

The +3.3 V supply is similar except the +3.3 V uses a transformer primary winding as its inductor. The secondary winding is used for the 15 V VDD supply which supplies power to the programmable V_{PP} power supplies. This occurs during the flyback or discharge portion of the cycle. Energy stored in the core of the transformer is transferred into the +3.3 V load through the primary and into V_{DD} through the secondary. The secondary is added to the +3.3 V to make V_{DD}. The V_{PP} supplies are linear regulators which draw their power from V_{DD}. The two V_{PP}s are connected in parallel for increased load capacity of +12 V DC @ 120 mA.

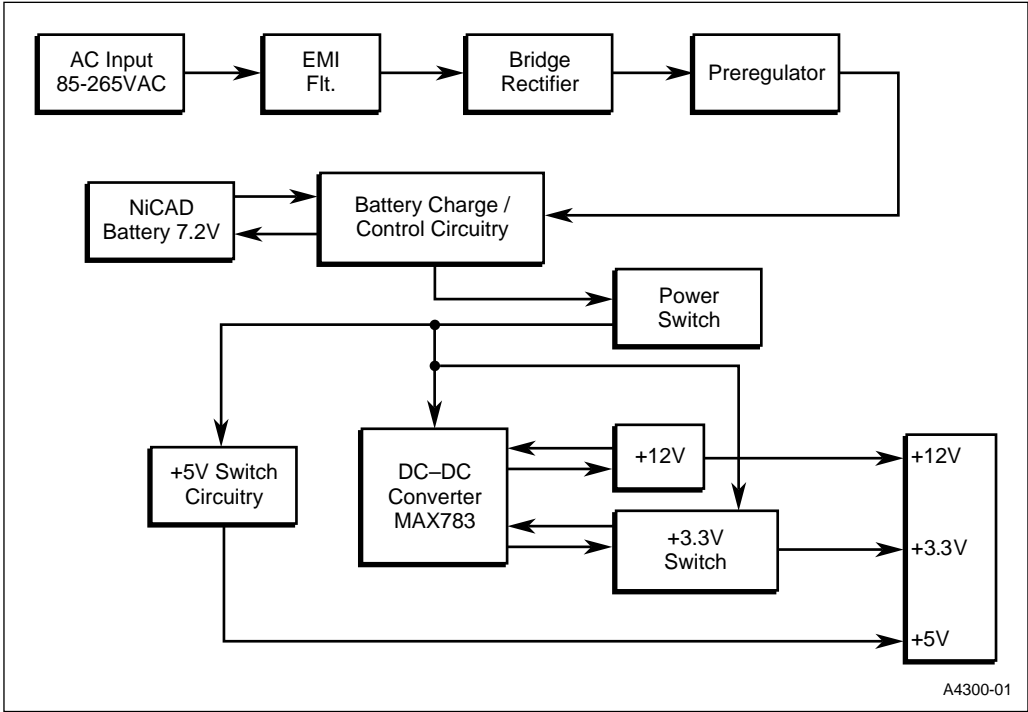


Figure B-1. Portable Power Supply Block Diagram

B



C

Flat-Panel Display



APPENDIX C FLAT-PANEL DISPLAY

The following panels have been tested to work with the evaluation board:

Table C-1. Tested Flat Panel Displays

Sharp	LM64C08P	Dual Scan Color STN
Sharp	LM64P80	Dual Scan Monochrome LCD
Sharp	LQ9D021	Color TFT

The default Cirrus Logic BIOS includes support for other flat panel displays. Consult Cirrus Logic documentation for cable diagrams for the following displays:

- Sanyo LCM-CK53 or LCM-5327
- Single Scan color STN 8-bit panels
- Single Scan mono STN 4-bit panels
- Sharp LQ10D3011

C.1 CONNECTOR CABLING

You may have to build cables for flat panels supported by the Cirrus Logic VGA chip.

C.1.1 LM64C08P Dual Scan Color STN Cabling

Jumper Settings:

- PANSEL0 = Jumper In
- PANSEL1 = Jumper Out
- PANSEL2 = Jumper In

Table C-2. LM64C08P Dual Scan Color STN Cabling

Flat Panel Conn	Evaluation Board Name	Evaluation Board Connector		Evaluation Board Name	Flat Panel Conn
CN1-5 (VDD) ⁽²⁾	SW_VCC	1	2	GND	(GND) ⁽¹⁾
NC	NC	3	4	LD0	CN2-17 (DL0)
to back light enable	FPBACKEN	5	6	LD1	CN2-18 (DL1)
CN1-4 (DISP)	FPVCCEN	7	8	GND	(GND) ⁽¹⁾
NC	FPVEEN	9	10	LD2	CN2-19 (DL2)
(GND) ⁽¹⁾	GND	11	12	LD3	CN2-20 (DL3)
NC	BMOD	13	14	GND	(GND) ⁽¹⁾
CN1-1 (YD)	BFLM	15	16	LD4	CN2-21 (DL4)
(GND)	GND	17	18	LD5	CN2-22 (DL5)
CN1-2 (LP)	BLP	19	20	GND	(GND) ⁽¹⁾
NC	FPDEN	21	22	LD6	CN2-23 (DL6)
(GND) ⁽¹⁾	GND	23	24	LD7	CN2-24 (DL7)
CN1-3 (XCK)	SHCLKR	25	26	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	27	28	R4	NC
CN1-8 (DU0)	SUD0	29	30	R5	NC
CN1-9 (DU1)	SUD1	31	32	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	33	34	FPSW_ADJ+	CN1-7 (VZZ) ⁽²⁾
CN1-10 (DU2)	SUD2	35	36	NC	NC
CN1-11 (DU3)	SUD3	37	38	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	39	40	-FPVADJ	NC
CN1-12 (DU4)	SUD4	41	42	NC	NC
CN1-13 (DU5)	SUD5	43	44	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	45	46	NC	NC
CN1-14 (DU6)	SUD6	47	48	SW_12V	for backlight pwr ⁽²⁾
CN1-15 (DU7)	SUD7	49	50	GND	(GND) ⁽¹⁾

NOTES:

1. GND = CN1-6, CN2-16, CN2-25
2. These power supplies need to be supplied by the user.

C.1.2 LM64P80 Dual Scan Monochrome

Jumper Settings:

- PANSEL0 = Jumper Out
- PANSEL1 = Jumper In
- PANSEL2 = Jumper In

Table C-3. LM64P80 Dual Scan Monochrome Cabling

Flat Panel Conn	Evaluation Board Name	Evaluation Board Connector		Evaluation Board Name	Flat Panel Conn
P5 - (VDD) ⁽²⁾	SW_VCC	1	2	GND	(GND) ⁽¹⁾
NC	NC	3	4	LD0	P12 - (DL0)
to back light enable	FPBACKEN	5	6	LD1	P13 - (DL1)
NC	FPVCCEN	7	8	GND	(GND) ⁽¹⁾
P4 - (DISP)	FPVEEN	9	10	LD2	P14 - (DL2)
(GND) ⁽¹⁾	GND	11	12	LD3	P15 - (DL3)
NC	BMOD	13	14	GND	(GND) ⁽¹⁾
P1 - (S)	BFLM	15	16	LD4	P8 - (DL4)
(GND)	GND	17	18	LD5	P9 - (DL5)
P2- (CP1)	BLP	19	20	GND	(GND) ⁽¹⁾
NC	FPDEN	21	22	LD6	P10 - (DL6)
(GND) ⁽¹⁾	GND	23	24	LD7	P11 - (DL7)
P3 - (CP2)	SHCLKR	25	26	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	27	28	R4	NC
NC	SUD0	29	30	R5	NC
NC	SUD1	31	32	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	33	34	FPSW_ADJ+	NC
NC	SUD2	35	36	NC	NC
NC	SUD3	37	38	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	39	40	-FPVADJ	P7 - (VZZ) ⁽²⁾
NC	SUD4	41	42	NC	NC
NC	SUD5	43	44	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	45	46	NC	NC
NC	SUD6	47	48	SW_12V	for backlight pwr ⁽²⁾
NC	SUD7	49	50	GND	(GND) ⁽¹⁾

NOTES:

1. GND = P6 (VSS)
2. These power supplies need to be supplied by the user.



C.1.3 LQ9DO21 Color TFT

Jumper Settings:

- PANSEL0 = Jumper Out
- PANSEL1 = Jumper Out
- PANSEL2 = Jumper In

Table C-4. LQ9DO21 Color TFT Cabling

Flat Panel Conn	Evaluation Board Name	Evaluation Board Connector		Evaluation Board Name	Flat Panel Conn
P22 & P24 - (VCC) ⁽²⁾	SW_VCC	1	2	GND	(GND) ⁽¹⁾
NC	NC	3	4	LD0	NC
to back light enable	FPBACKEN	5	6	LD1	P6 - (B0)
NC	FPVCCEN	7	8	GND	(GND) ⁽¹⁾
NC	FPVEEN	9	10	LD2	P10 - (B1)
(GND) ⁽¹⁾	GND	11	12	LD3	P12 - (B2)
NC	BMOD	13	14	GND	(GND) ⁽¹⁾
P4 - (VSYNC)	BFLM	15	16	LD4	NC
(GND)	GND	17	18	LD5	P13 - (G0)
P6- (HSYNC)	BLP	19	20	GND	(GND) ⁽¹⁾
P28 - (ENAB)	FPDEN	21	22	LD6	P17 - (G1)
(GND) ⁽¹⁾	GND	23	24	LD7	P19 - (G2)
P10 - (CK)	SHCLKR	25	26	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	27	28	R4	NC
NC	SUD0	29	30	R5	NC
P3 - (R0)	SUD1	31	32	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	33	34	FPSW_ADJ+	NC
P5 - (R1)	SUD2	35	36	NC	NC
P7 - (R2)	SUD3	37	38	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	39	40	-FPVADJ	NC
NC	SUD4	41	42	NC	NC
NC	SUD5	43	44	GND	(GND) ⁽¹⁾
(GND) ⁽¹⁾	GND	45	46	NC	NC
NC	SUD6	47	48	SW_12V	for backlight pwr ⁽²⁾
NC	SUD7	49	50	GND	(GND) ⁽¹⁾

NOTES:

1. (GND) = P2,P8, P9,P12,P15,P20, P21,P27,P30
2. These power supplies need to be supplied by the user.



INDEX

12 V power jumper, 4-8
82C42PE keyboard controller, 3-17

A

ammeter, 3-6
ANSI specifications
 drive compliance, 5-5
auto-repeat
 keyboard feature, 5-9
autotype fixed disk, 5-5
 hard disk drives, 5-5
 IDE drives, 5-5
 overrides LBA mode control, 5-6

B

banks of memory
 limitation, 3-6
battery
 cell, 3-19
 life, 3-19
 replacement, 3-19
BIOS
 advanced menu, 5-10
 Boot Options Sub-Menu, 5-4
 COM1 and COM2 ports, 5-12
 default settings, 5-2
 disabling setup prompt, 5-2
 entering setup, 5-2
 error, 5-1
 extension, 5-11
 in memory map, 4-27
 Flash ROM disk installation, 5-11
 floppy drive install, 5-3
 floppy drive search, 5-8
 IDE adapter sub-menus, 5-4
 Integrated Peripherals sub-menu, 5-12
 key click, 5-9
 keyboard auto-repeat delay, 5-9
 keyboard auto-repeat rate, 5-9
 keyboard features sub-menu, 5-4, 5-9
 main BIOS setup menu, 5-3
 Main menu, 5-3
 memory shadowing, 5-6
 numlock feature, 5-9
 restoring default values, 5-14
 saving changes, 5-14
 saving changes to the BIOS, 5-14
 selftest, 5-1

 setup prompt, 5-8
 Setup screens, 5-1
 software, setting up, 2-8
 summary screen, 5-8
 using the menus, 5-2

block diagram, 3-1
Boot Block flip bit, 3-8
Boot Options Sub-Menu, 5-7
boot process, 5-1
boundary scan diagnostic testing, 3-2
bulletin board system (BBS), 1-4

C

CGA monitor
 setup, 5-4
chipset signals, 3-4
Cirrus Logic, 6-1
 BBS, 6-1
 CL-GD6245 video controller, 3-13
 CL-PD6710 PCMCIA chip, 3-16
 software, 6-1
 VGA CL7543, 6-1
 video BIOS, 3-10
clock frequency, 4-6
 jumper, 4-6
CMOS RAM, 5-1, A-4
COM1 and COM2 ports, 5-12
CompuServe forums, 1-4
configuring the BIOS, 2-8
configuring the evaluation board, 2-4
connectors, 4-9
conserve mode, 9-2
 options, 9-5
controlling power management peripherals, 3-5
controlling serial ports, 3-15
controlling the LED, 3-18
core limitation, 3-6
customer service, 1-4
Cyber Quest, 4-3, 4-4, 8-15
 code, 3-10
 Flash Loader Utilities, 3-10
Cyber Quest Flash Loader Utilities, 3-10

D

default values
 BIOS Setups, 5-14
diagnostics, 3-2
display drivers, 6-1

DMA transfers, 3-4
 documents, related, 1-3
 double sided DRAM SIMM
 limitations, 3-6
 doze mode, 9-2
 options, 9-6
 Doze Mode Timeout, 9-2
 DRAM, 3-5
 controller
 3 RAS Mode, 3-6
 limitations to double-sided SIMM, 3-6
 memory controller, 3-3
 timing, 3-6

E

EGA monitor
 setup, 5-4
 EMI standards, 2-1
 Enhanced Parallel Port (EPP), 3-15
 error messages, A-1
 common errors, A-1
 during POST, 5-1
 floppy diskette errors, A-1, A-2
 general failure, A-4
 hard disk failure, A-1
 invalid drive problems, A-4
 keyboard errors, A-2
 missing operating system error, A-2
 MS-DOS operating system error messages,
 A-4
 non-system disk error, A-2
 stop booting if encountered during POST, 5-8
 Ethernet
 in memory map, 4-27
 evaluation board
 block diagram, 3-1
 Extended Capabilities Port (ECP) parallel port,
 3-15, 5-13
 extended memory manager, 4-27

F

Fast-ATA specification, 3-18
 FaxBack service, 1-4
 FDC37C665IR Serial Port Chip, 3-5
 Features, 2-1
 FIFOs
 provided by Super I/O chip, 3-13
 flash

 SIMM Modules, 3-5
 socket, 3-6
 flash boot device, 3-5, 3-9, 3-10, 4-3
 control jumper, 4-7
 memory address, 3-10
 protection, 3-10
 flash disks, formatting, 2-10
 flash loader utility, 4-4
 flash memory
 BIOS emulation, 7-1
 booting, 5-7
 formatting, 7-1
 programming, 2-14
 ROM disk, 5-7
 ROM disk BIOS extension, 5-11
 socket, 3-6
 FLASH ROM chip select, 3-3
 Flash Update, 4-3
 Flash Utilities diskette, 8-14
 flat-panel displays, 3-13, 4-3
 additional support, 3-10
 cables, C-1
 jumpers, 4-3
 tested flat-panels, C-1
 Flip Bit Select, 3-9
 floppy disk controller, 3-18
 floppy disk drive, 5-3
 BIOS search, 5-8
 configuring, 2-6
 configuring the BIOS, 2-8
 controller header, 5-13
 setup, 5-3, 5-8
 force update jumper, 4-7
 forcing a BIOS update, 4-7
 formatting flash, 2-10

H

handling interrupts, 3-4
 hard disk drive
 configuring the BIOS, 2-8
 connecting to the evaluation board, 2-6
 drives larger than 528 MBytes, 5-10
 Hardware Boot Block Flip bit, 3-11
 control, 3-9
 hardware reset, 5-1
 HBBF
 jumper, 4-4
 high data transfer rates

using parallel port, 5-13

I

I/O buffer, 4-27

IDE

controller, 3-18

disk, 5-5

interface

supports two hard disk drives, 3-18

IDE Adapter Master/Slave menus, 5-4

IDE Master, 5-6

in-circuit emulator connectors, 3-2

infrared connector, 5-12

infrared interface, 3-16

infrared port, 3-13, 3-16

Input/Output signal control, 3-3

Installation, 2-4

Intel 28F004BV-T, 3-10

interrupts, 3-4

ISA bus control signals, 3-4

ISA-bus passive backplane, 4-7

J

JP10, flash boot device control jumper, 4-7

JP11, 12V power jumper, 4-8

JP3, HBBF jumper, 4-4

JP4, processor core voltage jumpers, 4-5

JP5, clock frequency jumper, 4-6

JP6, force update jumper, 4-7

JP7, 5 V power jumper, 4-7

JP8, processor core voltage jumpers, 4-5

JP9, power supply jumper, 4-7

jumpers, 4-3, 4-6, 4-7

12 V power jumper, 4-8

5 V power jumper, 4-7

clock frequency jumper, 4-6

core voltage jumpers, 4-5

flash boot device control jumper, 4-7

force update jumper, 4-7

HBBF, 4-4

power supply jumper, 4-7

K

key click, 5-9

keyboard

auto-repeat delay, 5-9

auto-repeat rate, 5-9

features, 5-4

features menu, BIOS, 5-9

keyboard controller, 3-10, 3-17

L

large disk access mode, 5-10

LCD flat panels

standard cables, 4-4

LED control, 3-18

lithium coin cell, 3-19

logic analyzer

use of, 3-2

Logical Block Addressing (LBA), 5-6

Low Battery signal, 3-3

M

Main menu, 5-3

Maxim 696 chip, 3-4

maximum memory, 3-5

memory, 3-5

addressing in 32Kbyte blocks, 3-6

limitation, 3-5

search for size, 3-5

memory map, 4-27

memory shadow regions, 5-6

setup, 5-6

MISC control register, 3-14, 3-18

monitor

setup, 5-4

monochrome monitor

setup, 5-4

M-Systems diskette, 7-3

N

notational conventions, 1-2

Numlock

features, 5-9

setup, 5-4

O

onboard IDE controller

setup, 5-13

oscillator, 3-4

P

Page Control/Boot Block Register, 3-9

parallel port, 3-15

bi-directional (SPP), 3-15

ECP and EPP compatible, 3-15

setup, 5-12

PC Card

booting from a PC Card, 7-4

- configuring, 2-6
- configuring the BIOS, 2-8
- formatting, 2-10, 7-1
- PCMCIA
 - cards supported, 3-16
 - interface, 3-16
 - standards compliance, 3-16
- Phoenix MultiKey/42 firmware, 3-17
- PhoenixBIOS, 4-4
- PicoPower
 - chipset, 2-1, 4-27
 - chipset registers, 3-3
 - PT86C768 chip, 3-3
- PLL oscillator, 3-4
- PM.EXE, 9-1
 - command line options, 9-4
 - installing, 9-1
- Port 80 display
 - controlling by software, 3-18
- Port 80 LED
 - Disabling, 3-5
- portable battery power supply, 4-7, B-1
 - connector, 3-19
- ports, controlling, 3-15
- POST Errors, 5-8
- power consumption, 3-4
 - reducing, 3-2
- power control registers, 3-5
- power management
 - activity inputs, 3-15
 - and VGA controller, 3-13
 - circuitry, 3-3
 - controller, 3-3
 - modes, 9-2
 - primary events, 9-2
 - secondary events, 9-3
 - suspend mode, 3-4
 - using power management, 9-1
- Power Management Interrupt (PMI), 3-4
- power management modes
 - conserve mode, 9-2
 - doze mode, 9-2
 - entering commands, 9-4
 - sleep mode, 9-2
- power supply, 3-19
 - jumpers, 4-7
 - options, 2-5
- primary events, 9-2

- options, 9-8
- Primary Idle Detector, 9-2
- processor
 - core voltage jumpers, 4-5
 - current
 - maximum expected, 3-2
 - measuring, 3-2
 - frequency, 3-4, 4-6
 - setting voltage, 3-2
 - voltage, 4-5, 4-6
- programmable baud rate generator, 3-13

R

- RAS control line, 3-6
- reflashing the boot block, 8-15
- registers
 - MISC control, 3-14
 - Page Control/Boot Block, 3-9
- related documents, 1-3
- reset signals, 3-4
- reset switch, 3-4, 3-20
- Revive State, 9-3
- RFA

- BIOS extension, 5-11
- booting from the RFA, 7-4
- configuring the BIOS, 2-8
- formatting, 2-10, 7-1

S

- safety standards, 2-1
- saving BIOS edits to CMOS, 5-14
- schematics
 - portable power supply, B-1
- Secondary Activity Idle Detector, 9-3
- Secondary Activity Timer, 9-3
- secondary events, 9-3
 - options, 9-9
- self-hosted reflash, 8-14
- serial ports, 3-13
- setting up the evaluation board, 2-4
- setup
 - monitor and keyboard required, 5-2
 - prompt, 5-8
- shadow memory regions, 5-6
- shadow regions, 5-6
- shadowing, 3-3
- SIMM sockets
 - two supported, 3-5

SimulSCAN

- provided by VGA controller, 3-13

- sleep mode, 9-2

- options, 9-7

- Sleep Mode Timeout, 9-2

- Slow-Clock Divisor, 9-2

- SMC Super I/O FDC37C665IR chip, 3-13

- Software Boot Block flip bit, 3-9

- speaker, 3-19

- speed

- changing speeds, 3-4

- summary screen, 5-8

- system date and time

- setup, 5-3

T

- Technical support, 1-5

- TFFS, 5-7

- installing, 7-3

- using, 7-3

- timers, 3-4

- TrueFFS software, 7-1

U

- UARTs

- provided by Super I/O chip, 3-13

- UL-1950

- meets standard, 2-1

- Ultra Low-Power Intel486TM SX Processor

- circuitry, 3-2

- upper memory blocks, 4-27

V

- Very Low Battery signal, 3-3

- VGA

- controller

- resides on local bus, 3-13

- display drivers, 6-1

- changing, 2-14

- monitor

- setup, 5-4

- software installation, 6-2, 6-6

- utilities, 6-1

- video BIOS

- reflashing, 4-3

- video controller, 3-13, 6-1

- display drivers, 6-8

- SetRES utility, 6-6

- utility programs, 6-1

- Windows drivers, 6-9

W

- Windows 3.1 display drivers, 6-9

- World Wide Web, 1-4

X

- Xilinx XC2018 chip, 3-8

