PRELIMINARY

EMBEDDED ULTRA-LOW POWER Intel486™ SX PROCESSOR

- **Ultra-Low Power Version of the Intel486 SX Processor**
  - **— 32-Bit RISC Technology Core**
  - **— 8-Kbyte Write-Through Cache**
  - **— Four Internal Write Buffers**
  - **— Burst Bus Cycles**
  - **— Dynamic Bus Sizing for 8- and 16-bit Data Bus Devices**
  - **— Intel System Management Mode (SMM)**
  - **— Boundary Scan (JTAG)**
- **176-Lead Thin Quad Flat Pack (TQFP)**
- **Separate Voltage Supply for Core Circuitry**
- **Fast Core-Clock Restart**
- **Auto Clock Freeze**
- **Ideal for Embedded Battery-Operated and Hand-Held Applications**

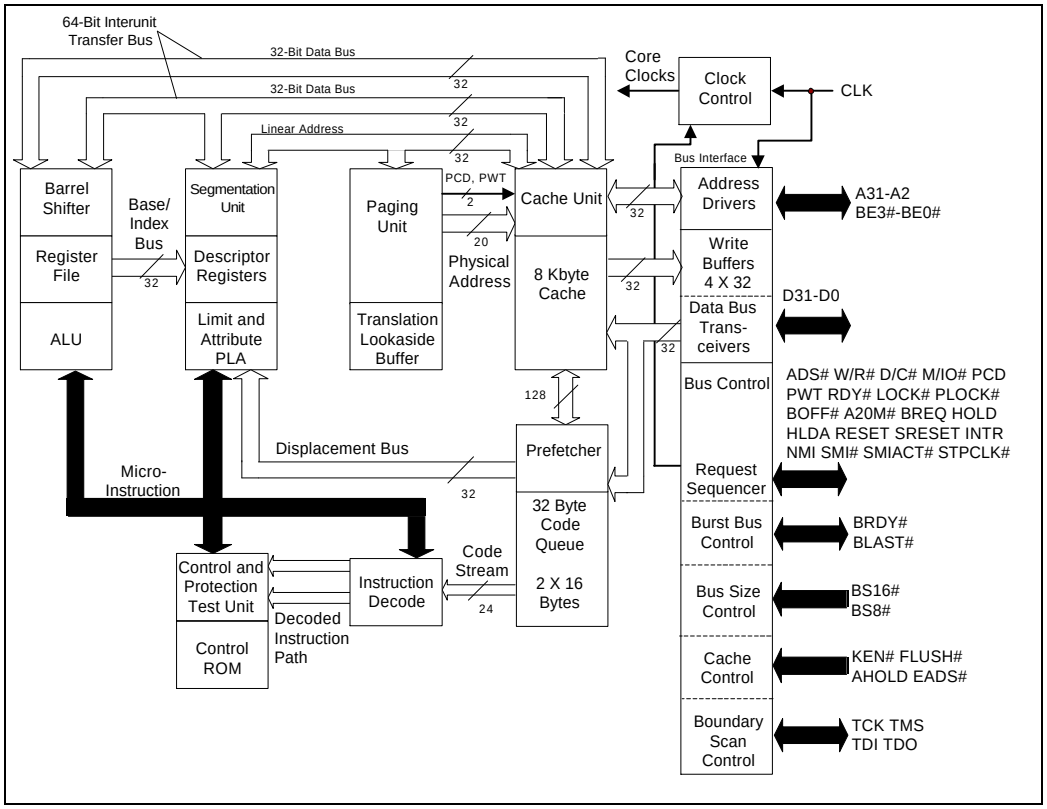

Figure 1. Embedded ULP Intel486™ SX Processor Block Diagram

September 1995 **Order Number: 272731-001**

EMBEDDED ULTRA-LOW POWER Intel486™ SX PROCESSOR

FIGURES

TABLES

1.0 INTRODUCTION

This data sheet describes the embedded Ultra-Low Power (ULP) Intel486™ SX processor. It is intended for embedded battery-operated and hand-held applications. The embedded ULP Intel486 SX processor provides all of the features of the Intel486 SX processor except for the external data-bus parity logic and the processor-upgrade pin. The processor typically uses 20% to 50% less power than the Intel486 SX processor. Additionally, the embedded ULP Intel486 SX processor external data bus has level-keeper circuitry and a fast-recovery core clock which are vital for ultra-low-power system designs. The processor is available in a Thin Quad Flat Package (TQFP) enabling low-profile component implementation.

The embedded ULP Intel486 SX processor consists of a 32-bit integer processing unit, an on-chip cache, and a memory management unit. The design ensures full instruction-set compatibility with the 8086, 8088, 80186, 80286, Intel386™ SX, Intel386 DX, and all versions of Intel486 processors.

1.1 Features

The embedded ULP Intel486 SX processor offers these features of the Intel486 SX processor:

- **32-bit RISC-Technology Core** — The embedded ULP Intel486 SX processor performs a complete set of arithmetic and logical operations on 8-, 16-, and 32-bit data types using a full-width ALU and eight general purpose registers.
- **Single Cycle Execution** — Many instructions execute in a single clock cycle.
- **Instruction Pipelining** — Overlapped instruction fetching, decoding, address translation and execution.
- **On-Chip Cache with Cache Consistency Support —** An 8-Kbyte, write-through, internal cache is used for both data and instructions. Cache hits provide zero wait-state access times for data within the cache. Bus activity is tracked to detect alterations in the memory represented by the internal cache. The internal cache can be invalidated or flushed so that an external cache controller can maintain cache consistency.
- **External Cache Control** — Write-back and flush controls for an external cache are provided so the processor can maintain cache consistency.
- **On-Chip Memory Management Unit** — Address management and memory space protection mechanisms maintain the integrity of memory in a multitasking and virtual memory environment. Both segmentation and paging are supported.
- **Burst Cycles** — Burst transfers allow a new double word to be read from memory on each bus clock cycle. This capability is especially useful for instruction prefetch and for filling the internal cache.
- **Write Buffers** — The processor contains four write buffers to enhance the performance of consecutive writes to memory. The processor can continue internal operations after a write to these buffers, without waiting for the write to be completed on the external bus.
- **Bus Backoff** — When another bus master needs control of the bus during a processor initiated bus cycle, the embedded ULP Intel486 SX processor floats its bus signals, then restarts the cycle when the bus becomes available again.
- **Instruction Restart** — Programs can continue execution following an exception generated by an unsuccessful attempt to access memory. This feature is important for supporting demand-paged virtual memory applications.
- **Dynamic Bus Sizing** — External controllers can dynamically alter the effective width of the data bus. Bus widths of 8, 16, or 32 bits can be used.
- **Boundary Scan (JTAG)** — Boundary Scan provides in-circuit testing of components on printed circuit boards. The Intel Boundary Scan implementation conforms with the IEEE Standard Test Access Port and Boundary Scan Architecture.
- **Intel System Management Mode (SMM)** — A unique Intel architecture operating mode provides a dedicated special purpose interrupt and address space that can be used to implement intelligent power management and other enhanced functions in a manner that is completely transparent to the operating system and applications software.
- **I/O Restart** — An I/O instruction interrupted by a System Management Interrupt (SMI#) can automatically be restarted following the execution of the RSM instruction.

- **Stop Clock** — The embedded ULP Intel486 SX processor has a stop clock control mechanism that provides two low-power states: a Stop Grant state (40–85 mW typical, depending on input clock frequency) and a Stop Clock state (~60 µW typical, with input clock frequency of 0 MHz).
- **Auto HALT Power Down —** After the execution of a HALT instruction, the embedded ULP Intel486 SX processor issues a normal Halt bus cycle and the clock input to the processor core is automatically stopped, causing the processor to enter the Auto HALT Power Down state (40–85 mW typical, depending on input clock frequency).

The embedded ULP Intel486 SX processor differs from the Intel486 SX processor in the following areas:

- **Processor Upgrade Removed —** The UP# signal is not provided.
- **Parity Signals Removed** — The DP3-DP0 and PCHK# signals are not provided.
- **Separate Processor-Core Power** — While the embedded ULP Intel486 SX processor requires a supply voltage of 3.3 V, the processor core has dedicated V_{CC} pins and operates with a supply voltage as low as 2.4 V.
- **Small, Low-Profile Package** — The 176-Lead Thin Quad Flat Pack (TQFP) package is approximately 26 mm square and only 1.5 mm in height. This is approximately the diameter and thickness of a U.S. quarter. The embedded ULP Intel486 SX processor is ideal for embedded hand-held and battery-powered applications.
- **Level Keeper Circuits** — The embedded ULP Intel486 SX processor has level-keeper circuits for its 32-bit external data bus signals. They retain valid high and low logic voltage levels when the processor is in the Stop Grant and Stop Clock states. This is a power-saving improvement from the floating data bus of the Intel486 SX processor.
- **Auto Clock Freeze** — The embedded ULP Intel486 SX processor monitors bus events and internal activity. The Auto Clock Freeze feature automatically controls internal clock distribution, turning off clocks to internal units when they are idle. This power-saving function is transparent to the embedded system.
- **Fast Clock Restart** — The embedded ULP Intel486 SX processor requires only eight clock periods to synchronize its internal clock with the CLK input signal. This provides for faster transition from the Stop Clock State to the Normal State. For 33-MHz operation, this synchronization time is only 240 ns compared with 1 ms (PLL startup latency) for the Intel486 processor.

1.2 Family Members

Table 1 shows the embedded ULP Intel486 SX processor and briefly describes its characteristics.

Table 1. The Embedded Ultra-Low Power Intel486™ SX Processor

Product	Supply Voltage (V_{CCP})	Processor Core Supply Voltage (V_{CC})	Processor Frequency (MHz)	Package
FA80486SXSF-33	3.3 V	2.4 V to 3.3 V	25	176-Lead TQFP
		2.7 V to 3.3 V	33	

2.0 HOW TO USE THIS DOCUMENT

The embedded ULP Intel486 SX processor has characteristics similar to the Intel486 SX processor. This document describes the new features of the embedded ULP Intel486 SX processor. Some Intel486 SX processor information is also included to minimize the dependence on the reference documents.

For a complete set of documentation related to the embedded ULP Intel486 SX processor, use this document in conjunction with the following reference documents:

- *Intel486™ Processor Family* datasheet — Order No. 242202
- *Intel486 Microprocessor Family Programmer's Reference Manual* — Order No. 240486
- Intel Application Note AP-485 — *Intel Processor Identification with the CPUID Instruction* — Order No. 241618

3.0 PIN DESCRIPTIONS

3.1 Pin Assignments

The following figures and tables show the pin assignments for the 176-pin Thin Quad Flat Pack (TQFP) package of the embedded ULP Intel486 SX processor. Included are:

- Figure 2, Package Diagram for 176-Lead TQFP Package Embedded ULP Intel486™ SX Processor (pg. 4)
- Table 2, Pin Assignment for 176-Lead TQFP Package Embedded ULP Intel486™ SX Processor (pg. 5)
- Table 3, Pin Cross Reference for 176-Lead TQFP Package Embedded ULP Intel486™ SX Processor (pg. 6)
- Table 4, Embedded ULP Intel486™ SX Processor Pin Descriptions (pg. 7)
- Table 5, Output Pins (pg. 13)
- Table 6, Input/Output Pins (pg. 13)
- Table 7, Test Pins (pg. 13)
- Table 8, Input Pins (pg. 14)

The tables and figures show "no-connects" as "N/C." These pins should always remain unconnected. Connecting N/C pins to V_{CC}, V_{CCP}, V_{SS}, or any other signal pin can result in component malfunction or incompatibility with future steppings of the embedded ULP Intel486 SX processor.

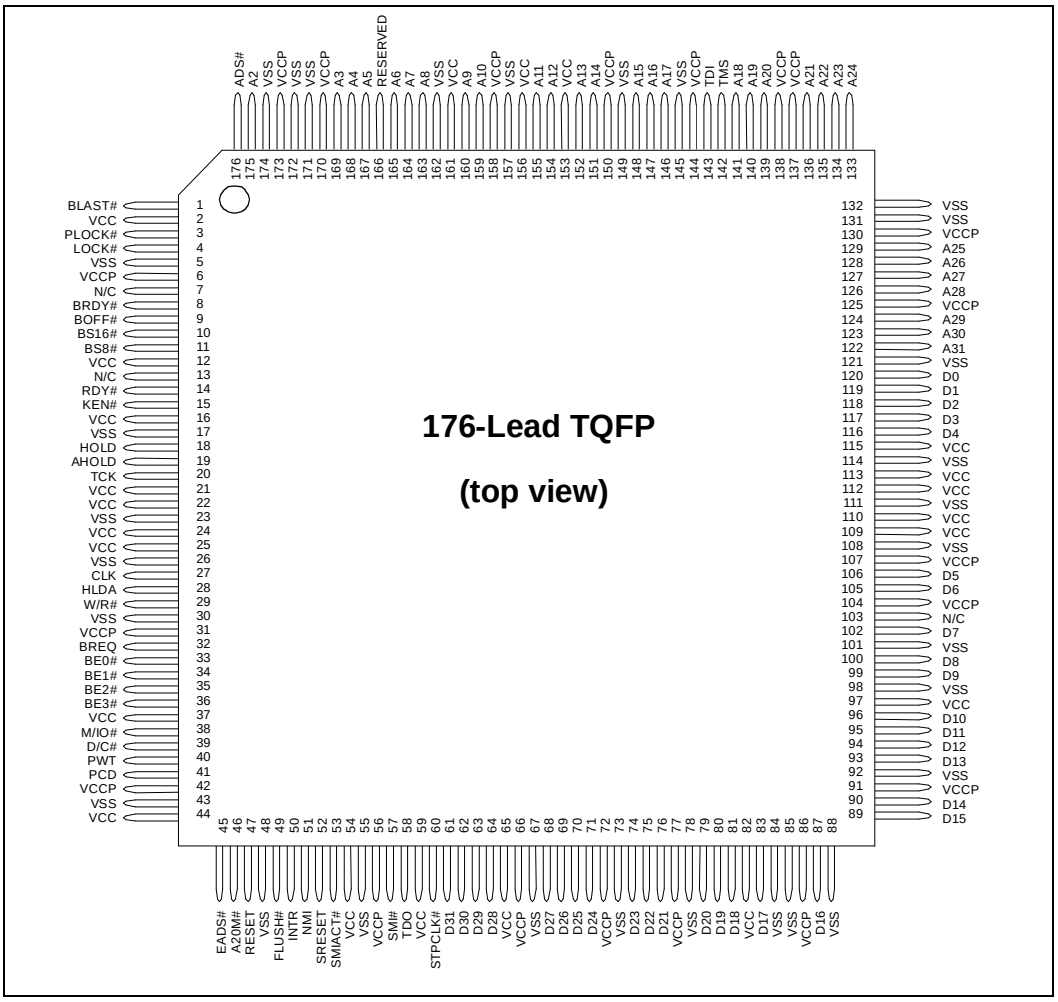

Figure 2. Package Diagram for 176-Lead TQFP Package Embedded ULP Intel486™ SX Processor

Table 2. Pin Assignment for 176-Lead TQFP Package
Embedded ULP Intel486™ SX Processor

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
1	BLAST#	45	EADS#	89	D15	133	A24
2	V_{CC}	46	A20M#	90	D14	134	A23
3	PLOCK#	47	RESET	91	V_{CCP}	135	A22
4	LOCK#	48	V_{SS}	92	V_{SS}	136	A21
5	V_{SS}	49	FLUSH#	93	D13	137	V_{CCP}
6	V_{CCP}	50	INTR	94	D12	138	V_{CCP}
7	N/C	51	NMI	95	D11	139	A20
8	BRDY#	52	SRESET	96	D10	140	A19
9	BOFF#	53	SMIACT#	97	V_{CC}	141	A18
10	BS16#	54	V_{CC}	98	V_{SS}	142	TMS
11	BS8#	55	V_{SS}	99	D9	143	TDI
12	V_{CC}	56	V_{CCP}	100	D8	144	V_{CCP}
13	N/C	57	SMI#	101	V_{SS}	145	V_{SS}
14	RDY#	58	TDO	102	D7	146	A17
15	KEN#	59	V_{CC}	103	N/C	147	A16
16	V_{CC}	60	STPCLK#	104	V_{CCP}	148	A15
17	V_{SS}	61	D31	105	D6	149	V_{SS}
18	HOLD	62	D30	106	D5	150	V_{CCP}
19	AHOLD	63	D29	107	V_{CCP}	151	A14
20	TCK	64	D28	108	V_{SS}	152	A13
21	V_{CC}	65	V_{CC}	109	V_{CC}	153	V_{CC}
22	V_{CC}	66	V_{CCP}	110	V_{CC}	154	A12
23	V_{SS}	67	V_{SS}	111	V_{SS}	155	A11
24	V_{CC}	68	D27	112	V_{CC}	156	V_{CC}
25	V_{CC}	69	D26	113	V_{CC}	157	V_{SS}
26	V_{SS}	70	D25	114	V_{SS}	158	V_{CCP}
27	CLK	71	D24	115	V_{CC}	159	A10
28	HLDA	72	V_{CCP}	116	D4	160	A9
29	W/R#	73	V_{SS}	117	D3	161	V_{CC}
30	V_{SS}	74	D23	118	D2	162	V_{SS}
31	V_{CCP}	75	D22	119	D1	163	A8
32	BREQ	76	D21	120	D0	164	A7
33	BE0#	77	V_{CCP}	121	V_{SS}	165	A6
34	BE1#	78	V_{SS}	122	A31	166	RESERVED
35	BE2#	79	D20	123	A30	167	A5
36	BE3#	80	D19	124	A29	168	A4
37	V_{CC}	81	D18	125	V_{CCP}	169	A3
38	M/IO#	82	V_{CC}	126	A28	170	V_{CCP}
39	D/C#	83	D17	127	A27	171	V_{SS}
40	PWT	84	V_{SS}	128	A26	172	V_{SS}
41	PCD	85	V_{SS}	129	A25	173	V_{CCP}
42	V_{CCP}	86	V_{CCP}	130	V_{CCP}	174	V_{SS}
43	V_{SS}	87	D16	131	V_{SS}	175	A2
44	V_{CC}	88	V_{SS}	132	V_{SS}	176	ADS#

Table 3. Pin Cross Reference for 176-Lead TQFP Package
Embedded ULP Intel486™ SX Processor

Address	Pin #	Data	Pin #	Control	Pin #	N/C	V_{CCP}	V_{CC}	V_{SS}
A2	175	D0	120	AHOLD	19	7	6	2	5
A3	169	D1	119	BE0#	33	13	31	12	17
A4	168	D2	118	BE1#	34	103	42	16	23
A5	167	D3	117	BE2#	35		56	21	26
A6	165	D4	116	BE3#	36		66	22	30
A7	164	D5	106	BLAST#	1		72	24	43
A8	163	D6	105	BOFF#	9		77	25	48
A9	160	D7	102	BRDY#	8		86	37	55
A10	159	D8	100	BREQ	32		91	44	67
A11	155	D9	99	BS16#	10		104	54	73
A12	154	D10	96	BS8#	11		107	59	78
A13	152	D11	95	CLK	27		125	65	84
A14	151	D12	94	D/C#	39		130	82	85
A15	148	D13	93	HLDA	28		137	97	88
A16	147	D14	90	HOLD	18		138	109	92
A17	146	D15	89	KEN#	15		144	110	98
A18	141	D16	87	LOCK#	4		150	112	101
A19	140	D17	83	M/IO#	38		158	113	108
A20	139	D18	81	PCD	41		170	115	111
A21	136	D19	80	PLOCK#	3		173	153	114
A22	135	D20	79	PWT	40			156	121
A23	134	D21	76	RESERVED	166			161	131
A24	133	D22	75	RDY#	14				132
A25	129	D23	74	TCK	20				145
A26	128	D24	71	W/R#	29				149
A27	127	D25	70	A20M#	46				157
A28	126	D26	69	EADS#	45				162
A29	124	D27	68	FLUSH#	49				171
A30	123	D28	64	INTR	50				172
A31	122	D29	63	NMI	51				174
		D30	62	RESET	47				
		D31	61	SMI#	57				
				SMIACT#	53				
				SRESET	52				
				STPCLK#	60				
				TDO	58				
				ADS#	176				
				TDI	143				
				TMS	142				
				W/R#	29				

3.2 Pin Quick Reference

The following is a brief pin description. For detailed signal descriptions refer to “Signal Description” in section 9 of the *Intel486™ Processor Family* datasheet.

Table 4. Embedded ULP Intel486™ SX Processor Pin Descriptions (Sheet 1 of 6)

Symbol	Type	Name and Function
CLK	I	**Clock** provides the fundamental timing and internal operating frequency for the embedded ULP Intel486 SX processor. All external timing parameters are specified with respect to the rising edge of CLK.
ADDRESS BUS		
A31-A4 **A3–A2**	I/O O	**Address Lines** A31–A2, together with the byte enable signals, BE3#–BE0#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the embedded ULP Intel486 SX processor to perform cache line invalidation. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.
BE3# **BE2#** **BE1#** **BE0#**	O O O O	**Byte Enable** signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3#–BE0# are active LOW and are not driven during bus hold. BE3# applies to D31–D24 BE2# applies to D23–D16 BE1# applies to D15–D8 BE0# applies to D7–D0
DATA BUS		
D31–D0	I/O	**Data Lines.** D7–D0 define the least significant byte of the data bus; D31–D24 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
BUS CYCLE DEFINITION		
M/IO# **D/C#** **W/R#**	O O O	**Memory/Input-Output**, **Data/Control** and **Write/Read** lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted. **M/IO# D/C# W/R# Bus Cycle Initiated** 0 0 0 Interrupt Acknowledge 0 0 1 HALT/Special Cycle (see details below) 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write **HALT/Special Cycle** **Cycle Name** — **BE3# - BE0#** — **A4-A2** Shutdown — 1110 — 000 HALT — 1011 — 000 Stop Grant bus cycle — 1011 — 100

Table 4. Embedded ULP Intel486™ SX Processor Pin Descriptions (Sheet 2 of 6)

Symbol	Type	Name and Function
LOCK#	O	**Bus Lock** indicates that the current bus cycle is locked. The embedded ULP Intel486 SX processor does not allow a bus hold when LOCK# is asserted (address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when Ready is returned. LOCK# is active LOW and not driven during bus hold. Locked read cycles are not transformed into cache fill cycles when KEN# is returned active.
PLOCK#	O	**Pseudo-Lock** indicates that the current bus transaction requires more than one bus cycle to complete. For the embedded ULP Intel486 SX processor, examples of such operations are segment table descriptor reads (64 bits) and cache line fills (128 bits). The embedded ULP Intel486 SX processor drives PLOCK# active until the addresses for the last bus cycle of the transaction are driven, regardless of whether RDY# or BRDY# have been returned. PLOCK# is a function of the BS8#, BS16# and KEN# inputs. PLOCK# should be sampled only in the clock in which Ready is returned. PLOCK# is active LOW and is not driven during bus hold.
BUS CONTROL		
ADS#	O	**Address Status** output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock in which the addresses are driven. ADS# is active LOW and not driven during bus hold.
RDY#	I	**Non-burst Ready** input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the embedded ULP Intel486 SX processor in response to a write. RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. RDY# is active during address hold. Data can be returned to the embedded ULP Intel486 SX processor while AHOLD is active. RDY# is active LOW and is not provided with an internal pull-up resistor. RDY# must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.

Table 4. Embedded ULP Intel486™ SX Processor Pin Descriptions (Sheet 3 of 6)

Symbol	Type	Name and Function
BURST CONTROL		
BRDY#	I	**Burst Ready** input performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. Data presented on the data bus is strobed into the embedded ULP Intel486 SX processor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely aborted. BRDY# is active LOW and is provided with a small pull-up resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.
BLAST#	O	**Burst Last** signal indicates that the next time BRDY# is returned, the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	**Reset** input forces the embedded ULP Intel486 SX processor to begin execution at a known state. The processor cannot begin executing instructions until at least 1 ms after V_{CC}, V_{CCP}, and CLK have reached their proper DC and AC specifications. The RESET pin must remain active during this time to ensure proper processor operation. However, for warm resets, RESET should remain active for at least 15 CLK periods. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
INTR	I	**Maskable Interrupt** indicates that an external interrupt has been generated. When the internal interrupt flag is set in EFLAGS, active interrupt processing is initiated. The embedded ULP Intel486 SX processor generates two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to ensure processor recognition of the interrupt. INTR is active HIGH and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
NMI	I	**Non-Maskable Interrupt** request signal indicates that an external non-maskable interrupt has been generated. NMI is rising-edge sensitive and must be held LOW for at least four CLK periods before this rising edge. NMI is not provided with an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
SRESET	I	**Soft Reset** pin duplicates all functionality of the RESET pin except that the SMBASE register retains its previous value. For soft resets, SRESET must remain active for at least 15 CLK periods. SRESET is active HIGH. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

Table 4. Embedded ULP Intel486™ SX Processor Pin Descriptions (Sheet 4 of 6)

Symbol	Type	Name and Function
SMI#	I	**System Management Interrupt** input invokes System Management Mode (SMM). SMI# is a falling-edge triggered signal which forces the embedded ULP Intel486 SX processor into SMM at the completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# does not break LOCKed bus cycles and cannot interrupt a currently executing SMM. The embedded ULP Intel486 SX processor latches the falling edge of one pending SMI# signal while it is executing an existing SMI#. The nested SMI# is not recognized until after the execution of a Resume (RSM) instruction.
SMIACT#	O	**System Management Interrupt Active**, an active LOW output, indicates that the embedded ULP Intel486 SX processor is operating in SMM. It is asserted when the processor begins to execute the SMI# state save sequence and remains active LOW until the processor executes the last state restore cycle out of SMRAM.
STPCLK#	I	**Stop Clock Request** input signal indicates a request was made to turn off or change the CLK input frequency. When the embedded ULP Intel486 SX processor recognizes a STPCLK#, it stops execution on the next instruction boundary (unless superseded by a higher priority interrupt), empties all internal pipelines and write buffers, and generates a Stop Grant bus cycle. STPCLK# is active LOW. **STPCLK# is an asynchronous signal, but must remain active until the embedded ULP Intel486 SX processor issues the Stop Grant bus cycle. STPCLK# may be de-asserted at any time after the processor has issued the Stop Grant bus cycle.**
BUS ARBITRATION		
BREQ	O	**Bus Request** signal indicates that the embedded ULP Intel486 SX processor has internally generated a bus request. BREQ is generated whether or not the processor is driving the bus. BREQ is active HIGH and is never floated.
HOLD	I	**Bus Hold Request** allows another bus master complete control of the embedded ULP Intel486 SX processor bus. In response to HOLD going active, the processor floats most of its output and input/output pins. HLDA is asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The embedded ULP Intel486 SX processor remains in this state until HOLD is de-asserted. HOLD is active HIGH and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.
HLDA	O	**Hold Acknowledge** goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the embedded ULP Intel486 SX processor has given the bus to another local bus master. HLDA is driven active in the same clock that the processor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.
BOFF#	I	**Backoff** input forces the embedded ULP Intel486 SX processor to float its bus in the next clock. The processor floats all pins normally floated during bus hold but HLDA is not asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The embedded ULP Intel486 SX processor remains in bus hold until BOFF# is negated. If a bus cycle is in progress when BOFF# is asserted the cycle is restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.

Table 4. Embedded ULP Intel486™ SX Processor Pin Descriptions (Sheet 5 of 6)

Symbol	Type	Name and Function
CACHE INVALIDATION		
AHOLD	I	**Address Hold** request allows another bus master access to the embedded ULP Intel486 SX processor's address bus for a cache invalidation cycle. The processor stops driving its address bus in the clock following AHOLD going active. Only the address bus is floated during address hold, the remainder of the bus remains active. AHOLD is active HIGH and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	**External Address** - This signal indicates that a *valid* external address has been driven onto the embedded ULP Intel486 SX processor address pins. This address is used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pull-up resistor. EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.
CACHE CONTROL		
KEN#	I	**Cache Enable** pin is used to determine whether the current cycle is cacheable. When the embedded ULP Intel486 SX processor generates a cycle that can be cached and KEN# is active one clock before RDY# or BRDY# during the first transfer of the cycle, the cycle becomes a cache line fill cycle. Returning KEN# active one clock before RDY# during the last read in the cache line fill causes the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pull-up resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for proper operation.
FLUSH#	I	**Cache Flush** input forces the embedded ULP Intel486 SX processor to flush its entire internal cache. FLUSH# is active LOW and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock.
PAGE CACHEABILITY		
PWT **PCD**	O O	**Page Write-Through** and **Page Cache Disable** pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry, page directory entry or control register 3 (CR3) when paging is enabled. When paging is disabled, the embedded ULP Intel486 SX processor ignores the PCD and PWT bits and assumes they are zero for the purpose of caching and driving PCD and PWT pins. PWT and PCD have the same timing as the cycle definition pins (M/IO#, D/C#, and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.
BUS SIZE CONTROL		
BS16# **BS8#**	I I	**Bus Size 16** and **Bus Size 8** pins (bus sizing pins) cause the embedded ULP Intel486 SX processor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The processor uses the state of these pins in the clock before Ready to determine bus size. These signals are active LOW and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.

Table 4. Embedded ULP Intel486™ SX Processor Pin Descriptions (Sheet 6 of 6)

Symbol	Type	Name and Function
ADDRESS MASK		
A20M#	I	**Address Bit 20 Mask** pin, when asserted, causes the embedded ULP Intel486 SX processor to mask physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at 1 Mbyte, which occurs on the 8086 processor. A20M# is active LOW and should be asserted only when the embedded ULP Intel486 SX processor is in real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled HIGH at the falling edge of RESET.
TEST ACCESS PORT		
TCK	I	**Test Clock**, an input to the embedded ULP Intel486 SX processor, provides the clocking function required by the JTAG Boundary scan feature. TCK is used to clock state information (via TMS) and data (via TDI) into the component on the rising edge of TCK. Data is clocked out of the component (via TDO) on the falling edge of TCK. TCK is provided with an internal pull-up resistor.
TDI	I	**Test Data Input** is the serial input used to shift JTAG instructions and data into the processor. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR TAP controller states. During all other Test Access Port (TAP) controller states, TDI is a “don’t care.” TDI is provided with an internal pull-up resistor.
TDO	O	**Test Data Output** is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times TDO is driven to the high impedance state.
TMS	I	**Test Mode Select** is decoded by the JTAG TAP to select test logic operation. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.
RESERVED PINS		
RESERVED	I	**Reserved** is reserved for future use. This pin MUST be connected to an external pull-up resistor circuit. The recommended resistor value is 10 kOhms.

Table 5. Output Pins

Name	Active Level	Output Signal		
		Floated During Address Hold	Floated During Bus Hold	During Stop Grant and Stop Clock States[1]
BREQ	HIGH			Previous State
HLDA	HIGH			As per HOLD
BE3#-BE0#	LOW		•	Previous State
PWT, PCD	HIGH		•	Previous State
W/R#, M/IO#, D/C#	HIGH/LOW		•	Previous State
LOCK#	LOW		•	HIGH (inactive)
PLOCK#	LOW		•	HIGH (inactive)
ADS#	LOW		•	HIGH (inactive)
BLAST#	LOW		•	Previous State
A3-A2	HIGH	•	•	Previous State
SMIACT#	LOW			Previous State

NOTE:

1. The term “Previous State” means that the processor maintains the logic level applied to the signal pin just before the processor entered the Stop Grant state. This conserves power by preventing the signal pin from floating.

Table 6. Input/Output Pins

Name	Active Level	Output Signal		
		Floated During Address Hold	Floated During Bus Hold	During Stop Grant and Stop Clock States[1,2]
D31-D0	HIGH		•	Level-Keeper
A31-A4	HIGH	•	•	Previous State

NOTES:

1. The term “Level-Keeper” means that the processor maintains the most recent logic level applied to the signal pin. This conserves power by preventing the signal pin from floating. If a system component, other than the processor, temporarily drives these signal pins and then floats them, the processor forces and maintains the most recent logic levels that were applied by the system component.
2. The term “Previous State” means that the processor maintains the logic level applied to the signal pin just before the processor entered the Stop Grant state. This conserves power by preventing the signal pin from floating.

Table 7. Test Pins

Name	Input or Output	Sampled/ Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Failing Edge of TCK
TMS	Input	Rising Edge of TCK

Table 8. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Pull-Up/ Pull-Down
CLK			
RESET	HIGH	Asynchronous	
SRESET	HIGH	Asynchronous	Pull-Down
HOLD	HIGH	Synchronous	
AHOLD	HIGH	Synchronous	Pull-Down
EADS#	LOW	Synchronous	Pull-Up
BOFF#	LOW	Synchronous	Pull-Up
FLUSH#	LOW	Asynchronous	Pull-Up
A20M#	LOW	Asynchronous	Pull-Up
BS16#, BS8#	LOW	Synchronous	Pull-Up
KEN#	LOW	Synchronous	Pull-Up
RDY#	LOW	Synchronous	
BRDY#	LOW	Synchronous	Pull-Up
INTR	HIGH	Asynchronous	
NMI	HIGH	Asynchronous	
RESERVED			
SMI#	LOW	Asynchronous	Pull-Up
STPCLK#	LOW	Asynchronous	Pull-Up
TCK	HIGH		Pull-Up
TDI	HIGH		Pull-Up
TMS	HIGH		Pull-Up

4.0 ARCHITECTURAL AND FUNCTIONAL OVERVIEW

The embedded ULP Intel486 SX processor architecture is essentially the same as the 3.3 V Intel486 SX processor with a 1X clock (CLK) input. Refer to the *Intel486™ Processor Family* datasheet (242202) for a description of the Intel486 SX processor. With some minor exceptions, the following datasheet sections apply to the embedded ULP Intel486 SX processor:

- Architectural Overview
- Real Mode Architecture
- Protected Mode Architecture
- On-Chip Cache
- System Management Mode (SMM) Architectures
- Hardware Interface
- Bus Operation
- Testability
- Debugging Support
- Instruction Set Summary
- Differences Between Intel486 Processors and Intel386™ Processors

Exceptions to these sections of the datasheet are:

- The information pertaining to parity signals for the external data bus does not apply. The embedded ULP Intel486 SX processor does not have DP0#, DP1#, DP2#, DP3# and PCHK# signal pins.

- References to the Upgrade Power Down Mode do not apply. The embedded ULP Intel486 SX processor does not have the UP# signal pin and does not support the Intel OverDrive® processor.
- References to "V_{CC}" are called "V_{CCP}" by the embedded ULP Intel486 SX processor when the supply voltage pertains to the processor's external interface drivers and receivers. The term "V_{CC}" pertains only to the processor core supply voltage of the embedded ULP Intel486 SX processor. Information about the split-supply voltage is provided in this datasheet.
- The Phase-Locked Loop (PLL) circuit of the 1X clock (CLK) input has been replaced by a proprietary Differential Delay Line (DDL) circuit that has a faster recovery time. Datasheet references to the PLL and its 1 ms recovery time are replaced with the DDL circuit and its eight-CLK recovery time. Information about the DDL circuit and recovery time is provided in this datasheet.
- The embedded ULP Intel486 SX processor has level-keeper circuits for its external 32-bit data bus signals (D31-D0). The Intel486 SX processor floats its data bus instead. More information about the level-keeper circuitry is provided in this datasheet.
- The datasheet describes the processor supply-current consumption for the Auto HALT Power Down, Stop Grant, and Stop Clock states. This supply-current consumption for the embedded ULP Intel486 SX processor is much less than that of the Intel486 SX processor. Information about power consumption and these states is provided in this datasheet.
- The CPU ID, Boundary-Scan (JTAG) ID, and boundary-scan register bits for the embedded ULP Intel486 SX processor are in this datasheet.
- The embedded ULP Intel486 SX processor has one pin reserved for possible future use. This pin is an input signal, pin 166. It is called RESERVED and must be connected to a 10-KΩ pull-up resistor.

4.1 Separate Supply Voltages

The embedded ULP Intel486 SX processor has separate voltage-supply planes for its internal core-processor circuits and its external driver/receiver circuits. The supply voltage for the internal core processor is named V_{CC} and the supply voltage for the external circuits is named V_{CCP}.

For a single-supply voltage design, the embedded ULP Intel486 SX processor is functional at 3.3 V ± 0.3 V. In this type of system design, the processor's V_{CC} and V_{CCP} pins must be tied to the same power plane.

Even though V_{CCP} must be 3.3 V ± 0.3 V, the processor's external-output circuits can drive TTL-compatible components. However, the processor's external-input circuits do not allow connection to TTL-compatible components. **Section 5.2, DC Specifications (pg. 22)** contains the DC specifications for the processor's input and output signals.

For lower-power operation, a separate, lower voltage for V_{CC} can be chosen, but V_{CCP} must be 3.3 V ± 0.3 V. Any voltage value between 2.4 V and 3.3 V can be chosen for V_{CC} for guaranteed processor operation up to 25 MHz. The embedded ULP Intel486 SX processor can also operate at 33 MHz, provided the V_{CC} value chosen is between 2.7 V and 3.3 V. **Section 5.2, DC Specifications (pg. 22)** defines supply voltage specifications.

In systems with separate V_{CC} and V_{CCP} power planes, the processor-core voltage supply must always be less than or equal to the processor's external-interface voltage supply; e.g., the system design must guarantee:

$$V_{CC} \leq V_{CCP}$$

Violating this relationship causes excessive power consumption. Limited testing has shown no component damage when this relationship is violated. However, prolonged violation is not recommended and component integrity is not guaranteed.

The $V_{CC} \leq V_{CCP}$ relationship must also be guaranteed by the system design during power-up and power-down sequences. Refer to Figure 3.

Even though V_{CC} must be less than or equal to V_{CCP}, it is recommended that the system's power-on sequence allows V_{CC} to quickly achieve its operational level once V_{CCP} achieves its operational level. Similarly, the power-down sequence should allow V_{CCP} to power down quickly after V_{CC} is below the operational voltage level. These recommendations are given to keep power consumption at a minimum. Deviating from the recommendations does not create a component reliability problem, but power consumption of the processor's external interface circuits increases beyond normal operating values.

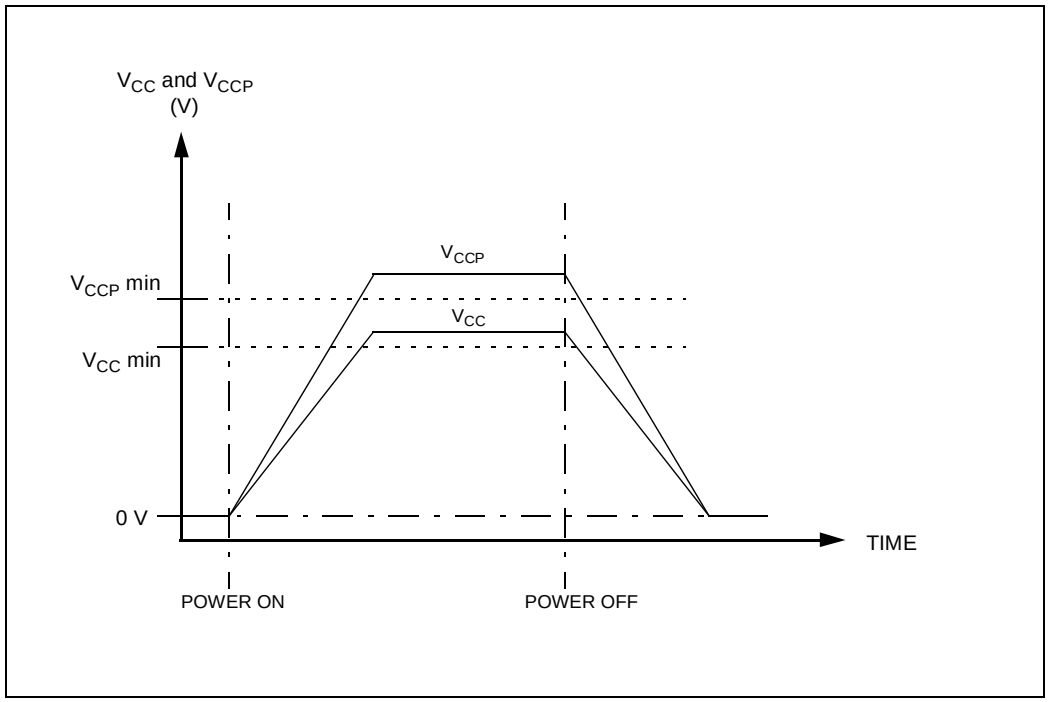

Figure 3. Example of Supply Voltage Power Sequence

4.2 Fast Clock Restart

The embedded ULP Intel486 SX processor has an integrated proprietary differential delay line (DDL) circuit for internal clock generation. The DDL is driven by the CLK input signal provided by the external system. During normal operation, the external system must guarantee that the CLK signal maintains its frequency so that the clock period deviates no more than 250 ps/CLK. This state, called the Normal State, is shown in Figure 4.

To increase or decrease the CLK frequency more quickly than this, the system must interrupt the processor with the STPCLK# signal. Once the processor indicates that it is in the Stop Grant State, the system can adjust the CLK signal to the new frequency, wait a minimum of eight CLK periods, then force the processor to return to the normal operational state by deactivating the STPCLK# interrupt.

This wait of eight CLK periods is much faster than the 1 ms wait required by earlier Intel486 SX processor products.

While in the Stop Grant State, the external system may deactivate the CLK signal to the processor. This forces the processor to the Stop Clock State — the state in which the processor consumes the least power. Once the system reactivates the CLK signal, the processor transitions to the Stop Grant State within eight CLK periods.

Normal operation can be resumed by deactivating the STPCLK# interrupt signal. Here again, the embedded ULP Intel486 SX processor recovers from the Stop Clock State much faster than the 1 ms PLL recovery of earlier Intel486 SX processors.

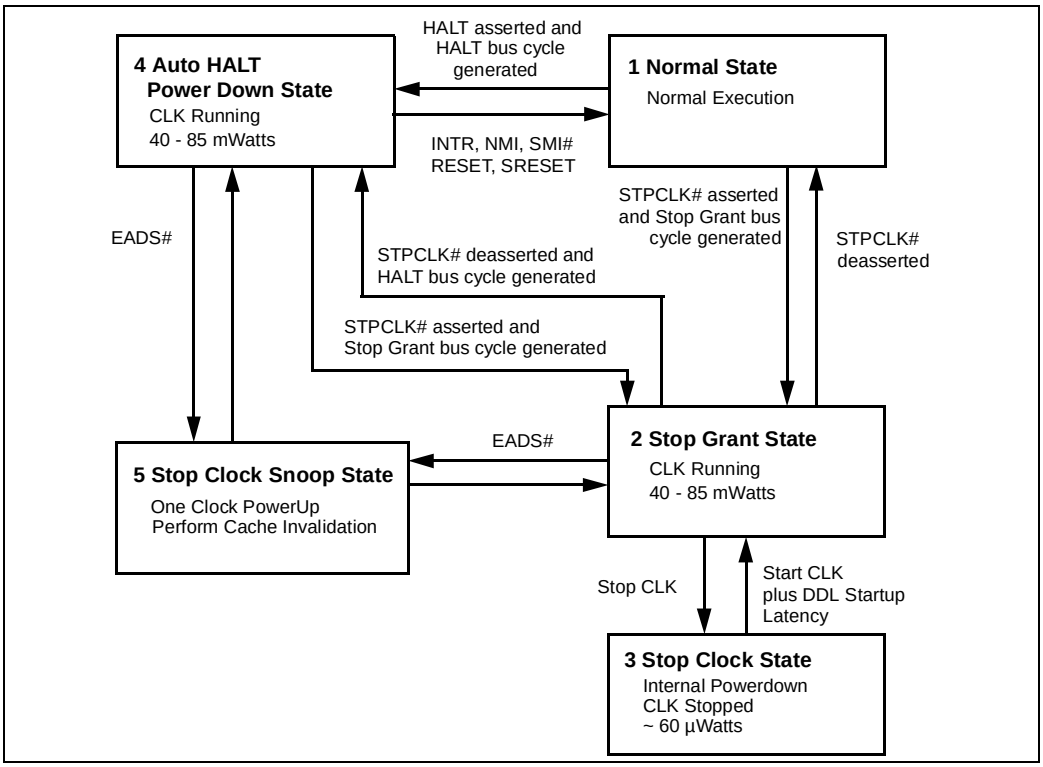

Figure 4. Stop Clock State Diagram with Typical Power Consumption Values

4.3 Level-Keeper Circuits

To obtain the lowest possible power consumption during the Stop Grant and Stop Clock states, system designers must ensure that:

- input signals with pull-up resistors are not driven LOW
- input signals with pull-down resistors are not driven HIGH

See Table 8, Input Pins (pg. 14) for the list of signals with internal pull-up and pull-down resistors.

All other input pins except A31-A4 and D31-D0 must be driven to the power supply rails to ensure lowest possible current consumption.

During the Stop Grant and Stop Clock states, most processor output signals maintain their previous condition, which is the level they held when entering the Stop Grant state. In response to HOLD driven active during the Stop Grant state when the CLK input is running, the embedded ULP Intel486 SX processor generates HLDA and floats all output and input/output signals which are floated during the HOLD/HLDA state. When HOLD is deasserted, processor signals which maintain their previous state return to the state they were in prior to the HOLD/HLDA sequence.

The data bus (D31-D0) also maintains its previous state during the Stop Grant and Stop Clock states, but does so differently, as described in the following paragraphs.

The embedded ULP Intel486 SX processor's data bus pins (D31-D0) have level keepers which maintain their previous states while in the Stop Grant and Stop Clock states. In response to HOLD driven active during the Stop Grant state when the CLK input is running, the embedded ULP Intel486 SX processor generates HLDA and floats D31-D0 throughout the HOLD/HLDA cycles. When HOLD is deasserted, the processor's D31-D0 signals return to the states they were in prior to the HOLD/HLDA sequence.

At all other times during the Stop Grant and Stop Clock states, the processor maintains the logic levels of D31-D0. When the external system circuitry drives D31-D0 to different logic levels, the processor flips its D31-D0 logic levels to match the ones driven by the external system. The processor maintains (keeps) these new levels even after the external circuitry stops driving D31-D0.

For some system designs, external resistors may not be required on D31- D0 (they are required on previous Intel486 SX processor designs). System designs that never request Bus Hold during the Stop Grant and Stop Clock states might not require external resistors. If the system design uses Bus Hold during these states, the processor disables the level-keepers and floats the data bus. This type of design would require some kind of data bus termination to minimize power consumption. It is strongly recommended that the D31-D0 pins do not have network resistors connected. External resistors used in the system design must be of a sufficient resistance value to "flip" the level-keeper circuitry and eliminate potential DC paths.

The level-keeper circuit is designed to allow an external 27-KΩ pull-up resistor to switch the D31-D0 circuits to a logic-HIGH level even though the level-keeper attempts to keep a logic-LOW level. In general, pull-up resistors smaller than 27 KΩ can be used as well as those greater than or equal to 1 MΩ. Pull-down resistors, when connected to D31-D0, should be least 800 KΩ.

4.4 Low-Power Features

As with other Intel486 processors, the embedded ULP Intel486 SX processor minimizes power consumption by providing the Auto HALT Power Down, Stop Grant, and Stop Clock states (see Figure 4). The embedded ULP Intel486 SX processor has an Auto Clock Freeze feature that further conserves power by judiciously deactivating its internal clocks while in the Normal Execution Mode. The power-conserving mechanism is designed such that it does not degrade processor performance or require changes to AC timing specifications.

4.4.1 Auto Clock Freeze

To reduce power consumption, during the following bus cycles — under certain conditions — the processor slows-up or freezes some internal clocks:

- Data-Read Wait Cycles (Memory, I/O and Interrupt Acknowledge)
- Data-Write Wait Cycles (Memory, I/O)
- HOLD/HLDA Cycles
- AHOLD Cycles
- BOFF Cycles

Power is conserved during the wait periods in these cycles until the appropriate external-system signals are sent to the processor. These signals include:

- READY
- NMI, SMI#, INTR, and RESET
- BOFF#
- FLUSH#
- EADS#
- BS8#, BS16# and KEN# transitions

The embedded ULP Intel486 SX processor also reduces power consumption by temporarily freezing the clocks of its internal logic blocks. When a logic block is idle or in a wait state, its clock is frozen.

4.5 CPUID Instruction

The embedded ULP Intel486 SX processor supports the CPUID instruction (see Table 9). Because not all Intel processors support the CPUID instruction, a simple test can determine if the instruction is supported. The test involves the processor's ID Flag, which is bit 21 of the EFLAGS register. If software can change the value of this flag, the CPUID instruction is available. The actual state of the ID Flag bit is irrelevant and provides no significance to the hardware. This bit is cleared (reset to zero) upon device reset (RESET or SRESET) for compatibility with Intel486 processor designs that do not support the CPUID instruction.

CPUID-instruction details are provided here for the embedded ULP Intel486 SX processor. Refer to Intel Application Note AP-485 *Intel Processor Identification with the CPUID Instruction* (Order No. 241618) for a description that covers all aspects of the CPUID instruction and how it pertains to other Intel processors.

4.5.1 Operation of the CPUID Instruction

The CPUID instruction requires the software developer to pass an input parameter to the processor in the EAX register. The processor response is returned in registers EAX, EBX, EDX, and ECX.

Table 9. CPUID Instruction Description

OP CODE	Instruction	Processor Core Clocks	Parameter passed in EAX (Input Value)	Description
0F A2	CPUID	9	0	Vendor (Intel) ID String
		14	1	Processor Identification
		9	> 1	Undefined (Do Not Use)

Vendor ID String - When the parameter passed in EAX is 0 (zero), the register values returned upon instruction execution are shown in the following table.

		31----------24	23----------16	15----------8	7----------0
High Value (= 1)	**EAX**	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1
Vendor ID String	**EBX**	u (75)	n (6E)	e (65)	G (47)
(ASCII	**EDX**	I (49)	e (65)	n (6E)	i (69)
Characters)	**ECX**	l (6C)	e (65)	t (74)	n (6E)

The values in EBX, EDX and ECX indicate an Intel processor. When taken in the proper order, they decode to the string "GenuineIntel."

Processor Identification - When the parameter passed to EAX is 1 (one), the register values returned upon instruction execution are:

		31----14	13,12	11----8	7----4	3----0
Processor Signature	**EAX**	(Do Not Use) Intel Reserved	0 0 Processor Type	0 1 0 0 Family	0 0 1 0 Model	XXXX Stepping

(Intel releases information about stepping numbers as needed)

		31----0
Intel Reserved	**EBX**	Intel Reserved
(Do Not Use)	**ECX**	Intel Reserved

		31----2	1	0
Feature Flags	**EDX**	0----0	1 VME	0 FPU

4.6 Identification After Reset

Processor Identification - Upon reset, the EDX register contains the processor signature:

		31----14	13,12	11----8	7----4	3----0
Processor Signature	**EDX**	(Do Not Use) Intel Reserved	0 0 Processor Type	0 1 0 0 Family	0 0 1 0 Model	XXXX Stepping

(Intel releases information about stepping numbers as needed)

4.7 Boundary Scan (JTAG)

4.7.1 Device Identification

Table 10 shows the 32-bit code for the embedded ULP Intel486 SX processor which is loaded into the Device Identification Register.

Table 10. Boundary Scan Component Identification Code

Version	Part Number				Mfg ID	1
	V_{CC} 0=5V 1=3.3 V	Intel Architecture Type	Family 0100 = Intel486 CPU Family	Model 00010 = embedded ULP Intel486 SX processor	009H = Intel	
31----28	27	26----------21	20----17	16--------12	11----------1	0
XXXX	1	000001	0100	00010	00000001001	1

(Intel releases information about version numbers as needed)
Boundary Scan Component Identification Code = x828 2013 (Hex)

4.7.2 Boundary Scan Register Bits and Bit Order

The boundary scan register contains a cell for each pin as well as cells for control of bidirectional and three-state pins. There are “Reserved” bits which correspond to no-connect (N/C) signals of the embedded ULP Intel486 SX processor. Control registers WRCTL, ABUSCTL, BUSCTL, and MISCCTL are used to select the direction of bidirectional or three-state output signal pins. A “1” in these cells designates that the associated bus or bits are floated if the pins are three-state, or selected as input if they are bidirectional.

- WRCTL controls D31-D0
- ABUSCTL controls A31-A2
- BUSCTL controls ADS#, BLAST#, PLOCK#, LOCK#, W/R#, BE0#, BE1#, BE2#, BE3#, M/IO#, D/C#, PWT, and PCD
- MISCCTL controls HLDA, and BREQ

The following is the bit order of the embedded ULP Intel486 SX processor boundary scan register:

TDO ← A2, A3, A4, A5, RESERVED, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, Reserved, D0, D1, D2, D3, D4, D5, D6, D7, Reserved, D8, D9, D10, D11, D12, D13, D14, D15, Reserved, D16, D17, D18, D19, D20, D21, D22, D23, Reserved, D24, D25, D26, D27, D28, D29, D30, D31, STPCLK#, Reserved, Reserved, SMI#, SMIACT#, SRESET, NMI, INTR, FLUSH#, RESET, A20M#, EADS#, PCD, PWT, D/C#, M/IO#, BE3#, BE2#, BE1#, BE0#, BREQ, W/R#, HLDA, CLK, Reserved, AHOLD, HOLD, KEN#, RDY#, BS8#, BS16#, BOFF#, BRDY#, Reserved, LOCK#, PLOCK#, BLAST#, ADS#, MISCCTL, BUSCTL, ABUSCTL, WRCTL ← **TDI**

5.0 ELECTRICAL SPECIFICATIONS

5.1 Maximum Ratings

Table 11 is a stress rating only. Extended exposure to the Maximum Ratings may affect device reliability.

Furthermore, although the embedded ULP Intel486 SX processor contains protective circuitry to resist damage from electrostatic discharge, always take precautions to avoid high static voltages or electric fields.

Functional operating conditions are given in **Section 5.2, DC Specifications** and **Section 5.3, AC Specifications**.

Table 11. Absolute Maximum Ratings

Case Temperature under Bias	-65 °C to +110 °C
Storage Temperature	-65 °C to +150 °C
DC Voltage on Any Pin with Respect to Ground	-0.5 V to V_{CCP} + 0.5 V
Supply Voltage V_{CC} with Respect to V_{SS}	-0.5 V to +4.6 V
Supply Voltage V_{CCP} with Respect to V_{SS}	-0.5 V to +4.6 V

5.2 DC Specifications

The following tables show the operating supply voltages, DC I/O specifications, and component power consumption for the embedded ULP Intel486 SX processor.

Table 12. Operating Supply Voltages

Product	V_{CCP} Range[1]	Max. CLK Frequency	V_{CC} Range[2]	V_{CC} Fluctuation	
FA80486SXSF-33	3.3 V ± 0.3 V	25	2.4 V min 3.3 V max	±0.2 V	at 2.4 V ≤ V_{CC} ≤ 2.7 V
		33	2.7 V min 3.3 V max	+0.3 V/-0.2 V ±0.3 V	at 2.7 V < V_{CC} < 3.0 V at 3.0 V ≤ V_{CC} ≤ 3.3 V

NOTES:

1. In all cases, V_{CCP} must be ≥ V_{CC}.
2. V_{CC} may be set to any voltage within the V_{CC} Range. The setting determines the allowed V_{CC} Fluctuation.

Table 13. DC Specifications

T_{CASE}=0 °C to +85 °C

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{IL}	Input LOW Voltage	-0.3	+0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CCP} +0.3	V	Note 1
V_{IHC}	Input HIGH Voltage of CLK	V_{CCP} -0.6	V_{CCP} +0.3	V	
V_{OL}	Output LOW Voltage I_{OL} = 2.0 mA I_{OL} = 100 µA		 0.4 0.2	 V V	
V_{OH}	Output HIGH Voltage I_{OH} = -2.0 mA I_{OH} = -100 µA	 2.4 V_{CCP} -0.2		 V V	
I_{LI}	Input Leakage Current		±15	µA	Note 2
I_{IH}	Input Leakage Current		200	µA	Note 3
I_{IL}	Input Leakage Current		-400	µA	Note 4
I_{LO}	Output Leakage Current		±15	µA	
C_{IN}	Input Capacitance		10	pF	Note 5
C_{OUT}	I/O or Output Capacitance		10	pF	Note 5
C_{CLK}	CLK Capacitance		6	pF	Note 5

NOTES:

1. All inputs except CLK.
2. This parameter is for inputs without pull-up or pull-down resistors and $0V \le V_{IN} \le V_{CCP}$.
3. This parameter is for inputs with pull-down resistors and V_{IH} = 2.4V, and for level-keeper pins at V=0.4V.
4. This parameter is for inputs with pull-up resistors and V_{IL} = 0.4V, and for level-keeper pins at V=2.4V.
5. F_C=1 MHz. Not 100% tested.

Table 14. Active I_{CC} Values

T_{CASE}=0 °C to +85 °C

Symbol	Parameter	Frequency	Supply Voltage	Typical I_{CC}	Max. I_{CC}	Notes
I_{CC1}	I_{CC} Active (V_{CC} pins)	25 MHz	V_{CC} = 2.4 ± 0.2 V	120 mA	195 mA	
			V_{CC} = 3.3 ± 0.3 V	165 mA	260 mA	
		33 MHz	V_{CC} = 2.7 ± 0.2 V	180 mA	280 mA	
			V_{CC} = 3.3 ± 0.3 V	220 mA	345 mA	
I_{CC2}	I_{CC} Active (V_{CCP} pins)	25 MHz	V_{CCP} = 3.3 ± 0.3 V	7 mA	25 mA	1
		33 MHz	V_{CCP} = 3.3 ± 0.3 V	9 mA	32 mA	1

NOTE:

1. These parameters are for C_L = 50 pF

Table 15. Clock Stop, Stop Grant, and Auto HALT Power Down I_{CC} Values

T_{CASE}= 0 °C to +85 °C

Symbol	Parameter	Frequency	Supply Voltage	Typical I_{CC}	Max. I_{CC}	Notes
I_{CCS0}	I_{CC} Stop Clock (V_{CC} pins)	0 MHz	V_{CC} = 2.4 ± 0.2 V	4 µA	120 µA	Note 1
			V_{CC} = 2.7 ± 0.2 V	4 µA	130 µA	
			V_{CC} = 3.3 ± 0.3 V	5 µA	150 µA	
I_{CCS2}	I_{CC} Stop Clock (V_{CCP} pins)	0 MHz	V_{CCP} = 3.3 ± 0.3 V	3 µA	80 µA	
I_{CCS1}	I_{CC} Stop Grant, Auto HALT Power Down (V_{CC} pins)	25 MHz	V_{CC} = 2.4 ± 0.2 V	14 mA	25 mA	
			V_{CC} = 3.3 ± 0.3 V	20 mA	30 mA	
		33 MHz	V_{CC} = 2.7 ± 0.2 V	20 mA	30 mA	
			V_{CC} = 3.3 ± 0.3 V	25 mA	35 mA	
I_{CCS3}	I_{CC} Stop Grant, Auto HALT Power Down (V_{CCP} pins)	25 MHz	V_{CCP} = 3.3 ± 0.3 V	425 µA	1.5 mA	
		33 MHz	V_{CCP} = 3.3 ± 0.3 V	610 µA	2.0 mA	

NOTE:

1. The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. For all input signals, the V_{IH} and V_{IL} levels must be equal to V_{CCP} and 0V, respectively, to meet the I_{CC} Stop Clock specifications.

5.3 AC Specifications

The AC specifications for the embedded ULP Intel486 SX processor are given in this section.

Table 16. AC Characteristics (Sheet 1 of 2)
valid over the operating supply voltages listed in Table 12, Operating Supply Voltages (pg. 22).
T_{CASE}= 0 °C to +85 °C; C_L= 50 pF

Symbol	Parameter	2.4V ≤ V_{CC} < 2.7V		2.7V ≤ V_{CC} ≤ 3.3V		Unit	Notes
		Min	Max	Min	Max		
	Frequency	0	25	0	33	MHz	Note 1
t_1	CLK Period	40		30		ns	Note 1
t_{1a}	CLK Period Stability		250		250	ps/CLK	Note 2
t_2	CLK High Time	14		11		ns	at 2V
t_3	CLK Low Time	14		11		ns	at 0.8V
t_4	CLK Fall Time		4		3	ns	2V to 0.8V Note 3
t_5	CLK Rise Time		4		3	ns	0.8V to 2V Note 3
t_6	A2-A31, PWT, PCD, BE0#-BE3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, SMIACT# Valid Delay	3	19	3	16	ns	
t_7	A2-A31, PWT, PCD, BE0#-BE3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, Float Delay		28		20	ns	Note 3
t_{8a}	BLAST#, PLOCK# Valid Delay	3	24	3	20	ns	
t_9	BLAST#, PLOCK# Float Delay		28		20	ns	Note 3
t_{10}	D0-D31 Write Delay	3	20	3	19	ns	
t_{11}	D0-D31 Float Delay		28		20	ns	Note 3
t_{12}	EADS# Setup Time	8		6		ns	
t_{13}	EADS# Hold Time	3		3		ns	
t_{14}	BS16#, BS8#, KEN# Setup Time	8		6		ns	
t_{15}	BS16#, BS8#, KEN# Hold Time	3		3		ns	
t_{16}	RDY#, BRDY# Setup Time	8		6		ns	
t_{17}	RDY#, BRDY# Hold Time	3		3		ns	
t_{18}	HOLD, AHOLD Setup Time	10		6		ns	
t_{18a}	BOFF# Setup Time	10		9		ns	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		3		ns	

Table 16. AC Characteristics (Sheet 2 of 2)

valid over the operating supply voltages listed in Table 12, Operating Supply Voltages (pg. 22).
T_{CASE}= 0 °C to +85 °C; C_L= 50 pF

Symbol	Parameter	2.4V ≤ V_{CC} < 2.7V		2.7V ≤ V_{CC} ≤ 3.3V		Unit	Notes
		Min	Max	Min	Max		
t_{20}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET Setup Time	10		6		ns	
t_{21}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET Hold Time	3		3		ns	
t_{22}	D0-D31, A4-A31 Read Setup Time	6		6		ns	
t_{23}	D0-D31, A4-A31 Read Hold Time	3		3		ns	

NOTES:

1. 0 Hz operation is tested and guaranteed by the STPCLK# and Stop Grant bus cycle protocol. 0 Hz < CLK < 8 MHz operation is confirmed by design characterization, but not 100% tested in production.
2. Specification t1a is available only when CLK frequency is changed without STPCLK# / STOP GRANT bus cycle protocol.
3. Not 100% tested, guaranteed by design characterization.
4. CLK reference voltage for timing measurement is 1.5 V except t2 through t5. Other signals are measured at 1.5 V.

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Table 17. AC Specifications for the Test Access Port

Symbol	Parameter	2.2 V ≤ Vcc < 3.0 V		Vcc = 3.3 ± 0.3 V		Unit	Figure	Notes
		Min	Max	Min	Max			
t_{24}	TCK Frequency		5		8	MHz	10	
t_{25}	TCK Period	200		125		ns	10	Note 1
t_{26}	TCK High Time	65		40		ns	10	@ 2.0V
t_{27}	TCK Low Time	65		40		ns	10	@0.8V
t_{28}	TCK Rise Time		15		8	ns	10	Note 2
t_{29}	TCK Fall Time		15		8	ns	10	Note 2
t_{30}	TDI, TMS Setup Time	16		8		ns	11	Note 3
t_{31}	TDI, TMS Hold Time	20		10		ns	11	Note 3
t_{32}	TDO Valid Delay	3	46	3	30	ns	11	Note 3
t_{33}	TDO Float Delay		52		36	ns	11	Notes 3, 4
t_{34}	All Outputs (except TDO) Valid Delay	3	80	3	30	ns	11	Note 3
t_{35}	All Outputs (except TDO) Float Delay		88		36	ns	11	Notes 3, 4
t_{36}	All Inputs (except TDI, TMS, TCK) Setup Time	16		8		ns	11	Note 3
t_{37}	All Inputs (except TDI, TMS, TCK) Hold Time	35		15		ns	11	Note 3

NOTES:

1. TCK period ≥ CLK period.
2. Rise/Fall Times are measured between 0.8 V and 2.0 V. Rise/Fall times can be relaxed by 1 ns per 10 ns increase in TCK period.
3. Parameter measured from TCK.
4. Not 100% tested, guaranteed by design characterization.

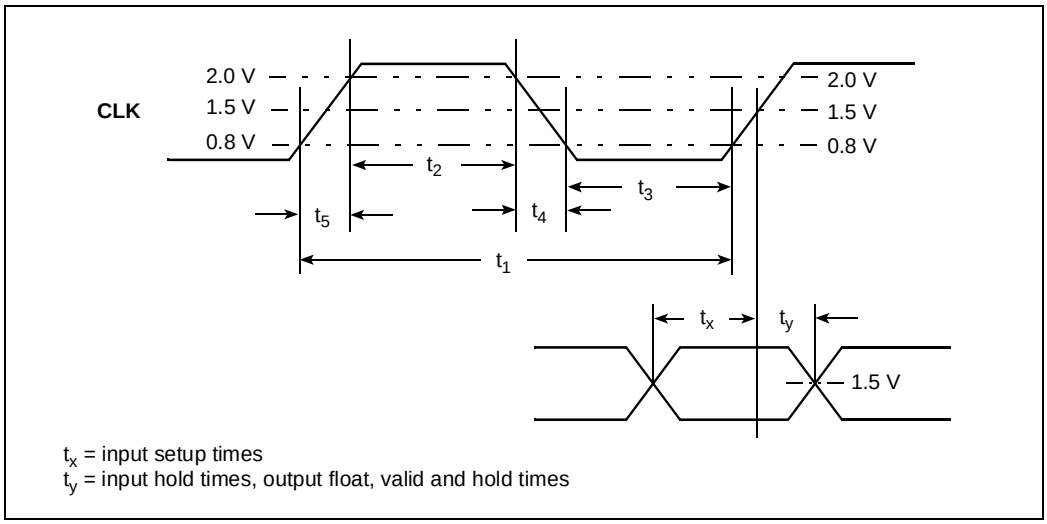


Figure 5. CLK Waveform

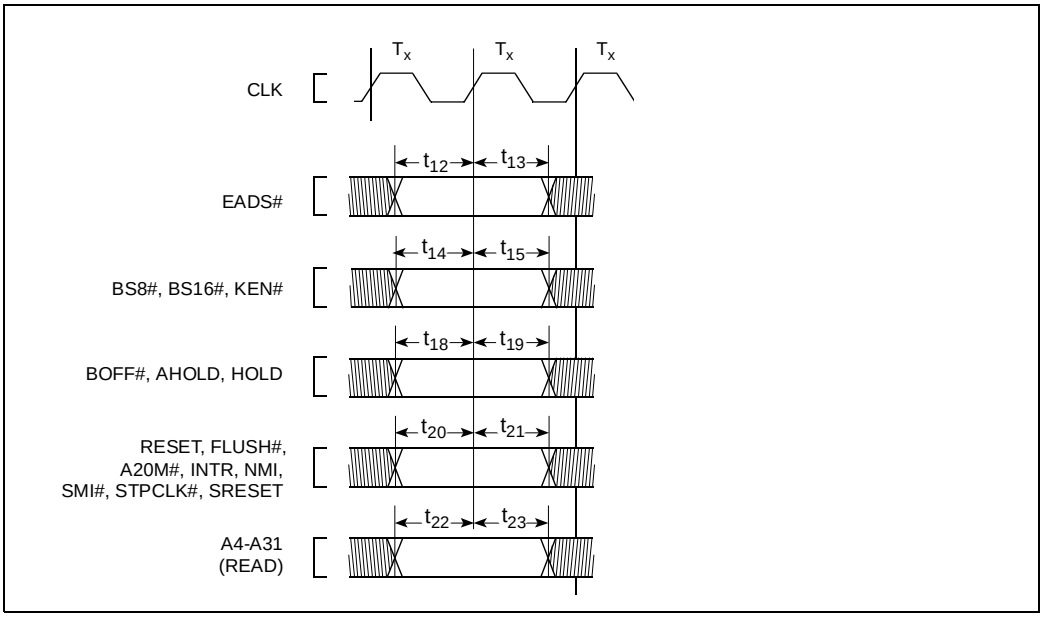


Figure 6. Input Setup and Hold Timing

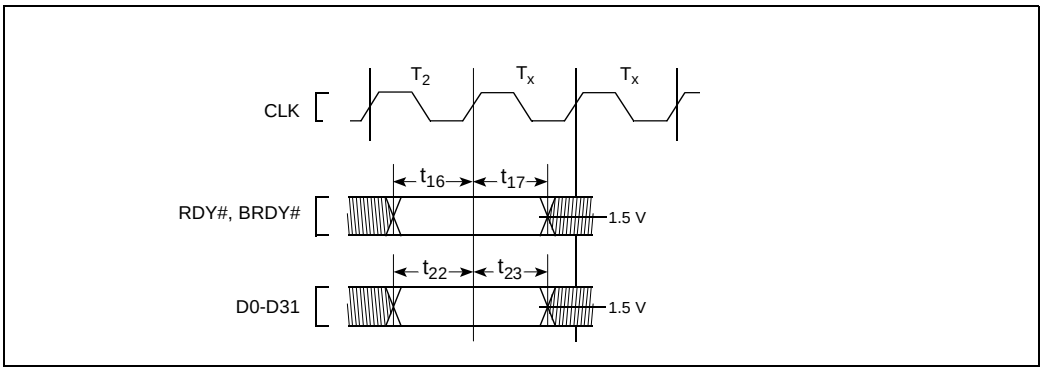


Figure 7. Input Setup and Hold Timing

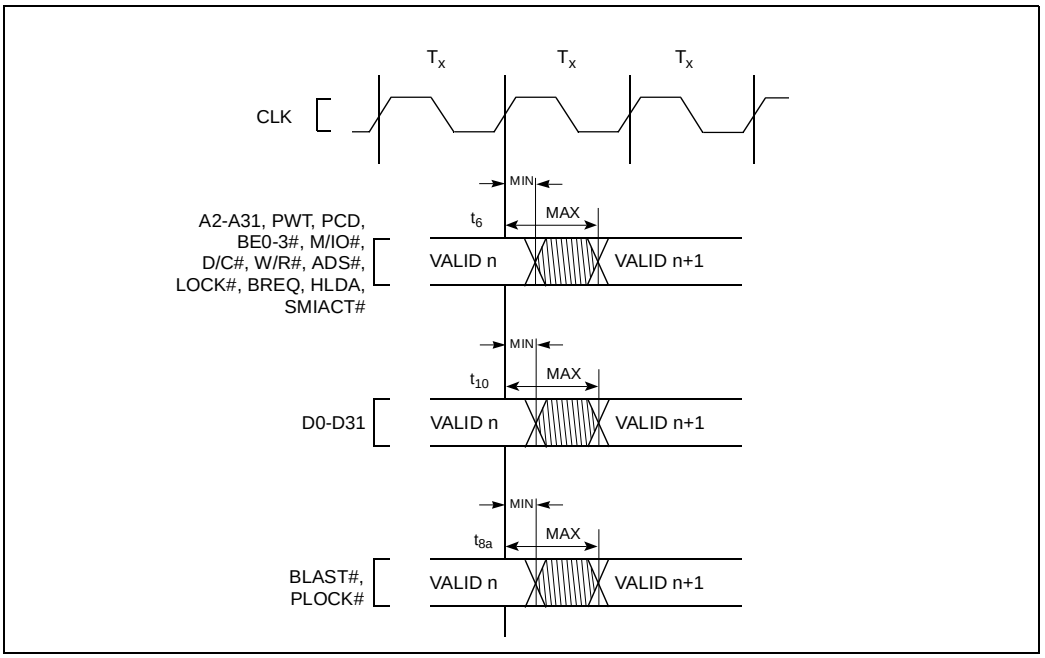


Figure 8. Output Valid Delay Timing

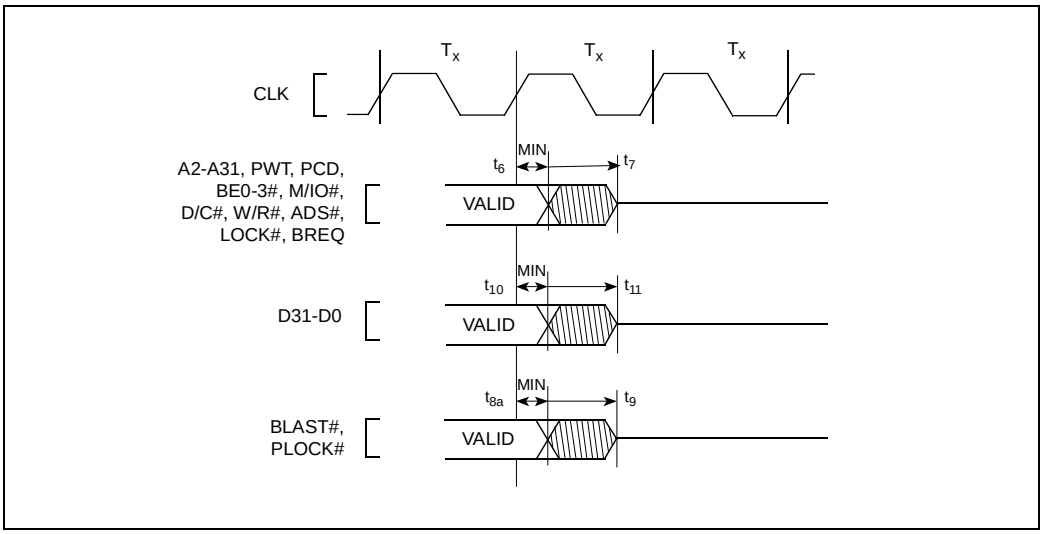


Figure 9. Maximum Float Delay Timing

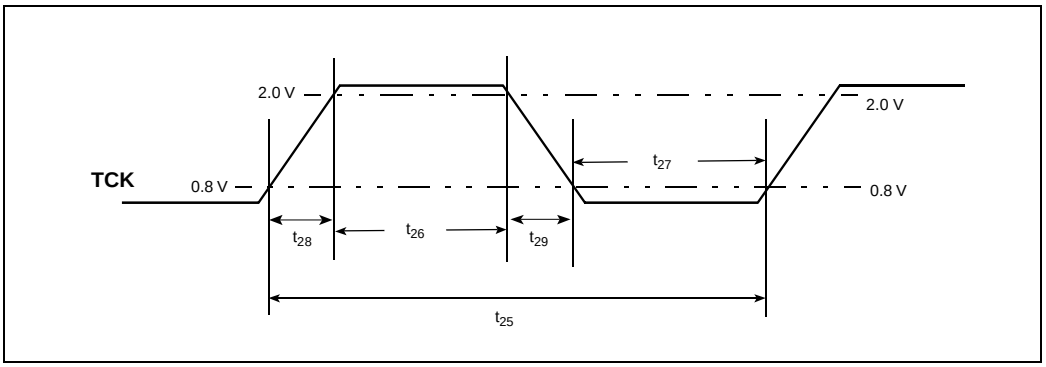


Figure 10. TCK Waveform

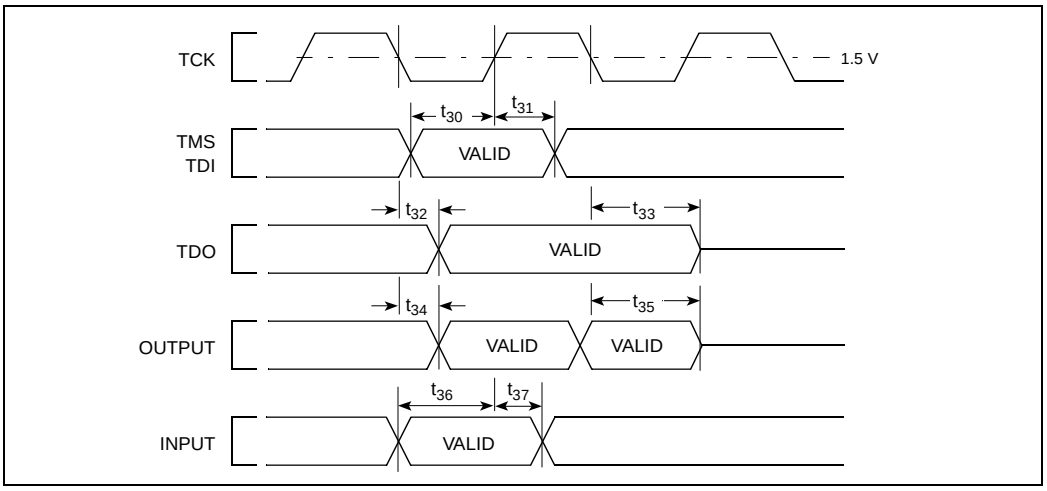
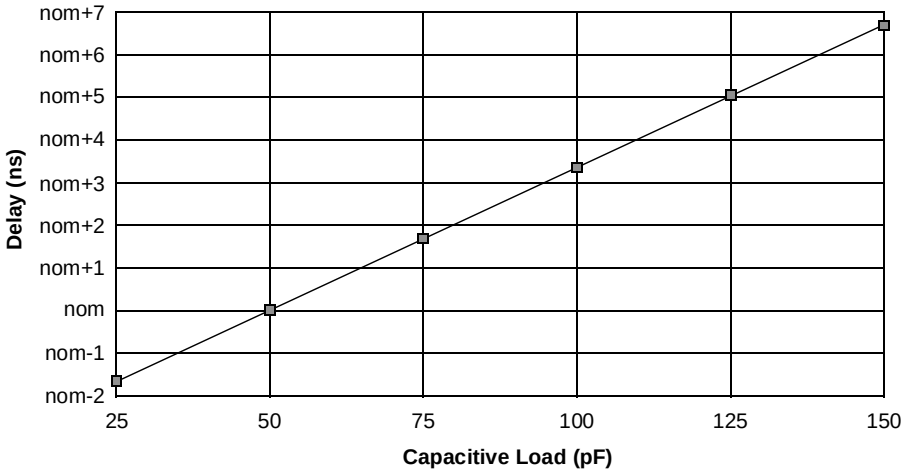


Figure 11. Test Signal Timing Diagram

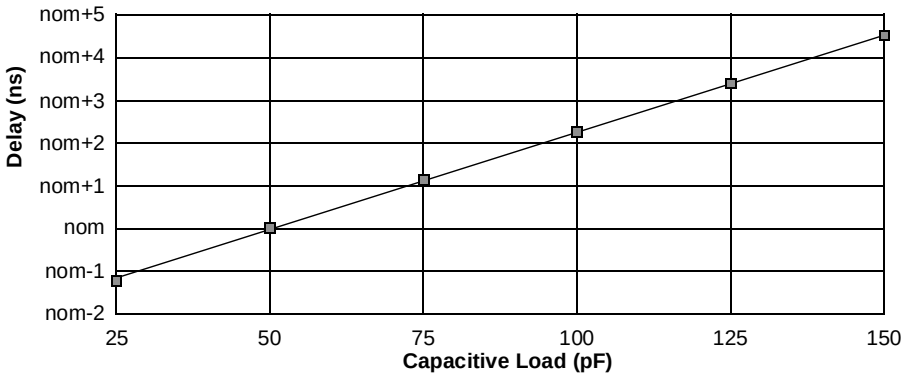
5.4 Capacitive Derating Curves

The following graphs are the capacitive derating curves for the embedded ULP Intel486 SX processor.



NOTE: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 12. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition



NOTE: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 13. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition

6.0 MECHANICAL DATA

This section describes the packaging dimensions and thermal specifications for the embedded ULP Intel486 SX processor.

6.1 Package Dimensions

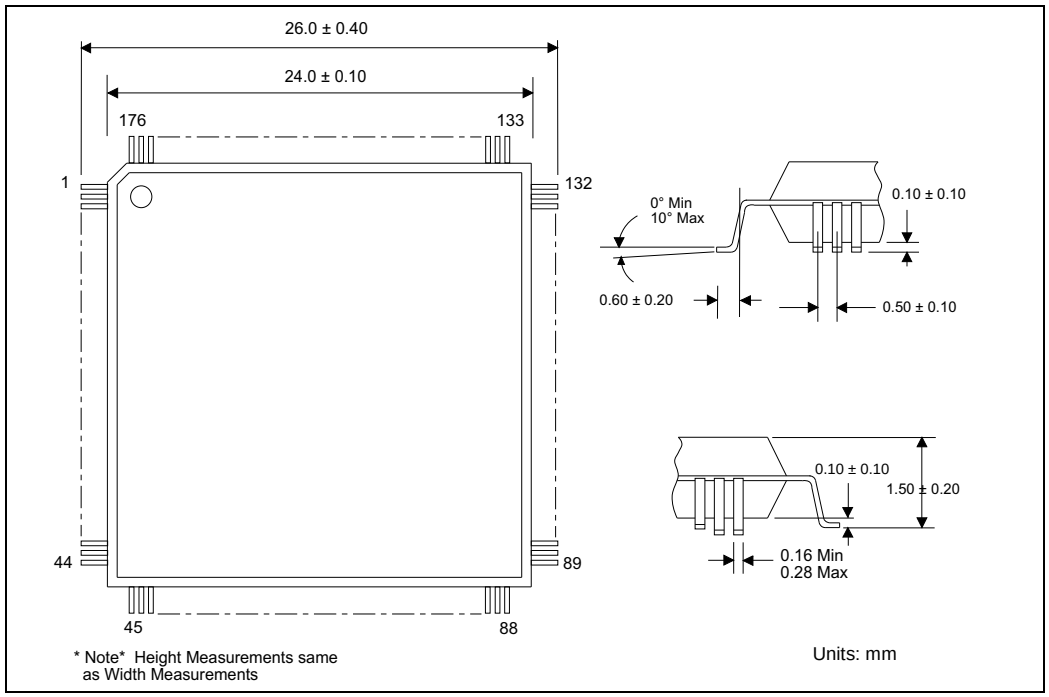


Figure 14. Package Mechanical Specifications for the 176 Lead TQFP Package

6.2 Package Thermal Specifications

The embedded ULP Intel486 SX processor is specified for operation when the case temperature (T_C) is within the range of 0°C to 85°C. T_C may be measured in any environment to determine whether the processor is within the specified operating range.

The ambient temperature (T_A) can be calculated from θ_{JC} and θ_{JA} from the following equations:

$T_J = T_C + P * \theta_{JC}$

$T_A = T_J - P * \theta_{JA}$

$T_C = T_A + P * [\theta_{JA} - \theta_{JC}]$

$T_A = T_C - P * [\theta_{JA} - \theta_{JC}]$

Where T_J, T_A, T_C equals Junction, Ambient and Case Temperature respectively. θ_{JC}, θ_{JA} equals Junction-to-Case and Junction-to-Ambient thermal Resistance, respectively. Maximum Power Consumption (P) is defined as

$P = V (typ) * I_{CC} (max)$

$P = [V_{CC} (typ) * I_{CC1} (max)] + [V_{CCP} (typ) * I_{CC2}(max)]$

where: I_{CC1} is the V_{CC} supply current

I_{CC2} is the V_{CCP} supply current

Values for θ_{JA} and θ_{JC} are given in the following tables for each product at its maximum operating frequencies.

Table 18. Thermal Resistance

(°C/W) θ_{JC} and θ_{JA} for the 176-Lead TQFP Package

θ_{JC} (°C/W)	θ_{JA} (°C/W) with no airflow
4.3	33.6

The following table shows maximum ambient temperatures of the embedded ULP Intel486 SX processor for each product and maximum operating frequencies. These temperatures are calculated using I_{CC1} and I_{CC2} values measured during component-validation testing using V_{CCP}=3.6 V and worst-case V_{CC} values.

Table 19. Maximum Ambient Temperature (T_A)

176-Lead TQFP Package

Frequency	V_{CC}	T_A (°C) with no airflow
25 MHz	2.4 V	76
	3.3 V	65
33 MHz	2.7 V	69
	3.3 V	59