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APPLICATION NOTE

Converting from the 8XC196KB/KC/KD to the 8XC196Nx Family

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CONVERTING FROM THE 8XC196KB/KC/KD TO THE 8XC196Nx FAMILY

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1.0 INTRODUCTION

The MCS® 96 microcontroller product family has three distinct product lines: the HSIO family consists of devices that have the High Speed Input/Output subsystem and is comprised of the 8XC196KB, 8XC196KC and 8XC196KD; the EPA family consists of devices that have the advanced peripherals, including a flexible input/output system and Event Processer Array (EPA). The EPA family includes the 8XC196KR, 8XC196KT, 8XC196NT and 8XC196NP; and the Motion Control family, which is comprised of devices that support motor control applications, and also uses the EPA system for I/O control, includes the 8XC196MC, 8XC196MD, and 8XC196MH.

As designs require higher performance and greater addressing capability, there is a need for converting from the HSIO family to the EPA family. In addition to the highly integrated peripherals, both the 8XC196NP and the 8XC196NT offer a performance and addressing-upgrade path in the MCS 96 microcontroller family. For even greater performance improvement, the 8XC196NP is the first member of the MCS 96 controller family with a dynamically selectable multiplexed/demultiplexed bus and low-power operation (3.3V at 16 MHz). Other key features of the 8XC196NP are the chip select unit, 3 PWM outputs, and increased operating frequency of 25 MHz at 5V.

To ease the difficulty in converting from the HSIO family to the 1 Mbyte addressable members of the EPA family, this application note will discuss the design considerations in making this conversion. The focus will be on converting from the 8XC196KB/KC/KD to the 8XC196NX family, which includes the 8XC196NT and the additional features of the 8XC196NP. The purpose of this paper is to highlight the benefits of the new features of the 8XC196NX family, to inform the user of the conversion issues which need to be considered, and to present code examples of several peripherals to make converting as straightforward as possible. For a more in-depth discussion of the differences between the HSIO and EPA, see AP-449 (literature order #270968): "A Comparison of the Event Processor Array and High Speed Input/Output Unit."

1.1 Related Documents

This document is intended to serve as a comparison between several of the MCS 96 Microcontroller devices. For details on how to use the features and peripherals of these devices, please refer to the following documents:

- *8XC196NP Microcontroller User's Manual,* Order Number 272479
- *8XC196NP Commercial CHMOS 16-Bit Microcontroller* datasheet, Order Number 272459
- *8XC196NT Microcontroller User's Manual,* Order Number 272317
- *8XC196NT CHMOS Microcontroller with 1 Mbyte Linear Address Space* datasheet, Order Number 272267
- AP-475, *Using the 8XC196NT,* Order Number 272315
- AP-449, *A Comparison of the Event Processor Array (EPA) and High Speed Input/Output (HSIO) Unit,* Order Number 270968
- AP-445, *8XC196KR Peripherals: A User's Point of View,* Order Number 270873
- *8XC196KC/8XC196KD User's Manual,* Order Number 272238
- *8XC196KD/8XC196KD20 Commercial CHMOS Microcontroller* datasheet, Order Number 272145
- *8XC196KC/8XC196KC20 Commercial/Express CHMOS Microcontroller* datasheet, Order Number 270942
- *8XC196KB/8XC196KB16 Commercial/Express CHMOS Microcontroller* datasheet, Order Number 270909
- *87C196KB/83C196KB/80C196KB 16-Bit High Performance CHMOS Microcontroller* (datasheet), Order Number 270918
- MCS 96 Microcontroller Family Fact Sheet, Order Number 272223
- ApBUILDER Interactive Programming Software Package, Order Number 272216

Also available is Intel's FaxBACK service [(800) 628-2283] which sends documents to your fax machine. Order catalog #2 for a listing of MCS 96 microcontroller documents.

2.0 ARCHITECTURAL OVERVIEW OF THE HSIO AND EPA FAMILY

The 8XC196KB is the first member of the CHMOS* MCS 96 controller family. It is available in CPU only, 8 Kbyte ROM, and 8 Kbyte OTPROM versions. All versions feature 232 bytes of register RAM. The 8XC196KB uses the High-Speed Input/Output (HSIO) structure for event control. The HSIO has up to 4 input and 6 output lines, and uses either of two 16-bit timer/counters as a time base. Additional features include a hardware-generated Pulse Width Modulator (PWM), a full-duplex Serial I/O (SIO) port, a watchdog timer and an 8-channel 10-bit resolution Analog to Digital (A/D) converter. The 8XC196KB has 48 Input/Output (I/O) lines that are shared with the peripherals.

The 8XC196KC is the next step up in the CHMOS 196 family. It is available in CPU only, 16 Kbyte ROM and 16 Kbyte OTPROM versions. All versions feature 488 bytes of Register RAM. The 8XC196KC is offered in a 20 MHz version, allowing an immediate 25% increase in performance. The 8XC196KC has all the same peripherals as the 8XC196KB, but adds the following features: There are now a total of three hardware PWM generators, the A/D converter has both 8- and 10-bit conversion modes with programmable sample and conversion times, and a Peripheral Transaction Server (PTS) has been added. The PTS acts as a microcoded interrupt handler, which greatly reduces CPU overhead during interrupt servicing.

The 8XC196KD has all the features of the 8XC196KC, but has extended the on-chip memory. The 8XC196KD is available in 32 Kbyte ROM and 32 Kbyte OTPROM versions. Both versions feature 1000 bytes of Register RAM. With the availability of 32K of memory, program development in high-level languages becomes much more practical. The 8XC196KD is also offered in a 20 MHz version.

The 8XC196KR is a highly integrated, advanced member of the MCS 96 controller family. The 8XC196KR has an optional 16 Kbyte OTPROM and has 488 bytes of Register Ram and 256 bytes of Internal RAM. The Internal RAM can be used for program execution or data storage. The 8XC196KR uses a modular Event Processor Array (EPA) for event monitoring and control. The EPA has 250 ns resolution at 16 MHz, and has 10 capture/compare modules plus two compare only modules. The EPA is extremely flexible, and has pulse width modulation (PWM) generation capability. The 8XC196KR includes the Peripheral Transaction Server (PTS), with modes to support PWM generation with the EPA. The 8XC196KR has a slave port which is used to interface to another system's bus. The slave-port feature can be used to make the 8XC196KR a versatile, programmable peripheral attached to any PC's bus. There are two serial ports on the 8XC196KR; one is the standard SIO module found on the 8XC196KB, and the other is a Synchronous Serial I/O (SSIO) port. The SSIO is capable of full-duplex synchronous communication. Both serial ports have their own programmable baud rate generators. The 8XC196KR A/D converter is based on the 8XC196KC design but offers additional modes which allow programmable threshold detection and offset correction.

The 8XC196KT is an enhanced version of the 8XC196KR with an optional 32 Kbyte OTPROM and has 1000 bytes of Register RAM and 512 bytes of Internal RAM. The 8XC196KT's bus controller has new modes which allow no wait-state operation with slower external memory.

The 8XC196NT has the same features as the 8XC196KT but has 1 Mbyte external addressability, which allows the design to handle large software code. Four of the A/D inputs were replaced with the Extended Address Port (EPORT). The four EPORT pins can be used as additional address lines (A16–A19) or standard low speed I/Os, or a combination of both. The 8XC196NT has increased speed, starting at 20 MHz operation.

The 8XC196NP is the first member of the MCS 96 controller family with a chip-select unit and low voltage-over-power operation (3.3V at 16 MHz). The six programmable chip selects can reduce or eliminate the need for external decode logic. The 3.3V version of the 8XC196NP will be ideal for portable, battery-powered applications. This currently is the only low voltage, 3V part in the MCS 96 controller family. Another new feature of the 8XC196NP is the dynamically selectable multiplexed/demultiplexed bus. The dynamic dual mode bus allows the interface of inexpensive memory devices resulting in lower overall system cost, while at the same time increasing performance. It allows cost-effective, zero wait-state designs at 25 MHz. The dynamic mux/demux bus structure also makes the 8XC196NP compatible with existing MCS 96 microcontroller family designs. The new system bus also compensates for the lack of an OTPROM version of the 8XC196NP by allowing access to low cost external memory. The 8XC196NP also has 1 Mbyte addressing, 3 PWM outputs, and 25 MHz operation at 5V. To

compensate for the additional features, some peripherals were reduced or removed. The 8XC196NP has 4 EPA channels compared to the 10 EPA channels and 2 compare-only channels on the 8XC196NT. The analog to digital convertor, the watch dog timer, the SSIO, and the slave port were removed. Regarding internal memory, the 8XC196NP has 1000 bytes register RAM and optional 4K of ROM.

3.0 ADDITIONAL FEATURES OF THE 8XC196Nx FAMILY

3.1 Additional Registers and Pins to Support 1 Mbyte Addressability

(See Memory Partitions Chapter for the Memory Address Space.) To support 1 Mbyte addressability, new CCBs were added. [See also Memory Partitions (Chip Configuration Register) section 4.2.] The 8XC196NT has 3 CCBs (CCB0-3). An additional bit (LDCCB2) was added to CCR1 that enables the loading of CCR2. The LDCCB2 bit must be set to load the CCB2 register which determines the addressing mode and mapping of internal OTPROM. Additional bits (MSEL0-1) were added to CCR1 to select different bus-timing modes. Both the 8XC196NT and the 8XC196NP have added a CCR (CCR2 and CCR1 respectively) to select either 16-bit or 24-bit addressing mode. This register also controls whether the internal OTPROM is mapped into both page 0FFH and page 00H or into page 0FFH only. The 8XC196NP has added bits in CCR0 for Wait States and Demuxed/Muxed Mode.

The 8XC196NT has selectable bus-timing modes, controlled by the MSEL0 and MSEL1 bits (bit 6 and 7) of CCR1. Mode 3 is the standard timing mode. This mode should be used for systems that need to emulate the 8XC196KR. Mode 0 is the standard timing mode with a minimum of one wait state added to each bus cycle. Mode 1 is the long read/write mode. This allows the memory more time to get its data on the bus without the wait-state penalty of Mode 0. Mode 2 is similar to Mode 1 in that RD#, WR#, and ALE begin ½ TOSC earlier in the bus cycle and the widths of RD# and WR# are 1 TOSC longer than in Mode 3. It differs from Mode 1 in that the address is also placed onto the bus ½ TOSC earlier in the bus cycle. This mode trades a longer TRHDX for a shorter TAVDV.

Table 3-1. Bus Timing Mode Control

MSEL1 (CCR1.7)	MSEL0 (CCR1.6)	Bus Timing Mode
0	0	Mode 0, 8XC196KR compatible timing with one automatic wait state
0	1	Mode 1, Long Read/Write Mode
1	0	Mode 2, Long Read/Write with early address
1	1	Mode 3, 8XC196KR compatible mode

The 8XC196NT and 8XC196NP both control the addressing modes (16 vs. 24-bit) in the same manner. (Only 20 address lines are bonded out so, externally, 24-bit addressing will appear to be 20-bit addressing.) For 24-bit addressing, the MODE16 bit (bit 1 in CCR2/CCR1 for the 8XC196NT/NP) must be cleared. In both 16-bit and 24-bit modes, the 8-bit extended slave program counter (ESPC) is concatenated with the 16-bit master program counter to form a 24-bit PC. In 16-bit mode, the ESPC is forced to 0FFH. Therefore, using non-extended instructions can only access page FFH (64 Kbytes). Extended load, store, and block-move instructions can access data in any page, but extended jump, branch, and call instructions will not function in 16-bit mode. In 24-bit mode, the ESPC can have any value and can therefore access up to 1 Mbyte. By using extended instructions the ESPC is changed to the value of the destination page.

The remapping function is an additional feature that is done the same for the 8XC196NT and 8XC196NP. The REMAP bit (bit 2 in CCR2/CCR1 for the 8XC196NT/NP) controls the memory mapping of internal OTPROM. Set the bit to map the internal OTPROM into both pages 00H and FFH. This allows data tables that are stored in OTPROM to be accessed in page 00H. Clear the bit to map internal OTPROM into page FFH only. This will leave page 00H free for other uses. The REMAP bit is only effective when EA# is high. When EA# is low, execution is external and the REMAP bit is ignored, leaving page 00H free.

Wait-state control is different for the 8XC196NT than it is for the 8XC196NP. For the 8XC196NT, the Internal Ready Control bits (IRC0-IRC2) define the maximum number of wait states that will be inserted; see Table 3-2. When all three bits are set, the bus controller inserts wait states until the external memory device asserts the READY signal high. Otherwise, the bus con-

troller inserts wait states until either the external memory device asserts the READY signal, or the number of wait states equals the number (0, 1, 2, or 3) specified by the bit settings. These wait-state settings apply to all external devices.

Table 3-2. Wait-State Control for the 8XC196NT

IRC2 (CCB1.1)	IRC1 (CCB0.5)	IRC0 (CCB0.4)	Maximum Wait States
0	0	0	Limit to 0
1	0	0	Limit to 1
1	0	1	Limit to 2
1	1	0	Limit to 3
1	1	1	Infinite (controlled by READY signal)

For the 8XC196NP, the Wait-State control bits (WS0-1) define the number of wait states that will be generated internally. (See Table 3-3.) The READY input can then be used by the external device to insert additional wait states. The wait-state settings programmed by the CCB are the default settings until the BUSCON registers are programmed. (See "Chip Select Unit of the 8XC196NP", section 3.2.)

Table 3-3. Wait-State Control for the 8XC196NP

WS1 (BUSCONx.1)	WS0 (BUSCONx.0)	Wait States
0	0	0 inserted
0	1	1 inserted
1	0	2 inserted
1	1	3 inserted

To support 1 Mbyte addressability, the EPORT was added. See Figure 3-1. The EPORT is a four-bit, bi-directional, memory-mapped I/O port that acts as address lines 16–19. If these pins are not needed for address lines, they can also be configured for I/O. The EP__MODE register controls whether the port pin is an address line or an I/O port. If the port is in address mode (EP__MODE set) then the ADDRESS MUX determines the address source. For an instruction fetch, the ADDRESS MUX is set to the CODE input and the Extended Slave Program Counter (ESPC) is selected as the address source. For a data fetch, or while there is no bus activity, the ADDRESS MUX is set to the DATA input, and the Extended Data Address Register (EDAR) is selected as the address source. The EDAR is loaded from two different sources, depending on whether the data access is extended or non-extended. For extended data accesses, the DATA MUX is set to the 24-bit input and EDAR is loaded with the extended address. For non-extended data accesses, the DATA MUX is set to the 16-bit input and EDAR is loaded from EP__REG. The last value loaded remains in EDAR until the next data access.

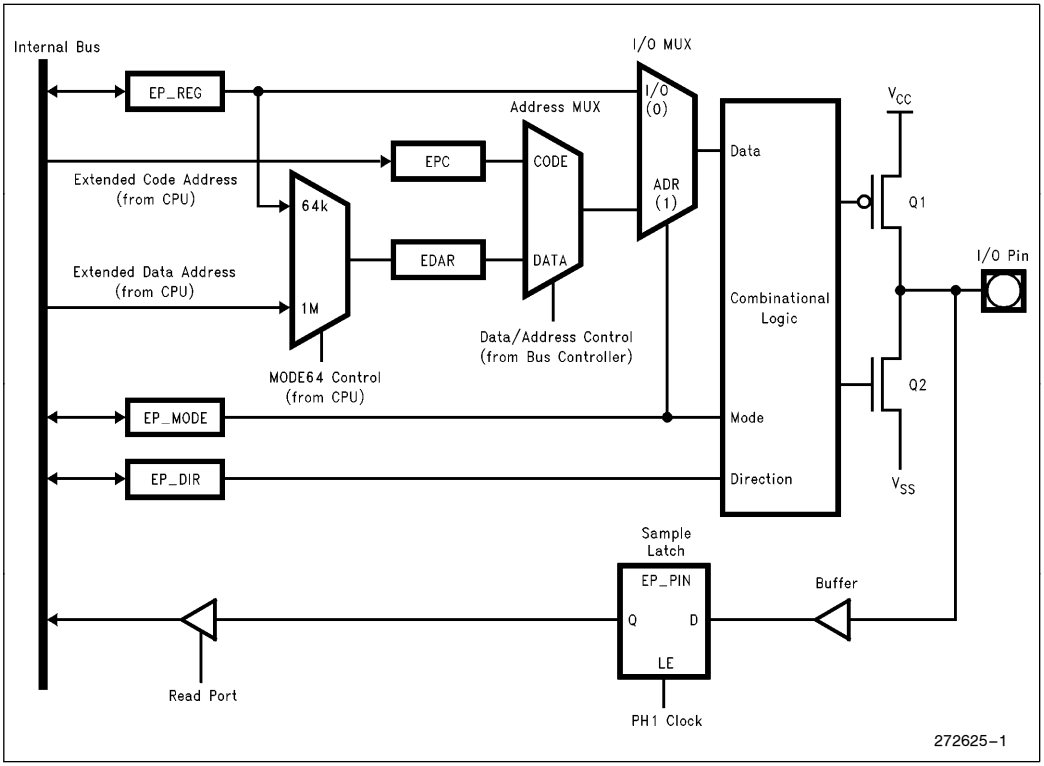

Figure 3-1. EPORT Block Diagram

Keep the following points in mind:

During extended accesses, the EPORT pins are determined by the upper four bits of the address, assuming that the pins are configured for their special function as an extended address port pin. Regardless of the value in EP__REG or the current operating page, any non-extended instruction that accesses address locations 0000H–03FFH will be directed to the Register File and any non-extended instruction that accesses address locations 1F00H–1FDFH will be directed to the Special Function Registers. Non-extended accesses outside of these ranges will be directed to the page defined by the value currently in EP__REG. This effectively maps the Register File and the windowable SFRs into every page. Extended instructions can access the "mapped over" areas of each page. For example, if location 010045H is addressed with an extended instruction, i.e., eld, est, 010045H will actually be accessed.

Example:

```
ldb temp,   #03h
estb  temp, EP_REG
ldb  temp, #0aah
stb  temp, lfd4h     ; AA written to Pl_REG
stb  temp, 300h      ; AA written to upper reg file
stb  temp, 60h       ; AA written to lower reg file
stb  temp, 3000h     ; AA written to page 03 @ 3000h
stb  temp, lfe5h     ; AA written to page 03 @ lfe5h
```

3.2 Chip Select Unit of 8XC196NP

In previous versions of the MCS 96 controller family, chip selects for external devices needed to be decoded through external logic. The bus width was previously determined by BW bits in the CCBs, or it could be controlled dynamically with the BUSWIDTH pin. The 8XC196NP has a chip-select unit that provides six outputs—CS5:0#, for selecting external devices. The chip selects are programmed to be asserted when the external address falls within the range of that chip select. For each separate chip select, the bus width, the number of wait states, the address range, and multiplexed or demultiplexed address/data lines are programmed independently. These parameters are selected with the BUSCONx register. If the address range falls outside the range for each chip select, then BUSCON5 determines the bus width, the wait states, and multiplexing. The register ADDRCOMx holds the upper 12 bits of the base address of the address range assigned to CSx#. The register ADDRMSKx determines the size of the address range. The first lines of your code should be to set up the stack pointer and to then initialize all of the chip select registers.

3.3 Demultiplexed/Multiplexed Bus of the 8XC196NP

The demultiplexed bus mode allows the interface of slower, less inexpensive memory devices. In multiplexed mode, the address is only on the bus for half of the cycle, so external devices have less time to receive it. In demultiplexed mode, the address and data are both on the bus for the full cycle; consequently, latches are not necessary, and slower external devices can be used. The DEMUX bit (BUSCONx.7) controls the address/data multiplexing on the external bus. Set the DEMUX bit for data only on AD0-15 (demultiplexed mode) and clear it for address and data on AD0–15 (multiplexed mode). See the Users Manual for timing comparisons between demuxed/muxed modes.

3.4 Lower Voltage (3.3V) Operation of the 8XC196NP

The 8XC196NP is the first 3.3V MCS 96 controller device. At 5V, the device can run up to 25 MHz and at 3.3V the device can run up to 16 MHz. Although the device functions across 2.97V to 5.5V, it is specified across two ranges, 2.97V–4.5V and 4.5V–5.5V. See the data sheet for exact specifications.

4.0 MEMORY PARTITIONS

This section describes the addressable memory space of the HSIO (8XC196KB/KC/KD) devices and the 8XC196Nx devices. The HSIO family has 64 Kbytes of addressable memory space. The 8XC196Nx devices feature a non-segmented, 24-bit address space, of which only the lower 20 bits are available to the user, providing 1 Mbyte addressability. The lower 16 address/data lines (AD0–AD15) of the 8XC196Nx are the same as those of the HSIO family devices. On the 8XC196Nx, the four extended address lines (A16-A19) are made available on a special port, the EPORT.

Since the 8XC196Nx has 24 address bits internally, code must be written as though all 24 bits are being used. Since the device resets from page FFH, code must be written in this page. For example, when generating assembly code, use "CSEG at 0FF2080H" for user code and "CSEG at 0FF2000H" for the interrupt vectors. If using external memory, the device will still reset to page FFH, and this will be overlayed to page 0FH since only 20 lines are bonded out. For future compatibility, also take into consideration that future devices may have all 24 address lines bonded out.

The top-level memory maps shown following in Tables 4-1 and 4-2 show the differences in the memory space of the HSIO devices and the 8XC196Nx devices. In addition to the shown pages 00H and FFH on the 1 Mbyte addressable devices pages 10H to EFH are overlayed memory and pages 01H to 0FH are for external memory, which can be considered as 14 pages of 64 Kbytes each for 896 Kbytes total.

Table 4-1. Top-Level Memory Map for 8XC196KB/KC/KD

	8XC196KB	8XC196KC	8XC196KD
External Memory or I/O	0FFFFH 4000H	0FFFFH 6000H	0FFFFH 0A000H
Program Memory	3FFFH 2080H	5FFFH 2080H	9FFFH 2080H
Special Purpose Memory	207FH 2000H	207FH 2000H	207FH 2000H
Port 4	1FFFH	1FFFH	1FFFH
Port 3	1FFEH	1FFEH	1FFEH
External Memory	1FFDH 100H	1FFDH 200H	1FFDH 400H
Register File	0FFH 0H	1FFH 0H	3FFH 0H

Table 4-2. Top Level Memory Map for 8XC196Nx

	8XC196NT Page 0FFH	8XC196NP Page 0FFH		8XC196NT Page 00H	8XC196NP Page 00H
External Memory or I/O	0FF FFFFH 0FF A000H	0FF FFFFH 0FF 3000H	External Memory or I/O	00 FFFFH 00 A000H	00 FFFFH 00 3000H
Program Memory	0FF 9FFFH 0FF 2080H	0FF 2FFFH 0FF 2080H	External Memory or Remapped Page 0FFH	00 9FFFH 00 2080H	00 2FFFH 00 2080H
Special Purpose Memory	0FF 207FH 0FF 2000H	0FF 207FH 0FF 2000H	External Memory or Remapped Page 0FFH	00 207FH 00 2000H	00 207FH 00 2000H
External Memory	0FF 1FFFH	0FF 1FFFH	Memory-Mapped Peripheral SFRs	00 1FFFH 00 1FE0H	00 1FFFH 00 1FE0H
			Peripheral SFRs	00 1FDFH 00 1F00H	00 1FDFH 00 1F00H
External Memory	0FF 0600H		External Memory	00 1EFFH 00 0600H	00 1EFFH 00 0400H
Internal RAM (NT)	0FF 05FFH 0FF 0400H		Internal RAM (NT)	00 05FFH 00 0400H	
External Memory	0FF 03FFH 0FF 0100H	0FF 0100H	Upper Register File	00 03FFH 00 0100H	00 03FFH 00 0100H
Reserved for ICE	0FF 00FFH 0FF 0000H	0FF 00FFH 0FF 0000H	Lower Register File	00 00FFH 00 0000H	00 00FFH 00 0000H

There are a few key points to keep in mind when using the 1 Mbyte addressability of the 8XC196Nx devices.

1. Program and Special-Purpose memory can be located in either internal OTPROM/ROM (87C196NT/83C196NP) or external memory, depending on the state of EA#. Just as in earlier MCS 96 controller devices, if EA# is held low, accesses to memory locations 0FF2000H–0FF9FFFH for the 87C196NT or 0FF2000H–0FF2FFFH for the 83C196NP are directed to external memory and internal OTPROM/ROM is unavailable. Although internally there are 24 address lines, keep in mind that only 20 address lines are actually bonded out. Therefore, when addressing locations in 0FF2000H–0FF9FFFH/0FF2FFFH, the external device will actually be addressed as locations 0F2000H–0F9FFFH/0F2FFFH. For example, when code is written at 0FF2080H and EA# is low, the address on the 8XC196Nx address lines will be 0F2080H.
2. Internal RAM (on the 8XC196NT only) is mapped into both pages 00H and FFH. This is the same physical RAM and can be accessed through either page. Internal RAM is not windowable and therefore it must be used with indirect or indexed addressing. This memory may also be used as dynamic program memory.
3. The internal OTPROM of the 87C196NT and the internal ROM of the 83C196NP are located in page FFH and can optionally be mapped into page 00H as well. Remapping this internal memory is done by setting the REMAP bit, which for the 87C196NT is bit 2 of the CCR2 register (added to support extended addressing) and for the 83C196NP is bit 2 of the CCR1. This offers compatability with previous MCS 96 devices.
4. Memory-mapped Peripheral SFRs (1FE0H–1FFFH) must be accessed using indirect or indexed addressing modes and cannot be windowed. Non-extended instructions can access memory-mapped SFRs only when EP__REG is equal to 00H. Extended instructions can access these locations from any page as long as an indirect or indexed instruction is used.

Example 4.1

Here the Port 4 register will be configured as output ports using non-extended and extended instructions.

Non-extended instructions used:

```
ldb  tmpreg0, #00h
stb  tmpreg0, EP_REG[0]  .
ldb  tmpreg0, #0fh
stb  tmpreg0, lfd8h[0]   ;#0Fh will be stored at location lFD8h which is
                         ;the P4_M0DE register on the 8XCl96NP only if
                         ;EP_REG contains 00H.
```

Extended instructions used:

```
ldb  tmpreg0, #0lh
estb tmpreg0, EP_REG[0]
ldb  tmpreg0, #0fh
estb tmpreg0, lfd8h      ;#0Fh will be stored at location lFD8h which is
                         ;the P4_M0DE register regardless of the value
                         ;stored in EP_REG.
```

5. The non-memory-mapped peripheral SFRs (1F00H–1FDFH) are physically located in the on-chip peripherals, can be addressed as bytes or as words (some registers are addressed as bytes, some as words, and some as both), and they can be windowed. The SFRs are mapped into all pages when non-extended instructions are used, so any value for EP__REG is valid. Therefore, if using only non-extended instructions, a "hole" in memory will exist on each page from 1F00H–1FDFH. Note, this also applies to the Register RAM (000000H–0003FFH). Extended load and store instructions can access these locations through page 00H only. When extended instructions are used, references to these locations in any other page are directed to external memory. To access external locations in page 00 that overlap the register RAM and SFRs, use the following, since page 10H overlays page 00 externally: est temp, 10 0050H. (See Example 4.2.)
6. The registers of the 8XC196Nx can be both read from and written to the same address location. Therefore, horizontal windowing is no longer necessary.

Example 4.2: To access non-memory-mapped peripheral SFRs, use non-extended instructions.

Non-extended instructions used:

```
ldb   tmpreg0, #00h        ; EP_REG must be 00H.
stb   tmpreg0, EP_REG[0]
ldb   tmpreg0, #0c0h
stb   tmpreg0, lfbah[0]    ; #0C0H will be written internally to 001FBAH
                           ; which is the SBUF_TX register.
```

To access external locations at 051F00H–051FDFH, use extended instructions. A non-extended store would go to special function registers in page 0.

Extended intructions used:

```
cseg at 053000h            ; Program Counter is in Page 05.
ld    tmpreg0, #01h
est   tmpreg0, 051fd0h     ; This will access external location 051FD0h.
```

To access external locations at 1F00H–1FDFH in Page 00h, use extended instructions to Page 0x0h.

Extended instructions used:

```
cseg at 013000h            ; Program Counter is in Page 01
ldb   tmpreg0, #0c0h
estb tmpreg0, 101fbah      ; 0C0h will be stored externally in Page 0 since
                           ; 10H overlays page 0.
```

4.1 Special-Purpose Memory

There are only a few differences in the Special-Purpose Memory among the different devices (see Table 4-3). Some of the reserved bytes require different values to be written to these locations. For example, make sure that locations 0FF2019H for the 8XC196NT/NP, and locations 0FF201BH, 0FF201DH, and 0FF201FH for the 8XC196NT are written as 20H to prevent possible bus contention during the CCBx fetch. The primary difference is the location and the contents of the Chip Configuration Bytes (CCBs). Section 4.2 discusses the Chip-Configuration Registers for the different devices.

Table 4-3. Special-Purpose Memory Addresses

	8XC196KB	8XC196KC/KD		8XC196NT	8XC196NP
207FH 205EH	Reserved-0FFH	Reserved-0FFH	0FF 207FH 0FF 205EH	Reserved-0FFH	Reserved-0FFH
205DH 2040H	Reserved-0FFH	PTS Vectors	0FF 205DH 0FF 2040H	PTS Vectors	PTS Vectors
203FH 2030H	Upper Interrupt Vectors	Upper Interrupt Vectors	0FF 203FH 0FF 2030H	Upper Interrupt Vectors	Upper Interrupt Vectors
202FH 2020H	Security Key	Security Key	0FF 202FH 0FF 2020H	Security Key	Reserved-0FFH
201FH	Reserved-0FFH	Reserved-0FFH	0FF 201FH	Reserved-20H	Reserved-0FFH
201EH	Reserved-0FFH	Reserved-0FFH	0FF 201EH	Reserved-0FFH	Reserved-0FFH
201DH	Reserved-0FFH	Reserved-0FFH	0FF 201DH	Reserved-20H	Reserved-0FFH
201CH	Reserved-0FFH	Reserved-0FFH	0FF 201CH	CCB2	Reserved-0FFH
201BH	Reserved-0FFH	Reserved-0FFH	0FF 201BH	Reserved-20H	Reserved-0FFH
201AH	Reserved-0FFH	Reserved-0FFH	0FF 201AH	CCB1	CCB1
2019H	Reserved-20H	Reserved-20H	0FF 2019H	Reserved-20H	Reserved-20H
2018H	CCB	CCB	0FF 2018H	CCB0	CCB0
2017H 2014H	Reserved-0FFH	Reserved-0FFH	0FF 2017H 0FF 2014H	Reserved-0FFH	Reserved-0FFH
2013H 2000H	Lower Interrupt Vectors	Lower Interrupt Vectors	0FF 2013H 0FF 2000H	Lower Interrupt Vectors	Lower Interrupt Vectors

4.2 Chip-Configuration Registers (CCR)

The Chip-Configuration Bytes (CCBs) identify the environment in which the device is operating. The 8XC196KB/KC/KD CCR controls internal memory protection, internal READY mode, bus control signals, bus-width options, and Powerdown mode. The 8XC196NT CCRs control bus width, bus-control mode, bus-timing mode, and wait states. They also control OTPROM protection, Powerdown mode, the Watchdog timer, internal OTPROM mapping, and addressing mode. The 8XC196NP CCRs control the bus width, bus mode (multiplexed or demultiplexed), write-control mode, wait states for the CCB1 fetch, power-down enabling, and the 1 Mbyte or 64 Kbyte mode. The rest of this section outlines the bits in each CCR.

8XC196KB/KC/KD CCR
8XC196NT CCR0

Bit 7							Bit 0
LOC1	LOC0	IRC1	IRC0	ALE	WR	BW0	PD

PD Powerdown Enable

BW0 Bus Width Control

WR Select Write-Strobe Mode

ALE Select Address-Valid-Strobe Mode

IRC0–IRC1 Internal Ready Control

LOC0–LOC1 Lock Bits

8XC196NT CCR1

Bit 7							Bit 0
MSEL1	MSEL0	0	1	WDE	BW1	IRC2	LDCCB2

LDCCB2 Load CCB2

IRC2 Ready Control

BW1 Bus Width Control

WDE Watchdog Timer Enable

MSEL0–MSEL1 External Access Timing Mode Select

These bits—MSEL0–MSEL1, control the bus-timing modes that have been added to the 8XC196NT.

MSEL1	MSEL0	
0	0	Standard mode plus one wait state. The TRLDV and TAVDV timings are each 2 TOSC longer in Mode 0 than in Mode 3.
0	1	Long Read/Write. This allows the memory more time to get its data on the bus without the wait-state penalty of Mode 0.
1	0	Long Read/Write with Early Address. This mode is similar to Mode 1 but trades a longer TRHDX for a shorter TAVDV.
1	1	Standard mode. This should be used to emulate an 8XC196KR system.

8XC196NT CCR2
8XC196NP CCR1

Bit 7							Bit 0
1	1	1	1	1	REMAP	MODE16	0

MODE16 Addressing Mode

Selects 16- or 24-bit addressing.

0 = selects 24-bit addressing

1 = selects 16-bit addressing

REMAP OTPROM/internal ROM Mapping

Controls the internal OTPROM mapping.

0 = maps to page FF only

1 = maps to page 00 and FF

8XC196NP CCR0

Bit 7							Bit 0
1	1	WS1	WS0	DEMUX	BHE#	BW16	PDEN

PDEN Powerdown Enable

BW16 Bus Width Control

BHE# Write-control Mode

DEMUX Select Demultiplexed Bus

Selects the demultiplexed bus mode for an external fetch of CCB1:

1 = Demultiplexed: data only on AD15:0.

0 = Multiplexed: address and data are multiplexed on AD15:0.

WS0–WS1 Wait States

These two bits control the number of wait states that are used for an external fetch of CCB1.

WS0	WS1	
0	0	zero wait states
0	1	one wait state
1	0	two wait states
1	1	three wait states

5.0 HARDWARE

The 8XC196KB/KC/KD and 8XC196Nx parts are not socket compatible. The newer 8XC196NT and 8XC196NP have a more flexible EPA and pins were added to support the 1 Mbyte addressability of the 8XC196Nx parts. The addition of the Chip Select Unit and the Demultiplexed bus of the 8XC196NP requires a 100-ld package. This section outlines the differences in the pinouts and compares each of the pins on each device.

5.1 Pinout Diagrams

Refer to current data sheets to get a complete package description.

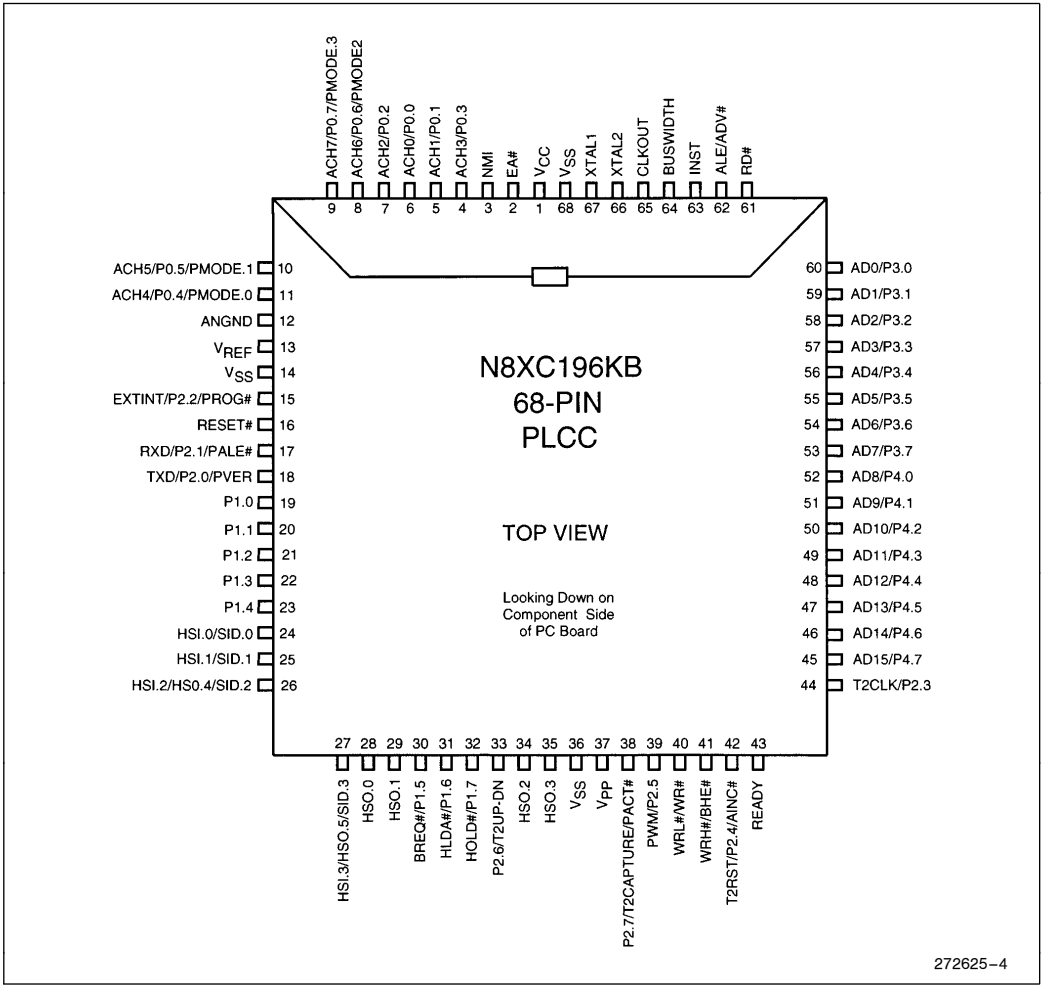

Figure 5-1. N8XC196KB 68-Pin PLCC Package Diagram

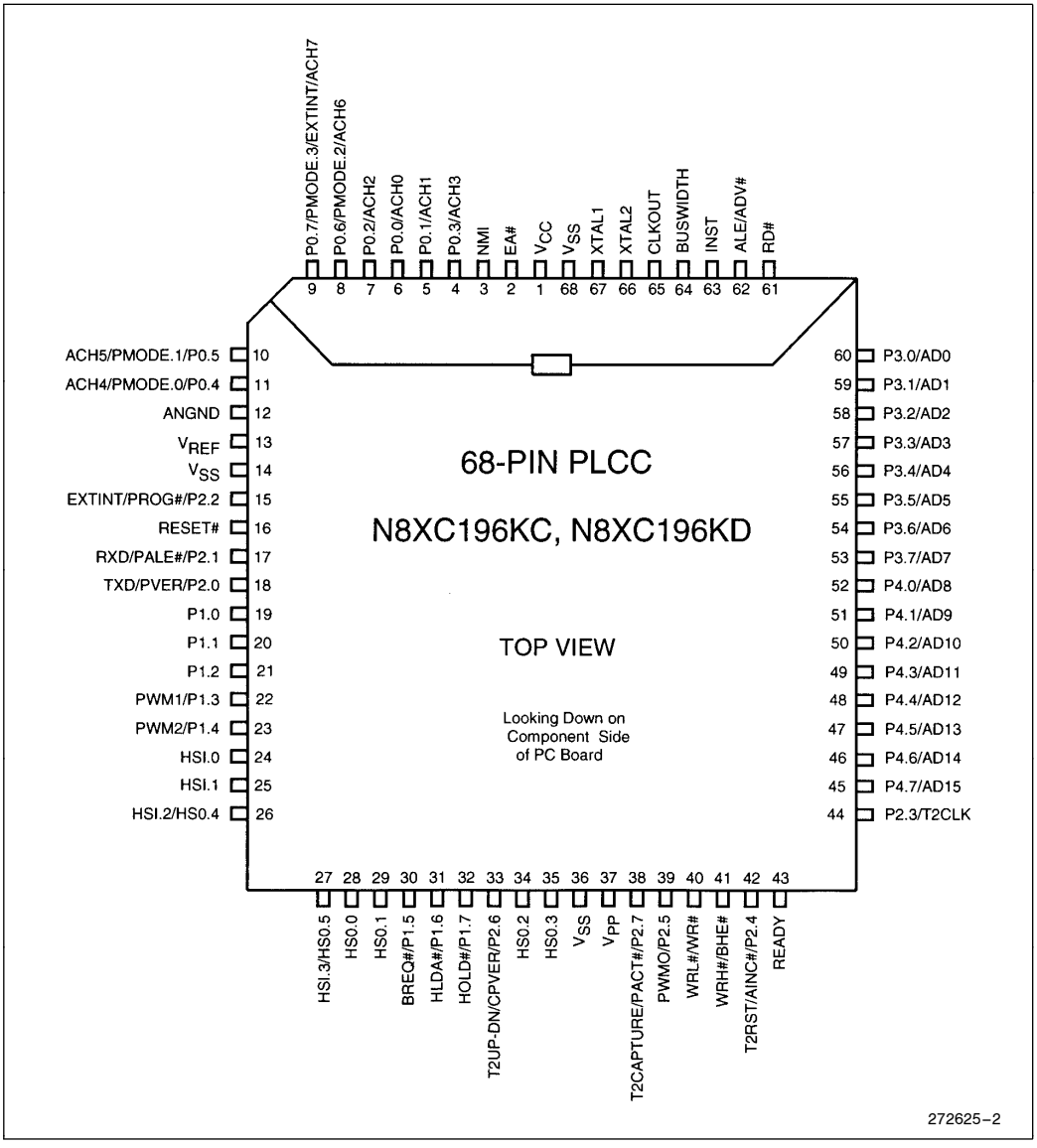

Figure 5-2. N8XC196KC/KD 68-Pin PLCC Package Diagram

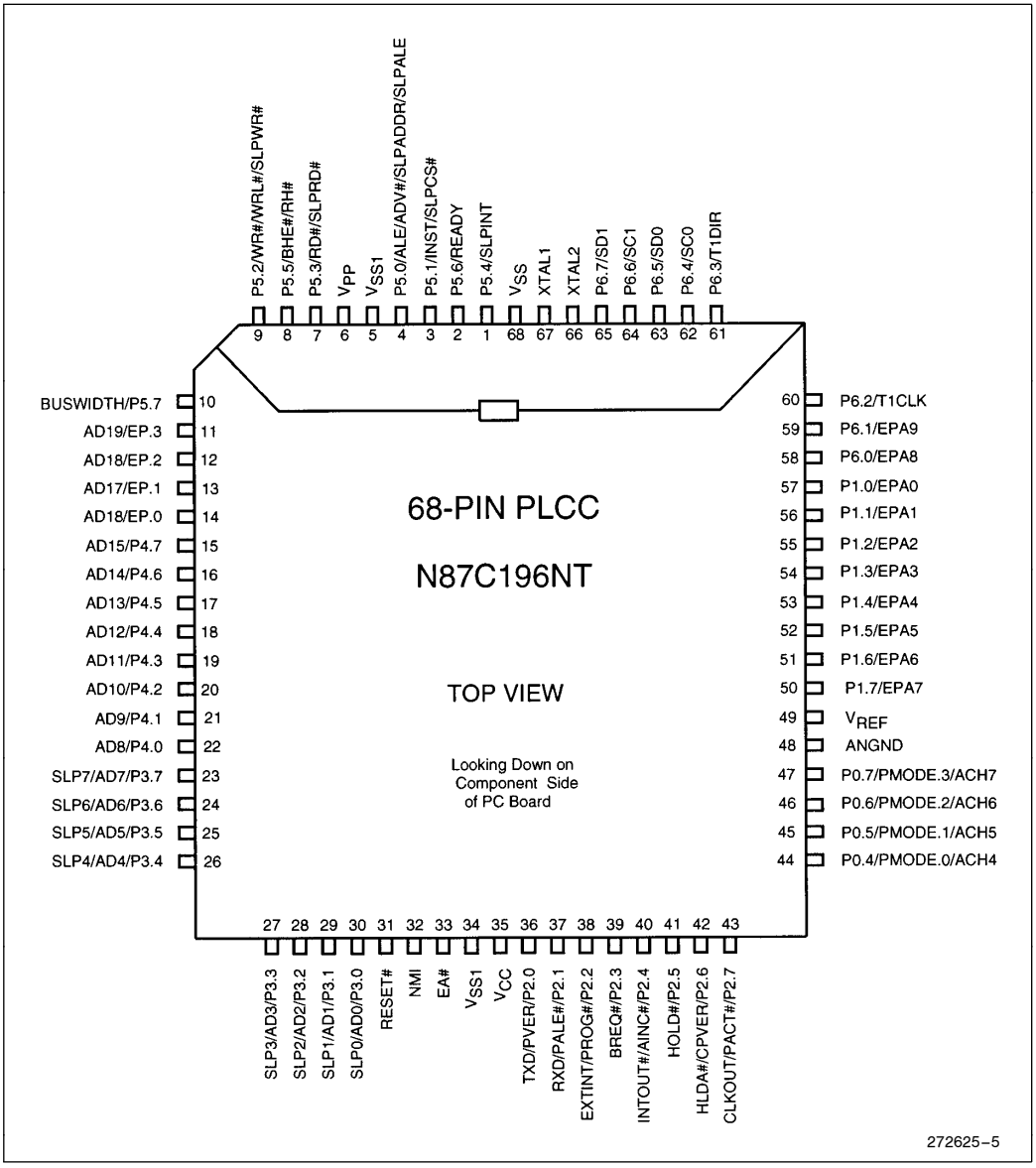

Figure 5-3. N8XC196NT 68-Pin PLCC Package Diagram

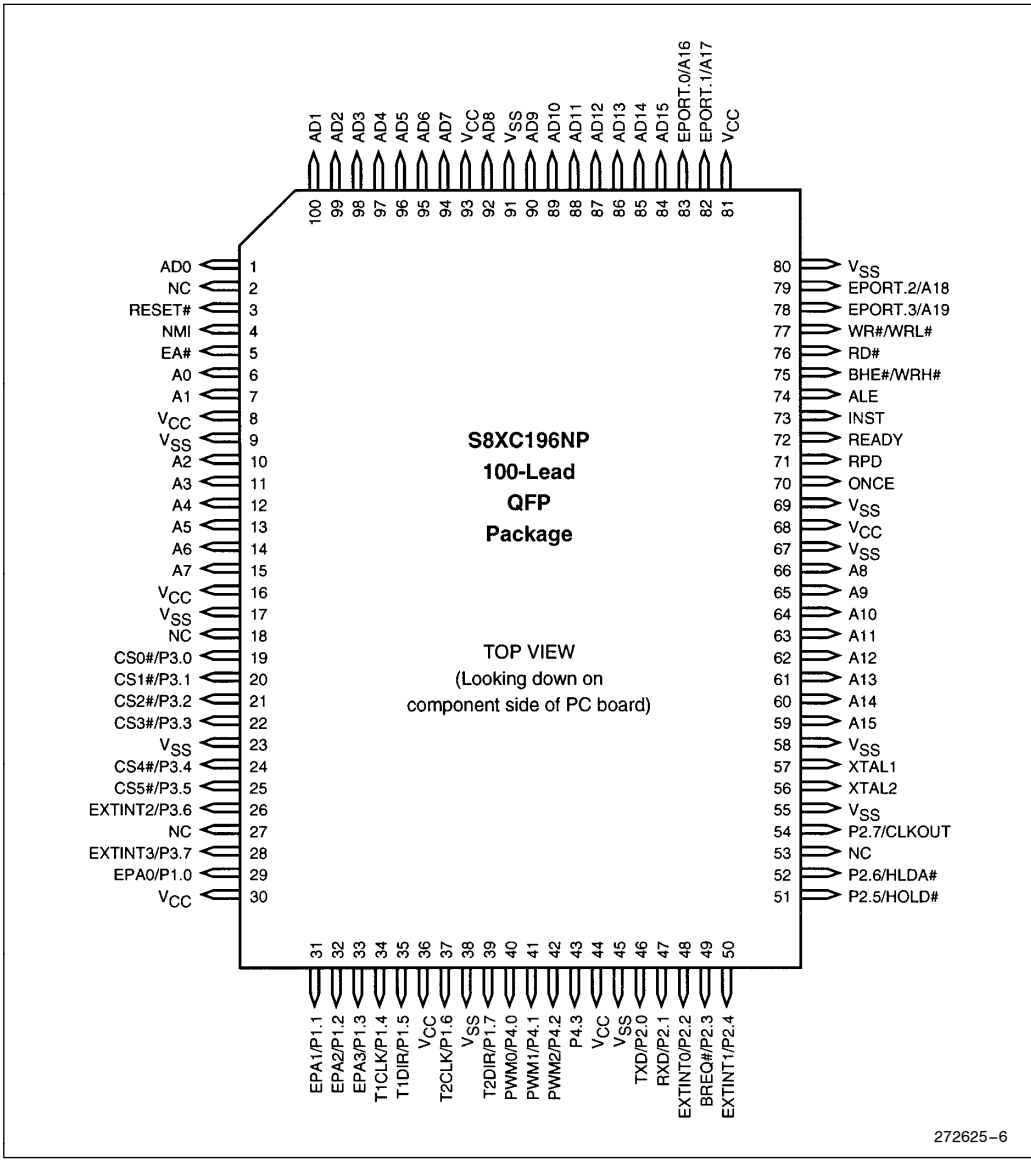

Figure 5-4. S8XC196NP 100-Pin QFP Package Diagram

5.2 Pin Differences

A Yes indicates that the pin is available. A No indicates that the pin is not available. An explanation is included when the pins are not the same for every device.

Pin Symbol	Pin Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
A0–15	System Address Bus.	No. Bus is Multiplexed.	No. Bus is Multiplexed.	No. Bus is Multiplexed.	Yes.
A16–19	Address Lines 19–16.	No.	No.	Yes. Shared with EPORT.0–3.	Yes. Shared with EPORT.0–3.
ACH0–ACH7	Analog Inputs.	Yes. Shared with Port 0.	Yes. Shared with Port 0.	Yes. Shared with Port 0. Has 4 channels (ACH4–7).	No A/D or Port 0.
AD0–15	Multiplexed address/data bus.	Yes. Shared with Port 3 and 4.	Yes. Shared with Port 3 and 4.	Yes. Shared with Port 3 and 4 and the Slave Port address/data bus.	Yes. Multiplexed in multiplexed bus mode. Data-only bus in demultiplexed bus mode.
AINC#	Auto Increment.	Yes. Shared with P2.4/T2RST.	Yes. Shared with P2.4/T2RST.	Yes. Shared with P2.4/INTOUT#.	No. Programming modes are not supported.
ALE/ADV#	Address Latch Enable or Address Valid output.	Yes.	Yes.	Yes. Shared with P5.0/SLPADDR/ SLPALE.	Yes. ALE is used in MUX BUS mode. ADV# is not needed for chip select since the Chip Select Unit is used for this function.
ANGND	Reference ground for the A/D converter.	Yes.	Yes.	Yes.	No A/D available.
BHE#	Byte High Enable.	Yes. Shared with WRH#.	Yes. Shared with WRH#.	Yes. Shared with WRH#/P5.5.	Yes. Shared with WRH#.
BREQ#	Bus Request	Yes. Shared with P1.5.	Yes. Shared with P1.5.	Yes. Shared with P2.3.	Yes. Shared with P2.3.
BUSWIDTH	Input for bus width selection.	Yes.	Yes.	Yes. Shared with P5.7.	No. Not necessary since bus width is selected through the Chip-Select function.
CLKOUT	Output of the internal clock generator.	Yes.	Yes.	Yes. Shared with P2.7/PACT.	Yes. Shared with P2.7.
CPVER	Cumulative Program Output Verification.	No.	Yes. Verifies that all locations have been correctly programmed. Shared with P2.6/ T2UPDN.	Yes. Verifies that all locations have been correctly programmed. Shared with P2.6/ HLDA#.	No. Programming modes are not supported.
CS0–5#	Chip Select Output.	No.	No.	No.	Yes. Shared with P3.0–5.

Pin Symbol	Pin Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
EA#	Input for memory select (External Access). EA# = 1 directs memory accesses to OTP/ROM locations. EA# = 0 directs all memory accesses to off-chip memory.	Yes. EA# = 12.5V causes execution to begin in the Programming Mode.	Yes. EA# = 12.5V causes execution to begin in the Programming Mode.	Yes. EA# = 12.5V causes execution to begin in the Programming Mode.	Yes.
EPA pins	Event Processor Array I/O pins.	No EPA. Use HSIO.	No EPA. Use HSIO.	Yes (EPA0–9). Shared with P1.0–1.7 and P6.0–6.1/T2CLK/T2DIR.	Yes (EPA0–3). Shared with P1.0-3.
EPORT.0–3	Extended Port. 4-bit bi-directional I/O port.	No EPORT.	No EPORT.	Yes. Shared with the extended address bus, A16–A19.	Yes. Shared with the extended address bus, A16–A19.
EXTINTx	External Interrupt.	Yes. EXTINT pins are shared with P2.2/PROG# and P0.7/PMODE.3/ACH7. The IOC1.1 register determines if the EXTINT interrupt source is P0.7 or P2.2. The EXTINT1 interrupt source is P2.2.	Yes. EXTINT pins are shared with P2.2/PROG# and P0.7/PMODE.3/ACH7. The IOC1.1 register determines if the EXTINT interrupt source is P0.7 or P2.2. The EXTINT1 interrupt source is P2.2.	Yes. EXTINT is shared with P2.2/PROG#.	Yes. 4 External Interrupt signals: EXTINT0–3. Shared with P2.2, P2.4, P3.6, P3.7.
HLDA#	Bus Hold Acknowledge.	Yes. Shared with P1.6.	Yes. Shared with P1.6.	Yes. Shared with P2.6.	Yes. Shared with P2.6.
HOLD#	Bus Hold request input.	Yes. Shared with P1.7.	Yes. Shared with P1.7.	Yes. Shared with P2.5.	Yes. Shared with P2.5.
HSI	Inputs to High Speed Input.	Yes. HSI.0–3 are shared with SID. HSI.2–3 are shared with HSO.4–5.	Yes. HSI.0 shared with T2RST. HSI.1 is shared wtih T2CLK. HSI.2–3 are shared with HSO.4–5.	No HSIO. Use EPA.	No HSIO. Use EPA.
HSO	Outputs from High Speed Output.	Yes. HSO.4–5 are shared with HSI.2–3 and SID.	Yes. HSO.4–5 are shared with HSI.2–3.	No HSIO. Use EPA.	No HSIO. Use EPA.
INST	Instruction Fetch Signal.	Yes.	Yes.	Yes. Shared with P5.1/SLPCS#.	Yes.
NMI	Non-Maskable interrupt.	Yes. Vectors through 203EH.	Yes. Vectors through 203EH.	Yes. Vectors through 0FF203EH.	Yes. Vectors through 0FF203EH.

Pin Symbol	Pin Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
ONCE	On-circuit Emulation pin.	No. ONCE mode entered by driving ALE high, INST low and RD# low on the rising edge of RESET#.	No. ONCE mode is entered if P2.0 is held low during the rising edge of RESET#.	No. ONCE mode is entered if HLDA# (P2.6) is held low during the rising edge of RESET#.	Yes. ONCE mode is entered if the ONCE pin is held high during the rising edge of RESET#.
PACT#	Programming Active.	Yes. Shared with P2.7/ T2CAPTURE.	Yes. Shared with P2.7/ T2CAPTURE.	Yes. Shared with P2.7/CLKOUT.	No. Programming modes are not supported.
PALE#	Programming ALE.	Yes. Shared with P2.1/RXD.	Yes. Shared with P2.1/RXD.	Yes. Shared with P2.1/RXD.	No. Programming modes are not supported.
PMODE.0–3	Programming Mode Select Pins.	Yes. Shared with Port 0 pins (also A/D channels).	Yes. Shared with Port 0 pins (also A/D channels).	Yes. Shared with Port 0 pins (also A/D channels).	No. Programming modes are not supported.
Port 0	Input-only port.	Yes. Also used for A/D converter inputs and programming modes.	Yes. Also used for A/D converter inputs and programming modes. P0.7 is shared with EXTINT.	Yes. Also used for A/D converter inputs (ACH4–7) and programming modes.	No Port 0 or A/D.
Port 1	I/O port.	Yes. Quasi-bidirectional. P1.5–7 are shared with BREQ#, HLDA#, and HOLD#.	Yes. Quasi-bidirectional. P1.3–4 are shared with PWM1 and PWM2. P1.5–7 are shared with BREQ#, HLDA#, and HOLD#.	Yes. P1.0–7 are shared with the EPA, T2CLK, and T2DIR.	Yes. P1.0–3 are shared with the EPA. P1.4 is shared with T1CLK. P1.5 is shared with T1DIR. P1.6 is shared with T2CLK. P1.7 is shared with T2DIR.
Port 2	Multi-functional port.	Yes. P2.0 is shared with TXD/ PVER#. P2.1 is shared with RXD/ PALE#. P2.2 is shared with EXTINT/PROG#. P2.3 is shared with T2CLK. P2.4 is shared with T2RST and AINC#. P2.5 is shared with PWM. P2.6 is shared with T2UPDN. P2.7 is shared with T2CAPTURE and PACT#.	Yes. P2.0 is shared with TXD/ PVER#. P2.1 is shared with RXD/ PALE#. P2.2 is shared with EXTINT/PROG#. P2.3 is shared with T2CLK. P2.4 is shared with T2RST and AINC#. P2.5 is shared with PWM0. P2.6 is shared with T2UPDN and CPVER. P2.7 is shared with T2CAPTURE and PACT#.	Yes. P2.0 is shared with TXD/ PVER#. P2.1 is shared with RXD/ PALE#. P2.2 is shared with EXTINT/PROG#. P2.3 is shared with BREQ#. P2.4 is shared with INTOUT# and AINC#. P2.5 is shared with HOLD#. P2.6 is shared with HLDA# and CPVER. P2.7 is shared with CLKOUT and PACT#.	Yes. P2.0–2 are shared with TXD, RXD and EXTINT0. P2.3 is shared with BREQ#. P2.4 is shared with EXTINT1. P2.5 is shared with HOLD#. P2.6 is shared with HLDA#. P2.7 is shared with CLKOUT.

Pin Symbol	Pin Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
Port 3 and 4	Bidirectional I/O ports.	Yes. Shared with multiplexed address/data bus and PVAL. During programming, used to pass commands, addresses, and data to and from slaves.	Yes. Shared with multiplexed address/data bus. During programming, used to pass commands, addresses, and data to and from slaves.	Yes. Shared with multiplexed address/data bus. During programming, used to pass commands, addresses, and data to and from slaves.	Yes. P3.0–5 are shared with CS0–5# (Chip-Select output). P3.6–7 are shared with EXTINT2–3. P4.0–2 are shared with PWM0–2. No P4.4–7.
Port 5	8-bit standard I/O port.	No Port 5.	No Port 5.	Yes. Shared with several other pins (Bus and Slave-Port pins).	No Port 5.
Port 6	8-bit standard I/O port.	No Port 6.	No Port 6.	Yes. Shared with several other pins (EPA, Timer 1, and SSIO pins).	No Port 6.
PROG#	Programming Start.	Yes. Shared with P2.2/EXTINT.	Yes. Shared with P2.2/EXTINT.	Yes. Shared with P2.2/EXTINT.	No. Programming modes are not supported.
PVAL#	Program Valid.	Yes. Indicates success or failure in Auto Programming Mode.	No.	No.	No. Programming modes not supported.
PVER	Program Verification.	Yes. Shared with P2.0/TXD.	Yes. Shared with P2.0/TXD.	Yes. Shared with P2.0/TXD.	No. Programming modes are not supported.
PWM	Pulse Width Modulator output.	Yes. PWM is shared with P2.5.	Yes. PWM0–2 are shared with P2.5, P1.3–4.	No PWM unit. Use EPA.	Yes. PWM0–2 are shared with P4.0–2.
RD#	Read signal output.	Yes.	Yes.	Yes. Shared with P5.3/SLPRD#.	Yes.
READY	Ready input to lengthen memory cycles.	Yes.	Yes.	Yes. Shared with P5.6.	Yes.
RESET#	Reset input to the chip.	Yes. Hold low for at least 4 state times.	Yes. Hold low for at least 1 state time.	Yes. Hold low for at least 1 state time.	Yes. Hold low for at least 1 state time.
RPD	Return from Powerdown.	No. Use V_{PP} instead.	No. Use V_{PP} instead.	No. Use V_{PP} instead.	Yes.
RXD	Receive Serial Data.	Yes. Shared with P2.1/PALE#.	Yes. Shared with P2.1/PALE#.	Yes. Shared with P2.1/PALE#.	Yes. Shared with P2.1.
SID	Slave ID Number.	Yes. Used to identify the slave device for gang-programming in slave-programming mode.	No. Feature removed.	No. Feature removed.	No. Programming modes not supported.

Pin Symbol	Pin Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
Slave Port Pins.	Slave Port pins.	No Slave Port.	No Slave Port.	Yes. Shared with several other pins (Port 3 and Port 5.0–4).	No Slave Port.
SSIO (SC0, SD0, SC1, SD1)	Synchronous Serial I/O pins.	No SSIO.	No SSIO.	Yes. Shared with pins 6.4–6.7.	No SSIO.
T1CLK	External Clock for Timer 1.	No. Timer 1 cannot be clocked externally.	No. Timer 1 cannot be clocked externally.	Yes. Can be used in conjunction with T1DIR for quadrature counting mode. Shared with P6.2. Also the external clock for the serial I/O baud-rate generator.	Yes. Can be used in conjunction with T1DIR for quadrature counting mode. Shared with P1.4. Also the external clock for the serial I/O baud-rate generator.
T1DIR	Timer 1 direction input.	No. Timer 1 cannot be clocked externally.	No. Timer 1 cannot be clocked externally.	Yes. Can be used in conjunction with T1CLK for quadrature counting mode. Shared with P6.3.	Yes. Can be used in conjunction with T1CLK for quadrature counting mode. Shared with P1.5.
T2CAPTURE	Timer 2 Capture interrupt input pin.	Yes. Shared with P2.7/PACT#.	Yes. Shared with P2.7/PACT#.	No. Use EPA pins for Capture interrupts.	No. Use EPA pins for Capture interrupts.
T2CLK	Timer 2 clock input.	Yes. Also serial port baud rate generator input. Shared with P2.3.	Yes. Also serial port baud rate generator input. Shared with P2.3.	Yes. Also used in conjunction with T2DIR in quadrature counting mode. If T2CLK is used, EPA channel 0 cannot be used. Can use T1CLK for serial port baud rate generator input.	Yes. Also used in conjunction with T2DIR in quadrature counting mode. Use T1CLK for serial port baud rate generator input. Shared with P1.6.
T2DIR	Timer 2 Direction Pin.	No. Use T2UPDN.	No. Use T2UPDN.	Yes. When high, Timer 2 increments. Also used in conjunction with T2CLK for quadrature counting mode. Shared with P1.2/ EPA2. If using T2DIR, EPA channel 2 cannot be used.	Yes. When high, Timer 2 increments. Also used in conjunction with T2CLK for quadrature counting mode. Shared with P1.7.

Pin Symbol	Pin Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
T2RST	Timer 2 Reset.	Yes. Shared with P2.4/AINC#.	Yes. Shared with P2.4/AINC#.	No. Timer 2 is free-running.	No. Timer 2 is free-running.
T2UPDN	Timer 2 Up/Down Control pin.	Yes. When high, Timer 2 decrements.	Yes. When high, Timer 2 decrements	No. Use T2DIR.	No. Use T2DIR.
TXD	Transmit Serial Data.	Yes. Shared with P2.0/PVER.	Yes. Shared with P2.0/PVER.	Yes. Shared with P2.0/PVER.	Yes. Shared with P2.0.
V_{CC}	Main Supply Voltage.	Yes. 5V.	Yes. 5V.	Yes. 5V.	Yes. 3.3V or 5V
V_{PP}	Programming voltage.	Yes.	Yes.	Yes.	No Programming Modes available.
V_{REF}	Reference and Supply voltage for the A/D converter and Port 0.	Yes.	Yes.	Yes.	No A/D available.
V_{SS}	Digital Ground.	Yes.	Yes.	Yes.	Yes.
WR#/WRL#	Write and Write-Low output.	Yes.	Yes.	Yes. Shared with P5.2/SLPWR#.	Yes.
WRH#	Write-High output	Yes. Shared with BHE#.	Yes. Shared with BHE#.	Yes. Shared with BHE#/P5.5.	Yes. Shared with BHE#.
XTAL1/ XTAL2	XTAL1 is the clock input. Alternatively, a crystal can be connected across XTAL1 and XTAL2 to utilize the on-board oscillator.	Yes.	Yes.	Yes. XTAL1 can also be the internal clock source for the serial port baud-rate generator.	Yes. XTAL1 can also be the internal clock source for the serial port baud-rate generator, timers, and the PWM unit.

6.0 REGISTERS

This section contains several tables that compare the Registers between the 8XC196KB, the 8XC196KC/KD, the 8XC196NT, and the 8XC196NP. The registers are broken down by modules. If a Yes appears in the product column, then this register is available for this particular device. The registers are assumed to be the same unless noted after the "yes".

6.1 Register Table

A/D Converter

Register Name	Register Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
AD__COMMAND	A/D Command. Selects the A/D channel, the conversion source, and the mode.	Yes. A 0 in bit 3 determines that the HSO will initiate the conversion. Only 10-bit conversion available so bit 4 is reserved (0).	Yes. A 0 in bit 3 determines that the HSO will initiate the conversion. Bit 4 determines the A/D Conversion Mode (8-bit or 10-bit conversion).	Yes. Bits 2–0 are invalid for values of 000, 001, 010, and 011 since ACH0–3 are not available. A 0 in bit 3 determines that the EPA will initiate the conversion. Bits 4–5 determine the A/D Conversion Mode (8-bit, 10-bit, threshold detect high, or threshold detect low.)	No A/D.
AD__RESULT	A/D Result. Contains the channel number, the status, and the result from the conversion.	Yes. Bits 4 and 5 are reserved (0).	Yes. Bit 4 indicates 8-bit or 10-bit conversion. Bit 5 is reserved.	Yes. Bits 4 and 5 reserved (0). The high byte can be written to set the Successive Approximation Register (SAR) to a desired value. This value is used as the reference voltage for the A/D threshold-detection modes. (See section 8.4, A/D Converter, for more details on this new feature.)	No A/D.

Register Name	Register Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
AD__TEST	A/D Conversion Test. Enables conversions and specifies DC offset compensation.	No.	No.	Yes. Added feature. (See section 8.4, A/D Converter, for more details.)	No A/D.
AD__TIME	A/D Conversion Time. Programs the sample and conversion time.	No.	Yes. These values are used if IOC2.3 is set.	Yes. These values are always used.	No A/D.
IOC2 (Bits 3 and 4)	Input/Output Control 2. Bit 4 controls the sample and conversion time by enabling or disabling the A/D clock prescaler.	Yes. Bit 3 is reserved (0).	Yes. Bit 3 determines the source of the conversion time. If bit 3 is clear (8XC196KB-compatible mode), then bit 4 controls the sample and conversion time.	No.	No A/D.

Chip Configuration (See Memory Partitions Section for bits of CCRs.)

Register Name	Register Description	8XC196KB/KC/KD	8XC196NT	8XC196NP
CCR	Chip Configuration.	Yes. Contains PD, BW0, WR, ALE, IRC0–1, and LOC0–1.	No.	No.
CCR0	Chip Configuration 0.	No.	Yes. Contains PD, BW0, WR, ALE, IRC0–1, and LOC0–1.	Yes. Contains PD, BW16, BHE#, DEMUX, and WSO–1.
CCR1	Chip Configuration 1.	No.	Yes. Contains LDCCB2, IRC2, BW1, WDE, and MODE__SEL.	Yes. Contains MODE64 and REMAP.
CCR2	Chip Configuration 2.	No.	Yes. Contains MODE16 and REMAP.	No.

Chip Selects

Register Name	Register Description	8XC196KB/ KC/KD/NT	8XC196NP
ADDRCOMx (x = 0–5)	Address Compare x Register. Specifies the base address of the address range.	No.	Yes.
ADDRMSKx	Address Mask x Register. Specifies the size of the memory block.	No.	Yes.
BUSCONx	Bus Control Register. Specifies the wait states, the bus width, and the address/data multiplexing for all external bus cycles that access locations within the memory block.	No.	Yes.

CPU

Register Name	Register Description	8XC196KB/KC/KD	8XC196NT	8XC196NP
PSW	Program Status Word. Contains the status word and the INT__MASK register.	Yes.	Yes.	Yes.
SP	Stack Pointer. Contains value of stack pointer.	Yes. May point anywhere in the 64K internal or external memory.	Yes. May point anywhere in an internal or external memory page. Use caution when the stack is not located in Register RAM since changes to EP__REG could affect the stack location.	Yes. May point anywhere in an internal or external memory page. Use caution when the stack is not located in Register RAM since changes to EP__REG could affect the stack location.
ZERO__REG	Zero Register. Always equal to zero.	Yes.	Yes. Using the extended addressing mode with a LD or ST instruction forces a 24-bit ZERO__REG value.	Yes. Using the extended addressing mode with a LD or ST instruction forces a 24-bit ZERO__REG value.
ONES__REG	Ones Register. Always equal to FFH.	No.	No.	Yes.

Event Processor Array (EPA)

Register Name	Register Description	8XC196KB/ KC/KD	8XC196NT (n = 0–1) (x = 0–9)	8XC196NP (x = 0–3)
COMPn__CON	EPA Compare x Control. Determines the function of the two EPA compare modules. Identical to the EPAx__CON register.	No. See HSIO.	Yes.	No compare-only modules.
COMPn__TIME	EPA Compare x Time. These are the event-time registers for the EPA compare modules. Functionally identical to the EPAx__TIME registers.	No. See HSIO.	Yes.	No compare-only modules.
EPAx__CON	EPA Capture/Compare x Control. Controls the function of the capture/ compare modules.	No. See HSIO.	Yes. Bit 2 allows the EPA to start an A/D conversion.	Yes. Bit 2 is reserved.
EPAx__TIME	EPA Capture/Compare x Time. Contains timer value.	No. See HSIO.	Yes.	Yes.
EPAIPV	EPA Interrupt Priority Vector Register. Controls the interrupt priorities for EPA4–9, COMP0–1, input overrun interrupts and timer overflow interrupts.	No. See HSIO.	Yes.	No.
EPA__MASK	EPA Interrupt Mask. Masks interrupts.	No. See HSIO.	Yes. Masks EPA4–9 interrupt and EPA overrun interrupts.	Yes. Masks EPA overflow interrupts (0–3).
EPA__MASK1	EPA Interrupt Mask 1. Masks interrupts.	No. See HSIO.	Yes. Masks Timer Overflow interrupts and Compare interrupts.	No.
EPA__PEND	EPA Interrupt Pending. Detects pending EPAx interrupts (corresponding to EPA__MASK.)	No. See HSIO.	Yes.	No. See EPA__STAT.
EPA__PEND1	EPA Interrupt Pending 1. Detects pending EPAx interrupts (corresponding to EPA__MASK1.)	No. See HSIO.	Yes.	No.
EPA__STAT	EPA Interrupt Status. Detects pending EPAx overflow interrupts (corresponding to EPA__MASK.)	No. See HSIO.	No. See EPA__PEND.	Yes.

Extended Port

Register Name	Register Description	8XC196KB/ KC/KD	8XC196NT	8XC196NP
EP__DIR	Extended Port I/O Direction. Determines the I/O direction for each EPORT pin.	No.	Yes.	Yes.
EP__MODE	Extended Port Mode. Determines whether each pin is standard I/O port or Extended Address Port pin.	No.	Yes.	Yes.
EP__PIN	Extended Port Pin Input. Contains current state of each port pin.	No.	Yes.	Yes.
EP__REG	Extended Port Data Output. Contains data to be written out to port pins.	No.	Yes.	Yes.

High Speed Input (HSI)

Register Name	Register Description	8XC196KB/ KC/KD	8XC196NT/NP
HSI__MODE	HSI Mode. Determines what kind of transition triggers a capture.	Yes.	No. See EPA.
HSI__STATUS	HSI Status. Indicates HSI event status and current pin states.	Yes.	No. See EPA.
HSI__TIME	HSI Time. Contains the time that the HSI event was triggered.	Yes.	No. See EPA.
IOC0 (Bits 0, 2, 4, 6)	Input/Output Control 0. Enables and disables the HSI input function of the four HSI pins.	Yes.	No.
IOC1 (Bit 7)	Input/Output Control 1. Selects HSI Interrupt Source (INT02) as either HSI FIFO Full or HSI Holding Register loaded.	Yes.	No.
IOS1 (Bits 6 and 7)	Input/Output Status 0. Bits 6 and 7 indicate the status of the HSI FIFO.	Yes.	No.

High Speed Output (HSO)

Register Name	Register Description	8XC196KB/ KC/KD	8XC196NT/NP
HSO__COMMAND	HSO Command. Determines what event or events will occur within the HSO module at the time specified in the HSO__TIME register.	Yes.	No. See EPA.
HSO__TIME	HSO Time. Specifies the time at which an HSO command is to be executed.	Yes.	No. See EPA.
IOC1 (Bits 4 and 6)	Input/Output Control 1. Bits 4 and 6 enable HSO.4 and HSO.5 as outputs.	Yes.	No.
IOC2 (Bits 0, 1, 5–7)	Input/Output Control 2. Controls three Timer 2 options, enables and disables locking commands into the HSO CAM, and it can clear entries from the HSO CAM.	Yes.	No.
IOS0	Input/Output Status 0. Bits 0–5 indicate the current state of the HSO pins. Bits 6 and 7 indicate the current state of the HSO CAM file and the HSO holding register.	Yes.	No.
IOS1 (Bits 0–5)	Input/Output Status 1. Bits 0–5 contain flags that indicate which events triggered interrupts.	Yes.	No.
IOS2	Input/Output Status 2. Contains flags that indicate which HSO events have occured.	Yes.	No.

Interrupts

Register Name	Register Description	8XC196KB/KC/KD	8XC196NT	8XC196NP
INT__MASK	Interrupt Mask. Enables or disables individual interrupts.	Yes. 0: Timer 1 or 2 Overflow 1: A/D Conversion Complete 2: HSI Data Available/ FIFO Full 3: HSO Output Event 4: HSI.0 External 5: Software Timer 6: Serial Port 7: EXTINT (P2.2 or P0.7)	Yes. 0: EPAx 1–4: EPA3–0 5: A/D Conversion Complete 6: Slave-Port Output Buffer Empty 7: Slave-Port Input Buffer Full	Yes: 0–1: Timer 1–2 Overflow/Underflow 2: Reserved 3–4: EXTINT0–1 5: SIO Transmit 6: SIO Receive 7: EPA0
INT__MASK1	Interrupt Mask 1. Enables or disables individual interrupts.	Yes. 0: Transmit 1: Receive 2: HSI FIFO 4 3: Timer 2 Capture 4: Timer 2 Overflow 5: EXTINT1 (P2.2 pin) 6: HSI FIFO Full 7: NMI	Yes. 0: Slave-Port Command Buffer Full 1: SSIO0 Transfer 2: SSIO1 Transfer 3: SIO Transmit 4: SIO Receive 5: Reserved 6: EXTINT 7: NMI	Yes. 0–2: EPA1–3 3-4: Multiplexed Capture Overrun 5–6: EXTINT2–3 7: NMI
INT__PEND	Interrupt Pending. Indicates which interrupts are pending.	Yes. Mirrors INT__MASK.	Yes. Mirrors INT__MASK.	Yes. Mirrors INT__MASK.
INT__PEND1	Interrupt Pending 1. Indicates which interrupts are pending.	Yes. Mirrors INT__MASK1.	Yes. Mirrors INT__MASK1.	Yes. Mirrors INT__MASK1.

I/O Ports

Register Name	Register Description	8XC196KB/KC/KD	8XC196NT	8XC196NP
IOPORT0	Input Port 0. Contains the current state of P0.0–7. Writing to this register does not affect Port 0.	Yes.	No. See Px__PIN/ Px__REG.	No. See Px__PIN/ Px__REG.
IOPORT1	Input/Output Port 1. Contains the current state of P1.0–7. Can be read or written to.	Yes.	No. See Px__PIN/ Px__REG.	No. See Px__PIN/ Px__REG.
IOPORT2	Input/Output Port 2. Contains the current state of P2.0–7. Writing to this register does not affect the input port pins.	Yes.	No. See Px__PIN.	No. See Px__PIN.
IOPORT3, 4	Input/Output Ports 3 and 4. Contains the current state of P3.0–7 and P4.0–7. Must be read and written to as a word.	Yes.	No. See Px__PIN.	No. See Px__PIN.
P34__DRV	Port 3/4 Push-Pull Enable. Bits 6 and 7 determine whether the port is configured as push-pull or open-drain outputs.	No.	Yes.	No.
Px__DIR	Port x I/O Direction. Determines the I/O direction of the pin.	No.	Yes. (x = 1, 2, 5, 6).	Yes. (x = 1–4)
Px__MODE	Port x Mode. Determines whether the corresponding pin functions as a standard I/O port pin or as a special-function signal.	No. See IOCx.	Yes. (x = 1, 2, 5, 6).	Yes. (x = 1–4).
Px__PIN	Port x Pin Input. Contains the current state of each port pin.	No. See IOPORTx.	Yes. (x = 0–6).	Yes. (x = 1–4).
Px__REG	Port x Data Output. Contains data to be driven out by the respective pins. When a port pin is configured as an input, the corresponding bit in Px__REG must be set.	No. See IOPORTx.	Yes.(x = 0–6).	Yes. (x = 1–4).

Memory Control

Register Name	Register Description	8XC196KB/KC/KD	8XC196NT	8XC196NP
IRAM__CON	Internal RAM Control. Selects whether code RAM memory accesses are directed to the internal code RAM or to off-chip memory.	No internal code RAM.	Yes.	No internal code RAM.
WSR	Window Select. Enables and disables the bus-hold protocol and selects Windows.	Yes. Bits 0–6 select horizontal windows and vertical windows. Horizontal windows allow access to the Special Function Registers by mapping a 24-byte window into the lowest 24 bytes of the Lower Register File. Vertical windows map sections of RAM into the upper section of the Lower Register File, in 32-, 64-, or 128-byte increments.	Yes. Bits 0–6 select Windows, which map SFRs and Register RAM into the upper section of the lower Register File, in 32-, 64-, or 128-byte increments. Horizontal windowing is not necessary.	Yes. Bits 0–6 select Windows, which map SFRs and Register RAM into the upper section of the lower Register File, in 32-, 64-, or 128-byte increments. Horizontal windowing is not necessary.

OTPROM

Register Name	Register Description	8XC196KB/KC/KD	8XC196NT	8XC196NP
PPW	Programming Pulse Width. Contains a value which determines the programming pulse width.	Yes.	Yes.	No Programming modes.
SP__PPW	Serial Port Programming Pulse Width. Contains a value which determines the programming pulse width. Only accessible during Serial Port programming mode.	No Serial-Port Programming mode.	Yes.	No.
USFR	UPROM Special Function Register.	Yes. Bits 2–3 disable external fetches of data and instructions.	Yes. Bit 0 enables the device to detect a failed oscillator. Bits 2–3 disable external fetches of data and instructions.	No.

Peripheral Transaction Server (PTS)

Register Name	Register Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
PTSBLOCK	PTS Block. Specifies number of transfers to take place.	No PTS.	Yes. Used for block transfer mode, HSO, and HSI modes.	Yes. Used for block transfer mode.	Yes. Used for block transfer mode.
PTSCON	PTS Control. Determines PTS mode.	No PTS.	Yes. Determines the PTS mode: Single transfer, block transfer, A/D, HSO, or HSI.	Yes. Determines the PTS mode: Single transfer, block transfer, A/D, PWM Remap, or PWM Toggle.	Yes. Determines the PTS mode: Single transfer, block transfer, PWM Remap, or PWM Toggle.
PTSCONST1	PTS Constant 1. Contains PWM on-time.	No PTS.	No.	Yes. Used in PWM Toggle and PWM Remap modes.	Yes. Used in PWM Toggle and PWM Remap modes.
PTSCONST2	PTS Constant 2. Contains PWM off-time.	No PTS.	No.	Yes. Used in PWM Toggle mode.	Yes. Used in PWM Toggle mode.
PTSCOUNT	PTS Count. Defines the number of PTS cycles to be executed.	No PTS.	Yes. Used in all PTS Modes.	Yes. Used in PTS single transfer, block transfer, and A/D modes.	Yes. Used in PTS single and block transfer modes.
PTSDST	PTS Destination. Points to destination memory location.	No PTS.	Yes. Used in single transfer, block transfer, and HSI modes.	Yes. Used in single and block transfer modes.	Yes. Used in single and block transfer modes.
PTSPTR1	PTS Pointer 1. Points to memory location.	No PTS.	No. See PTS__S/D.	Yes. Used in A/D mode and the PWM modes. In A/D modes, points to A/D conversion table. In PWM mode, points to memory location, usually EPAx__TIME.	Yes. Used in the PWM modes to point to memory location, usually EPAx__TIME.
PTSPTR2	PTS Pointer 2. Points to memory location.	No PTS.	No. See PTS__REG.	Yes. Used in A/D mode to point to the AD__RESULT register.	No.
PTS__REG	PTS AD. Points to AD__RESULT register.	No PTS.	Yes. Used in A/D mode.	No. See PTSPTR2.	No.
PTS__S/D	PTS Source/ Destination. Points to the A/D conversion table.	No PTS.	Yes. Used in A/D mode.	No. See PTSPTR1.	No.

Register Name	Register Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
PTSSEL	PTS Select Register (HI/LO). Determines whether interrupt is serviced by PTS or standard interrupt routine.	No PTS.	Yes: 0: Timer Overflow 1: A/D Conversion Complete 2: HSI Data Available/FIFO Full 3: HSO Output Event 4: HSI.0 External 5: Software Timer 6: Serial Port 7: EXTINT (P2.2 or P0.7) 8: Transmit 9: Receive 10: HSI FIFO 4 11: Timer 2 Capture 12: Timer 2 Overflow 13: EXTINT1 (P2.2) 14: HSI FIFO Full 15: Reserved (0)	Yes. 0: EPAx 1–4: EPA3–0 5: A/D Conversion Complete 6: Slave Port Output Buffer Full 7: Slave Port Input Buffer Full. 8: Slave Port Command Buffer Full 9–10: SSIO0–1 Transfer 11: SIO Transmit 12: SIO Receive 13: Reserved (0) 14: EXTINT 15: Reserved (0)	Yes. 0–1: OVRTMR1–2 2: Reserved (0) 3–4: EXTINT0–1 5: SIO Transmit 6: SIO Receive 7–10: EPA0–3 11–12: OVR0__1–2__3 13–14: EXTINT2–3 15: Reserved(0)
PTSSRC	PTS Source. Points to source memory location.	No PTS.	Yes. Used in single transfer, block transfer, and HSO modes.	Yes. Used in single and block transfer modes.	Yes. Used in single and block transfer modes.
PTSSRV	PTS Service. Indicates that final PTS cycle has been serviced. Corresponds to PTSSEL register.	No PTS.	Yes.	Yes.	Yes.

Pulse Width Modulator (PWM)

Register Name	Register Description	8XC196KB	8XC196KC/KD	8XC196NT	8XC196NP
CON__REG0 (Bit 0)	Control Register. Controls clock prescaler. Bit 0 controls prescaler for all 3 PWMs.	No. See IOC2.	No. See IOC2.	No PWM.	Yes.
PWM0__CONTROL	PWM0 Control Register. Controls duty cycle.	Yes.	Yes.	No PWM.	Yes.
PWM1__CONTROL	PWM1 Control Register. Controls duty cycle.	No PWM1.	Yes.	No PWM.	Yes.
PWM2__CONTROL	PWM2 Control Register. Controls duty cycle.	No PWM2.	Yes.	No PWM.	Yes.
IOC1 (Bit 0)	Input/Output Control Register 1. Bit 0 = 1 for PWM output.	Yes.	Yes.	No PWM.	No. See P4__MODE.
IOC2 (Bit 2)	Input/Output Control Register 2. Bit 2 controls prescaler on PWMs.	Yes.	Yes. (Controls all 3 PWMs.)	No PWM.	No. See CON__REG0.
IOC3 (Bits 2 and 3)	Input/Output Control Register 3. Bit 2 = 1 for PWM1 output, bit 3 = 1 for PWM2 output.	No.	Yes.	No PWM.	No. See P4__MODE.

Serial Port

Register Name	Register Description	8XC196KB/KC/KD	8XC196NT	8XC196NP
BAUD__RATE	Baud Rate. Selects serial port baud rate and clock source.	Yes. It must be written with two bytes, the least-significant byte first.	No. See SP__BAUD.	No. See SP__BAUD.
SBUF__RX	Serial Port Receive Buffer Register. Contains data received from the serial port.	Yes.	Yes.	Yes.
SBUF__TX	Serial Port Transmit Buffer Register. Contains data that is ready for transmission.	Yes.	Yes.	Yes.
SP__BAUD	Selects serial port baud rate and clock source.	No. See BAUD__RATE.	Yes. It must be addressed and written as a word and must be written using a single load instruction.	Yes. It must be addressed and written as a word and must be written using a single load instruction.
SP__CON	Serial Port Control. Selects the communications mode and other serial port functions.	Yes. Bit 5 is reserved (0) and is always even parity.	Yes. Bit 5 is the Parity Selection bit for even or odd parity.	Yes. Bit 5 is the Parity Selection bit for even or odd parity.
SP__STAT	Serial Port Status. Indicates status of the serial port.	Yes.	Yes.	Yes.
IOC1 (Bit 5)	Input/Output Control Register 1. Bit 5 = 1 for serial port TXD output.	Yes.	No. See P2__MODE.	No. See P2__MODE.

Slave Port

Register Name	Register Description	8XC196KB/KC/KD and 8XC196NP	8XC196NT
SLP__CMD	Slave-Port Command. Accepts commands from the master to the slave.	No Slave Port.	Yes.
SLP__CON	Slave-Port Control. Configures the Slave Port.	No Slave Port.	Yes.
SLP__STAT	Slave-Port Status. Contains the status of the slave.	No Slave Port.	Yes.

Synchronous Serial Port (SSIO)

Register Name	Register Description	8XC196KB/ KC/KD/NP	8XC196NT
SSIO__BAUD	Synchronous Serial Baud Rate. Enables/disables the baud-rate generator and selects the SSIO baud rate.	No SSIO.	Yes.
SSIO0__BUF/ SSIO1__BUF	Synchronous Serial Buffer x. Contains the received data or the data for transmission.	No SSIO.	Yes.
SSIO0__CON/ SSIO1__CON	Synchronous Serial x Control. Control the communication mode and clock source and reflect the status of the SSIO ports.	No SSIO.	Yes.

Timers

Register Name	Register Description	8XC196KB/KC/KD	8XC196NT/NP
TIMER1	Timer 1. Contains the value of Timer 1.	Yes.	Yes.
T1CONTROL	Timer 1 Control. Determines the clock source, counting direction, and count rate for Timer 1.	No. See IOCx registers.	Yes. 0–2: EPA Clock Prescaler Bits 3–5: EPA Clock Direction Mode Bits 6: Up/Down 7: Counter Enable
TIMER2	Timer 2. Contains the value of Timer 2.	Yes.	Yes.
T2CAPTURE	Timer 2 Capture. Contains the value of Timer 2 when a rising edge occurs on P2.7.	Yes.	No.
T2CONTROL	Timer 2 Control. Determines the clock source, counting direction, and count rate for Timer 2.	No. See IOCx registers.	Yes. 0–2: EPA Prescaler Bits 3–5: EPA Clock Direction Mode Bits (Can use Timer 1 overflow as source) 6: Up/Down 7: Counter Enable
IOC0 (Bits 1,3,5,7)	Input/ Output Control 0. Bits 1,3,5,7 select the external clock and reset sources for Timer 2.	Yes. 1: Timer 2 Software Reset 3: Timer 2 External Reset Source 5: Timer 2 Reset Source 7: Timer 2 Clock Source	No. See T2CONTROL.
IOC1 (Bits 2 and 3)	Input/ Output Control 1. Bits 2-3 select interrupt sources for Timer Overflow.	Yes. 2: Enable Timer 1 Overflow Interrupt. 3: Enable Timer 2 Overflow Interrupt.	No. An overflow on the timers always generates an interrupt pending.
IOC2 (Bits 0–1, 5)	Input/ Output Control 2. Bits 0,1,5 control Timer 2 options.	Yes. 0: Enable Timer 2 Fast Increment 1: Enable Timer 2 Up/Down Count 5: Select Timer 2 Overflow Boundary	No. See T2CONTROL.
IOC3 (Bit 0)	Input/ Output Control 3. Bit 0 selects either an internal or an external clock source for Timer 2.	Yes. (8XC196KC/KD only) 0: Timer 2 Internal Clock Enable	No. See T2CONTROL.
IOS1 (Bits 4 and 5)	Input/ Output Status 1. Bits 4 and 5 indicate triggered Timer Overflow Interrupts.	Yes. 4: Timer 2 Overflow Flag 5: Timer 1 Overflow Flag	No. The timer overflow interrupts are handled by individual interrupts.

Watchdog

Register Name	Register Description	8XC196KB/KC/KD/NT	8XC196NP
WATCHDOG	Watchdog Timer. Contains the current value of the Watchdog timer. Also used to enable the Watchdog timer.	Yes.	No Watchdog Timer.

7.0 INTERRUPT PROCESSING UNIT

The MCS 96 Microcontroller family devices process interrupts via two methods: using the Interrupt Controller and using the Peripheral Transaction Server. The Standard Interrupt Control Unit of the 8XC196KB/KC/KD and the 8XC196Nx function identically. However, the interrupt sources are different as well as the interrupt vector locations. This section contains tables (see Tables 7-1 through 7-3) which show the interrupt vector sources, locations, and priorities for each of the devices discussed in this application note. The Peripheral Transaction Server (PTS), a microcoded hardware interrupt handler, has been added to all the CMOS MCS 96 devices following the 8XC196KB. The PTS can service an interrupt in the time required to execute a single instruction. This section will briefly describe the different PTS modes available to the 8XC196KC/KD, the 8XC196NT, and the 8XC196NP.

7.1 Interrupt Controller

The Interrupt Controller generates vectors to software interrupt service routines. When the hardware detects an interrupt, it generates and executes an interrupt call. Upon completion of the interrupt service routine, program execution continues. The vector locations for the 1 Mbyte addressable parts are located in the 0FFh page.

Table 7-1. 8XC196KB/KC/KD Interrupt Vector Sources, Locations, and Priorities

Number	Source	Interrupt Controller Service		PTS Service (for 8XC196KC/KD only)	
		Vector Location	Priority	Vector Location	Priority
INT15	NMI	203EH	30	—	—
INT14	HSI FIFO Full	203CH	14	205CH	29
INT13	EXTINT1(P2.2)	203AH	13	205AH	28
INT12	Timer 2 Overflow	2038H	12	2058H	27
INT11	Timer 2 Capture	2036H	11	2056H	26
INT10	HSI FIFO Fourth Entry	2034H	10	2054H	25
INT09	Receive Flag	2032H	9	2052H	24
INT08	Transmit Flag	2030H	8	2050H	23
SPECIAL	Unimplemented Opcode	2012H	—	—	—
SPECIAL	Software Trap	2010H	—	—	—

Table 7-1. 8XC196KB/KC/KD Interrupt Vector Sources, Locations, and Priorities (Continued)

Number	Source	Interrupt Controller Service		PTS Service (for 8XC196KC/KD only)	
		Vector Location	Priority	Vector Location	Priority
INT07	EXTINT (P2.2 or P0.7)	200EH	7	204EH	22
INT06	Serial Port (RI and TI Flag)	200CH	6	204CH	21
INT05	Software Timer (Software Timer 0–3, Timer 2 Reset, or A/D Conversion Start	200AH	5	204AH	20
INT04	HSI.0 Pin	2008H	4	2048H	19
INT03	High Speed Outputs (0–5)	2006H	3	2046H	18
INT02	HSI Data Available (HSI FIFO Full or HSI Holding Register Loaded	2004H	2	2044H	17
INT01	A/D Conversion Complete	2002H	1	2042H	16
INT00	Timer 1 or Timer 2 Overflow	2000H	0	2040H	15

Table 7-2. 8XC196NT Interrupt Vector Sources, Locations, and Priorities

Number	Source	Interrupt Controller Service		PTS Service	
		Vector Location	Priority	Vector Location	Priority
INT15	NMI	FF 203EH	30	—	—
INT14	EXTINT Pin	FF 203CH	14	FF 205CH	29
INT13	Reserved	FF 203AH	13	FF 205AH	28
INT12	SIO Receive	FF 2038H	12	FF 2058H	27
INT11	SIO Transmit	FF 2036H	11	FF 2056H	26
INT10	SSIO Channel 1 Transfer	FF 2034H	10	FF 2054H	25
INT09	SSIO Channel 0 Transfer	FF 2032H	9	FF 2052H	24
INT08	SLP Command Buffer Full	FF 2030H	8	FF 2050H	23
SPECIAL	Unimplemented Opcode	FF 2012H	—	—	—
SPECIAL	Software TRAP Instruction	FF 2010H	—	—	—
INT07	SLP Input Buffer Full	FF 200EH	7	FF 204EH	22
INT06	SLP Output Buffer Empty	FF 200CH	6	FF 204CH	21
INT05	A/D Conversion Complete	FF 200AH	5	FF 204AH	20
INT04	EPA0	FF 2008H	4	FF 2048H	19
INT03	EPA1	FF 2006H	3	FF 2046H	18
INT02	EPA2	FF 2004H	2	FF 2044H	17
INT01	EPA3	FF 2002H	1	FF 2042H	16
INT00	EPAx (EPA4–9, EPA0–9 Overrun, EPA Compare 0–1, Timer 1 Overflow, Timer 2 Overflow)	FF 2000H	0	FF 2040H	15

Table 7-3. 8XC196NP Interrupt Vector Sources, Locations, and Priorities

Number	Source	Interrupt Controller Service		PTS Service	
		Vector Location	Priority	Vector Location	Priority
INT15	NMI	FF 203EH	30	—	—
INT14	EXTINT3 Pin	FF 203CH	14	FF 205CH	29
INT13	EXTINT2 Pin	FF 203AH	13	FF 205AH	28
INT12	EPA Overrun Error in Module 2 and/or 3	FF 2038H	12	FF 2058H	27
INT11	EPA Overrun Error in Module 0 and/or 1	FF 2036H	11	FF 2056H	26
INT10	EPA3	FF 2034H	10	FF 2054H	25
INT09	EPA2	FF 2032H	9	FF 2052H	24
INT08	EPA1	FF 2030H	8	FF 2050H	23
SPECIAL	Unimplemented Opcode	FF 2012H	—	—	—
SPECIAL	Software TRAP Instruction	FF 2010H	—	—	—
INT07	EPA0	FF 200EH	7	FF 204EH	22
INT06	SIO Receive	FF 200CH	6	FF 204CH	21
INT05	SIO Transmit	FF 200AH	5	FF 204AH	20
INT04	EXTINT1 Pin	FF 2008H	4	FF 2048H	19
INT03	EXTINT0 Pin	FF 2006H	3	FF 2046H	18
INT02	Reserved	FF 2004H	2	FF 2044H	17
INT01	Timer 2 Overflow	FF 2002H	1	FF 2042H	16
INT00	Timer 1 Overflow	FF 2000H	0	FF 2040H	15

7.2 Peripheral Transaction Server

The PTS can be used in place of a standard interrupt service routine for each of the maskable interrupts. Since the PTS does not modify the stack, the PTS can service interrupts with less overhead. There are several different special microcoded modes for the different devices with the PTS feature. Each PTS interrupt requires a block of data called the PTS Control Block (PTSCB). The PTS vector location (for example, 0FF2042h for the EPA3 Interrupt on the 8XC196NT) vectors to the address where the PTSCB is located.

NOTE:
For the 8XC196Nx devices, the PTSCB must be located in register RAM, in page 00H, and must be aligned on a quad-word boundary (divisible by 8).

PTS cycles perform non-extended data moves, so the rules for non-extended instructions apply to data locations (that is, data is moved within the page specified by the EP__REG register). For example, if code is being executed from page 0FFh when the PTS interrupt occurs, any data transfers will be made to and from page 0FFh.

Table 7-4. PTS Modes

PTS Modes	8XC196KC/KD	8XC196NT	8XC196NP
Single Transfer Mode	Yes	Yes	Yes
Block Transfer Mode	Yes	Yes	Yes
A/D Scan Mode	Yes	Yes	No
HSO Mode	Yes	No	No
HSI Mode	Yes	No	No
PWM Toggle Mode	No	Yes	Yes
PWM Remap Mode	No	Yes	Yes

7.2.1 SINGLE TRANSFER MODE

The PTS in the Single Transfer Mode transfers a single byte or word during each PTS cycle from one memory location to another. This mode is typically used with the serial port interrupts. The number of transfers is determined by the PTSCOUNT register. The PTSSRC register points to the source location and the PTSDST register points to the destination location.

7.2.2 BLOCK TRANSFER MODE

The PTS in the Block Transfer Mode transfers a block of data from one memory location to another. The PTSBLOCK register specifies the number of bytes or words in each block. The PTSCOUNT register specifies the number of transfers. The PTSSRC register points to the source location and the PTSDST register points to the destination location.

7.2.3 A/D SCAN MODE

The PTS in the A/D Scan Mode causes the A/D converter to perform multiple conversions on one or more channels and then stores the results. A table is used to store the commands and the data from the conversion. The A/D scan mode is initiated with a user software routine which starts the first conversion. The A/D Conversion Complete interrupt is then generated and the PTS cycle is begun. The number of conversions is determined by the PTSCOUNT register.

7.2.4 HSO MODE

The PTS in the HSO Mode loads the HSO CAM file with the contents of a table located in external or internal memory. The PTSSRC register contains the address of the HSO table. The table contains the HSO Time (determines when the action should occur with respect to Timer 1 or Timer 2) and the HSO Command (specifies what action will occur). The PTSBLOCK register specifies the number of HSO entries (8 maximum). The PTSCOUNT register specifies the number of PTS cycles that will occur.

7.2.5 HSI MODE

The PTS in the HSI Mode dumps the contents of the HSI FIFO to a table in either internal or external memory. The PTSDST register contains the address of the HSI Table. The table contains the HSI Time (the time with respect to Timer 1 or Timer 2 that the event occurred) and the HSI Status (describes the event that has occurred). The PTSBLOCK register specifies how many FIFO blocks will be transferred to the table during each PTS cycle. This number should correspond to the interrupt that generates the PTS cycle. For example, if the interrupt used for the PTS cycle is the HSI FIFO 4 interrupt (fourth entry triggers an interrupt) then a 4 should be loaded into the PTSBLOCK register so that all entries in the FIFO will be dumped into the HSI table.

7.2.6 PWM TOGGLE MODE

The PTS in the PWM Toggle Mode uses the EPA to generate pulse-width modulated output signals. In the toggle mode, a single EPA channel is used to generate the PWM signal. The PTSCON register determines the mode and the initial value of the EPA pin (with the Toggle Bit (TBIT)). The PTSPTR1 register is usually EPAx__TIME. It is then added to either the PTSCONST 1 or 2 register, depending on the value of TBIT. This new time is loaded back into the PTSPTR1 register and this is when the next event will occur.

7.2.7 PWM REMAP MODE

The PTS in the PWM Remap Mode also uses the EPA to generate PWM output signals. Unlike the toggle mode, the remap mode uses two EPA channels that allow for duty cycles closer to 0% or 100%. One EPA channel sets the output and the other EPA channel clears the output. Both EPA channels have an associated PTSCB. The PTSPTR1 register is usually EPAx__TIME that indicates the first event. This value is then added to PTSCONST1 and then stored back into the PTSPTR1 register. This is when the next event will occur.

8.0 PERIPHERALS

The MCS 96 Microcontroller devices have some of the same peripherals, although in some cases they are implemented differently. This section will outline the differences in several of the peripherals. For details on how to program the peripherals, please refer to the respective User's Manual.

8.1 I/O Ports

The I/O ports of the 8XC196KB/KC/KD and the 8XC196Nx devices function similarly, but are implemented with different registers. The 8XC196KB/KC/KD devices have five 8-bit I/O ports. Ports 3 and 4 are multiplexed with the address/data bus. If using the external bus, it is not recommended that ports 3 and 4 be used as standard I/O. Most of the pins of ports 0-2 can also be used as special function pins such as A/D inputs and bus control pins. The 8XC196NT device has 8 I/O ports (Ports 0, 1, 2, and 6 are standard 8-bit I/O ports, Ports 3, 4 and 5 are 8-bit memory mapped I/O ports, and the EPORT is a 4-bit memory-mapped I/O port). Port 0 is an input-only port and can be used as analog and digital inputs. Ports 3 and 4 are multiplexed with the 16-bit external address/data bus. All the other port pins can be selected as their special function pins such as EPA, SSIO, and bus-control pins. The EPORT provides additional address signals to support extended addressing. The 8XC196NP has four standard 8-bit I/O ports (although Port 4 is functionally a 4-bit port) and one memory-mapped 4-bit I/O port (EPORT), which was added to support extended addressing. Each pin has an associated special function. Since the 8XC196NP device has a demultiplexed address/data bus, Ports 3 and 4 can be used as standard I/O pins. Ports 1–4 have such special functions as EPA, SIO, external interrupts, chip-select pins, and PWM pins.

The 8XC196KB/KC/KD I/O ports are programmed using IOPORTx or location 1FFEH for Ports 3 and 4 and several different IOCx registers. (See Table 8-1 for a comparison.) The I/O port registers for the 8XC196Nx are very straight forward and consistent across each port. The registers to configure all the I/O ports on the 8XC196Nx devices are Px__DIR, Px__MODE, Px__PIN, and Px__REG. The examples following show a comparison of the registers used to program Port 1.3 as an output high and as an input.

Table 8-1 Registers Used to Program I/O Ports

Function Accomplished	8XC196KB/KC/KD Register	8XC196Nx Register
Contains the data to be driven out by port pin.	IOPORTx	Px__REG
Determines the I/O direction for the pin.	No register used. Different for different types of ports being used.	Px__DIR
Determines the mode. Can be Standard I/O or Special Function	Varies depending on the port. Mostly controlled with IOCx registers.	Px__MODE
Contains the current state of each port pin.	IOPORTx	Px__PIN

Example 8.1: Configure pin P1.3 as an output high.

```
8XC196KB/KC/KD:
 ldb  WSR, #01h
 ldb  IOC3, #00h          ;IOC3 in horizontal window 1
                          ;Selects the P1.3 pin function as quasi-bi-directional
                          ;port pin instead of as a special function pin.
 ldb  WSR, #00h
 ldb  IOPORT1, #08h       ;writes a 1 to IOPORT 1.3.
8XC196Nx:
 ldb  WSR, #1fh           ;Select vertical window to access SFRs.
 ldb  P1_REG_1F, #08h     ;initial value in P1_REG.
 ldb  P1_DIR_1F, #0f7h    ;selects P1.3 as a complementary output instead of
                          ;as an input or open-drain output.
 ldb  P1_MODE_1F, #00h    ;selects as a standard I/O instead of as a special
                          ;function pin.
```

Example 8.2: Configure Pin P1.3 as an Input.

```
8XC196KB/KC/KD:
 ldb  WSR, #00h
 ldb  IOPORT1, #08h       ;must write a 1 to IOPORT bit for it to be an input.
 ldb  WSR, #01h
 ldb  IOC3, #00h          ;selects as a standard I/O instead of as a special
                          ;function pin.
8XC196Nx:
 ldb  WSR, #1fh           ;Select vertical window to access SFRs.
 ldb  P1_REG_1F, #08h     ;initial value in P1_REG.
 ldb  P1_DIR_1F, #08h     ;selects as an input instead of as a complementary
                          ;output.
 ldb  P1_MODE_1F, #00h    ;selects standard I/O.
```

8.2 Serial I/O Port

The Asynchronous Serial Ports on the 8XC196KB/KC/KD/NT/NP function identically. The initialization for the SIO is slightly different for the 8XC196Nx devices. (See Example 8.3.) The BAUD_RATE register of the 8XC196KB/KC/KD contains the same value as the SP_BAUD register the 8XC196Nx devices. They differ only in how they are written. The BAUD_RATE register must be written with two bytes, least-significant byte first, and the SP_BAUD register must be written as a word. Also, only even parity is allowed for the 8XC196KB/KC/KD, but the 8XC196Nx devices allow for odd parity as well. As outlined in Section 8.1, I/O Ports, the ports for the TXD pin are initialized differently as well. The 8XC196NT has an additional feature of a Synchronous Serial Port. See the 8XC196NT User's Manual for details on how to program this peripheral.

Example 8.3: Initialize the Serial Port for Mode 1, Even Parity Enabled, Using an External Clock Source of 5 MHz Transmitting at 9600 Baud.

8XC196KB/KC/KD:

```
 ldb  WSR, #00h
 ldb  BAUD_RATE, #041h     ; The Baud Rate register must be written with two
                           ;bytes, the least-significant byte first. The most-
                           ;significant bit selects the clock source.
 ldb  BAUD_RATE, #00h
 ldb  SP_CON, #05h         ; Bit 2 enables even parity (odd parity is not an
                           ;option as it is with the 8XC196Nx devices).
                           ;Mode 1 selected.
 ldb  IOC1, #020h          ; Selects P2.0 as special-function signal serial-
                           ;port
                           ;TXD Output instead of as a standard I/O.
```

8XC196Nx:

```
 ldb  WSR, #1fh            ;Select vertical window to access SFRs.
 ldb  SP_CON_1F, #005h     ;Bit 2 enables parity; bit 5 enables even parity
                           ;instead of odd.
 ld  SP_BAUD_1F, #041h     ;The Baud Rate register must be addressed and
                           ;written as a word and must be written using a
                           ;single load instruction.
 ldb  P2_REG_1F, #07fh     ; Initial TXD pin output.
 ldb  P2_DIR_1F, #07eh     ; Selects P2.0 as TXD output instead of as an input.
 ldb  P2_MODE_1F, #081h    ; Selects P2.0 as special-function signal serial-
                           ;port
                           ;TXD Output instead of as a standard I/O.
 ldb  P6_REG_1F, #0ffh     ; Initial T1CLK pin input.
 ldb  P6_DIR_1F, #0ffh     ; Selects T1CLK pin an input.
 ldb  P6_MODE_1F, #04h     ; Selects T1CLK as special-function signal Timer 1
                           ;clock instead of as a standard I/O.
```

8.3 High Speed Input/Output (HSIO) and Event Processor Array (EPA) Unit

The HSIO family devices (8XC196KB/KC/KD) and the EPA family devices, to which the 8XC196Nx family belongs, have similar yet different input/output capabilities. Their functionality is quite similar but they are implemented quite differently. The HSIO has 8 associated input/output pins (4 HSO, 2 HSI, and 2 selectable HSI/O pins). The programmed events for the HSO are stored in a Content-Addressable Memory (CAM) file. The CAM can store a maximum of 8 events at one time and is used for all HSO outputs. The HSI module records predefined events that occur on the HSI inputs and stores the events and times in a FIFO queue (up to seven). From the FIFO, events move into a holding register (which can store an additional event) until the data is read. The FIFO is shared between all HSI inputs.

The EPA is different in that output events are programmed—and input events are stored—individually for each input/output, called capture/compare modules. The 8XC196NT has ten capture/compare modules (EPA0–9) and two dedicated compare modules that share pins with EPA8 and EPA9. EPA0 and EPA1, and EPA2 and EPA3 can be remapped so that both modules control the same pin. This feature can be used for higher speed pulse-width modulated output signals or greater speed inputs as well. The 8XC196NP has four capture/compare modules (EPA0–3). These modules can be remapped, just as the 8XC196NT.

The EPA unit has several advantages over the HSIO unit. The timers for the EPA unit can increment every two state times, whereas the timers for the HSIO unit can only increment every eight state times. This allows the EPA unit to have higher resolution. The EPA also offers more flexibility since any of the EPA modules can be configured as an input or an output. The EPA offers a more modular design where all the available EPA modules can be used (12 on the 8XC196NT and 4 on the 8XC196NP) since they are all programmed independently. The number of HSIO events is limited by the eight HSO CAM and eight HSI FIFO entries. AP-Note 449, *A Comparison of the EPA and HSIO,* discusses the differences in great detail. It also gives several examples. Please refer to this document to learn more about the differences in these two peripherals.

8.4 Analog-to-Digital Converter

The Analog-to-Digital Converter (A/D) on all of the MCS 96 microcontroller devices functions similarly. The 8XC196KB/KC/KD devices have eight analog inputs and the 8XC196NT has four analog inputs. The 8XC196KB devices allow only 10-bit conversion, the 8XC196KC/KD devices allow 8-bit or 10-bit conversion, and the 8XC196NT devices allow 8-bit or 10-bit conversion as well as threshold detection. Some of the registers are different to support these differences. Please see section 6.1 for more information on the register differences. The A/D converter has been removed from the 8XC196NP.

A new feature on the 8XC196NT is A/D Offset Compensation. The AD__TEST register enables conversions on ANGND and V_{REF} and specifies adjustments for DC offset errors. Its functions allow the user to perform two conversions, one on ANGND and one on V_{REF}. With these results, a software routine can calculate the offset and gain errors. This feature can reduce or eliminate off-chip compensation hardware.

In addition to 8-bit and 10-bit normal modes, the 8XC196NT also has high and low threshold-detect modes. In threshold-detection mode, the high byte of the AD__RESULT register is written to specify a threshold value. This selects a reference voltage, which is compared with the value of an analog input pin. When the voltage on the analog input pin crosses the threshold value, the A/D Complete interrupt flag is set.

An A/D conversion can be started in different manners. Using the HSO or the EPA is one method that can be used for starting an A/D conversion. On the 8XC196KB/KC/KD, an A/D conversion can be started with a CAM entry having an 0FH in the first four bits of the HSO__COMMAND register. On the 8XC196NT, an A/D conversion can be started with an EPA compare event. To do this, a 1 should be written in bit 2 of the EPAx__CON register.

The AD__TIME register is written with the sample and conversion times to be used for the conversion. The 8XC196NT always uses this register. The 8XC196KC/KD only uses the AD__TIME register for the sample and conversion times if the 8XC196KB-compatible mode is not used. If using the 8XC196KB-compatible mode, the conversion time is determined by the IOC2 register.

Example 8.4: Initialize the A/D Converter for a 10-Bit Conversion on Channel 4. The A/D conversion is initiated by the HSO on the 8XC196KC/KD and by the EPA on the 8XC196NT.

8XC196KC/KD:

```
init_atod_converter:
 ldb  WSR, #00h
 ldb  IOC2, #08h          ;setting bit 3 determines that the A/D conversion
                          ;times are controlled by the AD_TIME register.
                          ;This is not done on the 8XC196NT since the A/D
                          ;conversion times are always controlled by the
                          ;AD_TIME register.
 ldb  WSR, #01h
 ldb  AD_TIME, #0ffh      ;The A/D Time register programs the sample time
                          ;and convert time for the A/D converter.
 ldb  WSR, #00h
 ldb  AD_COMMAND, #04h    ;bits 0-2 select the channel number for conversion
                          ;(channel 4 in this case).

init_hso0_cam:
 ldb  WSR, #00h
 ldb  HSO_COMMAND, #0fh   ;An 0fh in bits 0-3 determines that the event that
                          ;will occur within the HSO module at the time
                          ;specified in the HSO Time Register will be the
                          ;start of an A/D conversion.
 ld  HSO_TIME, #064h      ;The HSO Time Register specifies the time when an
                          ;HSO command is to occur.
```

8XC196NT:

```
init_atod_converter:
 ldb  WSR, #1fh           ;Select vertical window to access SFRs
 ldb  AD_TIME_1F, #0ffh   ;The AD_TIME register programs the sample time
                          ;and conversion time for the A/D converter.
 ldb  AD_TEST _1F, #00h   ;This register sets the offset compensation at 0.0V.
 ldb  AD_COMMAND_1F, #04h
                          ;A/D conversion set up for 10-bit conversion on
                          ;channel 4 to be initiated by the EPA.

init_timer1:
 ld  T1CONTROL_1F, #080h; Setting bit 8 enables the timer.

init_epa0:
 ld  EPA0_CON_1F, #044h   ;initialize EPA0 to operate in compare mode using
                          ;timer 1 as the reference timer to start an A/D
                          ;conversion.
 ld  EPA0_TIME_1f, #064h;The EPA Time Register specifies the time when an
                          ;EPA event is to occur.
```

Example 8.5: Detect when Channel 4 Reaches 3.0V. This example shows the code necessary for the 8XC196KC/KD and the threshold detection feature of the 8XC196NT.

8XC196KC/KD:

```
cseg at 2080h
init_atod_converter:
 ldb WSR, #00h
 ldb  IOC2, #08h          ;Setting bit 3 enables the AD_TIME Register
                          ;instead of the 80C196KB-compatible mode.
 ldb  WSR, #01h
 ldb  AD_TIME, #0ffh      ;Programs the sample time and convert time for the
                          ;A/D converter.
 ldb  INT_MASK, #02h      ;Setting bit 1 enables the A/D Conversion Complete
                          ;interrupt.
 ei                       ;globally enable interrupts.

do_ad_conversion:
 ldb  WSR, #00h
 ldb  AD_COMMAND, #01ch ;Selects an 8-bit conversion on channel 4 that starts
                          ;immediately.
 br   $                   ;wait for interrupt.
atod_interrupt:           ;a software routine is required to check to see if the
                          ;threshold was met. This software routine is not
                          ;necessary on the 8XC196NT with the addition of
                          ;the threshold-detect mode.
 pusha
 clrb wsr
 ldb  tmpreg, AD_RESULT+1
 cmpb  tmpreg, #99h       ;subract #99h (value for 3V) from ad_result.
 jh   threshold_detected;if the A/D result is greater than 3V, jump to
                          ;threshold_detect routine.
no_threshold_detected:
 br   $                   ;loop here if threshold not detected.
threshold_detected:
 br   $                   ;loop here if threshold detected.

cseg at 200ah
atod_vector:
dcw atod_interrupt
```

Example 8.5: Detect when Channel 4 Reaches 3.0V. This example shows the code necessary for the 8XC196KC/KD and the threshold detection feature of the 8XC196NT. (Continued)

8XC196NT:

cseg at 0ff2080h

```
init_atod_converter:
 ldb  WSR, #1fh          ;Select vertical window to access SFRs.
 ldb  AD_TIME_1F, #0ffh  ;Programs the sample time and conversion time for
                         ;the A/D converter.
 ld AD_RESULT_1F, #09904h
                         ;In Threshold-Detection Mode, these bits are
                         ;written to specify a threshold value. This selects
                         ;a reference voltage, which is compared with the
                         ;value of an analog input pin. A value of 09904h
                         ;sets a reference voltage of 3V on channel 4.
ldb  INT_MASK_1F, #020h ;enables A/D interrupt bit.
ei                       ;globally enable interrupts.
ldb  AD_COMMAND_1F, #02ch
                         ;Programs the A/D to perform threshold detection
                         ;of a high voltage on A/D channel 4. The A/D
                         ;conversion will be started immediately.
br   $                   ;loop until threshold is met.

                         ; The atod_interrupt routine will be vectored to if
                         ;interrupts are enabled and a threshold has been
                         ;detected.
```

8.5 Pulse Width Modulator

The Pulse Width Modulator (PWM) is available on most MCS 96 devices. The 8XC196KB has one module and the 8XC196KC/KD and 8XC196NP have three modules. The PWM on the 8XC196NT was removed, but the EPA can be used to get a similar function. The PWM outputs a variable-duty-cycle pulse at a fixed frequency. The hardware for the PWM is identical on all of the devices, but there are a few differences in the registers that control how the PWM operates.

The PWM module provides two selectable PWM output frequencies for a specified XTAL1 frequency. The output frequency is determined by enabling or disabling the clock prescaler (Fosc/1024 and Fosc/512, respectively). The 8XC196KB/KC/KD clock prescaler is enabled by setting bit 2 of the IOC2 register. The 8XC196NP clock prescaler is enabled by setting bit 0 of the CON_REG0 register, which currently has only one bit—SLOW_PWM.

Each PWM output is multiplexed with a port pin. For the 8XC196KB/KC/KD, PWM0 is enabled by setting bit 0 of IOC1. PWM1 and PWM2 are enabled by setting bits 2 and 3 of IOC3, respectively for the 8XC196KC/KD. The 8XC196KB does not have an IOC3 register, so only PWM0 can be used. For the 8XC196NP, PWM0, PWM1, and PWM2 are enabled by setting bits 0,1, and 2 of the P4_MODE register.

Example 8.6: Initialize PWM1 for a PWM Output with a Duty Cycle of 75%. The clock prescaler is set to divide by 2.

8XC196KB/KC/KD:

```
cseg at 2080h
 ldb  WSR, #00h
 ldb  IOC2, #04h          ;Setting bit 2 enables the clock prescaler.
 ldb  WSR, #01h
 ldb  PWM1_CONTROL, #0c0h
                          ;PWM duty cycle = 75.00 %.
 ldb  IOC3, #04h          ;Enable PWM1 output.
 br   $
```

8XC196NP:

```
cseg at 0ff2080h
 ldb  WSR, #1fh           ;Select vertical window to access SFRs.
 ldb  CON_REG0_1F,#0ffh   ;Enables the clock prescaler for the three Pulse
                          ;Width Modulators (PWM0-PWM2).
 ldb  PWM1_CONTROL_1F, #0C0h
                          ;PWM duty cycle = 75.00 %.
 andb  P4_DIR_1F, #0fdh   ;Enables PWM pin as output.
 orb  P4_MODE_1F, #2      ;Enables PWM output as the SFR function instead
                          ;of as a standard I/O.
 br   $
```

9.0 NEW INSTRUCTIONS TO SUPPORT 1 MBYTE ADDRESSABILITY

This section contains a summary of the eight additional instructions to support the extended-addressing capability of the 8XC196Nx devices. These instructions have been added to enable code execution and data access anywhere in the 1 Mbyte address space. For detailed descriptions of these instructions, please see Appendix A in the 8XC196NT and 8XC196NP Microcontroller User's Manuals.

EBMOVI EXTENDED INTERRUPTABLE BLOCK MOVE. Moves a block of word data from one memory location to another. This instruction allows you to move blocks of up to 64K words between any two locations in the address space. It uses two 24-bit autoincrementing pointers and a 16-bit counter.

EBR EXTENDED BRANCH. This instruction is an unconditional indirect jump to anywhere in the address space. It functions only in extended addressing mode.

ECALL EXTENDED CALL. This instruction is an unconditional relative call to anywhere in the address space. It functions only in extended addressing mode. Note: In 1 Mbyte mode, ECALL, LCALL, and SCALL always push two words onto the stack; therefore, a RET must always pop two words from the stack. Because of the extra push/pop operation, interrupts and subroutine execution take slightly longer in 1 Mbyte mode than in 64 Kbyte mode.

EJMP EXTENDED JUMP. This instruction is an unconditional relative jump to anywhere in the address space. It functions only in extended addressing mode.

ELD EXTENDED LOAD WORD. Loads the value of the source (rightmost) word operand into the destination (leftmost) operand. This instruction allows you to move data from anywhere in the address space into the lower register file. It operates in extended-indirect, extended-indirect with autoincrement, and extended-indexed modes.

ELDB EXTENDED LOAD BYTE. Loads the value of the source (rightmost) byte operand into the destination (leftmost) operand. This instruction allows you to move data from anywhere in the address space into the lower register file. It operates in extended-indirect, extended-indirect with autoincrement, and extended-indexed modes.

EST EXTENDED STORE WORD. Stores the value of the source (leftmost) word operand into the destination (rightmost) operand. This instruction allows you to move data from the lower register file to anywhere in the address space. It operates in extended-indirect, extended-indirect with autoincrement, and extended-indexed modes.

ESTB EXTENDED STORE BYTE. Stores the value of the source (leftmost) byte operand into the destination (rightmost) operand. This instruction allows you to move data from the lower register file to anywhere in the address space. It operates in extended-indirect, extended-indirect with autoincrement, and extended-indexed modes.

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