i960® HA/HD/HT Superscalar Microprocessors

PRODUCT HIGHLIGHTS

■ **Superscalar RISC core**

■ **16 Kbyte four-way set associative instruction cache**

■ **8 Kbyte four-way set associative data cache**

■ **2 Kbyte on-chip data RAM**

■ **On-chip high-speed interrupt controller**

■ **Processor runs at 1x, 2x, or 3x external clock speed**

■ **Two 32-bit timers**

■ **Parity generation and checking**

■ **Guarded memory unit (GMU)**

■ **Object-code compatible with i960 CA/CF processor family**

■ **3.3 V supply, 5 V tolerant I/O**

■ **Socket compatible with i960 CA/CF processors[2]**

DESCRIPTION

The i960® HA, i960 HD, and i960 HT processors provide solutions for designers needing to increase performance while containing their total embedded system cost. The i960 Hx processor series has the highest performance of the i960 architecture.

The three versions are differentiated by the relationship of the core clock speed to the external bus speed. The i960 HA processor core speed is equal to the external bus speed, the i960 HD processor core speed is double that of the external bus speed, and the i960 HT processor is triple that of the external bus speed.

The features of the processor were selected with the assistance of customer input and simulation tools. The result is a superscalar processor that can execute up to three instructions per core clock and not be starved by a slow external system.

On-chip memory has been substantially increased, resulting in an increased hit-rate and reduced accesses to the external bus. The instruction cache for the i960 Hx processor series is 16 Kbytes, 4-way set associative. Critical code or interrupt routines may be locked into the cache for increased performance and decreased latency. The data cache is 8 Kbytes, 4-way set associative. Also on-chip is a 2 Kbyte data RAM which can be used for permanent storage of critical variables or interrupt vectors, further enhancing performance.
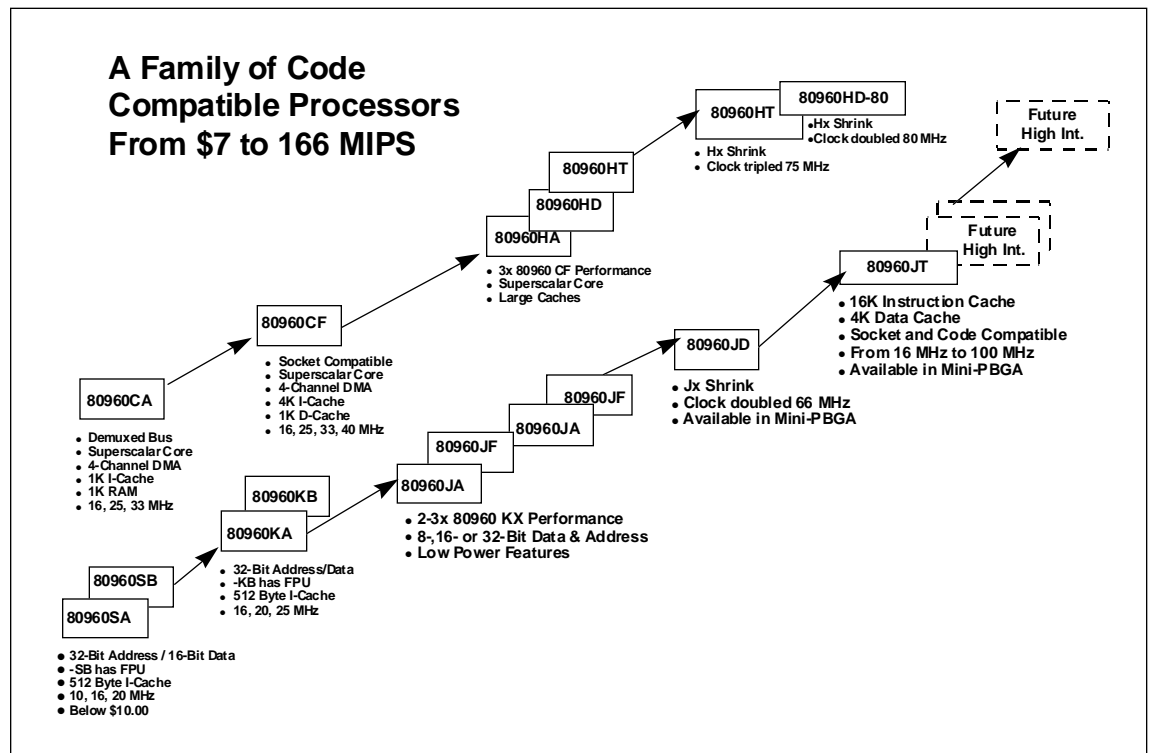
The i960 Hx processor series is object-code compatible with all i960 processor family members. This enables quick migration of code, reduced time-to-market, and use of existing development tool knowledge.

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Providing 166 MIPS, the i960® HD-80 MHz processor significantly increases the performance level previously available from the i960 architecture. Because the i960 HT processor runs at triple the external bus, the 75 MHz version connects to a low-cost 25 MHz external bus. This simplifies the design and lowers the total system cost.

Of course, not all embedded applications require such high performance. For that reason the product offering from the i960 Hx processors will start with the i960 HA 25 MHz processor, providing 50 MIPS. The series will meet several different price/performance points, adding to the product breadth of the i960 architecture. This increases the advantages for manufacturers to standardize around this popular family.

The i960 Hx processor series is 100% pin compatible and supported by an array of development tools, allowing for quick introduction of new products. The on-chip features have been designed specifically for the embedded market, providing fast interrupt responses, reduced access to external memory, and integrated timers. To learn more about the i960 HA, HD, or HT processors, please contact your local sales representative or call
1-800-628-8686.

Processor	External Bus Speed (MHz)	Core Bus Speed (MHz)	Peak MIPS	Packages
i960® HA processors	25, 33, 40	25, 33, 40	80	A, FC
i960® HD processors	16, 25, 33, 40	32, 50, 66, 80	166	A, FC
i960® HT processors	20, 25	60, 75	166	A, FC

A Family of Code Compatible Processors From $7 to 166 MIPS

Room to Grow: i960® Microprocessor Roadmap

Features	Benefits
Ease of Design	
Object code-compatible with all members of i960® CA/CF processor family	Utilize existing knowledge and code
Excellent development tools from over 70 vendors	Design with familiar tools
One PGA socket may be designed to accept i960® Cx and Hx processor[2]	Quick migration to higher performance with low design costs
Guarded Memory Unit	Code debug enhanced with protected segments
32-bit demultiplexed bus	Eliminates need for transceivers and latches
Performance	
1.28 Gbyte/sec internal bandwidth (128 bits/cycle @ 80 MHz)	Keep the processor fed with data and code from internal caches
Clock multiplied core	High performance processing with low-cost memory system
Large instruction cache on-chip 16 Kbyte four-way set associative 128-bit path to instruction sequencer Cache-lock, cache-off mode	Accelerates execution of standard software and time-critical interrupt routines
Large data cache on-chip 8 Kbyte four-way set associate slower memory 128 bits/clock on cache hit	Reduce external bus traffic, allowing for slower memory
Superscalar	Provides 166 native MIPS at 80 MHz
Profiling compiler	Reorganizes code for up to 30% performance improvement
Unaligned accesses handled in hardware, not software New CISC instructions 3.3 volt, 0.35 micron process	Reduced faults, increased useful code execution Reduce branches, code size by 10% Low power requirement
Integration	
Two 32-bit timers Optional byte parity Wait state generator Interrupt controller	High resolution event timing control All parity checking done on-chip Simplifies design for multiple memory types Provides prioritization of hardware and software interrupts with fast response times
JTAG - IEEE 1149.1 standard	Enables debug and test of products

[2] Requires board to be designed to specifications available from Intel.

i960® HA/ i960 HD/ i960 HT MICROPROCESSOR APPLICATION AREAS

Office Automation
Page printer controllers
Image scanners
X terminals
Database engines

Networking Applications
RAID
Telecommunications and data
  communications equipment
Router
HUB
Local area network (LAN) controllers and
  communications bridges (ATM, FDDI)
I/O processing for workstations/servers

Industrial Robotics
Automated vision systems
Factory process control
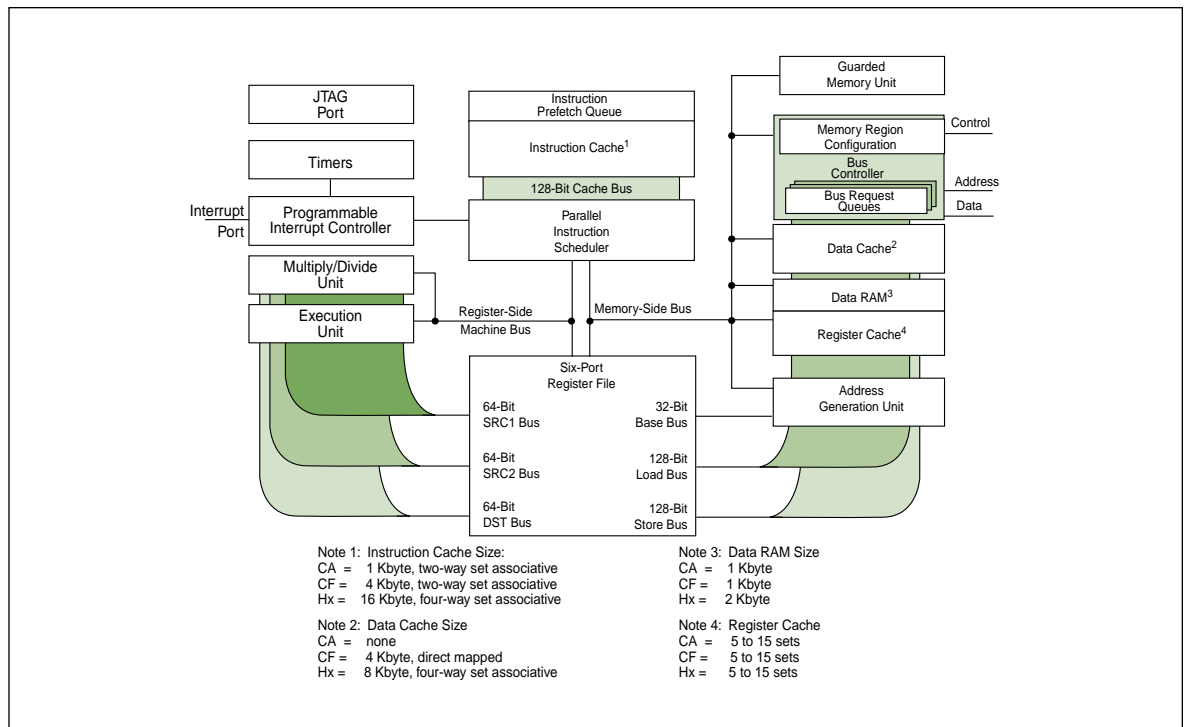
Medical Instrumentation
Real-time data collection and analyses
Monitoring systems
Ultrasound imaging displays

Avionics and Aerospace
Flight control equipment
Ground to air communication systems
Satellite navigation computers
Celestial telescope systems

Other
Arcade games
Global Positioning Systems
Theater Controls

Note 1: Instruction Cache Size:
CA = 1 Kbyte, two-way set associative
CF = 4 Kbyte, two-way set associative
Hx = 16 Kbyte, four-way set associative

Note 2: Data Cache Size
CA = none
CF = 4 Kbyte, direct mapped
Hx = 8 Kbyte, four-way set associative

Note 3: Data RAM Size
CA = 1 Kbyte
CF = 1 Kbyte
Hx = 2 Kbyte

Note 4: Register Cache
CA = 5 to 15 sets
CF = 5 to 15 sets
Hx = 5 to 15 sets

Intel's i960® Hx Microprocessor Block Diagram

Intel Reference Numbers	
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FaxBack System:	**1 (800) 525-3019 or (503) 264-6835**
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