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MCS®-96 A/D Converter
Quick Reference

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1.0 The MCS-96 A/D Converter

Analog inputs to the MCS-96 family are handled by the A/D converter system. As shown in Figure 1, the converter system has an 8 channel multiplexer, a sample and hold, and a 10-bit successive approximation A/D converter. Conversions can be performed on one of 8 channels, the inputs of which share pins with port 0.

There are various versions of the A/D converter, depending on the specific device type. The 8X9X family offers a 10-bit fixed conversion time. The 8XC196KB family offers a 10-bit conversion with either a fast or slow conversion time. The 8XC196KC family offers an 8- or 10-bit conversion with programmable sample and convert times. The 8XC196KR has all of the KC features, with the addition of offset correction and internal conversion of V_{ref} and ANGND. The 8XC196MC includes all of the KR features, and the multiplexer has been expanded to 13 analog input channels.

This chapter describes the basic operation and terminology of the A/D converter. The different devices control the A/D in different ways, but the principals of operation remain the same throughout.

1.1 A/D Conversion Process

The conversion process is initiated by an HSO or EPA command, or by writing a one to the GO Bit in the A/D Control Register. Either activity causes a start conversion signal to be sent to the A/D converter control logic.

Once the A/D unit receives a start conversion signal, there is a one state time delay before sampling (Sample Delay) while the successive approximation register is reset and the proper multiplexer channel is selected. After the sample delay, the multiplexer output is connected to the sample capacitor and remains connected for the sample time. After the "sample window" closes, the input to the sample capacitor is disconnected from the multiplexer so that changes on the input pin will not alter the stored charge while the conversion is in progress. The comparator is then auto-zeroed and the conversion begins. The sample delay and sample time uncertainties are each approximately ± 50 ns, independent of clock speed.

To perform the actual analog-to-digital conversion the MCS-96 implements a successive approximation algorithm. The converter hardware consists of a 256-resistor ladder, a comparator, coupling capacitors and a 10-bit successive approximation register (SAR) with logic that guides the process. The resistor ladder provides 20 mV steps (V_{REF} = 5.12V), while capacitive coupling creates 5 mV steps within the 20 mV ladder voltages. Therefore, 1024 internal reference voltages are available for comparison against the analog input to generate a 10-bit conversion result.

A successive approximation conversion is performed by comparing a sequence of reference voltages, to the analog input, in a binary search for the reference voltage that most closely matches the input. The $^1\!/_2$ full scale reference voltage is the first tested. This corresponds to a 10-bit result where the most significant bit is zero, and all other bits are ones (0111.1111.11b). If the analog input was less than the test voltage, bit 10 of the SAR is left a zero, and a new test voltage of $^1\!/_4$ full scale (0011.1111.11b) is tried. If this test voltage was lower than the analog input, bit 9 of the SAR is set and bit 8 is cleared for the next test (0101.1111.11b). This binary search continues until 10 tests have occurred, at which time the valid 10-bit conversion result resides in the SAR where it can be read by software.

1.2 A/D Interface Suggestions

The external interface circuitry to an analog input is highly dependent upon the application, and can impact converter characteristics. In the external circuit's design, important factors such as input pin leakage, sample capacitor size and multiplexer series resistance from the input pin to the sample capacitor must be considered.

These factors are idealized in Figure 1. The external input circuit must be able to charge a sample capacitor (C_S) through a series resistance (R_I) to an accurate voltage given a DC leakage (I_L). Typically C_S is around 2 pF, R_I is around 5 KΩ and I_L is specified as 3 μA. In determining the necessary source impedance R_S, the value of V_{BIAS} is not important.
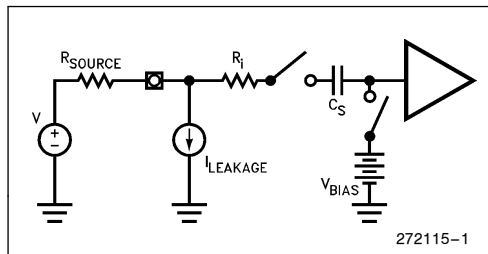

Figure 1. Idealized A/D Sampling Circuitry

External circuits with source impedances of 1 KΩ or less will be able to maintain an input voltage within a tolerance of about ± 0.61 LSB (1.0 KΩ $\times$ 3.0 μA = 3.0 mV) given the DC leakage. Source impedances above 2 KΩ can result in an external error of at least one LSB due to the voltage drop caused by the 3 μA leakage. In addition, source impedances above 25 KΩ may degrade converter accuracy as a result of the internal sample capacitor not being fully charged during the sample window.

If large source impedances degrade converter accuracy because the sample capacitor is not charged during the sample time, an external capacitor connected to the pin compensates for this. Since the sample capacitor is 2 pF, a 0.005 μF capacitor (2048 * 2 pF) will charge the sample capacitor to an accurate input voltage of ± 0.5 LSB. An external capacitor does not compensate for the voltage drop across the source resistance, but charges the sample capacitor fully during the sample time.

Placing an external capacitor on each analog input will also reduce the sensitivity to noise, as the capacitor combines with series resistance in the external circuit to form a low-pass filter. In practice, one should include a small series resistance prior to the external capacitor on the analog input pin and choose the largest capacitor value practical, given the frequency of the signal being converted. This provides a low-pass filter on the input, while the resistor will also limit input current during over-voltage conditions.

Figure 2 shows a simple analog interface circuit based upon the discussion above. The circuit in the figure also provides limited protection against over-voltage conditions on the analog input. Should the input voltage inappropriately drop significantly below ground, diode D2 will forward bias at about 0.8 DCV. Since the specification of the pin on most devices has an absolute maximum low voltage of -0.3V, this will leave about 0.5V across the 270Ω resistor, or about 2 mA of current. This should limit the current to a safe amount. Note that if any input pins are driven much beyond V_{REF} or below ANGND, the accuracy of all analog input channels may be adversely affected. This is because the input protection circuit will start to conduct, thus injecting current into the internal reference circuitry and upsetting the reference voltage. Refer to the data sheet for exact device specifications.

However, before any circuit is used in an actual application, it should be thoroughly analyzed for applicability to the specific problem at hand.
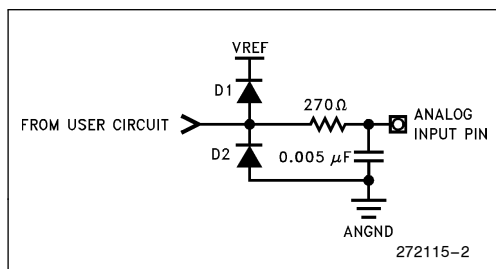

Figure 2. Suggested A/D Input Circuit

ANALOG REFERENCES

Reference supply levels and noise strongly influence the absolute accuracy of the conversion. For this reason, it is recommended that the ANGND pin be tied to the V_{SS} pins close to the device. Bypass capacitors should also be used between V_{REF} and ANGND. ANGND should be within about a tenth of a volt of V_{SS}. V_{REF} should be well regulated and used only for the A/D converter. The V_{REF} supply needs to be able to source around 5 mA.

Note that if only ratiometric information is desired, V_{REF} can be connected to V_{CC}. In addition, V_{REF} and ANGND must be connected even if the A/D converter is not being used. Remember that Port 0 receives its power from the V_{REF} and ANGND pins even when it is used as digital I/O.

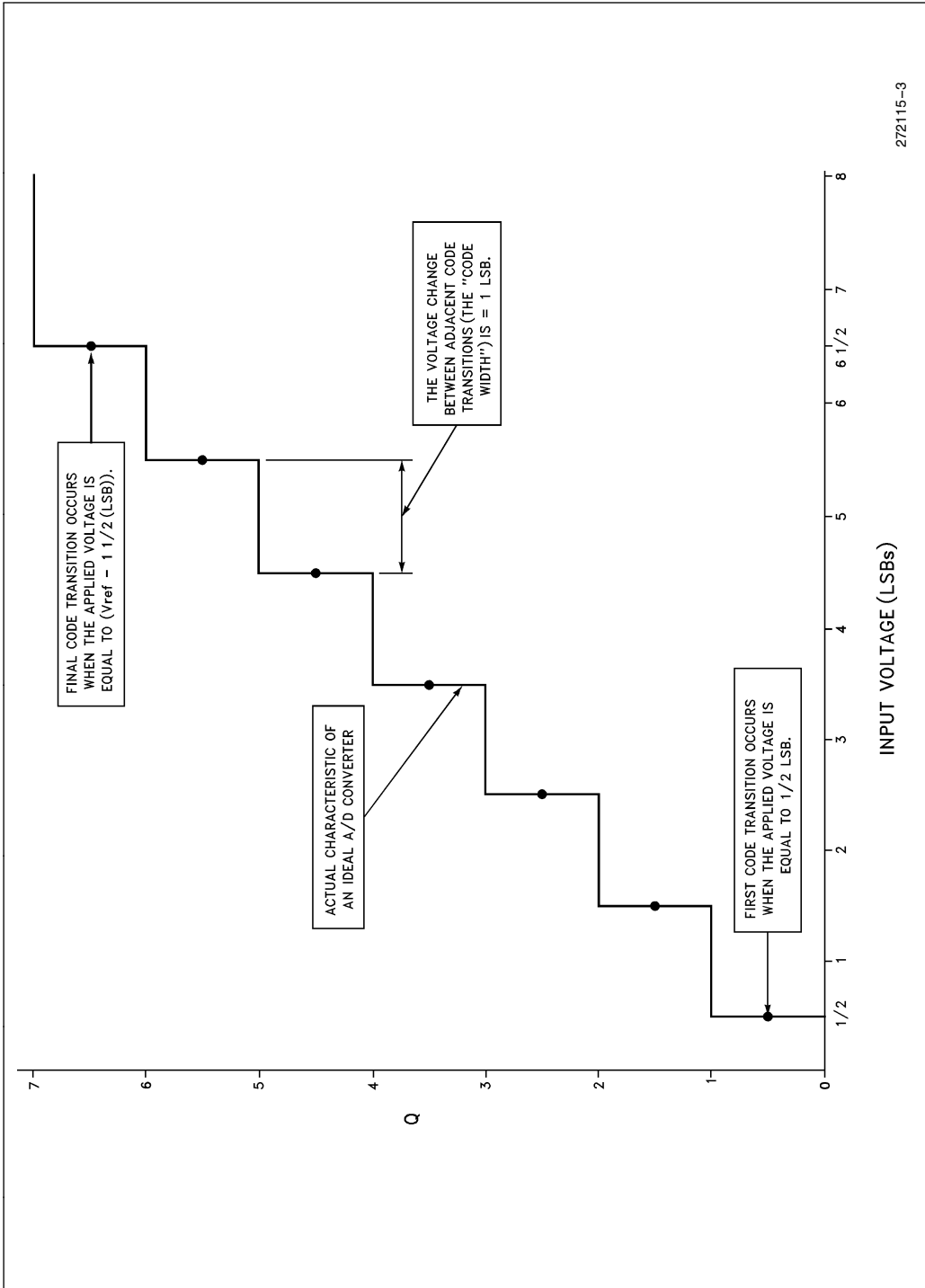## 1.3 The A/D Transfer Function

The conversion result is a 8- or 10-bit ratiometric representation of the input voltage, so the numerical value obtained from the conversion will be:

INT [255 $\times$ (V_{IN} $-$ ANGND)/(V_{REF} $-$ ANGND)] or

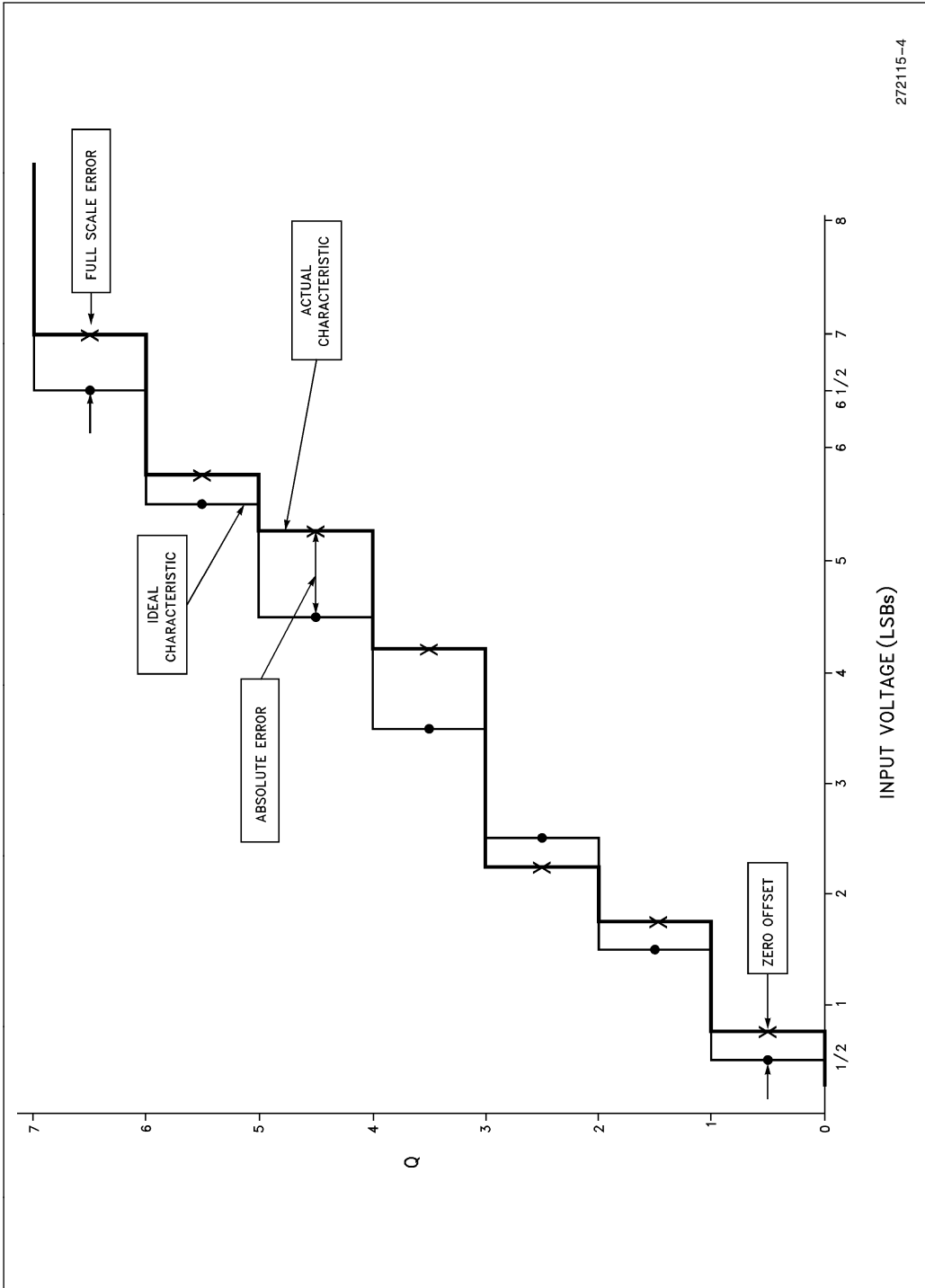INT [1023 $\times$ (V_{IN} $-$ ANGND)/(V_{REF} $-$ ANGND)]

This produces a stair-stepped transfer function when the output code is plotted versus input voltage (see Figure 3). The resulting digital codes can be taken as simple ratiometric information, or they provide information about absolute voltages or relative voltage changes on the inputs. The more demanding the application is on the A/D converter, the more important it is to fully understand the converter's operation. For simple applications, knowing the absolute error of the converter is sufficient. However, closing a servo-loop with analog inputs necessitates a detailed understanding of an A/D converter's operation and errors.

The errors inherent in an analog-to-digital conversion process are many: quantizing error, zero offset, full-scale error, differential non-linearity and non-linearity. These are "transfer function" errors related to the A/D converter. In addition, converter temperature drift, V_{CC} rejection, sample-hold feedthrough, multiplexer off-isolation, channel-to-channel matching and random noise should be considered. Fortunately, one "Absolute Error" specification is available which describes the sum total of all deviations between the actual conversion process and an ideal converter. However, the various sub-components of error are important in many applications. These error components are described in the text below where ideal and actual converters are compared.

FINAL CODE TRANSITION OCCURS WHEN THE APPLIED VOLTAGE IS EQUAL TO (Vref − 1 1/2 (LSB)).

THE VOLTAGE CHANGE BETWEEN ADJACENT CODE TRANSITIONS (THE "CODE WIDTH") IS = 1 LSB.

ACTUAL CHARACTERISTIC OF AN IDEAL A/D CONVERTER

FIRST CODE TRANSITION OCCURS WHEN THE APPLIED VOLTAGE IS EQUAL TO 1/2 LSB.
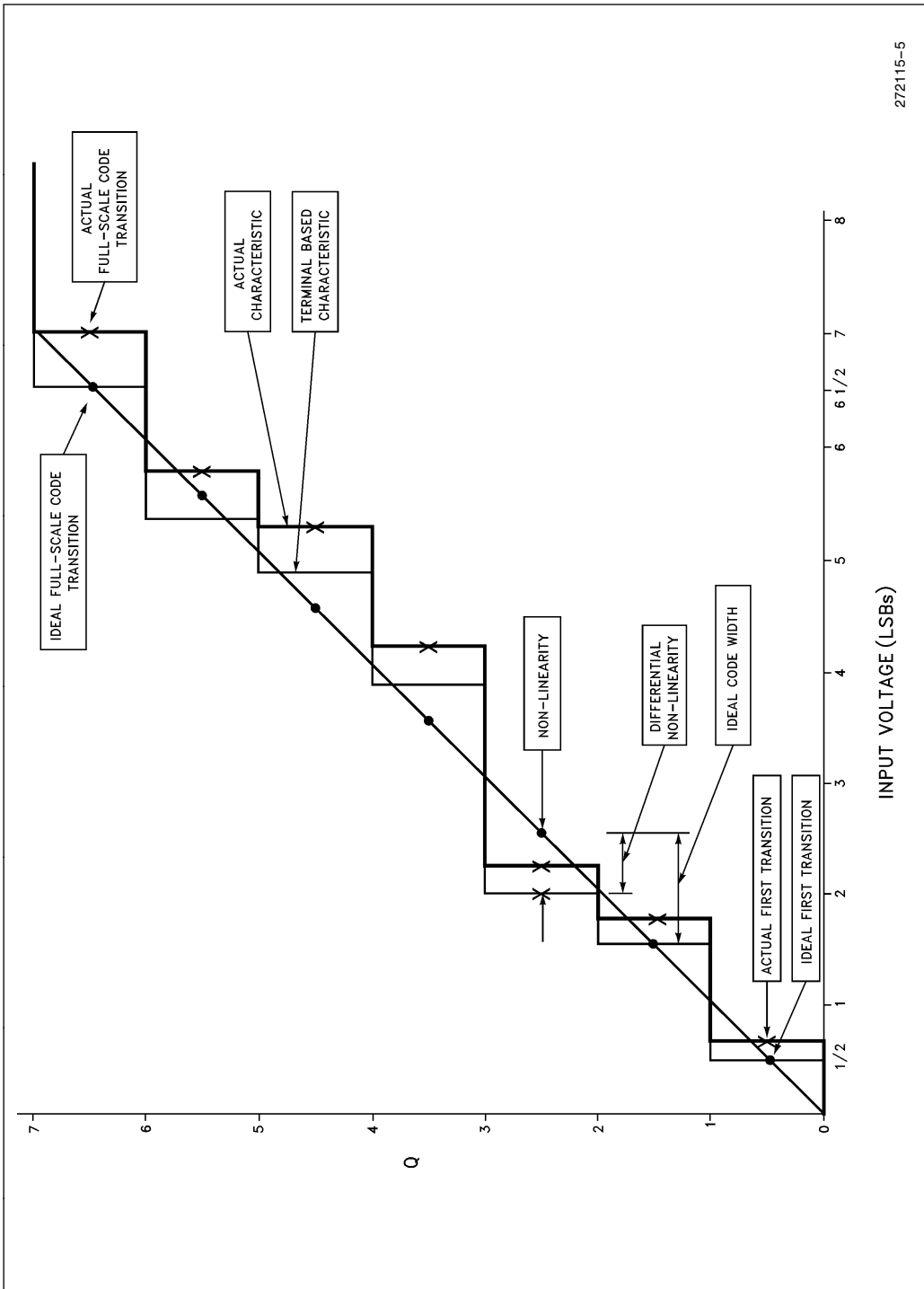
INPUT VOLTAGE (LSBs)

272115−3

Figure 3. Ideal A/D Characteristic

272115–4

Figure 4. Actual and Ideal Characteristics

Figure 5. Terminal Based Characteristic

An unavoidable error simply results from the conversion of a continuous voltage to an integer digital representation. This error is called quantizing error, and is always ±0.5 LSB. Quantizing error is the only error seen in a perfect A/D converter, and is obviously present in actual converters. Figure 3 shows the transfer function for an ideal 3-bit A/D converter (i.e., the Ideal Characteristic).

Note that in Figure 3 the Ideal Characteristic possesses unique qualities: its first code transition occurs when the input voltage is 0.5 LSB; its full-scale code transition occurs when the input voltage equals the full-scale reference minus 1.5 LSB; and its code widths are all exactly one LSB. These qualities result in a digitization without offset, full-scale or linearity errors. In other words, a perfect conversion.

Figure 4 shows an Actual Characteristic of a hypothetical 3-bit converter, which is not perfect. When the Ideal Characteristic is overlaid with the imperfect characteristic, the actual converter is seen to exhibit errors in the location of the first and final code transitions and code widths. The deviation of the first code transition from ideal is called "zero offset", and the deviation of the final code transition from ideal is "full-scale error". The deviation of the code widths from ideal causes two types of errors. Differential Non-Linearity and Non-Linearity. Differential Non-Linearity is a local linearity error measurement, whereas Non-Linearity is an overall linearity error measure.

Differential Non-Linearity is the degree to which actual code widths differ from the ideal one LSB width. It gives the user a measure of how much the input voltage may have changed in order to produce a one count change in the conversion result. Non-Linearity is the worst case deviation of code transitions from the corresponding code transitions of the Ideal Characteristic. Non-Linearity describes how much Differential Non-Linearities could add up to produce an overall maximum departure from a linear characteristic. If the Differential Non-Linearity errors are too large, it is possible for an A/D converter to miss codes or exhibit non-monotonicity. Neither behavior is desirable in a closed-loop system. A converter has no missed codes if there exists for each output code a unique input voltage range that produces that code only. A converter is monotonic if every subsequent code change represents an input voltage change in the same direction.

Differential Non-Linearity and Non-Linearity are quantified by measuring the Terminal Based Linearity Errors. A Terminal Based Characteristic results when an Actual Characteristic is shifted and rotated to eliminate zero offset and full-scale error (see Figure 5). The Terminal Based Characteristic is similar to the Actual Characteristic that would be seen if zero offset and full-scale error were externally trimmed away. In practice, this is done by using input circuits which include gain

and offset trimming. In addition, V_{REF} could also be closely regulated and trimmed within the specified range to affect full-scale error.

Other factors that affect a real A/D Converter system include sensitivity to temperature, failure to completely reject all unwanted signals, multiplexer channel dissimilarities and random noise. Fortunately these effects are small.

Temperature sensitivities are described by the rate at which typical specifications change with a change in temperature.

Undesired signals come from three main sources. First, noise on $V_{CC} - V_{CC}$ Rejection. Second, input signal changes on the channel being converted after the sample window has closed – Feedthrough. Third, signals applied to channels not selected by the multiplexer – Off-Isolation.

Finally, multiplexer on-channel resistances differ slightly from one channel to the next causing Channel-to-Channel Matching errors, and random noise in general results in Repeatability errors.

1.4 A/D Glossary of Terms

Figures 3, 4 and 5 display many of these terms. Refer to AP-406 'MCS-96 Analog Acquisition Primer' for additional information on the A/D terms.

ABSOLUTE ERROR – The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

ACTUAL CHARACTERISTIC – The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An Actual Characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversion under the same conditions.

BREAK-BEFORE-MAKE – The property of a multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected. (e.g., the converter will not short inputs together.)

CHANNEL-TO-CHANNEL MATCHING – The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

CHARACTERISTIC – A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

CODE–The digital value output by the converter.

CODE CENTER–The voltage corresponding to the midpoint between two adjacent code transitions.

CODE TRANSITION–The point at which the converter changes from an output code of Q, to a code of Q+1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

CODE WIDTH–The voltage corresponding to the difference between two adjacent code transitions.

CROSSTALK–See "Off-Isolation".

DC INPUT LEAKAGE–Leakage current to ground from an analog input pin.

DIFFERENTIAL NON-LINEARITY–The difference between the ideal and actual code widths of the terminal based characteristic of a converter.

FEEDTHROUGH–Attenuation of a voltage applied on the selected channel of the A/D converter after the sample window closes.

FULL SCALE ERROR–The difference between the expected and actual input voltage corresponding to the full scale code transition.

IDEAL CHARACTERISTIC–A characteristic with its first code transition at $V_{IN} = 0.5$ LSB, its last code transition at $V_{IN} = (V_{REF} - 1.5$ LSB) and all code widths equal to one LSB.

INPUT RESISTANCE–The effective series resistance from the analog input pin to the sample capacitor.

LSB (LEAST SIGNIFICANT BIT)–The voltage value corresponding to the full scale voltage divided by 2^n, where n is the number of bits of resolution of the converter. For a 10-bit converter with a reference voltage of 5.12 volts, one LSB is 5.0 mV. Note that this is different than digital LSBs, since an uncertainty of two LSBs, when referring to an A/D converter, equals 10 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 20 mV.)

MONOTONIC–The property of successive approximation converters which guarantees that increasing input voltages produce adjacent codes of increasing value, and that decreasing input voltages produce adjacent codes of decreasing value.

NO MISSED CODES–For each and every output code, there exists a unique input voltage range which produces that code only.

NON-LINEARITY–The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristics.

OFF-ISOLATION–Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

REPEATABILITY–The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

RESOLUTION–The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

SAMPLE DELAY–The delay from receiving the start conversion signal to when the sample window opens.

SAMPLE DELAY UNCERTAINTY–The variation in the Sample Delay.

SAMPLE TIME–The time that the sample window is open.

SAMPLE TIME UNCERTAINTY–The variation in the sample time.

SAMPLE WINDOW–Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

SUCCESSIVE APPROXIMATION–An A/D conversion method which uses a binary search to arrive at the best digital representation of an analog input.

TEMPERATURE COEFFICIENTS–Change in the stated variable per degree centigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effects of temperature drift.

TERMINAL BASED CHARACTERISTIC–An Actual Characteristic which has been rotated and translated to remove zero offset and full-scale error.

V_{CC} REJECTION–Ratio of the change in the A/D characteristic to the change in V_{CC}.

ZERO OFFSET–The difference between the expected and actual input voltage corresponding to the first code transition.