

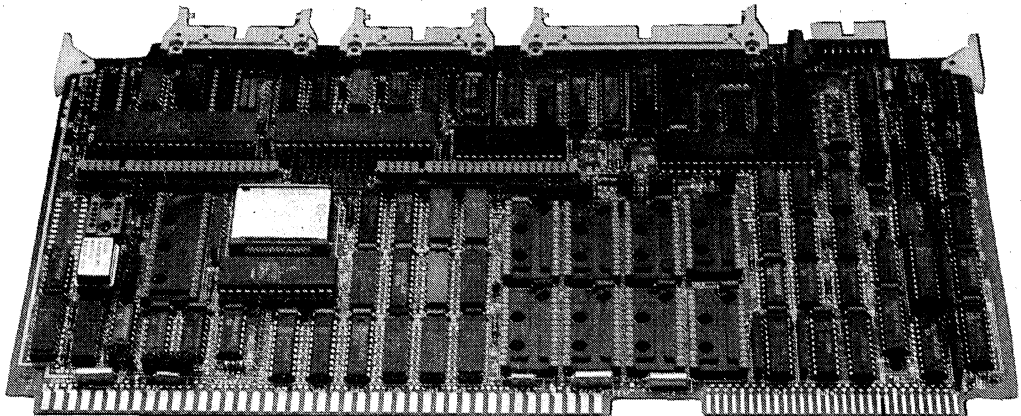


## iSBC® 186/03A SINGLE BOARD COMPUTER

- 8.0 MHz 80186 Microprocessor with Optional 8087 Numeric Data Processor
- Eight (Expandable to 12) JEDEC 28-Pin Sites
- Six Programmable Timers and 27 Levels of Vectored Interrupt Control
- MULTIBUS® Interface for System Expansion and Multimaster Configuration
- 24 Programmable I/O Lines Configurable as a SCSI Interface, Centronics Interface or General Purpose I/O
- Two iSBX™ Bus Interface Connectors for Low Cost I/O Expansion
- iLBX™ (Local Bus Extension) Interface for High-Speed Memory Expansion
- Two Programmable Serial Interfaces; One RS 232C, the Other RS 232C or RS 422 Compatible

The iSBC 186/03A Single Board Computer is a member of Intel's complete line of microcomputer modules and systems that take advantage of Intel's VLSI technology to provide economical, off-the-shelf, computer-based solutions for OEM applications. The board is a complete microcomputer system on a 7.05 x 12.0 inch printed circuit card. The CPU, system clock, memory, sockets, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board.

The iSBC 186/03A board incorporates the 80186 CPU and SCSI interface on one board. The extensive use of high integration VLSI has produced a high-performance single-board system. For large memory applications, the iLBX local bus expansion maintains this high performance.



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## OVERVIEW

### Operating Environment

The iSBC 186/03A single board computer features have been designed to meet the needs of numerous microcomputer applications. Typical applications include:

- Multiprocessing single board computer
- BITBUS master controller
- Stand-alone single board system

### MULTIPROCESSING SINGLE BOARD COMPUTER

High-performance systems often need to divide system functions among multiple processors. A multiprocessing single board computer distributes an applications processing load over multiple processors that communicate over a system bus. Since these applications use the system bus for inter-processor communication, it is required that each processor has local execution memory.

The iSBC 186/03A board supports loosely coupled multiprocessing (where each processor performs a specific function) through its MULTIBUS compatible architecture. The IEEE 796 system bus facilitates processor to processor communication, while the iLBX bus makes high-speed data and execution memory available to each CPU as shown in Figure 1. This architecture allows multiple processors to run in parallel enabling very high-performance applications.

### BITBUS™ MASTER CONTROLLER

The BITBUS interconnect environment is a high performance low-cost microcontroller interconnect technology for distributed control of intelligent industrial machines such as robots and process controllers. The BITBUS interconnect is a special purpose serial bus which is ideally suited for the fast transmission of short messages between the microcontroller nodes in a modularly distributed system.

The iSBC 186/03A board can be implemented as the MULTIBUS-based master controller CPU which monitors, processes and updates the control status of the distributed system. The iSBX 344 board is used to interface the iSBC 186/03A board to the BITBUS interconnect. Actual message transfer over the iSBX bus can be accomplished by either software polling by the CPU or by using the on-chip 80186 DMA hardware instead of the CPU. Using DMA, the CPU is only required to start the DMA process and then poll for the completion of the message transfer, thus dramatically improving the data transmission rate and master control processor efficiency. The maximum transfer rates over the iSBX bus for the iSBC 186/03A board are about 900 messages/second in polled mode and 2500 messages/second in DMA mode. An 8 MHz iSBC 186/03A board in DMA mode is 3 times as fast as a typical 5 MHz iSBC 86/30 board running in polled mode. The iSBC 186/03A board in DMA mode provides the highest performance/price solution for BITBUS message transmission out of all of Intel's complete line of 16-bit CPU modules.

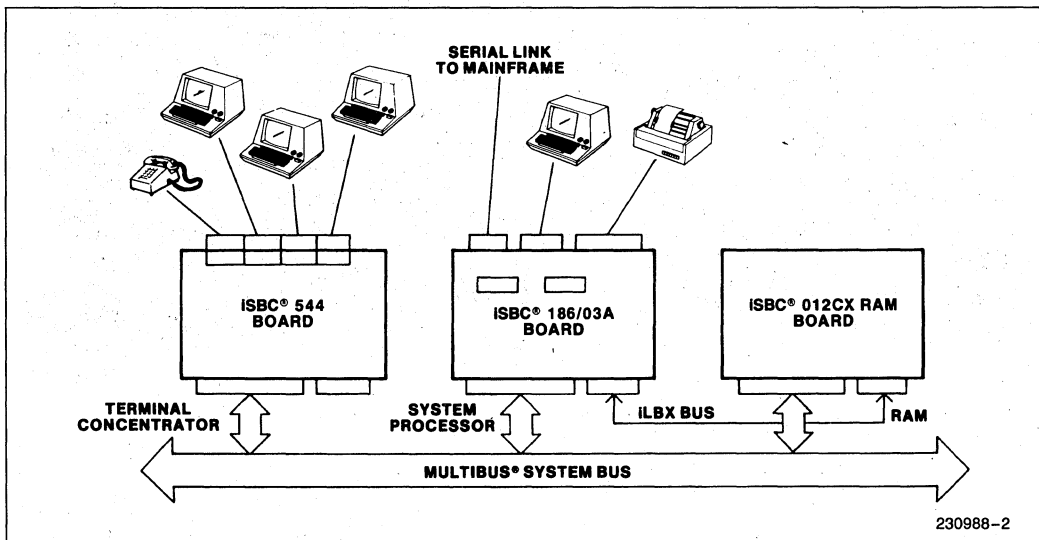


Figure 1. A Multiprocessing Single Board Computer Application

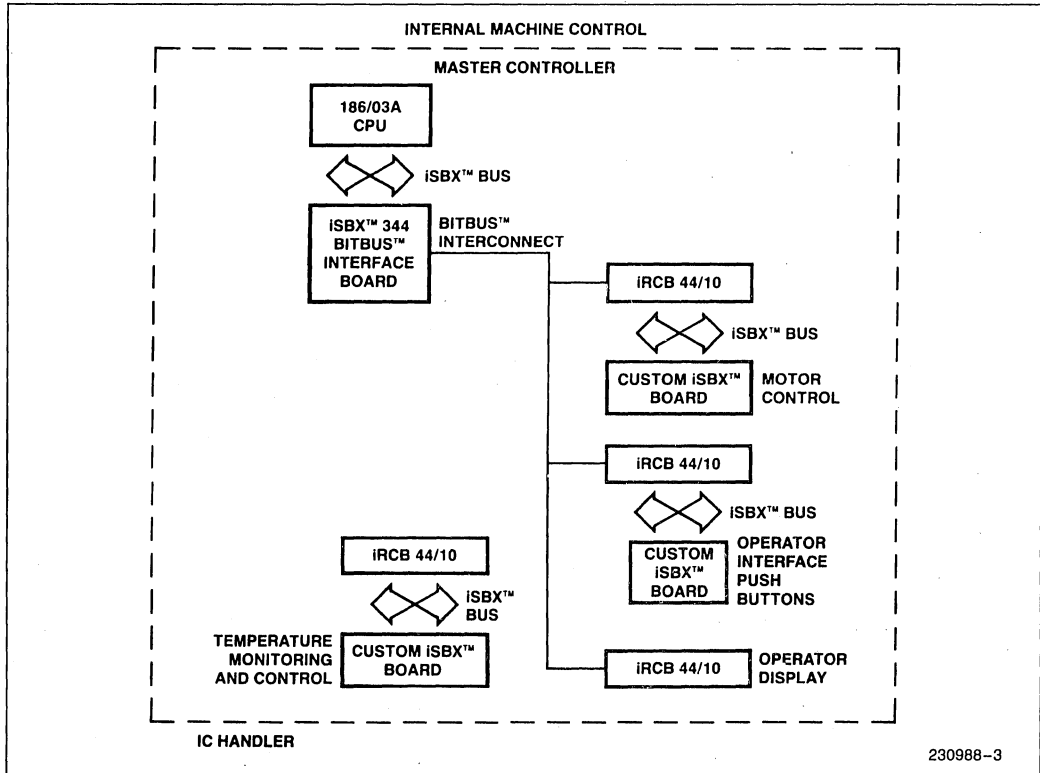


Figure 2. Sample iSBC® 186/03A BITBUS™ Master Application

### STAND-ALONE SINGLE BOARD SYSTEM

A stand-alone single board system is a complete computer system on one board. By reducing the system's board count, the single board system saves space, power, and ultimately, costs. The on-board resources need to be capable of performing all of the basic system functions. These applications typically require terminal support, peripheral control, local RAM and program execution. In previous generations of single board computers, these functions could only be obtained with multiple board solutions.

The iSBC 186/03A board integrates all the functions of a general purpose system (CPU, memory, I/O and peripheral control) onto one board. The iSBC 186/03A board can also be customized as a single board system by the selection of memory and iSBX I/O options. The board's 8 JEDEC 28-pin sockets can accommodate a wide variety of byte-wide memory devices. For example, four 27256 EPROMs and four 2186 IRAMs can be installed for a total of 128 KB of EPROM program storage and 32 KB of RAM data storage. In addition, Intel's JEDEC site compatible 27916 KEPR0M™ (Keyed Access EPROM) memory device may be configured for use on the

iSBC 186/03A board. The KEPR0M memory device employs a data protection mechanism which makes the memory array unreadable until unlocked by an authorized 64-bit "key". KEPR0Ms protect system software from unauthorized use. If more memory is needed, an optional iSBC 341 memory site expansion board can be added to provide an additional four JEDEC sites. Two iSBX MULTIMODULE™ boards can be added to the iSBC 186/03A board to customize the board's I/O capabilities. As shown in Figure 3, the iSBX connectors can support a single-board system with the analog input and output modules needed by machine or process control systems.

### FUNCTIONAL DESCRIPTION

#### Architecture

The iSBC 186/03A board is functionally partitioned into six major sections: central processor, memory, SCSI compatible parallel interface, serial I/O, interrupt control and MULTIBUS bus expansion. These areas are illustrated in Figure 4.

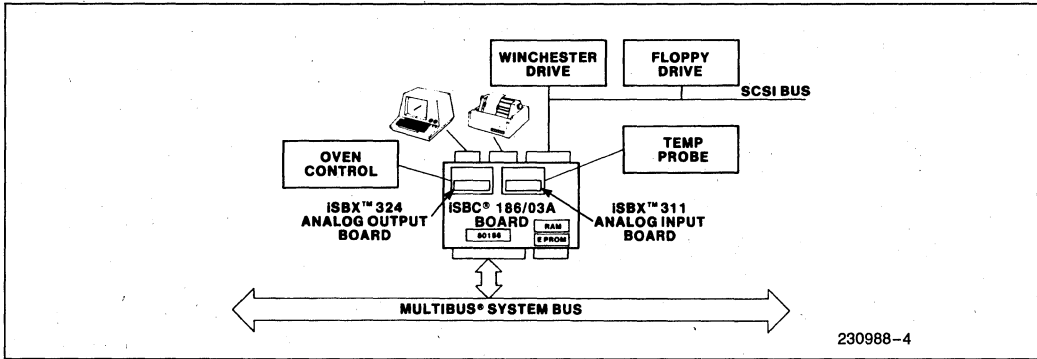


Figure 3. A Stand-Alone Single Board System Application

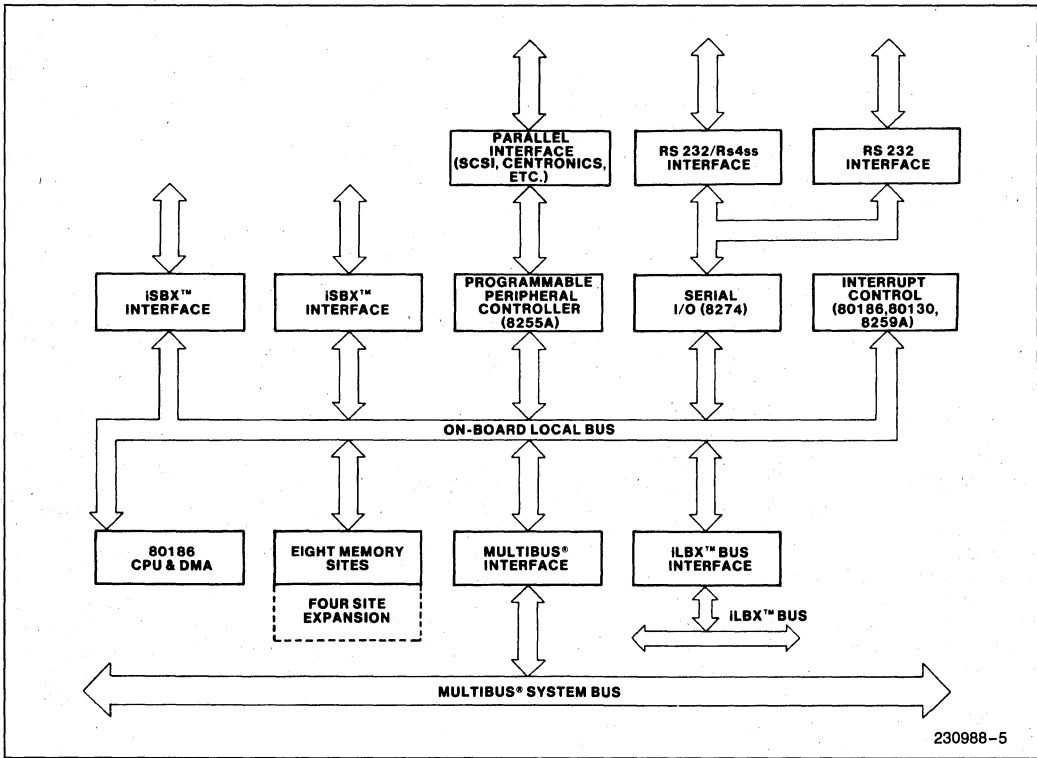


Figure 4. ISBC® 186/03A Board Block Diagram

## CENTRAL PROCESSOR

The 80186 component is a high-integration 16-bit microprocessor. It combines several of the most common system components onto a single chip (i.e. Direct Memory Access, Interval Timers, Clock Generator and Programmable Interrupt Controller). The 80186 instruction set is a superset of the 8086. It maintains object code compatibility while adding ten new instructions. Added instructions include: Block I/O, Enter and Leave subroutines, Push Immediate, Multiply Quick, Array Bounds Checking, Shift and Rotate by Immediate, and Pop and Push All.

Use of the 80130 component is limited to the 3 timers and 8 levels of interrupts available. Direct processor execution of the 16K bytes of iRMX 86 Operating System nucleus primitives is not supported.

An optional 8087 Numeric Data Processor may be installed by the user to dramatically improve the 186/03A board's numerical processing power. The interface between the 8087 and 80186 is provided by the factory-installed 82188 Integrated Bus Controller which completes the 80186 numeric data processing system. The 8087 Numeric Data Processor option adds 68 floating-point instructions and eight 80-bit floating point registers to the basic iSBC 186/03A board's programming capabilities. Depending on the application, the 8087 will increase the performance of floating point calculations by 50 to 100 times.

## TIMERS

The 80186 provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (two per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. As shipped on the iSBC 186/03A board, these two timers are connected to the serial interface, and provide baud rate generation. The third timer is not connected to any external pins, and is useful for real-time coding and time-delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source. The 80130 provides three more programmable timers. One is a factory default baud rate generator and outputs an 8254 compatible square wave that can be used as an alternate baud rate source to either serial channel. The 80130's second timer is used as a system timer. The third timer is reserved for use by the iRMX Operating System. The system software configures each timer independently to select the desired function. Available functions include: interrupt on terminal count, programmable one-shot, rate

generator, square-wave generator, software triggered strobe, hardware triggered strobe and event counter. The contents of each counter may be read at any time during system operation.

## MEMORY

There are eight JEDEC 28-pin memory sites on the iSBC 186/03A board providing flexible memory expansion. Four of these sites (EPROM sites) may be used for EPROM or E<sup>2</sup>PROM program storage, while the other four (RAM sites) may be used for static RAM or iRAM data storage or used as additional program storage. The eight sites can be extended to twelve by the addition of an iSBC 341 MULTIMODULE board. These additional sites will provide up to 64K bytes of RAM using 8K x 8 SRAM or iRAM devices. The EPROM sites (Bank B) are compatible with 8K x 8 (2764), 16K x 8 (27128A), 32K x 8 (27256), 64K x 8 (27512) as well as 2K x 8 (2817A) and 8K x 8 (2864) E<sup>2</sup>PROMs. The RAM sites (Bank A) are compatible with all byte-wide SRAM, iRAM or NVRAM devices. NVRAM usage requires additional circuitry in order to guarantee data retention. (Refer to AP-173 for further information.) Bank A can be reassigned to upper memory just below the assigned memory space for Bank B to support additional EPROM or E<sup>2</sup>PROMs.

Memory addressing for the JEDEC sites depends on the device type selected. The four EPROM sites are top justified in the 1 MB address space and must contain the power-on instructions. The device size determines the starting address of these devices. The four RAM sites are, by default, located starting at address 0. The addressing of these sites may be relocated to upper memory (immediately below the EPROM site addresses) in applications where these sites will contain additional program storage. The optional iSBC 341 MULTIMODULE sites are addressable immediately above the RAM site addresses.

Power-fail control and auxiliary power are provided for protection of the RAM sites when used with static RAM devices. A memory protect signal is provided through an auxiliary connector (J4) which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences. An auxiliary power bus is also provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

**SCSI PERIPHERAL INTERFACE**

The iSBC 186/03A board includes a parallel peripheral interface that consists of three 8-bit parallel ports. As shipped, these ports are configured for general purpose I/O. The parallel interface may be reconfigured to be compatible with the SCSI disk interface by adding two user-supplied and programmed Programmable Array Logic (PAL) devices, moving jumpers and installing a user-supplied 74LS640-1 device. Alternatively, the parallel interface may be reconfigured as a DMA controlled Centronics compatible line printer interface by adding one PAL and changing jumpers. Refer to the iSBC 186/03A Hardware Reference Manual for PAL equations and a detailed implementation procedure.

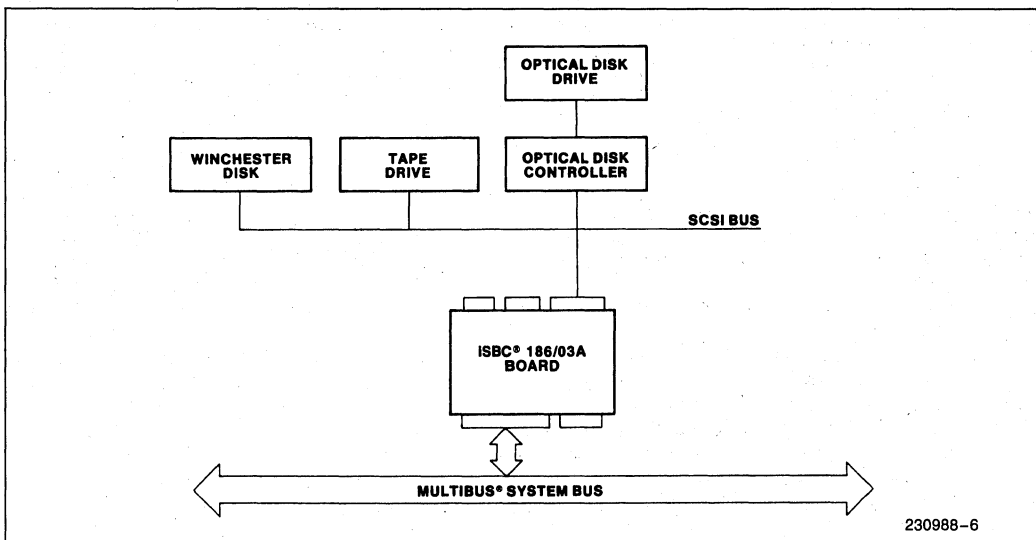
The SCSI (Small Computer Systems Interface) interface allows up to 8 mass storage peripherals such as Winchester disk drives, floppy disk drives and tape drives to be connected directly to the iSBC 186/03A board. Intel's iSBC 186/03A board utilizes a single initiator, single target implementation of the SCSI bus specification. Bus arbitration and deselect/reselect SCSI features are not supported. Single host, multiple target configurations can be used. However, the iSBC 186/03A board will stay connected to one target until the transaction is completed before switching to the second target. The iSBC 186/03A board's SCSI interface implements a 5 megabit/second transfer rate. A sample SCSI application is shown in Figure 5. Intel tested iSBC 186/03A board compatible SCSI controllers include Adaptek 4500, DTC 1410, Iomega Alpha 10, Shugart 1601 and 1610, Vermont Research 8103 and Xebec 1410.

The Centronics interface requires very little software overhead since a PAL device is used to provide necessary handshake timing. Interrupts are generated for printer fault conditions and a DMA request is issued for every character. The interface supports Centronics type printers compatible with models 702 and 737.

**SERIAL I/O**

The iSBC 186/03A Single Board Computer contains two programmable communications interfaces using the Intel 8274 Multi-Protocol Serial Controller (MPSC).

Two 80186 timer outputs are used as software selectable baud rate generators capable of supplying the serial channels with common communications frequencies. An 80130 baud rate timer may be jumpered to either serial port to provide higher frequency baud rates. The mode of operation (i.e., asynchronous, byte synchronous or bisynchronous protocols), data format, control character format, parity, and baud rate are all under program control. The 8274 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the MPSC. The iSBC 186/03A board supports operation in the polled, interrupt and DMA driven interfaces through jumper options. The default configuration is with channel A as RS422A/RS449, channel B as RS232C. Channel A can optionally be configured to support RS232C. Both channels are default configured as data set (DCE). Channel A can be reconfigured as data terminal (DTE) for connection to a modem-type device.



**Figure 5. Sample SCSI Application**

## INTERRUPT CONTROL

The iSBC 186/03A board provides 27 on-board vectored interrupt levels to service interrupts generated from 33 possible sources.

The interrupts are serviced by four programmable interrupt controllers (PICs): one in the 80186 component, one in the 80130 component, one in the 8259A component and one in the 8274 component. The 80186, 8259A and 8274 PICs act as slaves to the 80130 master PIC. The highest priority interrupt is the Non-Maskable Interrupt (NMI) line which is tied directly to the 80186 CPU. This interrupt is typically used to signal catastrophic events (e.g. power failure). The PICs provide prioritization and vectoring for the other 26 interrupt requests from on-board I/O resources and from the MULTIBUS system bus. The PICs then resolve the requests according to the programmable priority resolution mode, and if appropriate, issue an interrupt to the CPU.

Table 1 contains a list of devices and functions capable of generating interrupts. These interrupt sources are jumper configurable to the desired interrupt request level.

## Expansion

### OVERVIEW

The iSBC 186/03A board architecture includes three bus structures: the MULTIBUS system bus, the

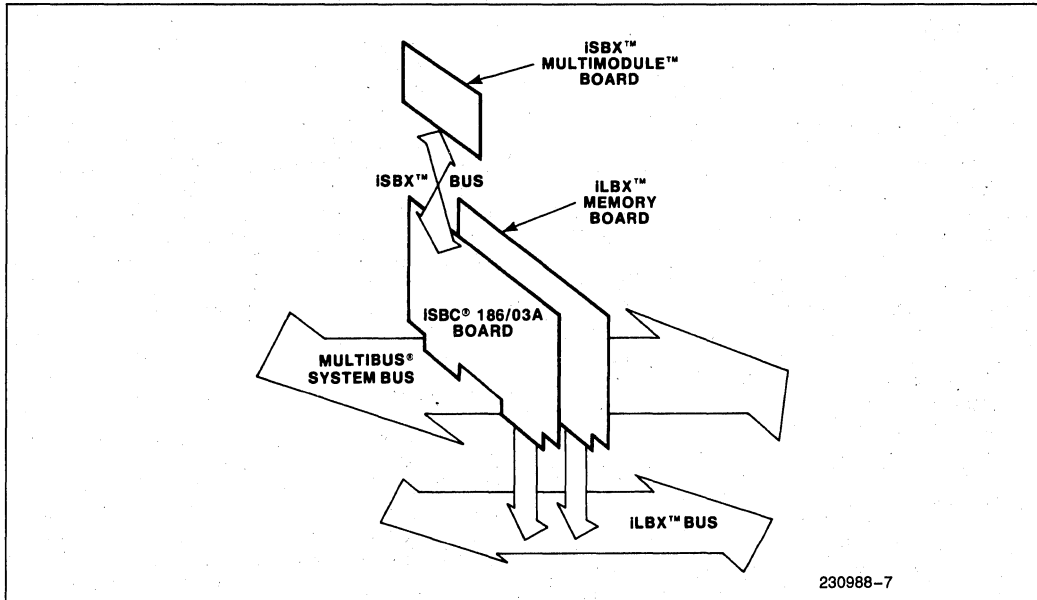
iLBX local bus expansion and the iSBX MULTIMODULE expansion bus as shown in Figure 6. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The iLBX bus allows large amounts of high performance memory to be accessed by the iSBC 186/03A board over a private bus. The iSBX MULTIMODULE expansion board bus is a means of adding inexpensive I/O functions to the iSBC 186/03A board. Each of these bus structures are implemented on the iSBC 186/03A board providing a flexible system architecture solution.

### MULTIBUS® SYSTEM BUS—IEEE 796

The MULTIBUS system bus is an industry standard (IEEE 796) microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 20 or 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations with multiple processors and intelligent slave, I/O and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board-level products, LSI interface components, detailed published specifications and application notes.

**Table 1. Interrupt Request Sources**

Device	Function	Number of Interrupts
MULTIBUS Bus Interface INT0-INT7	Requests from MULTIBUS Bus Resident Peripherals or Other CPU	8
8274 Serial Controller	Transmit Buffer Empty, Receive Buffer Full and Channel Errors	8
Internal 80186 Timer and DMA	Timer 0, 1, 2, Outputs (Function Determined by Timer Mode) and 2 DMA Channel Interrupts	5
80130 Timer Output	iRMX System Timer (SYSTICK)	1
iSBX Bus Connectors	Function Determined by iSBX MULTIMODULE Board	6 (3 per iSBX Connector)
Bus Fail-Safe Timer	Indicates Addressed MULTIBUS Bus Resident Device Has Not Responded to Command within 10 ms	1
8255A Parallel I/O Controller	Parallel Port Control	2
J4 Connector	External/Power-Fail Interrupts	2



**Figure 6. iSBC® 186/03A Board System Architecture**

### **iLBX™ BUS—LOCAL BUS EXTENSION**

The iSBC 186/03A board provides a local bus extension (iLBX) interface. This standard extension allows on-board memory performance with physically off-board memory. The combination of a CPU board and iLBX memory boards is architecturally equivalent to a single board computer and thus can be called a "virtual single board computer". The iLBX bus is implemented over the P2 connector and requires independent cabling or backplane connection.

### **iSBX™ BUS MULTIMODULE™ ON-BOARD EXPANSION**

Two iSBX MULTIMODULE board connectors are provided on the iSBC 186/03A microcomputer board. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, and graphics control. The iSBX bus connectors on the iSBC 186/03A board provide all signals necessary to interface to the local on-board bus, including 16 data

lines for maximum data transfer rates. MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 186/03A board. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX bus modules may also be designed. An iSBX bus interface specification is available from Intel.

### **OPERATING SYSTEM SUPPORT**

Intel's iRMX 86 Operating System is a highly functional operation system with a very rich set of features and options based on an object-oriented architecture. In addition to being modular and configurable, functions include a sophisticated file management and I/O system, and a powerful human interface. The iRMX 86 Release 6 Operating System can be used with the iSBC 186/03A board to generate application code for iRMX 86 based systems.

#### **NOTE:**

Intel does not support the direct processor execution of the 16K bytes of the iRMX 86 Operating System nucleus primitives from the 80130 component.



## DEVELOPMENT ENVIRONMENT

Intel offers numerous tools to aid in the development of iSBC 186/03A board applications. These include on-target development, full development systems, in-circuit emulators and programming languages. Some of the features of each are described below.

Using the iRMX 86 Operating System, software development can be performed directly on the iSBC 186/03A board. This on-target development is the most economical way to develop iSBC 186/03A board based projects.

The development cycle of iSBC 186/03A board products can be significantly reduced and simplified by using either the System 86/3XX (iRMX 86-based) or the Intellec® Series Microcomputer Development Systems.

The Integrated Instrumentation In-Circuit Emulator (i<sup>2</sup>ICE™) provides the necessary link between an Intellec development system and the "target" iSBC 186/03A execution system. In addition to providing the mechanism for loading executable code and data into the iSBC 186/03A boards, the i<sup>2</sup>ICE 186 emulator provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software.

Intel has two systems implementation languages, PL/M 86 and C 86. Both are available for use on the iRMX 86 Operating System, on the System 86/3XX and on the Intellec Microcomputer Development System. PL/M 86 provides the capability to program in algorithmic language and eliminates the need to manage register usage or allocate memory while still

allowing explicit control of the system's resources when needed. C 86 is especially appropriate in applications requiring portability and code density. FORTRAN 86, PASCAL 86, and BASIC 86 are also available on the iRMX 86 operating system, on the System 86/3XX and on the Intellec development system.

## SPECIFICATIONS

### Word Size

Instruction—8, 16, 24 or 32 bits  
Data—8 or 16 bits

### System Clock

8.0 MHz

### Numeric Data Processor (Optional)

8087-1

### Basic Instruction Cycle Time

750 ns  
250 ns (assumes instruction in the queue)

**NOTE:**

Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles plus instruction fetch). Zero wait-state memory is assumed.

## MEMORY RESPONSE TIMES

Device Type	Max Access Time (from Chip Enable)	Min Cycle Time
EPROM Memory Sites		
0 Wait States	245 ns	318 ns
1 Wait State	370 ns	443 ns
RAM Memory Sites		
with SRAMs or EPROMs		
0 Wait States	197 ns	318 ns
1 Wait States	322 ns	443 ns
with 2186 IRAMs		
1 Wait State	261 ns	443 ns
2 Wait States	386 ns	568 ns

**NOTE:**

The number of wait states inserted is jumper selected depending on memory device specifications.

**MEMORY CAPACITY/ADDRESSING**

Four EPROM Sites		
Device	Capacity	Address Range
2764 EPROM	32 KB	F8000 <sub>H</sub> -FFFFF <sub>H</sub>
27128 EPROM	64 KB	F0000 <sub>H</sub> -FFFFF <sub>H</sub>
27256 EPROM	128 KB	E0000 <sub>H</sub> -FFFFF <sub>H</sub>
27512 EPROM	256 KB	C0000 <sub>H</sub> -FFFFF <sub>H</sub>
Four RAM Sites		
Device	Capacity	Address Range
2K SRAM	8 KB	0-01FFF <sub>H</sub>
8K SRAM	32 KB	0-07FFF <sub>H</sub>
32K SRAM	128 KB	0-1FFFF <sub>H</sub>
2186 RAM	32 KB	0-07FFF <sub>H</sub>
2817A E <sup>2</sup> PROM	8 KB	F0000 <sub>H</sub> -F7FFF <sub>H</sub> *
2764 EPROM	32 KB	F0000 <sub>H</sub> -F7FFF <sub>H</sub> (below EPROM Sites)
27128 EPROM	64 KB	E0000 <sub>H</sub> -EFFFF <sub>H</sub> (below EPROM Sites)
27256 EPROM	128 KB	C0000 <sub>H</sub> -DFFFF <sub>H</sub> (below EPROM Sites)
Four iSBIC® 341 Expansion Sites		
Device	Capacity	Address Range
2K SRAM	8 KB	02000 <sub>H</sub> -03FFF <sub>H</sub>
8K SRAM	32 KB	08000 <sub>H</sub> -0FFFF <sub>H</sub>
32K SRAM	128 KB	10000 <sub>H</sub> -1FFFF <sub>H</sub>
2186 RAM	32 KB	08000 <sub>H</sub> -0FFFF <sub>H</sub>
2817A E <sup>2</sup> PROM	8 KB	02000 <sub>H</sub> -03FFF <sub>H</sub> **

**NOTE:**

All on board memory is local to the CPU (i.e. not dual-ported).

\*Must use 8k x 8 decode option, there are four copies of the E<sup>2</sup>PROM in the 8K x 8 address area.

\*\* (May be mixed with 2K x 8 SRAM)

**Serial Communications Characteristics**

**Synchronous**— 5–8 bit characters, internal or external character synchronization; automatic sync insertion; break character generation

**Asynchronous**— 5–8 bit characters; 1, 1/2, or 2 stop bit; false start bit detection.

**Common Baud Rates**

Using 80186 Timers:	Using 80130 Timer:
500K	750K
125K	500K
64K	125K
48K	64K
19.2K	48K
9600	19.2K
4800	9600
2400	4800
1200	2400
600	1200
300	600
150	300
110*	150
75*	110*
	75*

\*Asynchronous use only

**NOTE:**

Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register of 80186 or 80130 timers.

**Timer Input Frequency**

80186 Reference: 2.0 MHz ±0.1%

80130 Reference: 8.0 MHz ±0.1%

**Interface Compliance**

**MULTIBUS**— IEEE 796 compliance: Master D16 M24 116 VO EL

**iSBX Bus**— Two 8/16 bit iSBX bus connectors allow use of up to 2 single-wide modules or 1 single-wide and 1 double-wide module. Intel iSBX bus compliance: D16/16 DMA

**iLBX**— Intel iLBX bus compliance: PM D16

**Serial**— Channel A: Configurable as RS 422A or RS 232C compatible, configurable as a data set or data terminal

Channel B: RS 232C compatible, configured as data set

**Parallel I/O**— SCSI (ANSI—X3T9, 2/82-s) compatible or Centronics 702 or 737 compatible (requires user supplied PALs and 74LS640-1)

**CONNECTORS**

Interface	Double-sided Pins	Mating Connectors
MULTIBUS System	86 (P1)	Viking 3KH43/9AMK12 Wire Wrap
	60 (P2)	Viking 3KH30/9JNK
iSBX Bus 8-Bit Data	36	Viking 000292-0001
	44	Viking 000293-0001
16-Bit Data		
Serial I/O	26	3M 3452-0001 Flat AMP88106-1 Flat
iLBX Bus	60	Kelam RF30-2853-542
Parallel Interface	50	3M 3425-6000 3M 3425-6050 w/strain Ansley 609-5001M

**PHYSICAL CHARACTERISTICS**

Width: 12.00 in. (30.48 cm)  
 Length: 7.05 in (17.90 cm)  
 Height: 0.50 in. (1.78 cm)  
 Weight: 13 ounces

**ENVIRONMENTAL CHARACTERISTICS**

Operating Temperature: 0°C to 60°C at 6 CFM air-flow over the board.

Relative Humidity: to 90% (without condensation)

**ELECTRICAL CHARACTERISTICS**

The maximum power required per voltage is shown below. These numbers do not include the power required by the optional memory devices, SCSI PALs, battery back-up or expansion modules.

Voltage (volts)	Max. Current (amps)	Max Power (watts)
+5	5.4	27
+12	0.04	0.48
-12	0.04	0.48

**ORDERING INFORMATION**

Part Number	Description
SBC 186/03A	186-based single board computer

**REFERENCE MANUAL**

iSBC® 186/03A Single Board Computer Hardware Reference Manual—Order Number 148060