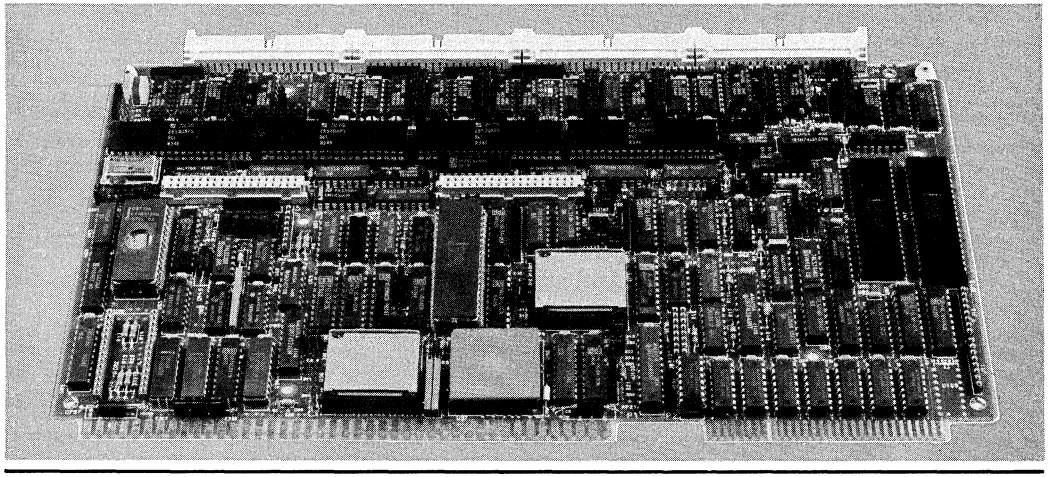
iSBC® 188/48 ADVANCED COMMUNICATING COMPUTER

- **iSBC® Single Board Computer or Intelligent Slave Communication board**
- **8 Serial Communications channels, expandable to 12 channels on a single MULTIBUS® board**
- **6 MHz iAPX 188 Microprocessor**
- **Supports RS232C interface on 6 channels, RS422A/449 or RS232C interface configurable on 2 channels**
- **Supports Async, Bisync HDLC/SDLC, on-chip baud rate generation, half/full-duplex, NRZ, NRZI or FM encoding/decoding**
- **7 on-board DMA channels for serial I/O, 2 80188 DMA channels for iSBX™ MULTIMODULE™ board**
- **MULTIBUS® Interface for system expansion and Multimaster configuration**
- **2 iSBX™ connectors for low cost I/O expansion**
- **64K Bytes Dual-ported RAM expandable to 192K Bytes with Parity using the iSBC® 307 RAM MULTIMODULE™ board**
- **2 28-pin JEDEC PROM sites expandable to 6 sites with the iSBC® 341 MULTIMODULE™ board for a maximum of 192K Bytes EPROM**
- **Resident firmware to handle up to 12 RS232C Async lines**
- **Optional Operating System firmware**

The iSBC® 188/48 Advanced Communicating Computer (COMMputer™) is an intelligent 8-channel single board computer. This iSBC board adds 6MHz iAPX 188 microprocessor-based communications flexibility to the Intel line of OEM microcomputer systems. Acting as a stand-alone CPU or intelligent slave for communication expansion, this board provides a high performance, low-cost solution for multi-user systems. The features of the iSBC 188/48 board are uniquely suited to manage higher-layer protocol requirements needed in today's data communications applications. This single board computer takes full advantage of Intel's VLSI technology to provide state-of-the-art, economic, computer-based solutions for OEM communications-oriented applications.



SEPTEMBER 1984
ORDER NUMBER: 230890-002

OPERATING ENVIRONMENT

The iSBC 188/48 COMMputer™ features have been designed to meet the needs of numerous communications applications. Typical applications include:

1. Terminal/cluster controller
2. Front-end processor
3. Stand-alone communicating computer

Terminal/cluster controller

A terminal/cluster controller concentrates communications in a central area of a system. Efficient handling of messages coming in or going out of the system requires sufficient buffer space to store messages and high speed I/O channels to transmit messages. More sophisticated applications, such as cluster controllers, also require character and format conversion capabilities to allow different types of terminals to be attached.

The iSBC 188/48 Advanced Communicating Computer is well suited for multi-terminal systems (See Figure 1). Up to 12 serial channels can be serviced in multi-user or cluster applications by adding two iSBX 354 MULTIMODULE boards. The dual-port RAM provides a large on-board buffer to handle incoming and outgoing messages at data rates up to 19.2K Baud. Two channels are supported for continuous data rates greater than 19.2K Baud. Each serial channel can be individually programmed for different Baud rates to allow system configurations with differing terminal types. The firmware supplied on the iSBC 188/48 board supports up to 12 asynchronous RS232C serial channels, provides modem control and performs power-up diagnostics. The high performance of the on-board CPU provides intelligence to handle protocols and character handling typically assigned to the system CPU. This distribution of intelligence results in optimizing system performance by releasing the system CPU of routine tasks.

Front-end Processor

A front-end processor off-loads a system's central processor of tasks such as data manipulation and text editing of characters collected from the attached terminals. A variety of terminals require flexible terminal interfaces. Program code

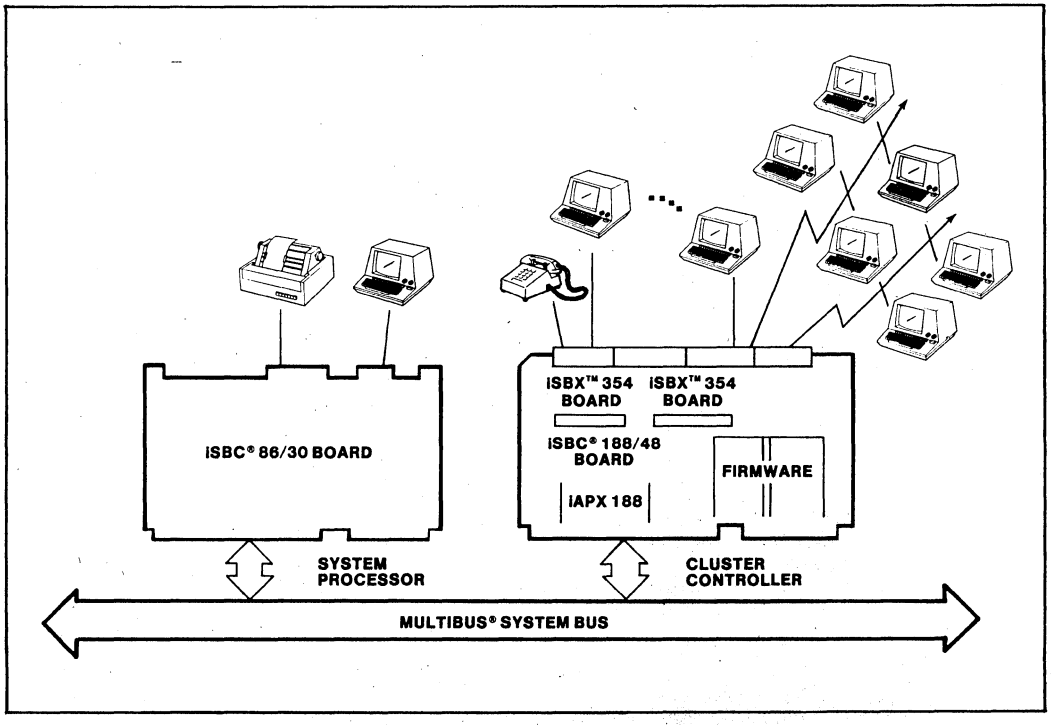


Figure 1. Terminal/Cluster Controller Application

is often dynamically down-loaded to the front-end processor from the system CPU. Downloading code requires sufficient memory space for protocol handling and program code. Flow control and efficient handling of interrupts require an efficient operating system to manage the hardware and software resources.

The iSBC 188/48 board features are designed to provide a high performance solution for front-end processor applications (see Figure 2). A large amount of random access memory is provided for dynamic storage of program code. In addition, local memory sites are available for storing routine programs such as X.25, SNA or bisync protocol software. The serial channels can be configured for links to mainframe systems, point-to-point terminals, modems or multi-drop configurations.

STAND-ALONE COMMputer™ APPLICATION

A stand-alone communicating computer is a complete computer system. The CPU is capable of managing the resources required to meet the needs of multi-terminal, multi-protocol applications. These applications typically require multi-terminal support, floppy disk control, local memory allocation, and program execution and storage.

To support stand-alone applications, the iSBC 188/48 COMMputer board can combine the computational capabilities of an on-board CPU with the nucleus of a real-time operating system (optional) to provide a high-speed system solution controlling 8 to 12 channels of serial I/O (see Figure 3). The local memory available is large enough to handle special purpose code, execution code and routine protocol software. The MULTIBUS interface can be used to access additional system functions. Floppy disk control and graphics capability can be added to the iSBC stand-alone computer through the iSBX connectors.

ARCHITECTURE

The four major functional areas are Serial I/O, CPU, Memory and DMA. These areas are illustrated in Figure 4.

Serial I/O

Eight HDLC/SDLC serial interfaces are provided on the iSBC 188/48 board. The serial interface can be expanded to 12 channels by adding 2

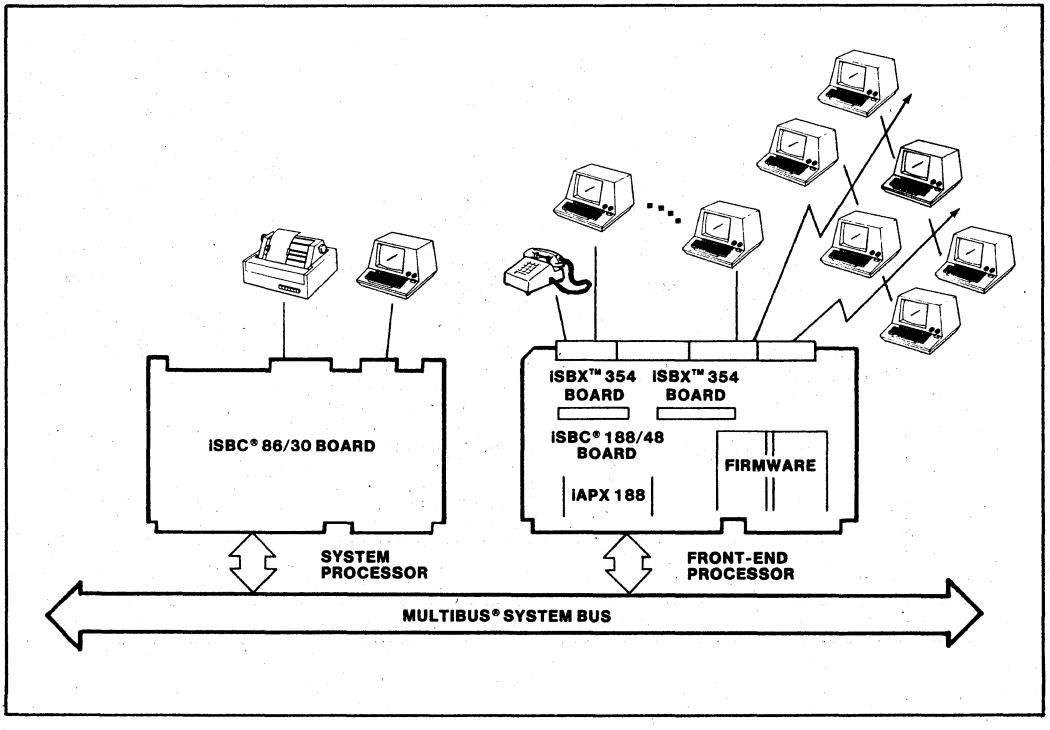


Figure 2. Front-end Processor Application

iSBX 354 MULTIMODULE boards. The HDLC/SDLC interface is compatible with IBM system and terminal equipment and with CCITT's X.25 packet switching interface.

Four 82530 Serial Communications Controllers (SCC) provide eight channels of half/full duplex serial I/O. Six channels support RS232C interfaces. Two channels are RS232C/422/449 configurable and can be tri-stated to allow multidrop networks. The 82530 component is designed to satisfy several serial communications requirements: asynchronous, byte-oriented synchronous, and bit-oriented synchronous (HDLC/SDLC) modes. The increased capability at the serial controller point results in off-loading the CPU of tasks formerly assigned to the CPU or its associated hardware. Configurability of the 82530 allows the user to configure it to handle all asynchronous data formats regardless of data size, number of start and stop bits, or parity requirements. An on-chip Baud rate generator allows independent Baud rates on each channel.

The clock can be generated either internally with the SCC chip, with an external clock or via the NRZ clock encoding mechanism.

All eight channels can be configured as Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). Table 1 lists the interfaces supported.

Central CPU

The iAPX 188 central processor along with the optional Operating System Firmware component provides high performance, flexibility and powerful processing power. The 80188 component is a highly integrated microprocessor with an 8-bit data bus interface an a 16-bit internal architecture to give high performance. The iAPX 188 is upward compatible with iAPX 86 and iAPX 186 software. The O.S. component provides timers and interrupt controllers as well as the optional iRMX™ 86 nucleus primitives for those applications requiring a real-time executive.

The 80188/82530 combination with on-board PROM/EPROM sites, and dual-port RAM provide the intelligence and speed to manage multi-user, multi-protocol communications operations.

Memory

There are two areas of memory on-board: dual-port RAM and universal site memory. The iSBC

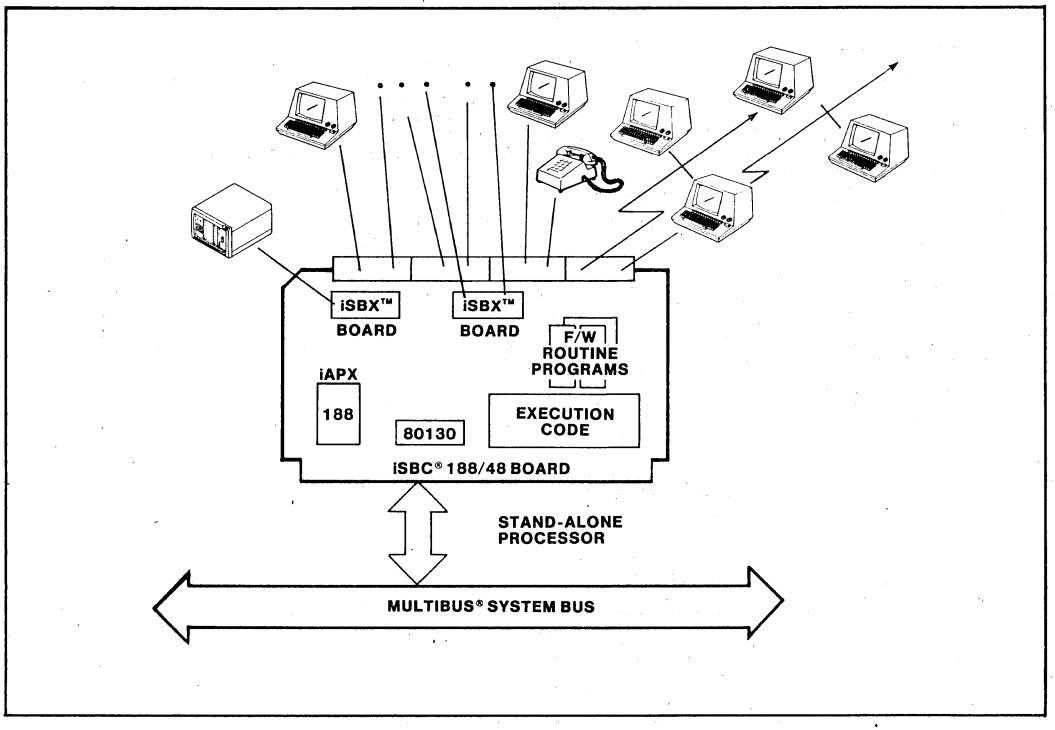


Figure 3. Stand-alone COMMputer™ Application

188/48 board contains 64K bytes of dual-port RAM that is addressable by the iAPX 188 on-board. The dual-port memory is configurable anywhere in a 16M Byte address space on 64K Byte boundaries as addressed from the MULTIBUS port. Not all of the 64K bytes are visible from the MULTIBUS side. The amount of dual-port memory visible to the MULTIBUS side can be set (with jumpers) to none, 16K bytes, or 48K bytes. The on-board RAM is expandable to a total of 192K bytes with parity by adding the iSBC 307 MULTIMODULE board. In a multiprocessor system these features provide local memory for each processor and shared system memory configurations where the total system memory size can exceed one megabyte without addressing conflicts.

The second area of memory is universal site memory providing flexible memory expansion. Two 28-pin JEDEC sockets are provided. One of these sockets is used for the resident firmware as described in the FIRMWARE section on Page 7.

The default configuration of the board supports 16K Byte EPROM devices such as the Intel 27128 component. However, these sockets can contain ROM, EPROM, Static RAM, or EEPROM. Both sockets must contain the same type of component (i.e. as the first socket contains an EPROM for the resident firmware, the second must also contain an EPROM with the same pinout). Up to 32K bytes can be addressed per socket giving a maximum universal site memory size of 64K bytes. By using the iSBC 341 MULTIMODULE board, a maximum of 192K bytes of universal site memory is available. This provides sufficient memory space for on-board network or resource management software.

Table 1. iSBC® 188/48 Interface Support

Connection	Synchronous Modem or Direct	Asynchronous Modem or Direct
Point-to-point	X**	X
Multidrop	Channels 0 and 1	Channels 0 and 1
Loop	X	N/A

** All 8 channels are denoted by X.

On-Board DMA

Seven channels of Direct Memory Access (DMA) are provided between serial I/O and on-board

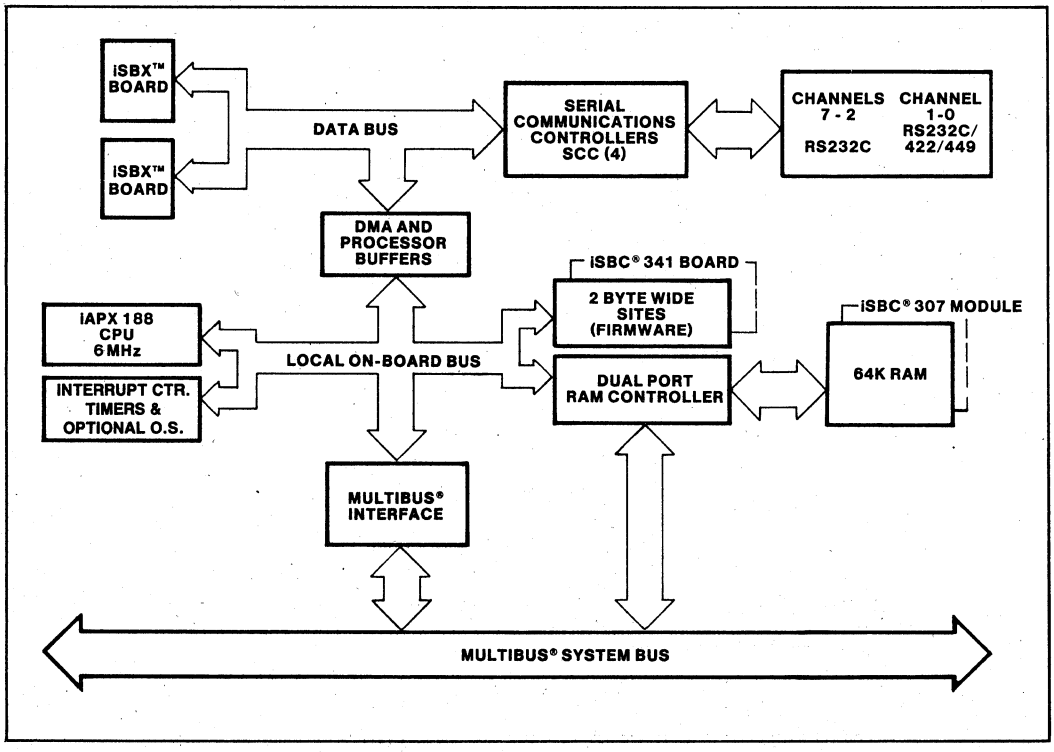


Figure 4. Block Diagram of iSBC 188/48 Board

dual-port RAM by two 8237-5 components. Each of channels 0,1, 2, 3, 5, 6, and 7 is supported by their own DMA line. Serial channels 0 and 1 are configurable for full duplex DMA. Configuring the full duplex DMA option for Channels 0 and 1 would require Channels 2 and 3 to be interrupt driven or polled. Channel 4 is interrupt driven or polled only.

Two DMA channels are integrated into the iAPX 188 processor. These additional channels can be connected to the iSBX interfaces to provide DMA capability to iSBX MULTIMODULE boards such as the iSBX 218A Floppy Disk Controller MULTIMODULE board.

OPERATING SYSTEM SUPPORT

Intel offers run-time foundation software to support applications that range from general purpose to high-performance solutions. Release 4 of the iRMX 88 Real-Time Executive provides an event-driven multitasking structure for the iSBC 188/48 board that includes task scheduling, task management, intertask communications and interrupt servicing for high-performance applications. Application tasks utilize intertask communications, asynchronous I/O control, priority-based resource allocation and file support for peripheral controllers. The small, high-performance iRMX 88 Executive can be located in EPROM or bootstrapped into iSBC 188/48 dual-port memory.

Release 6 of the iRMX 86 Operating System provides a rich set of features and options to support sophisticated stand-alone communications applications on the iSBC 188/48 Advanced Communicating Computer. In addition to supporting real-time requirements, the iRMX 86 Operating System Release 6 has a powerful, yet easy to use human interface. Services provided by the iRMX 86 Operating System include facilities for executing programs concurrently, sharing resources and information, servicing asynchronous events and interactively controlling system resources and utilities. The iRMX 86 Operating System is readily extended to support assembler, PL/M, PASCAL, and FORTRAN software development environments. The modular building block software lends itself well to customized application solutions. If the iSBC 188/48 is acting as an intelligent slave in a system environment, an iRMX 86 driver resident in the host CPU can be written by following the examples in Application Note 86, "Using the iRMX86 Operating System".

*UNIX is a trademark of Bell Laboratories.

SUPPORT FOR OPTIONAL OPERATING SYSTEM FIRMWARE

Release 3 of the iOSP 86 package provides the tools necessary to develope (P)ROM or RAM-based applications that use the optional Operating System Firmware component on the iSBC 188/48 board. All of the system initialization and run-time facilities are provided in libraries that may be configured to specific requirements and linked to application programs written in high level programming languages such as PL/M, Pascal or FORTRAN. The iOSP package also enables users to add higher level I/O functions from the fully compatible iRMX 86 Operating System, or to form custom, real-time systems. Please contact your local sales office for the implementation details of the operating system firmware.

The iSDM™ 86 System Debug Monitor supports target system debugging for the iSBC 188/48 Advanced Communicating COMMputer board. The monitor contains the necessary hardware, software and documentation required to interface the iSBC 188/48 target system to an Intel Microcomputer Development System for debugging application software.

The XENIX* 286 Operating System, Release 2, is a fully-licensed adaptation of the Bell Laboratories System III UNIX* Operating System. The XENIX system is an interactive, protected, multi-user, multi-tasking operating system with a powerful, flexible human interface. Release 2 of XENIX 286 includes a software driver for the iSBC 188/48 board (and up to two iSBX354 Multimodule Boards) acting as an intelligent slave for multi-user applications requiring multiple persons running independent, terminal-oriented jobs. Example applications include distributed data processing, business data processing, software development and engineering or scientific data analysis. XENIX 286 Release 2 Operating System services include device independent I/O, tree-structured file directory and task hierarchies, re-entrant/shared code and system accounting and security access protection.

FIRMWARE

The iSBC 188/48 Communicating COMMputer board is supplied with resident firmware that supports up to 12 RS232C asynchronous serial channels. In addition, the firmware provides a facility for a host CPU to download and execute code on the iSBC 188/48 board. Simple power-up confidence tests are also included to provide a quick diagnostic service. The firmware converts the iSBC 188/48 COMMputer to a slave communications controller. As a slave communications controller, it requires a separate MULTIBUS host CPU board and requires the use of a

Table 2. Features of the iSBC® 188/48 Firmware

Feature	Description
Asynchronous Serial Channel Support	Supports the serial channels in asynchronous ASCII mode. Parameters such as baud rate, parity generation, parity checking and character length can be programmed independently for each channel.
Block Data Transfer (On Output)	Relieves the host CPU of character-at-a-time interrupt processing. The iSBC 188/48 board accepts blocks of data for transmission and interrupts the processor only when the entire block is transmitted.
Limited Modem Control	Provides software control of the Data Terminal Ready (DTR) line on all channels. Transitions on the Carrier Detect (CD) line are sensed and reported to the host CPU.
Tandem Mode Support	Transmits an XOFF character when the number of characters in its receive buffer exceeds a threshold value and transmits an XON character when the buffer drains below some other threshold.
Download and execute capability	Provides a capability for the host CPU to load code anywhere in the address space of the iSBC 188/48 board and to start executing at any address in its address space.
Power Up Confidence Tests	On board reset, the firmware executes a series of simple tests to establish that crucial components on the board are functional.

MULTIBUS interrupt line to signal the host processor. Table 2 summarizes the features of the firmware.

INTERRUPT CAPABILITY

The iSBC 188/48 board has two programmable interrupt controllers (PICs). One is integrated into the 80188 processor and the other in the 80130 component. The two controllers are configured with the 80130 controller as the master and the 80188 controller as the slave. Two of the 80130 interrupt inputs are connected to the 82530 serial controller components to provide vector interrupt capablities by the serial controllers. The iSBC 188/48 board provides 22 interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 80188 CPU. This interrupt is typically used for signaling catastrophic events (e.g. power failure). There are 5 levels of interrupts internal to the 80188 processor. Another 8 levels of interrupts are available from the 80130 component. Of these 8, one is tied to the programmable interrupt controller (PIC) of the 80188 CPU. An additional 8 levels of interrupts are available at the MULTIBUS interface. The iSBC 188/48 board does not support bus vectored interrupts. Table 3 lists the possible interrupt sources.

EXPANSION

EPROM/RAM Expansion

Memory may be expanded by adding Intel compatible memory expansion boards. The universal site memory can be expanded to six sockets by adding the iSBC 341 MULTIMODULE board for a maximum total of 192K bytes of universal site memory. The 64K bytes of on-board dual-port RAM can be expanded to a maximum total of 192K bytes by adding the iSBC 307 MULTIMODULE board. The iSBC 307 MULTIMODULE board also provides parity for all 192K bytes of on-board RAM.

iSBX™ MULTIMODULE™ Expansion

Two 8-bit iSBX MULTIMODULE connectors are provided on the iSBC 188/48 board. Using iSBX modules additional functions can be added to extend the I/O capability of the board. In addition to specialized or custom designed iSBX boards, there is a broad range of iSBX MULTIMODULE boards from Intel including parallel I/O, analog I/O, IEEE 488 GPIB, floppy disk, magnetic bubbles, video and serial I/O boards.

The serial I/O MULTIMODULE boards available include the iSBX 354 Dual Channel Expansion

MULTIMODULE board. Each iSBX 354 MULTIMODULE board adds two channels of serial I/O to the iSBC 188/48 board for a maxmimum of twelve serial channels. The 82530 serial communications controller on the MULTIMODULE handles a large variety of serial communications protocols. This is the same serial controller as is used on the iSBC 188/48 board to offer directly compatible expansion capability for the iSBC 188/48 COMMputer board.

MULTIBUS® INTERFACE

The iSBC 188/48 Advanced COMMputer board can be a MULTIBUS master or intelligent slave in a multimaster system. The iSBC 188/48 board incorporates a flag byte signalling mechanism for use in multiprocessor environments where the iSBC 188/48 board is acting as an intelligent slave. This mechanism provides an interrupt handshake from the MULTIBUS System Bus to the on-board processor and vice-versa.

The Multimaster capabilities of the iSBC 188/48 board offers easy expansion of processing capacity and the benefits of multiprocessing. Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards.

Table 3. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS® Interface INT0 - INT7	Requests from MULTIBUS resident peripherals or other CPU boards.	8
82530 Serial Controllers	Transmit buffer empty, receive buffer full and channel errors 1 and external status	8 per 82530 Total = 32
Internal 80188 Timer and DMA	Timer 0,1,2 outputs and 2 DMA channel interrupts	5
80130 Timer Outputs	Timer 0,1,2, outputs of 80130	3
Interrupt from Flag Byte Logic	Flag byte interrupt set by MULTIBUS master (through MULTIBUS® I/O Write)	1
Bus Flag Interrupt	Interrupt to MULTIBUS® (Selectable for INT0 to INT7) generated from on-board 80188 I/O Write	1
iSBX™ connectors iSBX™ DMA	Function determined by iSBX™ MULTIMODULE™ board DMA interrupt from iSBX™(TDMA)	4 (Two per connector) 2
Bus fail-safe timeout Interrupt	Indicates iSBC® 188/48 board timed out either waiting for MULTIBUS® access or timed out from no acknowledge while on MULTIBUS System Bus	1
Latched Interrupt	Converts pulsed event to a level interrupt. Example: 8237A-5 EOP	1
OR-gate Matrix	Concentrates up to 4 interrupts to 1 interrupt (selectable by stake pins)	1
Ring Indicator Interrupt	Latches a ring indicator event from serial channels 4,5,6, or 7	1
NOR-Gate Matrix	Inverts up to 2 interrupts into 1 (selectable by stake pins)	1

SPECIFICATIONS

Word Size

Instruction — 8, 16, 24 or 32 bits
Data Path — 8 bits

Processor Clock	82530 Clock	DMA Clock
6 MHZ	4.9152 MHz	3 MHz

MEMORY CAPACITY/ADDRESSING

Dual-Port RAM

iSBC®188/48 Board — 64K bytes

As viewed from the iAPX 188 — 64K

As viewed from the MULTIBUS® System Bus —
Choice: 0, 16K or 48K

EPROM

Using:

iSBC® 188/48 Board	Size	On Board Capacity	Address Range
2732	4K	8K	FE000-FFFFF$_H$
2764	8K	16K	FC000-FFFFF$_H$
27128	16K	32K	F8000-FFFFF$_H$
27256	32K	64K	F0000-FFFFF$_H$

Memory Expansion

1. **Ram Memory** — with iSBC 307 Board

   Total Capacity — 192K

   As viewed from the MULTIBUS® System Bus —
   Choice: 0, 16K or 48K Public
   16K to 192K Private
   64K or 192K Total

2. **EPROM with iSBC® board using:**

	Total Capacity	Address Range
2732	24K	F8000-FFFFF$_H$
2764	48K	F0000-FFFFF$_H$
27128	96K	E0000-FFFFF$_H$
27256	192K	C0000-FFFFF$_H$

I/O Capacity

Serial — 8 programmable lines using 4 82530 components
iSBX™ MULTIMODULE™ Board — 2 iSBX™ single-wide boards

Serial Communications Characteristics

Synchronous — Internal or external character synchronization on one or two synchronous characters

Asynchronous — 5-8 bits and 1, 1½ or 2 stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection

Baud Rates

Synchronous X1 Clock	
Baud Rate	**82530 Count Value (Decimal)**
64000	36
48000	49
19200	126
9600	254
4800	510
2400	1022
1800	1363
1200	2046
300	8190
Asynchronous X16 Clock	
Baud Rate	**82530 Count Value (Decimal)**
19200	6
9600	14
4800	30
2400	62
1800	83
1200	126
300	510
110	1394

INTERFACES

iSBX™ Bus

The iSBC 188/48 board meets iSBX compliance level D8/8 DMA

MULTIBUS® System Bus

The iSBC 188/48 board meets MULTIBUS compliance level Master/Slave D8 M24 I16 V0 EL

Serial RS232C Signals

CD	Carrier Detect
CTS	Clear to Send
DSR	Data Set Ready
DTE TXC	Transmit Clock
DTR	Data Terminal Ready
RTS	Request to Send
RXC	Receive Clock
RXD	Receive Data
SG	Signal Ground
TXD	Transmit Data
RI	Ring Indicator

RS422A/449 Signals

RC	Receive Common
RD	Receive Data
RT	Receive Timing
SD	Send Data
TT	Terminal Timing

ENVIRONMENTAL CHARACTERISTICS

Temperature — 0 to 55°C, at 200 Linear Feet/Min. (LFM) Air Velocity

Humidity — to 90%, non-condensing (25°C to 70°C)

PHYSICAL CHARACTERISTICS

Width: 30.48 cm (12.00 in)

Length: 17.15 cm (6.75 in)

Height: 2.90 cm (1.14 in)

Weight: 595 gm (21 ounces)

ELECTRICAL CHARACTERISTICS

The power required per voltage for the iSBC 188/48 board is shown below. These numbers do not include the current required by universal memory sites or expansion modules.

Voltage (Volts)	Current (Amps) typ.	Power (Watts) typ.
+ 5	4.56A	22.8W
+12	.12A	1.5W
−12	.11A	1.3W

ORDERING INFORMATION

Part Number	Description
iSBC 188/48	8-Serial Channel Advanced Communicating Computer

REFERENCE MANUAL

iSBC 188/48 Advanced Communications Computer Reference Manual
Order Number 146218-002
(146218-002 Available in Nov '84)