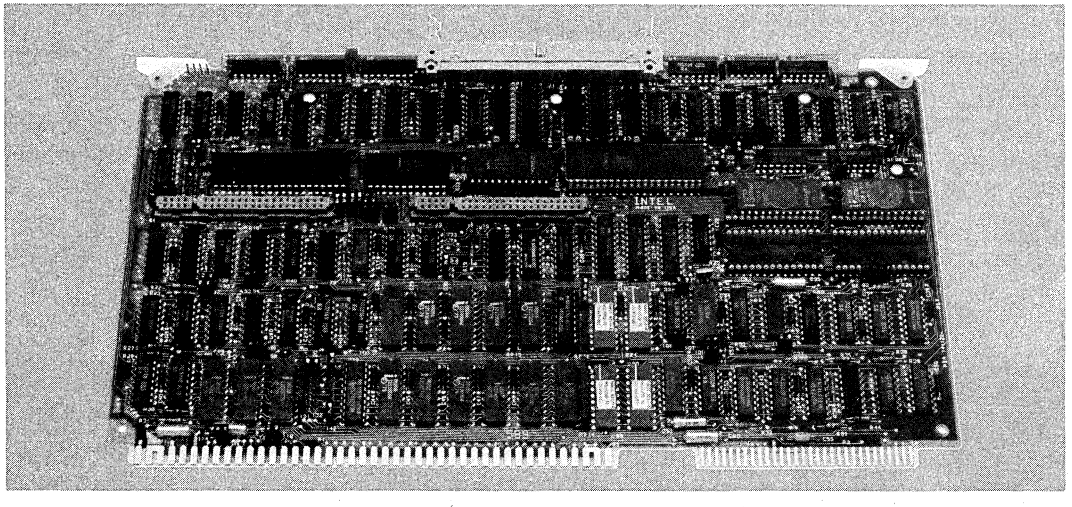
iSBC® 589
INTELLIGENT DMA CONTROLLER

- **Configurable as either an intelligent slave or MULTIBUS® master**
- **5 MHz 8089 I/O Processor**
- **MULTICHANNEL™ DMA I/O bus interface with Supervisor, Controller or Basic Talker/Listener capabilities**
- **Two 8/16-bit iSBX™ bus connectors**
- **DMA transfer rates up to 1.25 megabytes per second**
- **User Command Interface Firmware Package provides high level I/O commands**
- **8K bytes of high-speed dual-ported static read/write memory**
- **Sockets for up to 32K bytes of read only memory or additional byte-wide static RAMs**
- **Three programmable timers**

The iSBC 589 Intelligent DMA Controller is a member of Intel's complete line of MULTIBUS microcompter systems which take full advantage of VLSI technology to provide economical computer based solutions for OEM applications. The iSBC 589 board is a general purpose, programmable, high-speed DMA controller on a single 6.75 × 12.00 inch printed circuit board. Using the board's dual-port RAM and standard EPROM resident firmware, the on-board Intel 8089 I/O Processor can perform memory to memory block transfers and complex I/O operations via two iSBX connectors and the MULTICHANNEL I/O bus at DMA transfer rates up to 1.25 megabytes per second. Acting as an intelligent slave to one or more iSBC 286, iSBC 186, iSBC 86, iSBC 88 or iSBC 80, single board computers, the iSBC 589 board enhances the sytem's overall performance by relieving the host CPU of time consuming I/O operations. The board's unique combination of performance, on-board intelligence and flexible hardware I/O interfaces make the iSBC 589 board the ideal solution for applications with specialized I/O requirements, such as high-speed data acquisition, graphics, instrument automation and specialized peripheral control, that previously would have necessitated an expensive custom designed I/O controller.



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FUNCTIONAL DESCRIPTION

Two Modes of Operation

The iSBC 589 Intelligent DMA Controller is capable of operating either as a stand-alone, high-speed data acquisition controller or as an intelligent slave. In stand-alone mode, external requests cause the Intel 8089 I/O Processor to execute I/O programs contained in its on-board memory. As an intelligent slave to one or more Intel single board computers, the IOP can perform sophisticated DMA operations in response to high level commands issued by the host processor. While operating in either mode, the iSBC 589 board may act as a MULTIBUS master to access any system memory or I/O resources.

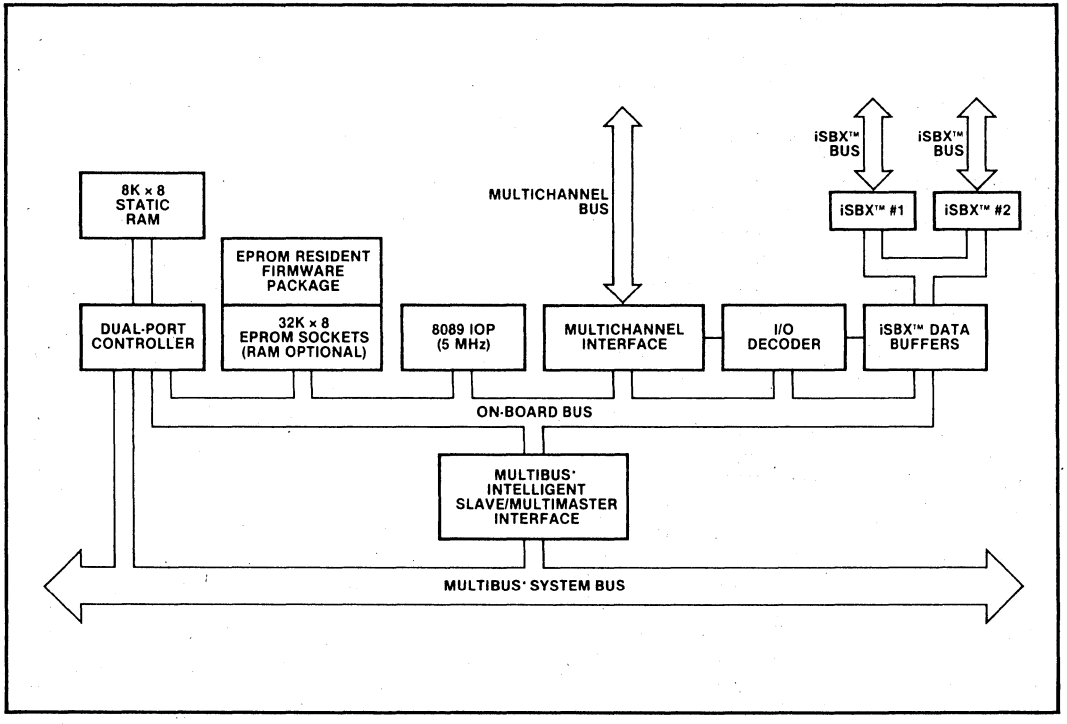
Input/Output Processor

The iSBC 589 board contains a 5 MHz Intel 8089 HMOS I/O Processor, whose architecture and instruction set have been optimized for performing DMA operations. The DMA function of the 8089 IOP uses a two cycle approach where the information actually flows through the 8089 IOP. This approach to DMA vastly simplifies the bus timings and enhances compatibility with memory and peripherals, in addition to allowing operations to be performed on the data as it is transferred. Operations can include such constructs as translate, where the 8089 automatically vectors through a lookup table and mask compare, both on the "fly". This DMA capability includes flexible termination conditions (such as external terminate, mask compare, single transfer and byte count expired).

The 8089 IOP supports two logically and physically separate I/O channels. The IOP maintains separate register sets for each I/O channel which allows the processor to alternate operation between the two channels without incurring context switching overhead delays.

DMA Capabilities

The iSBC 589 board supports both individual byte or word data transfers and DMA block transfer operations among its MULTICHANNEL interface, two iSBX connectors, on-board RAM and the MULTIBUS interface. Each of these devices may be combined



with any other as the source and destination for a DMA operation. The same firmware commands are used for all of the DMA source and destination combinations.

MULTICHANNEL Capabilities

The MULTICHANNEL bus provides a high-speed 8-bit or 16-bit wide data path for block data transfers between external devices, such as instruments, peripherals and other computers, and the iSBC 589 board. The iSBC 589 board can access up to 15 other devices on the MULTICHANNEL bus at distances of up to 15 meters and has the ability to address up to 16 megabytes of memory and 16 megabytes of I/O on each device.

The iSBC 589 Intelligent DMA Controller can interface to the MULTICHANNEL bus in one of three modes: as a Basic Talker/Listener, a Controller, and a Supervisor. In Basic Talker/Listener Mode, the iSBC 589 board monitors the MULTICHANNEL for requests from a Controller or the bus Supervisor to perform a read or a write operation, but it has no bus control capabilities. In Controller Mode, the board can request temporary control of the MULTICHANNEL bus from the bus Supervisor and thus initiate data transfer operations. In its MULTICHANNEL Supervisor configuration, the iSBC 589 has the capability to initiate data transfers on the bus, program other devices on the MULTICHANNEL bus, resolve and grant bus priority to other devices, monitor bus status, handle bus interrupts and control the MULTICHANNEL bus reset line. All of these functions are maintained by the on-board firmware based on parameter inputs from the host. Please refer to the MULTICHANNEL BUS SPECIFICATION for detailed descriptions of these modes.

iSBX™ Bus Capabilities

The iSBC 589 Controller contains two iSBX connectors which can support either 8-bit or 16-bit MULTIMODULE boards. The iSBX connectors are situated so that either two single-wide modules or one single-wide and one double-wide MULTIMODULE board may be installed. A wide variety of standard peripheral controllers and analog and digital I/O MULTIMODULE boards are currently available. In addition, the iSBX connectors provide an opportunity to add over 30 square inches of user designed hardware to the iSBC 589 board which can be used to implement specialized I/O interfaces. For more information on specific iSBX MULTIMODULE boards, consult the Intel OEM Microcomputer System Configuration Guide.

MULTIBUS® Capabilities

MULTIBUS system memory and I/O resources may be used as the source or the destination for an iSBC 589 board transfer operation. The iSBC 589 DMA Controller may also be used as a high-speed data mover to transfer blocks of data from one MULTIBUS system RAM area to another. MULTIBUS system memory may also be used to store Parameter Blocks to be executed by the on-board firmware package. The iSBC 589 board, acting as a MULTIBUS Master, can access up to 16 megabytes of MULTIBUS memory and up to 64K MULTIBUS I/O locations.

Two MULTIBUS transfer modes are available. Selection of the desired mode is done via the Parameter Block. Transfer rates of up to 900K bytes per second may be achieved in shared bus mode, where the iSBC 589 board requests access to the system bus for 1.4 microseconds to transfer one byte or word to or from memory. In BUSLOCK mode, the iSBC 589 is established as the sole master which may access the system bus for the duration of the block data transfer. In BUSLOCK mode, the iSBC 589 board can transfer up to one megabyte per second.

User Command Interface Firmware Package

The iSBC 589 board is supplied with a firmware package contained in two Intel 2732A EPROMs that greatly simplifies programming by providing a high level software interface to the on-board resources. In the majority of applications, the board may be programmed entirely via the firmware and without writing any 8089 IOP assembly language code. The firmware package supports the two channel operation of the 8089 IOP. Each channel has its own Parameter Block area containing the required information for independent channel operation.

To invoke an I/O operation, the user creates one or more Parameter Blocks in memory which describe the desired operation. The firmware, which consists of a series of 8089 IOP assembly language task programs, will interpret the Parameter Blocks to configure the board's interfaces or to perform byte, word or DMA block transfers. Each Parameter Block consists of a command byte, status byte, data source and destination pointers and

other information as shown in Table 1. Commands recognized by the firmware package are listed in Table 2. The Execute User Task command is of special interest because it allows the user to extend the capabilities of the iSBC 589 board by adding his own 8089 IOP assembly language routines to the firmware package, while retaining the structure and standard functions supplied by the firmware.

Table 1. User Command Interface Firmware Parameter Block Byte Format

Command Byte
Status Byte
Command Chaining Pointer
Command Chaining Pointer
Command Chaining Pointer
Command Chaining Pointer
Device Number
MULTICHANNEL Data Type
Memory Pointer or Register Number
Memory Pointer or Register Number
Memory Pointer or Data Storage Location
Memory Pointer or Data Storage Location
Device Number
MULTICHANNEL Data Type
Memory Pointer or Register Number
Memory Pointer or Register Number
Memory Pointer
Memory Pointer
Byte Counter
Byte Counter
Byte Counter

In addition to executing transfer operations, the firmware package executes an initialization sequence which prepares the 8089 IOP and the on-board RAM, EPROM and I/O resources for further firmware execution.

RAM Capabilities

In its standard configuration, the iSBC 589 board contains 8K bytes of high-speed, dual-ported static RAM. The first 256 bytes are dedicated for use by the on-board firmware. The remaining on-board RAM may be used for storing additional Parameter Blocks for the firmware or as a data buffer for I/O operations. This memory is always addressed by the 8089 IOP as locations 0000H to 1FFFH. However, for MULTIBUS accesses through the dual-port, the RAM base address may be configured on any 8K-byte boundary in the first megabyte page of the MULTIBUS memory space. Users may install additional on-board RAM by placing two byte-wide RAMs in the 28-pin JEDEC standard sockets. The additional RAM is accessible only by the on-board 8089 IOP.

EPROM Capabilities

The iSBC 589 board can be configured with up to 32K bytes of non-volatile read only memory. Four 28-pin sockets are provided for the use of Intel 2716, 2732 and 2764 EPROMs or byte-wide RAMs.

Table 2. User Command Interface Firmware Package Commands

Command	Description
NO-OP	Test the intelligent slave interface on the iSBC 589 board. The board reads the Parameter Block, generates status and interrupts the host on completion.
REGISTER WRITE	Write either a word or byte of data from the Data Storage Location within the Parameter Block to the location specified by the Parameter Block Device Number and Register Number.
REGISTER READ	Read either a word or byte of data from the location specified by the Parameter Block Device Number and Register Number to the Data Storage Location within the Parameter Block.
PERFORM DMA	Transfer data beginning at the location specified by the source Memory Pointer, Device Number and Register Number parameters to the location specified by the destination Memory Pointer, Device Number and Register Number parameters. The number of transfers is specified by the Byte Count parameter. A Byte Count of 0 enables DMA until an external terminate condition is sensed.
EXECUTE USER TASK	Transfer 8089 IOP program execution from the Firmware Package to a user defined 8089 assembly language routine beginning at the location specified by the Memory Pointer parameter. Upon completion, the user task returns control to the firmware.

In the default configuration, the board is jumpered for 32K devices, and, two 2732A EPROMs containing the firmware package are installed. Users who wish to extend the capabilities of the firmware may do so by programming unused locations in the firmware PROMs, installing two additional 2732A PROMs or copying the firmware into 2764s along with their own code. As an alternative, two byte-wide RAMs of equal or smaller capacity may be installed in the open sockets and used in conjunction with the firmware PROMs.

Programmable Interval Timers

Three independent, fully programmable 16-bit interval/event counters are provided by an 8254-12 Programmable Interrupt Timer. Each counter may operate in either BCD or binary mode. One counter is used by the firmware package, leaving two counters available to the firmware user. These timers may be used for a variety of on-board and off-board functions including timed-interval DMA requests and terminations or fail safe time out control for I/O operations.

System Development Capabilities

For applications where it is necessary to extend the User Command Firmware Package by writing additional 8089 IOP assembly language code, the development cycle can be significantly reduced and simplified by using the Intellec Series Microcomputer Development Systems. The 8089 IOP Software Support Package which includes a Macro assembler, linker, locater and PROM mapper is supported by the ISIS-II disk-based operating system.

In-Circuit Emulator

The ICE-86A or ICE-86 and ICE-86U upgrade kit provide the necessary link between the software development environment provided by the Intellec system and the "target" iSBC 589 execution system. In addition to providing a mechanism for loading executable code and data into the iSBC 589 board, the In-Circuit Emulator provides a sophisticated command set to assist in debugging software and in final integration of the user hardware and software.

SPECIFICATIONS

8089 IOP

WORD SIZE

Instruction — 16 to 40-bits

Data — 8, 16-bits

SYSTEM CLOCK

5.0 MHz ± 0.1%

CYCLE TIME

2.2 microseconds for the fastest instructions

System Access Time

Dual-port Memory — 550 nanoseconds (worst case, without contention from on-board access)

I/O Capacity

MULTICHANNEL I/O Bus — 1 MULTICHANNEL port which supports 8 and 16-bit transfers and can be configured as a Basic Talker/Listener, Controller or Supervisor

iSBX™ MULTIMODULE™ — Two (2) iSBX MULTIMODULE boards

I/O Addressing

Interface	I/O Addresses
iSBX Connector #1	FF80 thru FF9F
iSBX Connector #2	FFA0 thru FFBF
MULTICHANNEL	FFD0 thru FFEE
Interval Timer	FFC8 thru FFCE
Other On-board Devices	FFC0 thru FFC6 FFF0 thru FFFE

Memory Capacity

ON-BOARD EPROM

Device	Total Capacity	Address Range
2716	8K bytes	$FE000\text{-}FFFFF_H$
2732A	16K bytes	$FC000\text{-}FFFFF_H$
2764	32K bytes	$F8000\text{-}FFFFF_H$

ON-BOARD RAM

Total Capacity — 8K bytes

On-Board Address — $00000\text{-}01FFF_H$

MULTIBUS® Address — Jumper selectable on 8K byte boundaries. Default is 0_H.

I/O Transfer Rates (microseconds/tranfer)

	MULTICHANNEL	iSBX™	MULTIBUS®		On-Board RAM
			Shared	Buslock	
MULTICHANNEL	—	2.0	2.4	2.2	1.8
iSBX	2.0	2.0	2.4	2.2	2.0
MULTIBUS (Shared)	2.4	2.4	2.8	—	2.2
MULTIBUS (Buslock)	2.2	2.2	—	2.4	2.0
On-Board RAM	1.8	1.8	2.2	2.0	1.6

Timers

Input Frequencies — Jumper selectable at 1.25 MHz, 625 KHz or 312.5 KHz

Output Frequencies/Timing Intervals —

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Minimum	Maximum	Minimum	Maximum
Real-time delay	1.6 usec	210 msec	3.2 usec	1.37×10^4 sec
Programmable one-shot	1.6 usec	210 msec	3.2 usec	1.37×10^4 sec
Rate generator	4.76 Hz	625 KHz	7.3×10^{-5} Hz	312.5 KHz
Square-wave rate generator	4.76 Hz	625 KHz	7.3×10^{-5} Hz	312.5 KHz
Software triggered strobe	1.6 usec	210 msec	3.2 usec	1.37×10^4 sec
Hardware triggered strobe	1.6 usec	210 msec	3.2 usec	1.37×10^4 sec

Connectors

Interface	Double-Sided Pins (qty.)	Centers (in.)	Mating Connectors*
MULTIBUS System Bus	86	0.156	ELFAB BS1562043PBB Viking 2KH43/9AMK12 Soldered PCB Mount EDAC 337086540201 ELFAB BW1562D43PBB EDAC 337086540202 ELFAB BW1562A43PBB Wire Wrap
Auxiliary Bus	60	0.100	EDAC 345060524802 ELFAB BS1020A30PBB EDAC 345060540201 ELFAB BW1020D30PBB Wire Wrap
iSBX Bus (2)	36	0.100	iSBX 960-5
MULTICHANNEL Bus	60	0.100	3M 3334-6000 BERG 65949-960

*NOTE: Connectors compatible with those listed may also be used.

Interfaces

MULTIBUS® — All signals TTL compatible

MULTICHANNEL — All signals TTL compatible

iSBX™ Bus — All signals TTL compatible

Timers — All signals TTL compatible

Auxiliary Power/Memory Protect

There is no provision made on the iSBC 589 board for battery backup of RAM or for power fail detection.

MULTIBUS® Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	32
Address	Tri-state	32
Commands	Tri-state	32

Physical Characteristics

Width — 12.00 in (30.48 cm)

Height — 7.05 in (17.9 cm)

Depth — .50 in (1.27 cm)

Weight — 16 oz (453.6 gm)

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Relative Humidity — to 90% (without condensation)

Electrical Characteristics

DC POWER REQUIREMENTS

Configuration	Current Requirements (+5V +5% maximum)
Without EPROM	4.7 amps
With 8K EPROM (using four 2716s)	5.4 amps
With 8K EPROM* (using two 2732As)	5.0 amps
With 16K EPROM (using four 2732As)	5.3 amps
With 32K EPROM (using four 2164s)	5.3 amps

*Factory default configuration

Reference Manuals

142996-001 — iSBC 589 Intelligent DMA Controller Board Hardware Reference Manual (Not Supplied)

142686-001 — Intel iSBX Bus Specification (Not Supplied)

143269-001 — Intel MULTICHANNEL Bus Specification (Not Supplied)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051

ORDERING INFORMATION

Part Number	Description
SBC 589	Intelligent DMA Controller Board