iSBC® 86/35 SINGLE BOARD COMPUTER HARDWARE REFERENCE MANUAL

Order Number: 146245-001

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REV.	REVISION HISTORY	DATE
-001	Original Issue	6/84

PREFACE

This manual provides general information, installation and setup instructions, programming information, board level principles of operation, and service information for the iSBC 86/35 Single Board Computer. Related information is provided in the following publications:

Manual	Number
Microsystem Components Handbook	230843
Memory Components Handbook	210918
The 8086 Family User's Manual	9800722
iSBC® Applications Manual	142687
Intel MULTIBUS® Specification	9800683
Intel MULTIBUS® Interfacing, Application Note	AP-28A
MCS-86 Assembly Language Programming Manual	9800640
PL/M 86 Programming Manual	9800466
Intel iSBX™ Bus Specification	142686
Designing iSBX™ MULTIMODULE™ Boards, Application Note	AP-96
Using the iRMX™ 86 Operating System, Application Note	AP-86
The 8086 Primer, by Stephen P. Morse. Hayden Book Company, Inc., Rochelle Park, N.J., 1980. ISBN: 0-8104-5165-4	
IEEE Microcomputer System Bus Standard 796 Bus	210697

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CHAPTER 1. GENERAL INFORMATION

1.1 INTRODUCTION

The iSBC 86/35 Single Board Computer is a 16-bit computer system with system memory on a single printed circuit board and is compatible with the Intel MULTIBUS and iSBX MULTIMODULE architectures. The iSBC 86/35 board provides 512 K-bytes of dynamic dual port RAM and features 8-MHz CPU operation with I/O expansion via two iSBX bus connectors.

The iSBC 86/35 board is a complete computer system that is designed around the 16-bit iAPX 86/10 HMOS microprocessor (8086 CPU), the primary processing device on the board. The iAPX 86/10 microprocessor operates at an 8-MHz (or optionally at a 5-MHz) clock rate and performs both 8-bit and 16-bit data transfers to and from the board. Processing expansion features are available via the iSBC 337 Numeric Data Processor.

The iSBC 86/35 board can replace both the iSBC 86/30 board and a memory board. Appendix D at the back of this manual contains a brief description of the functional and operational differences between the iSBC 86/35 board and the iSBC 86/30 board. It is shipped with 512 K-bytes of dynamic RAM, four sockets for installation of as many as 256 K-bytes of user-provided EPROM devices, a serial communications port providing an RS232C interface, three parallel I/O ports providing 24 individual I/O lines, two iSBX bus connectors providing interface to either 8-bit or 16-bit MULTIMODULE board expansion, two independently programmable interval timers, and nine levels of interrupt priority including support for bus-vectored interrupts.

The iSBC 86/35 board is MULTIBUS interface compatible and is configurable for operation in a multi-master system environment. The on-board RAM is expandable through addition of the plug-in memory expansion boards available from Intel: the iSBC 304 RAM Expansion MULTIMODULE Board and the iSBC 314 RAM Expansion MULTIMODULE Board.

1.2 DESCRIPTION

The iSBC 86/35 Single Board Computer, shown in Figure 1-1, is a memory intensive processor board designed around the Intel 16-bit iAPX 86/10 Microprocessor (8086 CPU). The iSBC 86/35 board can be configured for compatibility with the software and hardware functions of the iSBC 86/30 board.

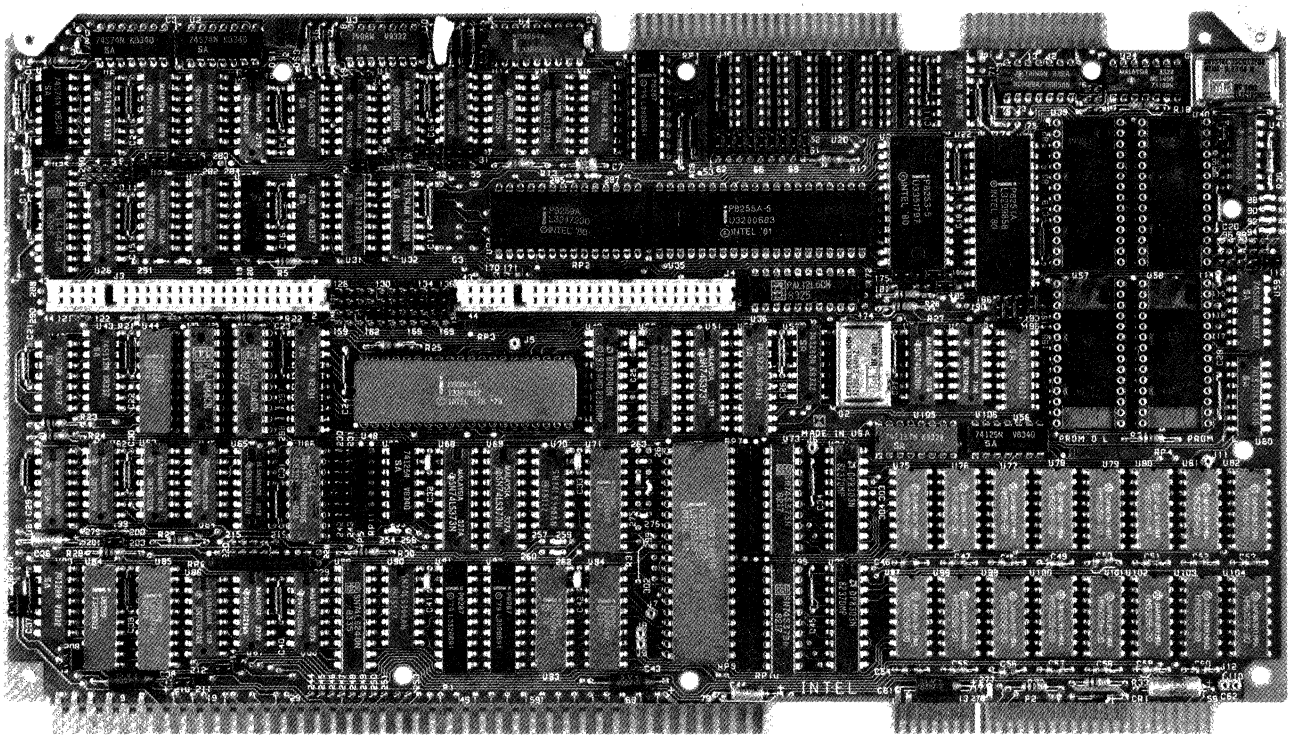

Figure 1-1. iSBC® 86/35 Single Board Computer

The iSBC 86/35 board uses an internal bus during all on-board memory and I/O operations, and uses the MULTIBUS interface during all off-board memory operations. Hence, local (on-board) operations do not involve the MULTIBUS interface and allow true parallel processing in a multi-master system. The following are features of the iSBC 86/35 board.

- 8Ø86 CPU (iAPX 86/1Ø), providing operation at 8- or 5-MHz clock frequency.
- Compatibility with iSBC 86/3Ø Single Board Computer.
- 512 K-bytes of dual-port RAM; expandable to 1 Mbyte on-board.

- Four JEDEC compatible 28 pin sockets for installation of as many as 256 K-bytes of EPROM on board.
- Two iSBX bus connectors, providing either 8-bit or 16-bit interfaces to MULTIMODULE boards.
- +5 volt only power requirement, unless using RS232C interface or certain MULTIMODULE boards.
- 24 programmable parallel I/O lines, through the 8255A Programmable Peripheral Interface.
- 9 levels of interrupt priority, through the 8259A Programmable Interrupt Controller, expandable to 65 levels.
- One serial I/O port, through the 8251A Programmable Communications Interface.
- Two user programmable 16-bit BCD or binary event timers/counters, through the 8253-5 Programmable Interval Timer.
- Full MULTIBUS interface compatibility (IEEE 796 BUS SPECIFICATION).
- 2Ø-bit addressing with bank-select, allowing for access to 16 Mbytes of system memory.

Two iSBX bus interfaces are available on the iSBC 86/35 board. Each is capable of accepting either an 8-bit or a 16-bit iSBX MULTIMODULE board. The J3 and J4 iSBX bus connectors allow additional functions of the iSBC 86/35 board by installing MULTIMODULE boards such as the iSBX 311 Analog Input MULTIMODULE Board, the iSBX 328 Analog Output MULTIMODULE Board, the iSBX 35Ø Parallel I/O MULTIMODULE Board, the iSBX 351 Serial I/O MULTIMODULE Board, and others.

Dual-port control logic is included to interface the dynamic RAM with the MULTIBUS interface so that the iSBC 86/35 board can function as a slave RAM device when not in control of the MULTIBUS interface. The 8Ø86 CPU has priority when accessing on-board RAM. After the CPU completes its read or write operation, the controlling bus master is allowed to access RAM and complete its operation. When both the CPU and the controlling bus master must write or read several bytes or words to or from on-board RAM, the operations are interleaved (unless restricted by MULTIBUS interface control signals).

The slave RAM feature on the board can be configured to allow restricted access by another bus master. Thus, the iSBC 86/35 board can be configured to allow other bus masters to access a segment of the on-board RAM and still reserve another segment strictly for on-board use. The addressing scheme accommodates 16-, 2Ø-, and 24-bit addressing.

Four 28-pin IC sockets are included to accommodate user-installed read only memory. Configuration jumpers allow installation of 16-, 32-, 64-, 128-, or 256-K-bytes of EPROM.

The iSBC 86/35 board includes 24 programmable parallel I/O lines implemented by an Intel 8255A-5 Programmable Peripheral Interface (PPI). Software configures the I/O lines in combinations of unidirectional input/output and bidirectional ports. The I/O interface may be customized to meet specific peripheral requirements; and, in order to take full advantage of the many possible I/O configurations, IC sockets are provided for either I/O line drivers or terminators. Hence, the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application further enhances the flexibility of the parallel I/O interface. The 24 programmable I/O lines and signal ground lines are brought out to 5Ø-pin edge connector J1.

An Intel 8251A Programmable Communications Interface (PCI) device controls and interfaces the RS232C compatible serial I/O port at connector J2. The PCI is programmable for operation in most synchronous or asynchronous serial data transmission formats (including IBM Bi-Synchronous). In both the synchronous and asynchronous modes, the serial I/O port features half- or full-duplex, double-buffered transmit and receive capability on an RS232C compatible interface. In addition, PCI error detection circuits can check for parity, overrun, and framing errors. A programmable baud rate generator supplies the PCI transmit and receive clocks. These clocks may optionally be supplied from an external source. The RS232C command lines, serial data lines, and signal ground lines are brought out to 26-pin edge connector J2.

An Intel 8253-5 Programmable Interval Timer (PIT) provides three independent, fully programmable 16-bit interval timer event counters. Each counter is capable of operating in either BCD or binary modes; two of these counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and trigger inputs of two of these counters may be independently configured in the interrupt jumper matrix. The gate/trigger inputs of the two counters may be controlled by the status register. The third counter is used as a programmable baud rate generator for the serial I/O port.

In using the PIT counters on the iSBC 86/35 board, the systems designer configures each counter independently through software to meet system requirements. Whenever a given time delay or count is required, software commands to the 8253-5 PIT select the desired function. The contents of each counter may be read at any time during system operation with simple operations for event counting applications, and special commands are included so that the contents of each counter can be read "on the fly".

The iSBC 86/35 board provides vectoring for bus-vectored (BV) and non-bus-vectored (NBV) interrupts. An on-board Intel 8259A Programmable Interrupt Controller (PIC) handles as many as eight BV or NBV interrupts. By using external PIC's slaved to the on-board PIC (master), the interrupt structure can be expanded to handle and resolve the priority as many as 64 BV sources.

The PIC, which can be programmed to respond to edge-sensitive or level-sensitive inputs, treats each true input signal condition as an interrupt request. After resolving the interrupt priority, the PIC issues a single interrupt request to the CPU. Interrupt priorities are independently programmable under software control.

The CPU includes a non-maskable interrupt (NMI) and a maskable interrupt (INTR). The NMI is intended for catastrophic events such as power failures that require immediate CPU action. The 8259A PIC generates the INTR interrupt to the CPU and also, upon demand, provides an 8-bit identifier of the interrupting source. The CPU multiplies the 8-bit identifier by four to derive a pointer to the service routine for the interrupting device.

Interrupt requests may originate from 28 sources without the necessity of external hardware. When a byte of information is ready for transfer to the 8Ø86 CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty), the 8255A PPI can automatically generate two jumper selectable interrupt requests. The 8251A PCI can automatically generate two jumper selectable interrupt requests when a character is ready for transfer to the 8Ø86 CPU (i.e., receive channel buffer is full) or when a character is ready to be transmitted (i.e., transmit channel data buffer is empty). In addition, two of the programmable counters can generate a jumper selectable interrupt request; and eight additional interrupt request lines are available to the user for direct interfaces to user designated peripheral devices via the MULTIBUS interface. One interrupt request line may be jumper routed directly from a peripheral via the parallel I/O driver/terminator section, and one power fail interrupt may be applied via auxiliary connector P2.

The iSBC 86/35 board includes resources for supporting a variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (e.g., several CPU's and/or controllers logically sharing system tasks over the MULTIBUS interface), the iSBC 86/35 board provides full bus arbitration control logic. This control logic allows as many as three bus masters (e.g., combination of iSBC 86/35 board, DMA controller, and diskette controller) to share the MULTIBUS interface in serial (daisy-chain) priority fashion or as many as 16 bus masters to share the MULTIBUS interface using an external parallel priority resolving network.

The MULTIBUS interface arbitration logic operates synchronously with the bus clock, which is either provided by the iSBC 86/35 board or generated by some other bus master. Data, however, is transferred via a handshake between the controlling master and the addressed slave module. This arrangement allows controllers that operate at different speeds to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, the transfer speed is dependent on transmitting and receiving devices only. This design prevents handicapping slower master modules in attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high-speed direct memory access (DMA) operations, and high-speed peripheral control; but the capabilities are by no means limited to these three applications.

The iSBC 86/35 board contains programmable resources for sending and receiving a 4-bit bank select address with any 2Ø-bit MULTIBUS address. This feature allows access to one of 16 1-Mbyte pages of MULTIBUS address space and mapping of on-board dual port RAM into any page of that space.

1.3 OPTIONAL RAM EXPANSION

Adding the optional iSBC 3Ø4 RAM Expansion MULTIMODULE Board to the iSBC 86/35 board expands the on-board RAM by 128 K-bytes (for an on-board total of 64Ø K-bytes). Installing the optional iSBC 314 RAM Expansion MULTIMODULE on the board expands the amount of on-board RAM by 512 K-bytes (for an on-board total of 1 Mbyte).

1.4 EQUIPMENT SUPPLIED

Each iSBC 86/35 board is shipped with a current revision of the schematic diagram. No other equipment is provided with the iSBC 86/35 board.

1.5 EQUIPMENT REQUIRED

Because the iSBC 86/35 board is designed to be used in a variety of applications, the user need purchase and install only those components required to satisfy his particular requirements. A list of components required to configure the iSBC 86/35 board is provided in Chapter 2.

1.6 COMPLIANCE LEVEL: 796 BUS SPECIFICATION (IEEE STANDARD)

All Intel MULTIBUS-compatible boards are designed around guidelines set forth in the 796 BUS SPECIFICATION (IEEE STANDARD - formerly the Intel MULTIBUS Specification). The standard requires that certain board operating characteristics, such as data bus width and memory addressing paths, be clearly stated in the board's printed specifications (i.e., reference manual). Used properly, this information quickly summarizes the level of compliance that board bears to the published 796 BUS SPECIFICATION. It clearly states the board's level of compatibility to the MULTIBUS structure. Refer to the 796 BUS SPECIFICATION or the INTEL MULTIBUS SPECIFICATION for additional information.

The following notation states the iSBC 86/35 board's level of compliance to the 796 BUS SPECIFICATION:

D16 M2Ø/24 I16 VØ EL

This notation is decoded as follows:

D16 = data path is 8 and/or 16 bits
M24 = memory address path is up to 24 bits
I16 = I/O address path is 8 or 16 bits
VØ = Non-bus-vectored interrupts are supported; and
EL = Level-triggered and Edge-triggered interrupts are supported

1.7 COMPLIANCE LEVEL: INTEL iSBX™ BUS SPECIFICATION

All Intel iSBX bus-compatible boards are designed around guidelines set forth in the Intel iSBX BUS SPECIFICATION. The standard requires that certain board operating characteristics, such as data bus width and employment of interlocked operation, be clearly stated in the board's printed specifications (i.e., reference manual). Used properly, this information quickly summarizes the level of compliance the board bears to the published iSBX BUS SPECIFICATION. It clearly states the board's level of compatibility to the iSBX bus structure. Refer to the iSBX BUS SPECIFICATION for additional information.

The following notation states the iSBC 86/35 board's level of compliance to the iSBX BUS SPECIFICATION:

D8/16

This notation is decoded as follows:

D8/16 = A 16-bit CPU board that can interface to an 8-bit expansion module.

1.8 SPECIFICATIONS

Specifications of the iSBC 86/35 Single Board Computer are listed in Table 1-1.

Table 1-1. Specifications

PHYSICAL CHARACTERISTICS	
Width:	12.ØØ in. (3Ø.48 cm)
Height:	6.75 in. (17.15 cm)
Depth:	Ø.7Ø in. (1.78 cm)
Weight:	14 oz (388 gm)

Table 1-1. Specifications (continued)

WORD SIZE	
Instruction:	8, 16, 24, 32, 4Ø, or 48 bits.
Data:	8 or 16 bits.
SYSTEM CLOCK SPEED	8 MHz or 5 MHz, jumper selectable.
INSTRUCTION CYCLE TIME	
8 MHz:	75Ø ns. 25Ø ns (assumes that instruction is in the queue).
5 MHz:	1.2 us. 4ØØ ns (assumes that instruction is in the queue).
MEMORY CYCLE TIME (8-MHz)	
RAM:	75Ø ns.
EPROM:	5ØØ to 875 ns, jumper selectable.
MEMORY ARRAY	
On-Board EPROM:	4 device sockets; user-provided EPROM devices in 8 k by 8-bit, 16 k by 8-bit, 32 k by 8-bit, or 64 k by 8-bit capacity.
On-Board Dynamic RAM:	512 K-bytes of dynamic RAM (64Ø K-bytes if iSBC 3Ø4 RAM Expansion MULTIMODULE Board is installed or 1 Mbyte if iSBC 314 RAM Expansion MULTIMODULE Board is installed); data integrity maintained during power failure with user-furnished batteries.
Off-Board Expansion:	Up to 16 Mbytes of user-specified combination of RAM, ROM, and EPROM.
MEMORY ADDRESS RANGES	
On-Board EPROM:	F8ØØØ-FFFFFH (using 8 k by 8 bit EPROM's), FØØØØ-FFFFFH (using 16 k by 8-bit EPROM's), EØØØØ-FFFFFH (using 32 k by 8-bit EPROM's), DØØØØ-FFFFFH (using 64 k by 8-bit EPROM's).

Table 1-1. Specifications (continued)

On-board Dual Port RAM (local CPU Access):	ØØØØØ-7FFFFH, as-shipped configuration. ØØØØØ-9FFFFH, if iSBC 3Ø4 RAM Expansion MULTIMODULE Board is installed. ØØØØØ-DFFFFH, if iSBC 314 RAM Expansion MULTIMODULE Board is installed. or ØØØØØ-EFFFFH
On-board RAM (MULTIBUS Interface Access):	Jumpers allow the board to act as slave RAM device for access by another bus master. Default MULTIBUS address of dual-port RAM is set at ØØØØØH through 7FFFFH; all on-board RAM is dual ported. MULTIBUS addresses (for dual-port RAM) may begin at Ø, 64 k, 128 k, or 256 k. When the iSBC 314 is installed, the MULTIBUS address of RAM may end at DFFFFH, EFFFFH, or FFFFFH.
I/O CAPABILITY	
Parallel:	24 programmable I/O lines using the 8255A PPI.
Serial:	1 programmable RS232C interface using the 8251A PCI.
Expansion:	2 iSBX bus connectors providing expansion through either single- or double-wide, 8- or 16-bit, MULTIMODULE boards.
SERIAL COMMUNICATIONS CHARACTERISTICS	
Synchronous:	5- to 8- bit characters; internal or external character synchronization; automatic sync bit insertion.
Asynchronous:	5- to 8- bit characters; break character generation; 1, 1 1/2, or 2 stop bits; false start bit detection.
TIMER FREQUENCIES	
	2.46 MHz ± Ø.1% Reference 1.23 MHz ± Ø.1% 153.6 kHZ ± Ø.1%

Table 1-1. Specifications (continued)

ELECTRICAL REQUIREMENTS

SUPPLY (Note 4)	+5V (Note 1) Typ	+5V (Note 1) Max	+5VB Typ	+5VB Max	+12V Typ	+12V Max	-12V Typ	-12V Max
Standard Bd	3.9A	4.4A	Ø.35A	Ø.84A	Ø.Ø16A		Ø.ØØ6A	
ADD FOR EPROM	Note 2	Note 2	---	---	---	---	---	---
ADD FOR 3Ø4 (Note 3)	Ø	Ø	Ø.Ø6A	Ø.14A	---	---	---	---
ADD FOR 314 (Note 3)	Ø	Ø	Ø.Ø6A	Ø.14A	---	---	---	---
ADD FOR EACH iSBX BD.	Note 2	Note 2	---	---	Note 2	Note 2	Note 2	Note 2
ADD FOR 337	Note 2	Note 2	---	---	---	---	---	---

Notes:
1. When Battery Backup option is not used, both +5V and +5VB requirements must be supplied through the +5V bus.
2. Refer to data sheet of device used.
3. This is not the total current drawn by the MULTIMODULE. It is the additional current required by the system when the MULTIMODULE is added, because only one set of RAMs can be active at a time.
4. Typical values measured at room temperature with Vcc = 5.ØV and processor running at 8 MHz.

ENVIRONMENTAL REQUIREMENTS

OPERATING:
- Temperature: Ø°C to 55°C with 2ØØLFM air flow.
- Relative Humidity: to 9Ø%, non-condensing.

STORAGE:
- Temperature: -4Ø°C to +75°C.
- Relative Humidity: to 9Ø%, non-condensing.

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CHAPTER 2. PREPARATION FOR USE

2.1 INTRODUCTION

This chapter provides instructions for preparing the iSBC 86/35 Single Board Computer for use in a user-defined environment. Included in this chapter are instructions on unpacking and inspection; installation considerations; component installation; jumper configuration; interface configuration for the MULTIBUS, the iSBX bus and the serial bus interfaces; and board installation information. The user should have a firm understanding of the contents of Chapters 1 and 4 of this manual before beginning the configuration and installation procedures contained in this chapter.

2.2 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that the salvageable shipping cartons and packing material be saved for future use in the event that the product must be shipped.

2.3 INSTALLATION CONSIDERATIONS

The following paragraphs outline installation considerations such as power, cooling, and physical size requirements.

2.3.1 POWER REQUIREMENTS

The iSBC 86/35 board requires only a +5 volt power source unless the RS232C interface is used or a MULTIMODULE board that requires ±12 volts is added to the system. However, even if neither the RS232C interface nor a MULTIMODULE board is used the iSBC 86/35 board will still draw current at ± 12V as specified in Table 1-1 if these voltages are supplied at the MULTIBUS connector P1. In such an instance, the iSBC 86/35 board passes ±12 volt power from the MULTIBUS interface to the MULTIMODULE board. The +5 volt supply current requirement varies, dependent upon the type and number of user-furnished EPROM devices installed on the board, and the types of iSBC expansion or iSBX I/O expansion MULTIMODULE boards installed on the board. Table 1-1 lists the various current requirements for each type of memory device and for each interface configuration.

2.3.2 COOLING REQUIREMENTS

The iSBC 86/35 board dissipates 45Ø.14 gram-calories of heat per minute (1.96 BTU per minute) and adequate circulation of air must be provided to prevent the temperature from exceeding 55°C (131° F).

2.3.3 PHYSICAL DIMENSIONS

The outside dimensions of the iSBC 86/35 board are as follows:

a. Width: 3Ø.48 cm (12.ØØ inches)
b. Length: 17.15 cm (6.75 inches)
c. Thickness: 1.78 cm (Ø.7Ø inch).

Greater detail of the outside dimension of the iSBC 86/35 board may be obtained from Chapter 5.

2.4 DEFAULT CONFIGURATION OVERVIEW

Table 2-1 presents the default configuration of the functional areas to be configured on the iSBC 86/35 board with references to the corresponding sections of this manual.

2.5 JUMPER CONFIGURATIONS

Much of the flexibility of your iSBC 86/35 board is due to the use of jumper connections that may be easily altered from the factory configurations to suit your particular applications. Sections 2.5.1 through 2.5.1Ø describe optional jumper connections for all of the iSBC 86/35 configurations. Appendix A lists the jumper connections in numerical order and the factory default connections.

Table 2-1. iSBC® 86/35 Board Default Configuration

Function	Default Configuration	Primary Reference	Related Reference
EPROM	Four 2764 (8 k x 8) 32 K-bytes total F8000H - FFFFFH.	2.5.1.3	2.7.1 for installation and all of 2.5.1.
RAM Local Address	Address Ø to 7FFFFH no RAM expansion MULTIMODULES.	2.5.1.4	All of 2.5.1 and Appendices B and C.
RAM MULTIBUS Address	Address Ø to 7FFFFH on each Mbyte page. None private. No RAM expansion.	2.5.1.5	All of 2.5.1 and Appendices B and C.
CPU access to system	2Ø-bit addressing. 1Mbyte address space.	2.5.1.6	All of 2.5.1
CPU Speed	8 MHz	2.5.2	
Wait States	2 for EPROM, 2 for I/O	2.5.2	
Interval Timer	Timer Ø: 1.23 MHz clk, output to PIC IR2. Timer 2: 1.23 MHz clk, output to PCI.	2.5.3	2.5.5, 2.5.6 for timer outputs and 2.5.8 for gate inputs.
Parallel Interface	Port A: output only. Port B: need driver/terminator. Port C: Basic I/O (mode Ø).	2.5.4	2.7.2 driver/terminator installation, 2.5.3 PIT, 2.5.5 interrupts, 2.5.6 serial interface, 2.8 power fail.
Interrupts	NMI disabled. IR2 from timer Ø IR5 from MULTIBUS INT 5. Bus vectored and non-bus vectored interrupts.	2.5.5	2.5.3 PIT, 2.5.4 parallel interface, 2.5.6 serial interface, 2.5.7 timeout, 2.5.8 status register, 2.5.9 iSBX bus, 2.8 power fail.
Serial Interface	RS232 Data Set. Transmit and receive clocks from PIT timer 2.	2.5.6	2.5.3 PIT, 2.5.4 parallel interface, 2.5.5 interrupts.
MULTIBUS Timeout	Timeout enabled - No indefinite wait.	2.5.7	2.5.5 interrupts.
Status Register	Two LED's and OVERRIDE (for dual port lock) are controllable.	2.5.8	2.5.1.1 & 2.5.1.6 memory, 2.5.3 PIT, 2.5.5 interrupts, 2.5.1Ø for MULTIBUS control.
MULTIBUS Interface Control	Driven: BCLK, CCLK, BPRO. Not driven: lock CBRQ to bus. ANYRQST HIGH: lower priority master may request arbitration.	2.5.9	2.5.8 status register.
Battery Backup	Battery backup/power fail option not selected.	2.8	2.5.4 parallel interface, 2.5.5 interrupts.

2.5.1 MEMORY JUMPER CONFIGURATION

When using the iSBC 86/35 board, one of your first tasks is to determine the amount of memory (both on-board and off-board) required to satisfy your particular application.

Because the configuration requirements are different, the information is separated into the following subsections:

2.5.1.1 Memory Jumper Configuration Overview

The iSBC 86/35 board memory is located by assigning two memory addresses: the local address and the MULTIBUS address. The local memory address is a 2Ø-bit address used by the 8Ø86 CPU to access the local memory. Local memory involves both EPROM and RAM resources. The EPROM resource is only accessible to the 8Ø86 CPU. The RAM resource is accessible to both the 8Ø86 CPU and a remote CPU. The MULTIBUS address is a 24-bit address used by other bus masters to gain access to the jumper selectable portion of the RAM resource. A remote CPU accesses the iSBC 86/35 board RAM after resolving system bus arbitration. The portion of RAM that is available to both the local CPU and the remote CPU is called dual-port RAM.

Configuring the iSBC 86/35 board memory involves four areas.

First, the EPROM device type is selected and the appropriate jumpers configured. EPROM is accessible only by the on-board CPU and not by other bus masters.

Second, the local address range of the RAM is configured. This choice depends on whether a RAM expansion MULTIMODULE is used. In the case of the iSBC 314 RAM expansion module, there is also a choice regarding the amount of RAM available to the on-board CPU.

Third, the MULTIBUS address range of the RAM is selected. Some or all of the RAM may be excluded from access by other MULTIBUS masters. Also the page address of the board may be selected. This determines to which of 16 1-Mbyte pages the iSBC 86/35 board will respond. Combinations of local address and MULTIBUS address can be used to define portions of memory as 86/35 private, MULTIBUS private, or shared (dual port).

Finally, jumpers are configured to determine the method used by the iSBC 86/35 board to access other system memory. Specifically, CPU access to on-board RAM above 128 K-byte may be temporarily disabled under program control to allow a larger range of accesses to MULTIBUS resources.

2.5.1.2 Memory Map (As-Shipped Configuration)

The iSBC 86/35 board is shipped with 512 K-bytes of RAM. The default jumper configuration assigns the RAM address range between ØØØØØH and 7FFFFH (512 K-bytes) and allocates all 512 K-bytes as dual-port address space (that is, all 512 K-bytes are available as a MULTIBUS memory resource as well as a local memory resource). The 1 Mbyte page select function is disabled. This means that the dual-port RAM will respond to every page.

When you receive your iSBC 86/35 board, you must install EPROM devices (containing a boot loader, monitor, or firmware program) into the byte-wide JEDEC sockets before you can use the board. You can install two or four 8 k x 8 devices into the JEDEC sockets (U39/U57 and U4Ø/U58) without reconfiguring the EPROM address range select jumpers. This immediate jumper configuration and the installation of four 8 k x 8 EPROM devices provides the upper 32 K-bytes of local memory that is accessible from F8ØØØH to FFFFFH. This memory is not accessible via the MULTIBUS to other CPU boards.

Figure 2-1 shows the default memory map configuration.

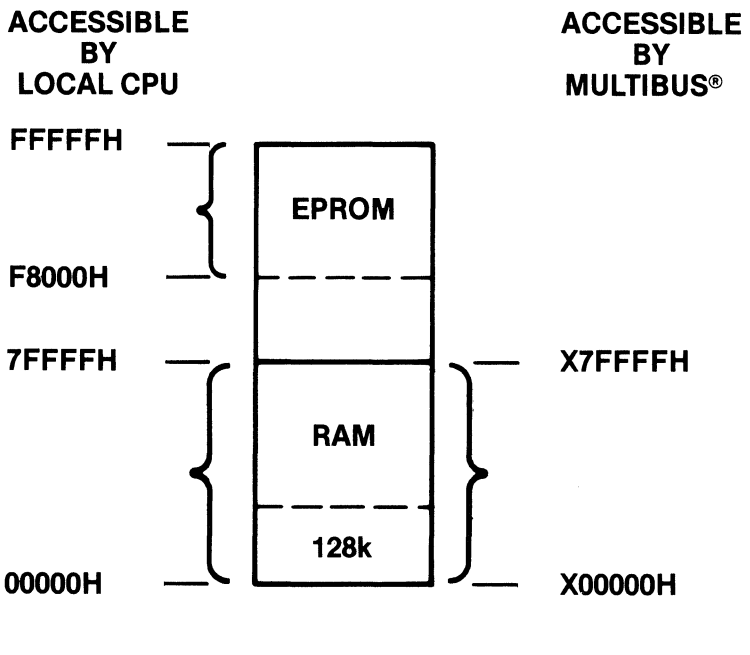

Figure 2-1. iSBC® 86/35 Default Memory Map

2.5.1.3 EPROM Jumper Configuration

The iSBC 86/35 board EPROM configuration involves installation of two or four devices. There are four different EPROM sizes that could be installed. The different sizes are jumper selectable. Table 2-2 lists the jumper configuration to select the device size and the corresponding address range. EPROM space is located from the top of memory (FFFFFH) down toward the bottom of memory. The address space depends on the size and the number of the devices installed. Thus, when four 8 k x 8 devices are installed onto the iSBC 86/35 board, the bottom of the EPROM address space is F8ØØØH.

A maximum of 256 K-bytes may be installed in the four sockets, using four 64 k x 8 byte 28-pin devices. Refer to Figure 2-2 for EPROM stake pin locations and corresponding default jumpers. Refer to section 2.6.1 for the EPROM device installation procedure.

Table 2-2. EPROM Jumpers and Address Assignments

Socket Address Assignments				
EPROM Type	Device Capacity	Bank Ø U57, U39	Bank 1 U58, U4Ø	Jumpers Required
2764	8 k x 8	F8ØØØ-FBFFF	FCØØØ-FFFFF	Factory default. E98-E99, E98-E1Ø4, plus see Note 1.
27128	16 k x 8	FØØØØ-F7FFF	F8ØØØ-FFFFF	E98-E99, E98-E1Ø4, E124-E125, E1Ø9-E11Ø, plus see Note 1.
27256	32 k x 8	EØØØØ-EFFFF	FØØØØ-FFFFF	E98-E99, E98-E1Ø4, E123-E124, E1Ø9-E11Ø, E1ØØ-E1Ø1, E1ØØ-E1Ø6, plus Note 1.
27512	64 k x 8	CØØØØ-DFFFF	EØØØØ-FFFFF	E123-E124, E124-E125, E99-E1Ø5, E1Ø4-E1Ø5, E1Ø9-E11Ø, E1ØØ-E1Ø1, E1ØØ-E1Ø6, plus Note 1.

Notes:
1. In addition to the above listed jumpers, all four device sizes require that the following jumpers be installed: E88-E89, E9Ø-E91, E92-E93, E94-E95, E96-E97, E96-E1Ø2, E112-E113.
2. The jumpers listed in this table are the only jumpers that should be installed at E82, E83, E86 thru E113, E116, E117, E123 through E125, E197, and E198.
3. Socket addresses are reserved for both banks Ø and Bank 1, even if only Bank 1 is used.

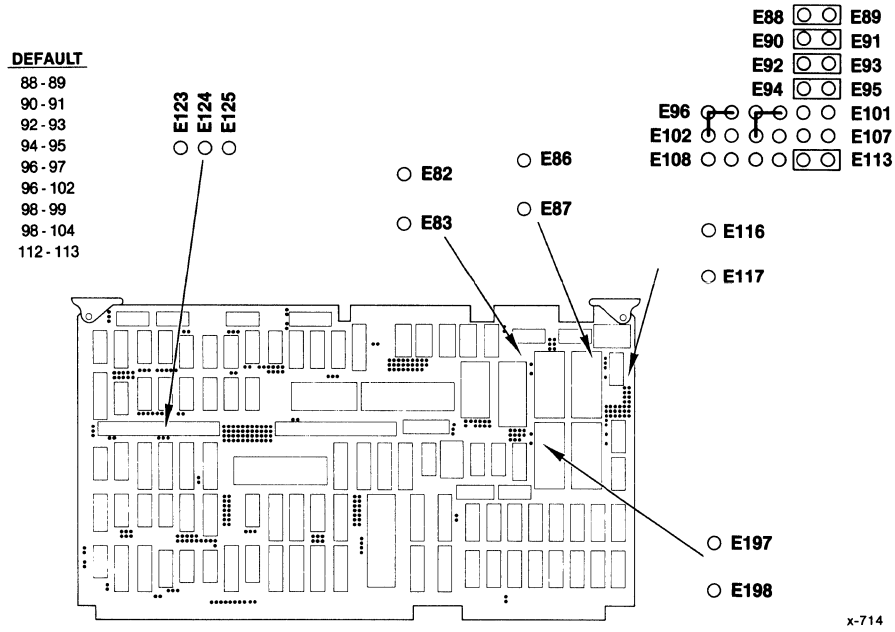

Figure 2-2. EPROM Stake Pin Locations

2.5.1.4 RAM Local Address Jumper Configuration

This section deals only with the on-board CPU accessing on-board RAM. The iSBC 86/35 board is shipped with 512 K-bytes of dynamic RAM installed.

With the default jumpers installed, the memory address range for RAM is from Ø to 512 K-bytes (ØØØØØH to Ø7FFFFH). There are two ways to increase the size of RAM space. Install either an iSBC 3Ø4 RAM expansion module or an iSBC 314 RAM expansion module. The installation of a iSBC 3Ø4 RAM expansion module increases the size of RAM from 512 K-bytes to 64Ø K-bytes. When you add an iSBC 3Ø4 board to the iSBC 86/35 board, the RAM address range available to the on-board CPU is ØØØØØH to Ø9FFFFH. The installation of an iSBC 314 RAM expansion module increases the size of RAM from 512 K-bytes to 1 Mbyte. However, the amount of EPROM space shadows the upper portion of the RAM space making it inaccessible to the on-board CPU. The amount of RAM available is determined by RAM jumpers and is not automatically selected by EPROM jumpers. Thus, when you add a iSBC 314 board to the iSBC 86/35 board, the RAM address range available to the on-board CPU is either ØØØØØH to ØDFFFFH or ØØØØØH to ØEFFFFH.

You may choose to make RAM continuous with EPROM or you may leave a gap, but the two must not overlap. Refer to Figure 2-3 for RAM local address stake pin locations and corresponding default jumpers. Refer to Table 2-3 for RAM decode jumper configurations.

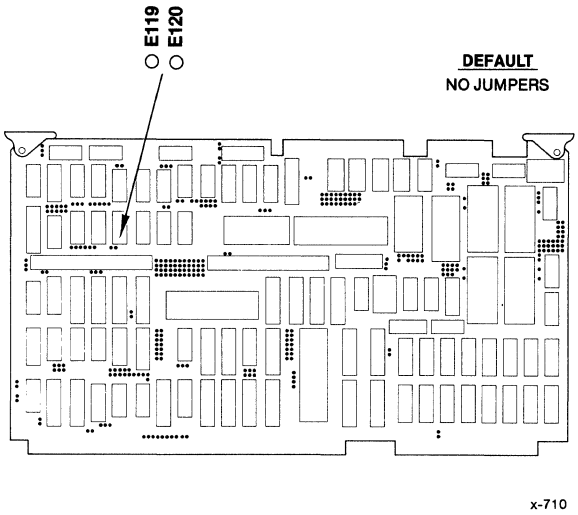

Figure 2-3. RAM Local Address Stake Pin Locations

Table 2-3. RAM Local Address Range Selection

Configuration	Amount Available to On-Board CPU	Address Range	Jumper E119 to E12Ø
iSBC 86/35 only	512 k	Ø to 7FFFFH	Out
iSBC 86/35 + iSBC 3Ø4	64Ø k	Ø to 9FFFFH	In
iSBC 86/35 + iSBC 314	896 k	Ø to DFFFFH	Out
iSBC 86/35 + iSBC 314	96Ø k	Ø to EFFFFH	In

2.5.1.5 RAM MULTIBUS® Address Jumper Configuration

This section deals only with other bus masters accessing RAM on the iSBC 86/35 board. The on-board EPROM cannot be accessed by other bus masters.

As shipped, the iSBC 86/35 board decodes only the 2Ø MULTIBUS address lines on the P1 connector. This is for use in a system that does not use the four address lines on the P2 connector that specify the 1-Mbyte page.

For use in a system that uses the 1-Mbyte page address lines, you can make the iSBC 86/35 board respond to only one page by installing jumper E218 to E223 and selecting the desired page according to Table 2-4.

Within the selected page, you can select the starting address (of the dual-port RAM) that is available to the MULTIBUS interface; that is, you can select the beginning of your MULTIBUS address sequence. When an iSBC 314 RAM Expansion Module is installed onto the iSBC 86/35 board, you can also select the ending address available. Refer to Figure 2-4 for RAM MULTIBUS address stake pin locations and corresponding default jumpers. Table 2-5 lists the jumpers that select the MULTIBUS address range.

If you wish to prohibit accesses by another board to the dual-port RAM, you must install a jumper E199 to E2ØØ.

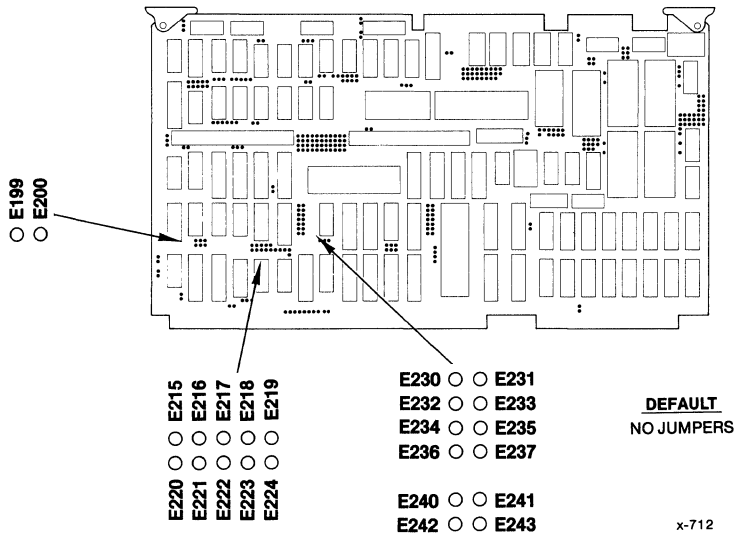

Figure 2-4. RAM MULTIBUS® Address Stake Pin Locations

Table 2-4. 1-Mbyte Address Selection

Page Selected	Jumpers Installed			
	E219-E224	E217-E222	E216-E221	E215-E22Ø
Ø	Out	Out	Out	Out
1	Out	Out	Out	In
2	Out	Out	In	Out
3	Out	Out	In	In
4	Out	In	Out	Out
5	Out	In	Out	In
6	Out	In	In	Out
7	Out	In	In	In
8	In	Out	Out	Out
9	In	Out	Out	In
A	In	Out	In	Out
B	In	Out	In	In
C	In	In	Out	Out
D	In	In	Out	In
E	In	In	In	Out
F	In	In	In	In

Notes: 1. The configuration to implement the page select function requires the installation of jumper E218-E223 to connect the address lines to the decoder.

2. The configuration to implement the denial of MULTIBUS access requires the installation of jumper E199 to E2ØØ.

Table 2-5. RAM MULTIBUS® Address Range Selection

Board Combination	Address Range Available to Other Bus Masters	Jumpers Between						
		E199 E2ØØ	E23Ø E231	E232 E233	E234 E235	E236 E237	E24Ø E241	E242 E243
86/35	None	In	X	X	X	X	X	X
	ØØØØØH to 7FFFFH	Out	Out	Out	Out	Out	X	X
	1ØØØØH to 7FFFFH	Out	Out	Out	Out	In	X	X
	2ØØØØH to 7FFFFH	Out	Out	Out	In	Out	X	X
	4ØØØØH to 7FFFFH	Out	Out	Out	In	In	X	X
86/35 + 3Ø4	None	In	X	X	X	X	X	X
	ØØØØØH to 9FFFFH	Out	Out	In	Out	Out	X	X
	1ØØØØH to 9FFFFH	Out	Out	In	Out	In	X	X
	2ØØØØH to 9FFFFH	Out	Out	In	In	Out	X	X
	4ØØØØH to 9FFFFH	Out	Out	In	In	In	X	X

Table 2-5. RAM MULTIBUS® Address Range Selection (continued)

Board Combination	Address Range Available to Other Bus Masters	Jumpers Between						
		E199 E2ØØ	E23Ø E231	E232 E233	E234 E235	E236 E237	E24Ø E241	E242 E243
86/35 + 314	None	In	X	X	X	X	X	X
	ØØØØØH to FFFFFH	Out	In	Out	Out	Out	Out	Out
	1ØØØØH to FFFFFH	Out	In	Out	Out	In	Out	Out
	2ØØØØH to FFFFFH	Out	In	Out	In	Out	Out	Out
	4ØØØØH to FFFFFH	Out	In	Out	In	In	Out	Out
	ØØØØØH to EFFFFH	Out	In	Out	Out	Out	Out	In
	1ØØØØH to EFFFFH	Out	In	Out	Out	In	Out	In
	2ØØØØH to EFFFFH	Out	In	Out	In	Out	Out	In
	4ØØØØH to EFFFFH	Out	In	Out	In	In	Out	In
	ØØØØØH to DFFFFH	Out	In	Out	Out	Out	In	Out
	1ØØØØH to DFFFFH	Out	In	Out	Out	In	In	Out
	2ØØØØH to DFFFFH	Out	In	Out	In	Out	In	Out
	4ØØØØH to DFFFFH	Out	In	Out	In	In	In	Out

Note: X = irrelevant

2.5.1.6 Jumper Configuration For Accessing Off-Board Memory Resources

Some MULTIBUS systems use only the 2Ø address lines on the P1 connector, which allow addressing a 1-Mbyte address space. Other systems may also use the four extra address lines available on the P2 connector to address a 16-Mbyte address space. The 8Ø86 CPU on the iSBC 86/35 board uses only 2Ø address lines, but additional circuitry on the board allows operation in either a 2Ø-bit or 24-bit address system. Refer to Figure 2-5 for stake pin locations and default jumpers for accessing off-board memory. Because the jumper configuration is different for these two cases, this section is divided into 2Ø-bit address systems and 24-bit address systems.

For purposes of the following description, assume that the top of RAM refers to the highest RAM local address accessible by the on-board CPU (as selected in Table 2-3), and the bottom of EPROM refers to the lowest address reserved for EPROM (as selected in Table 2-2).

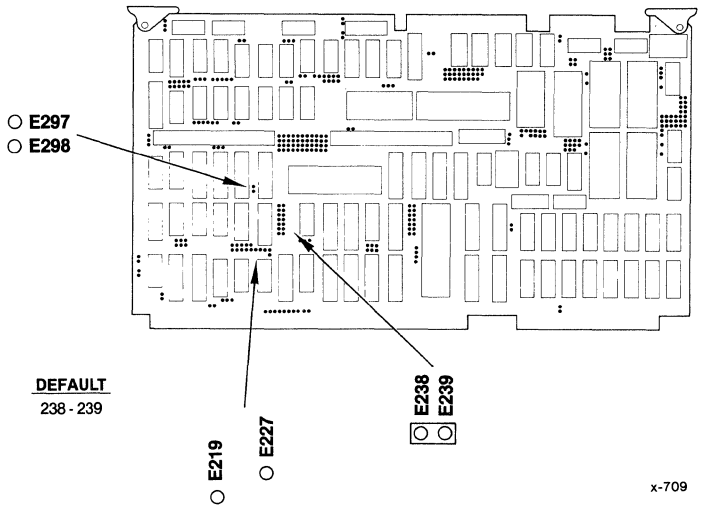

Figure 2-5. Accessing Off-Board Address Stake Pin Locations

Accesses to 2Ø-bit address systems

Certain ranges of MULTIBUS memory are inaccessible by the iSBC 86/35 board. These ranges are ØØØØØH to 1FFFFH and from the bottom of EPROM to FFFFFH. On-board memory addresses from ØØØØØH to 1FFFFH and the bottom of EPROM to FFFFFH are always accessible by the on-board CPU.

MULTIBUS memory from 2ØØØØH to the top of RAM can be accessed only by temporarily disabling local access to the on-board RAM within that range. This is done by removing jumper E238 to E239 and installing jumper E297 to E298 and using bit Ø of the status register to control the enabling and disabling of local access to this range of RAM. Refer to Chapter 3 for information on programming the status register.

Jumper E219 to E227 allows you to determine whether a 1 in status register bit Ø enables or disables this range of RAM. If jumper E219 to E227 is removed and you program bit Ø of the status register as a 1, this disables local RAM access within the range from 2ØØØØH to the top of RAM, allowing the on-board CPU to access the MULTIBUS memory resource within that range. When you program bit Ø of the status register as a Ø, this

allows the on-board RAM to respond. No MULTIBUS access occurs. With jumper E219 to E227 installed, the effects of Ø and 1 in status register bit Ø are reversed.

MULTIBUS memory between the top of RAM and the bottom of EPROM can always be accessed, regardless of the state of status register bit Ø or the position of jumpers E219 to E227, E238 to E239, and E297 to E298.

Accesses to 24-bit address systems

The Megabyte page register allows the on-board CPU with 2Ø address lines to access MULTIBUS boards with 24 address lines. One of the 16 1-Mbyte pages is selected by performing I/O writes to the Megabyte page register and the status register. See Chapter 3 for information on programming these registers.

Certain ranges of MULTIBUS memory on each page are inaccessible by the iSBC 86/35 board. These ranges are from ØØØØØH to 1FFFFH and from the bottom of EPROM to FFFFFH. For a range to be inaccessible on each page means that the range YØØØØH to Y1FFFFH (where Y equals the page number) cannot be accessed on the MULTIBUS, regardless of the number of page Y. In these MULTIBUS inaccessible ranges on each page, the on-board resources (RAM or EPROM) will always respond, making it appear that both are duplicated on every page.

MULTIBUS memory on each page from 2ØØØØH to the top of RAM can be accessed only by temporarily disabling local access to the on-board RAM within that range. The enabling/disabling of local access to this RAM and the disabling/enabling of the page drivers are controllable simultaneously by status register bit Ø. Note the distinction between the Megabyte page register, which contains the page number, and the Megabyte page drivers, which allow the contents of the Megabyte page register to be either driven onto connector P2 during accesses or left floating. To implement this scheme, remove jumper E238 to E239 and install jumper E297 to E298. Jumper E219 to E227 is usable to determine which state of status register bit Ø causes the disabling of local access to RAM and the enabling of the Megabyte page drivers. If jumper E219 to E227 is removed and you program a 1 in status register bit Ø, this disables local RAM access from 2ØØØØH to the top of RAM and enables the Megabyte page drivers, allowing the on-board CPU to access the MULTIBUS in that range instead. If you program a Ø in status register bit Ø, this disables the Megabyte page drivers, allowing the on-board RAM to respond. No MULTIBUS access occurs. With jumper E219 to E227 installed, the effects of Ø and 1 in status register bit Ø are reversed.

MULTIBUS memory on each page from the top of RAM to the bottom of EPROM can be accessed using the same scheme as previously described. The Megabyte page register contains the desired page number and status register bit Ø is used to enable/disable the Megabyte page drivers. Note that enabling the Megabyte page drivers still disables local RAM access from 2ØØØØH to the top of RAM. For this reason, you should not leave the Megabyte page drivers enabled continuously.

Page Ø between the top of RAM and the bottom of EPROM can be accessed in two different ways. One way, as previously described, is to load the Megabyte page register with the bits corresponding to page Ø and to enable the Megabyte page driver. As before, this disables local access to on-board RAM from 2ØØØØH to the top of RAM. The other method is to leave the Megabyte page drivers disabled and simply perform the access. Because the passive state of the four upper address lines on connector P2 is page Ø, only the resource at page Ø on the MULTIBUS will respond. This method has the advantage that no local access to any RAM had been disabled. Also, no I/O writes are required to change from accessing on-board memory to accessing off-board memory.

In some cases, it may be desirable to enable the Megabyte page drivers without disabling local access to any on-board RAM. This can be accomplished by replacing PAL U46. Refer to Appendix G for more information.

In some systems that use boards with 2Ø address lines and boards with 24 address lines, PAL U45 can be reprogrammed to reduce the number of I/O writes required to enable/disable the Megabyte page drivers. Refer to Appendix G for more information.

2.5.2 CPU SPEED AND WAIT STATE JUMPER CONFIGURATION

The iSBC 86/35 board wait state circuitry contains several jumpers (E4 through E14) that select the number of wait states to be inserted into the CPU execution cycles during EPROM and I/O accessing operations. These jumpers allow selection of zero to three wait-states for EPROM accesses and one or two wait states for I/O accesses. An EPROM access requires from zero to three wait-states depending on the type of device involved and an I/O access requires one or two wait-states depending on whether a 5-MHz or 8-MHz clock rate is selected. CPU clock rate is determined by jumpers E36-E37. Refer to Figure 2-6 for CPU speed and wait state stake pin locations and default jumpers. Table 2-6 lists the CPU speed and wait state jumper configuration.

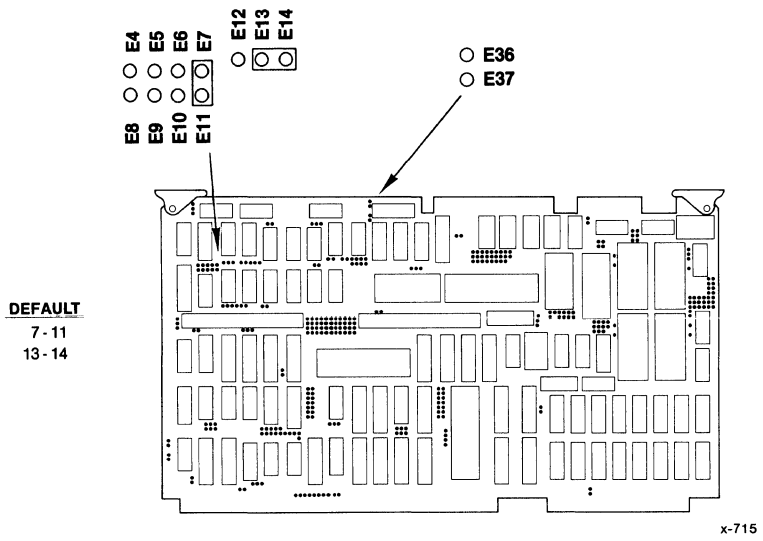

Figure 2-6. CPU Speed and Wait State Stake Pin Locations

Table 2-6. CPU Speed and Wait State Jumper Configuration

No. of Wait States	EPROM Accesses			I/O Accesses		
	Access Time		Jumpers	Access Time		Jumpers
	5 MHz	8 MHz		5 MHz	8MHz	
Ø	454ns	228ns	Remove E7-E11 Install E4-E8			---
1	654ns	353ns	Remove E7-E11 Install E5-E9	538ns		Remove E13-E14 Install E12-E13
2	854ns	478ns	Install E7-E11		438ns	Install E13-E14
3	1Ø54ns	6Ø3ns	Remove E7-E11 Install E6-E1Ø			---

Notes: 1. Assumes the use of an 8 MHz 8Ø86-2 processor.
2. 5 MHz CPU operation is selected by installing E36-E37. E36-E37 removed (factory default) selects 8 MHz operation.

2.5.3 INTERVAL TIMER JUMPER CONFIGURATION

The iSBC 86/35 board contains an 8253-5 Programmable Interval Timer (PIT) device providing one counter that is dedicated as a Baud Rate Clock Generator and two counters that are user configurable. The user configurable jumper options for the 8253-5 PIT device consist of selecting the input clock frequencies, enabling generation of an external clock to the parallel interface, configuring the gate inputs to the 8253-5 PIT, and configuring the output signals from the 8253-5 PIT device.

As shipped, the iSBC 86/35 board contains jumpers connecting E178 to E179, E184 to E185, and E175 to E176. These jumpers route a 1.23-MHz clock to the CLK2 and CLKØ input pins and a 153.6-kHz clock to the CLK1 input pin. Outputs TIMER Ø INTR and TIMER 1 INTR from the timer are routed directly to the interrupt matrix (refer to section 2.5.5). These outputs may then be jumpered to the desired on-board interrupt level, or routed off-board via the MULTIBUS interrupt lines, by connection to one of the bus posts (E246 to E253). Output OUT2 is used for the transmit and receive clocks for the 8251A PIC device.

Jumper stake pins E18Ø, E181, and E182 allow user configuration of the iSBC 86/35 board to drive a clock onto the J1 connector interface through use of the external clock signal (EXT CLK) output. Each output signal (OUTØ, OUT1, and OUT2) is routed to jumper posts to allow easy integration of the counter/timer output signals into the configuration of the iSBC 86/35 board. Refer to Figure 2-7 for the interval timer stake pin locations and default jumpers. Table 2-7 lists the jumper stake pins at which the signals are located and the signal names for each output signal.

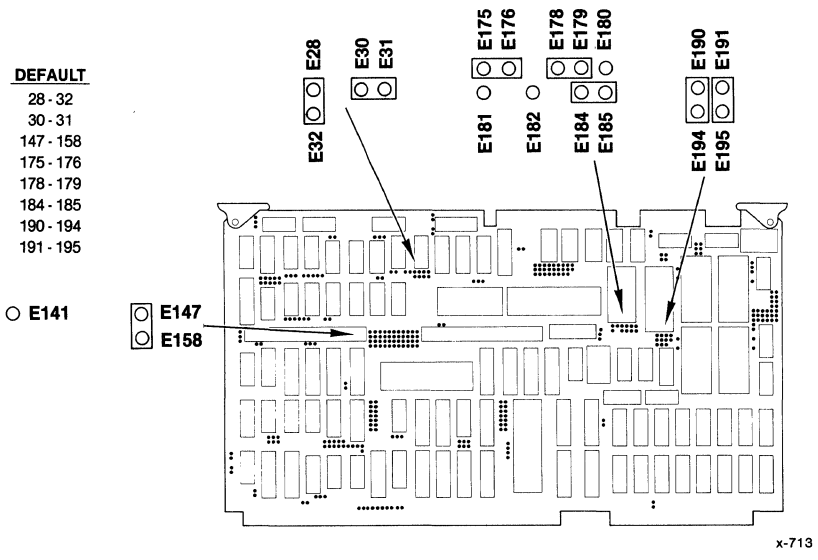

Figure 2-7. Interval Timer Stake Pin Locations

Table 2-7. Interval Timer Stake Pin Functions

Jumper	Signal	Electrical Input/Output	Function Performed
E28	GATE Ø	In	Gate input signal to Counter Ø.
E31	GATE 1	In	Gate input signal to Counter 1.
E141	TIMER 1 INTR	Out	Counter 1 output signal.
E158	TIMER Ø INTR	Out	Counter Ø output signal.
E175	CLK Ø	In	Input frequency to counter Ø.
E176	1.23 MHz	Out	Output from frequency counter to input of PIT.
E178	1.23 MHz	Out	Output from frequency counter to input of PIT.
E179	CLK2	In	Input frequency to counter 2.
E18Ø	OUT1	Out	Output connection from counter 1.
E181	OUTØ	Out	Output connection from counter Ø.
E182	EXT CLK	In	Connection from PIT to parallel interface.
E184	153.6 KHz	Out	Output from frequency counter to input of PIT.
E185	CLK 1	In	Input frequency to counter 1.
E194, E195	OUT2	Out	Counter 2 output signal

2.5.4 PARALLEL INTERFACE JUMPER CONFIGURATION

The iSBC 86/35 board uses an 8255A Programmable Peripheral Interface (PPI) device to provide three 8-bit ports of parallel I/O signals that are configurable for operation as inputs or outputs. There is a jumper matrix between the PPI device and the Parallel Port C driver/terminator sockets U18 and U19 permitting application flexibility.

Refer to Figure 2-8 for the parallel interface stake pin locations and default jumpers. Table 2-8 lists the parallel interface jumpers. Table 2-9 lists the jumpers from Port C stake pins to the stake pins that correspond to the input/output connector J1 pin numbers. Parallel Port B operation is determined entirely by programming and the type of devices installed in sockets U2Ø and U21. Refer to section 2.7.2 for information on installing drivers and/or terminators.

Jumper stake pin E52 provides access to the direction control input of the 8287 Octal Bus Transceiver provided as a buffer/driver for the Port A I/O signals. A bit from Port C may be used as an output to control the state of the direction control signal to the device.

Before configuring the parallel ports for your application, refer to the MICROSYSTEM COMPONENTS HANDBOOK for complete 8255A information.

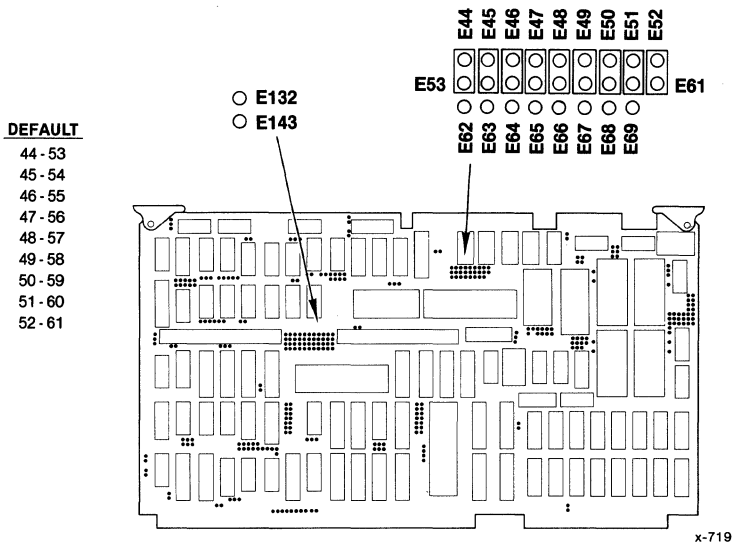

Figure 2-8. Parallel Interface Stake Pin Locations

Table 2-8. Parallel Interface Stake Pin Functions

Jumper	Connection	Jumper	Connection
E44	J1 pin 32*	E61	Pulldown to ground.
E45	J1 pin 3Ø*	E62	To TEST input of 8Ø86 CPU.
E46	J1 pin 28*	E63	PA INTR to E132 in interrupt jumper matrix.
E47	J1 pin 26*		
E48	J1 pin 24*	E64	PB INTR to E143 in interrupt jumper matrix.
E49	J1 pin 22*		
E5Ø	J1 pin 2Ø*	E65	To J8
E51	J1 pin 18*	E66	To J9
E52	Provides inverted direction control for transceiver U17.	E67	EXT CLK from E182 at PIT.
		E68	STxD to E177 and E196 at serial interface.
E53	Port C bit 7	E69	PFSN/ from P2 pin 17.
E54	Port C bit 6	E132	PAINTR to interrupt jumper matrix.
E55	Port C bit 5		
E56	Port C bit 4	E143	PBINTR to interrupt jumper matrix.
E57	Port C bit Ø		
E58	Port C bit 1		
E59	Port C bit 2		
E6Ø	Port C bit 3		

Notes: Transceiver is installed in U17 for Port A. Driver/Terminators are not installed at U18 - U21.

* Assumes that a driver or terminator is installed.

Table 2-9. Port C Jumper Configuration

Port C Bit	Jumper Connection	J1 Pin Number
Ø	48 - 57	24
1	49 - 58	22
2	5Ø - 59	2Ø
3	51 - 6Ø	18
4	47 - 56	26
5	46 - 55	28
6	45 - 54	3Ø
7	44 - 53	32

Note: Driver/Terminators not installed at factory.

2.5.5 INTERRUPT JUMPER CONFIGURATION

The iSBC 86/35 board accepts an interrupt request for the 8Ø86 CPU from several sources, including timer interrupts from the on-board 8253-5 PIT device, iSBX bus interface interrupts, serial I/O interface line interrupts, MULTIBUS interface interrupts, 8251A PCI interrupts, PLC or the PFI interrupts from the auxiliary connector P2, MINT interrupt from the iSBC 337 Numeric Data Processor, and EXT INTRØ/ interrupt on pin-5Ø of the J1 connector. The interrupt sources and priority levels are user configurable.

The iSBC 86/35 board sends and receives interrupt request signals on MULTIBUS interrupt request lines INTØ/ through INT7/. Refer to Figure 2-9 for the interrupt stake pin locations and default jumpers. Table 2-1Ø lists the stake pin numbers and corresponding functions.

The iSBC 86/35 board provides an OR function combining two or four interrupt requests signals into one interrupt signal. This feature permits applications requiring additional interrupt handling capabilities. OR INTR1 (E13Ø) OR's together OR2 (E131), OR3 (E142), OR4 (E139), and OR5 (E127). OR INTR2 (E128) OR's together ORØ (E138) and OR1 (E14Ø).

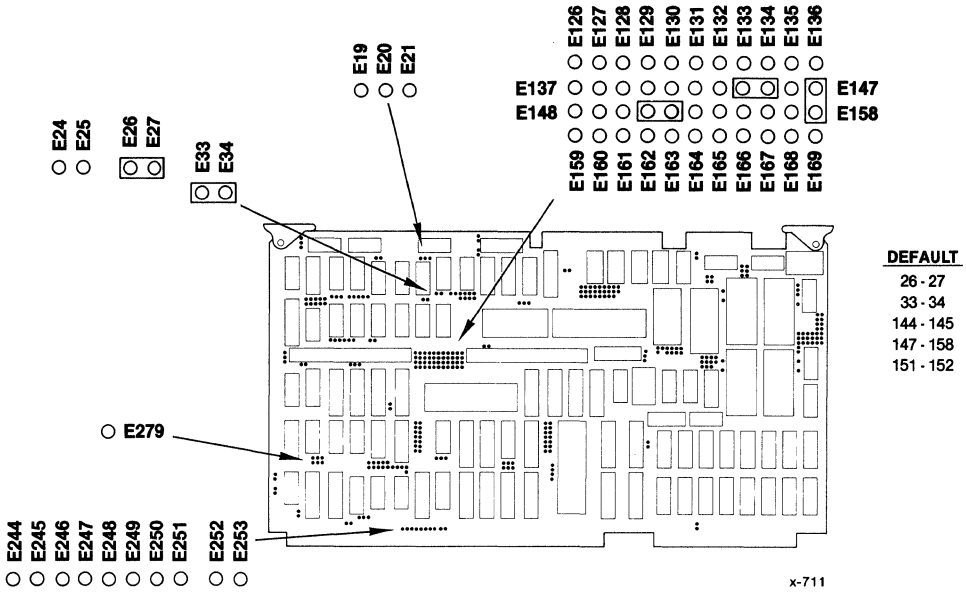

Figure 2-9. Interrupt Stake Pin Locations

Table 2-1Ø. Interrupt Stake Pin Functions

Interrupt Signal	Name	Post	Electrical Out/In/Bussed
Edge Interrupt	EDGE INTR	E135	I
Level Interrupt	LEVEL INTR	E146	O
iSBX Bus Interrupt	SBX1 INTØ	E156	O
iSBX Bus Interrupt	SBX1 INT1	E169	O
iSBX Bus Interrupt	SBX2 INTØ	E137	O
iSBX Bus Interrupt	SBX2 INT1	E126	O
Power Line Clock	PLC	E163	O
Power Fail Interrupt	PFIN	E168	O
Parity Interrupt	Reserved	E167	O
iSBC 337 Interrupt	MINT	E166	O
8253-5 PIT Interrupt	TIMER Ø INTR	E158	O
8253-5 PIT Interrupt	TIMER 1 INTR	E141	O
8251A PCI Tx Interrupt	TXRDY	E154	O
8251A PCI Rx Interrupt	RXRDY	E153	O
8255A PPI Interrupt	PA INTR	E132	O
8255A PPI Interrupt	PB INTR	E143	O
External J1 Interrupt	EXT INTRØ/	E2Ø	O
Signal Inverter Input		E19	I
Signal Inverter Output		E129	O
+5 Volts		E21	O
MULTIBUS Interrupt	BUS INTR OUT1/	E244	O

Table 2-1Ø. Interrupt Stake Pin Functions (continued)

Interrupt Signal	Name	Post	Electrical Out/In/Bussed
MULTIBUS Interrupt	BUS INTR OUT2/	E245	O
MULTIBUS Interrupt Input Ø	INTO	E16Ø	O
MULTIBUS Interrupt Input 1	INT1	E149	O
MULTIBUS Interrupt Input 2	INT2	E148	O
MULTIBUS Interrupt Input 3	INT3	E159	O
MULTIBUS Interrupt Input 4	INT4	E162	O
MULTIBUS Interrupt Input 5	INT5	E151	O
MULTIBUS Interrupt Input 6	INT6	E15Ø	O
MULTIBUS Interrupt Input 7	INT7	E161	O
Failsafe Timeout Interrupt	TIME OUT INTR/	E133	O
Failsafe Timeout Control**	AEN/	E279	O
Pulldown to ground		E144	O
OR-ed Interrupt Output	OR INTR1	E13Ø	O
OR-ed Interrupt Output	OR INTR2	E128	O
OR-ed Interrupt Input	ORØ	E138	I
OR-ed Interrupt Input	OR1	E14Ø	I
OR-ed Interrupt Input	OR2	E131	I
OR-ed Interrupt Input	OR3	E142	I
OR-ed Interrupt Input	OR4	E139	I
OR-ed Interrupt Input	OR5	E127	I
Non-Maskable Interrupt	NMI	E145	I
Interrupt Request Ø	IRØ	E165	I
Interrupt Request 1	IR1	E164	I
Interrupt Request 2	IR2	E147	I
Interrupt Request 3	IR3	E136	I
Interrupt Request 4	IR4	E157	I
Interrupt Request 5	IR5	E152	I
Interrupt Request 6	IR6	E155	I
Interrupt Request 7	IR7	E134	I
MULTIBUS Interrupt Output Ø	INTO/	E253	B
MULTIBUS Interrupt Output 1	INT1/	E252	B
MULTIBUS Interrupt Output 2	INT2/	E251	B
MULTIBUS Interrupt Output 3	INT3/	E25Ø	B
MULTIBUS Interrupt Output 4	INT4/	E249	B
MULTIBUS Interrupt Output 5	INT5/	E248	B
MULTIBUS Interrupt Output 6	INT6/	E247	B
MULTIBUS Interrupt Output 7	INT7/	E246	B

Notes: ** Allows AEN/ to disable the failsafe timeout during execution of a HALT instruction by iRMX 86.

O = output, I = input, and B = bussed; may only be driven by E245 or E246 (open-collector outputs).

iSBX™ MULTIMODULE Interrupts (SBX1 INTØ, SBX1 INT1, SBX2 INTØ, SBX2 INT1) Two interrupt request lines are available from each iSBX MULTIMODULE board installed on the iSBC 86/35 board.

Interval Timer Outputs (TIMER Ø INTR, TIMER 1 INTR) These two lines are directly from the 8253-5 PIT. The timer Ø line is jumpered at the factory to interrupt request line IR2 (E158-E147) of the 8259A PIC. As shipped, timer 1 output is not connected to the 8259A PIC.

Parallel Port Interrupts A, B (PA INTR and PB INTR) Essentially, these two lines are software programmable interrupt lines. Connect each line to the desired interrupt request input.

Transmit and Receive Interrupts (TxRDY and RxRDY) These signals originate at the 8251A PCI device. The signal TxRDY interrupt from the PCI indicates that the PCI is ready to accept a data character from the CPU. Likewise, the RxRDY interrupt from the PCI indicates that the PCI contains a data character to be read by the CPU. Refer to the MICROSYSTEM COMPONENTS HANDBOOK for additional PCI information.

Power Line Clock (PLC) This external signal is supplied by the iSBC 665 Modular Chassis, or similar circuit. It enters the board via auxiliary connector pin P2-31 and is specified as 12Ø Hz (double the AC line frequency).

Math Interrupt (MINT) This signal originates from the optional iSBC 337 Numeric Data Processor and is used only in conjunction with that option. Refer to section 2.7.3 for additional iSBC 337 board information.

Power Fail Interrupt (PFIN/) Furnished by a power supply, this signal indicates the occurrence of an ac line power failure and that dc voltage loss is imminent. Typically, this signal is connected to the NMI input on the 8Ø86 CPU and is used in conjunction with a user-written power down routine and battery backup scheme. Refer to section 2.8 for battery backup information.

External Interrupt Ø (EXT INTRØ/) This external interrupt signal enters the board via parallel port connector J1-5Ø. The incoming signal may be inverted by U11, if necessary, before being routed to the PIC.

Single Request Edge-Sensitive Feature (LEVEL INTR) The iSBC 86/35 board is equipped with special circuitry that senses an edge-type interrupt signal and converts it to a level-type interrupt signal while the 8259A PIC is in the level mode. This feature is useful when the PIC operates in the level mode and a critical edge-type interrupt signal must be monitored. The use of the edge-to-level conversion circuitry eliminates the possibility of losing an edge-type interrupt request signal that, typically, expires before the controller can acknowledge or service the request.

To enable EDGE INTR, several jumper connections are required. First, install a jumper from the desired interrupt request line to jumper stake pin E135 (edge converter circuit input); then install a jumper between interrupt jumper stake pin E146 and the desired PIC input stake pin. As an example, to implement the Failsafe Timer interrupt, install the first jumper at E133-E135; then install jumper E146-E164 to select the desired interrupt level (IR1) in the PIC. If either the edge sensitive latch or the status register is used, E42 to E43 must be installed. If neither is used, jumper E42 to E43 should be removed.

Non-Maskable Interrupt Input Mask The 8Ø86 CPU NMI input may be configured to be software selectable. This feature is called the Non-Maskable Interrupt Input Mask on the iSBC 86/35 board. The feature is programmable through the status register and hardware enabled via jumper E26-E27. A HIGH state on the NMI MASK/ line (E26-E27 installed) enables the mask gate to sense the condition of NMI. A LOW state disables the mask gate, preventing all non-maskable interrupts from reaching the 8Ø86 CPU.

MULTIBUS® Interrupt Output Option (BUS INTR OUT 1 and BUS INTR OUT 2) The iSBC 86/35 board has an optional status register configuration that provides two software programmable interrupt outputs. These signals allow you to issue an interrupt request on a system MULTIBUS line through software by programming the status register.

As shipped, the board fully enables BUS INTR OUT 2 to the interrupt matrix. However, a jumper must be installed connecting E245 to one of the MULTIBUS interrupt lines (E246 through E253).

The BUS INTR OUT 1 signal, when configured as shipped, requires an additional jumper to enable it to reach the interrupt matrix (E24-E25), and a jumper connecting E244 to one of the MULTIBUS interrupt lines (E246 through E253).

2.5.5.1 MULTIBUS® Vectored Interrupt Options

The iSBC 86/35 board has the capability to service interrupt requests that originate with a request to a slave (off-board) 8259A PIC. The slave INTR output is connected to the master PIC on the iSBC 86/35 board via the MULTIBUS lines, as shown in Figure 2-1Ø. This type of interrupt

request is called a bus-vectored (BV) interrupt. In general, a bus-vectored interrupt should be of lower priority than interrupt requests which are applied directly to the master PIC. The iSBC 86/35 board is configured at the factory to accept either bus-vectored or non-bus-vectored (NBV) interrupts. In this mode, the iSBC 86/35 board requests the use of the MULTIBUS interface for all interrupt cycles. To disable the bus vectored interrupt feature, remove jumper E33-E34 (see Figure 2-9). In this mode, the iSBC 86/35 board does not use the MULTIBUS interface to perform interrupt cycles which means that it can handle only NBV interrupts. Interrupts can still originate from off board, but not from slave PIC's.

Figure 2-1Ø shows, as an example, the on-board PIC (master) interfaced with two slave PIC devices. This arrangement leaves the master PIC with six inputs (IRØ through IR5) that can be used to handle various on-board or off-board interrupt functions. The example scheme is implemented by programming the master PIC to handle IR6 and IR7 as bus-vectored interrupts.

Each interrupt input (IRØ through IR7) to the master PIC may be individually programmed to be bus-vectored or non-bus-vectored. When programmed to the bus-vectored mode, the slave PIC identifies the interrupt type for the 8Ø86 CPU; when programmed to the non-bus-vectored mode, the master PIC identifies the interrupt type for the 8Ø86 CPU.

Slave PIC devices must be identified as such during initialization sequences (with ICW3). The master PIC must also be initialized to support slave PIC devices. Refer to the MICROSYSTEM COMPONENTS HANDBOOK for 8259A PIC programming and initialization information.

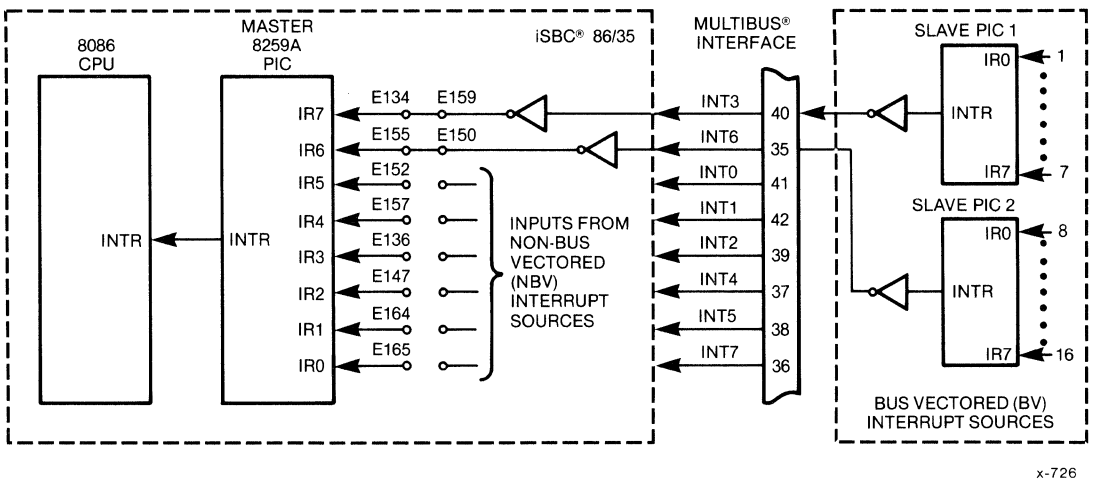

Figure 2-1Ø. Typical Master/Slave PIC Interconnect Example

2.5.6 SERIAL INTERFACE JUMPER CONFIGURATION

The 8251A Programmable Communication Interface (PCI) device contains jumper stake pins for configuration of the Transmit Clock (TxC), the Receive Clock (RxC), and the Data Set Ready (DSR) inputs.

The TxC signal may be derived from one of two sources: the Secondary Transmit Clock input signal from the RS232C interface via E186-E19Ø or the OUT2 clock from the PIT device via E19Ø-E194 (the as shipped configuration).

The RxC signal may be derived from one of two sources: the Secondary Transmit Clock input signal from the RS232C interface via E187-E191 or the OUT2 clock from the PIT device via E191-E195 (as-shipped configuration).

The DTR signal from the RS232C interface contains a jumper option E189-E193. The jumper allows user selection of the source signal for generating the Data Set Ready input to the PCI device.

Other serial interfaces signals that may be configured include the Request-To-Send input (E76), the Clear-To-Send output (E77), the Transmit Signal Element Timing output (E8Ø), the Secondary Receive output (E78), and the Secondary Clear-To-Send output (E81). The as-shipped configuration of the iSBC 86/35 board contains no jumpers for these signals. Refer to Figure 2-11 for serial interface stake pin locations and default jumpers. Table 2-11 lists the stake pin functions.

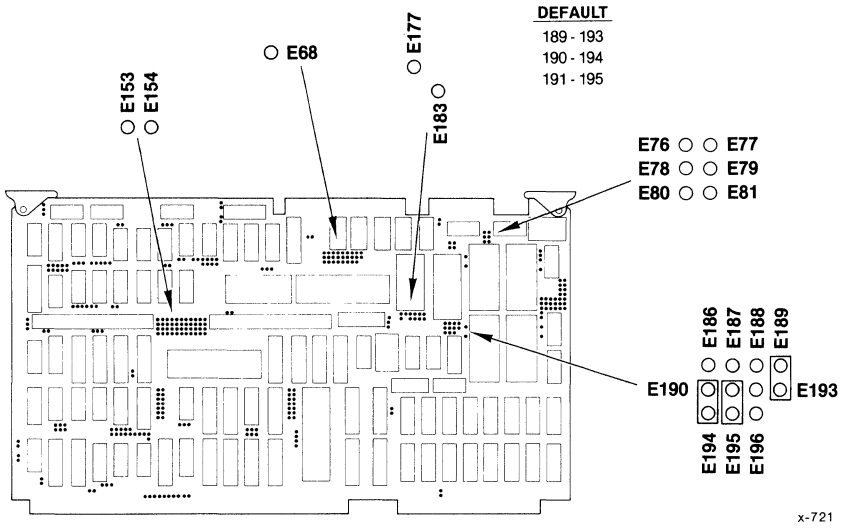

Figure 2-11. Serial Interface Stake Pin Locations

Table 2-11. Serial Interface Stake Pin Functions

Jumper	Signal	Direction	Function
E68	STxD		Provides STxD connection between the serial interface and the parallel interface.
E7Ø		In	Direct connection to J2-23.
E71	+5V	Out	+5 volts.
E72		In	Direct connection to J2-19.
E73		In	Direct connection to J2-22.
E74	-12V	Out	-12 volts.
E75	+12V	Out	+12 volts.
E76	RTS	In	Direct connection to J2-8, Request-To-Send.
E77	CTS	Out	Direct connection to J2-1Ø, Clear-To-Send.
E78		In	Direct connection to J2-5.
E79		Out	Output of configurable inverter.
E8Ø		In	Direct connection to J2-21.
E81		In	Direct connection to J2-26.
E153	RxRDY	Out	Receiver Ready output from the 8251A PCI to interrupt jumper matrix.
E154	TxRDY	Out	Transmitter Ready output from the 8251A PCI to interrupt jumper matrix.
E177	STxD		Provides STxD connection between the serial interface and the parallel interface.
E183	2.46 MHz	Out	2.46 MHz clock signal.
E186	SEC TRANS CLK	Out	Inverted input from J2-7.
E187	SEC TRANS CLK	Out	Inverted input from J2-7.
E188		Out	PCI receiver clock.
E189	DATA TERM RDY	Out	Inverted input from J2-13.
E19Ø	TxCLK	In	PCI transmitter clock input.
E191	RxCLK	In	PCI receiver clock input.
E192		In	Input of configurable inverter.
E193	DSR	In	PCI DSR input.
E194	OUT 2	Out	Output from PIT timer 2.
E195	OUT 2	Out	Output from PIT timer 2.
E196			Provides STxD connection between the serial interface and the parallel interface.

2.5.7 MULTIBUS® ACCESS FAILSAFE TIMER JUMPER CONFIGURATION

The iSBC 86/35 board contains jumper options for configuration of the Failsafe Timer feature of the board. Jumper connection E38-E39 enables a bus timeout signal (TIME OUT INTR/) to apply a timeout signal to the READY input of the on-board 8Ø86 CPU when an expected response from another MULTIBUS System Bus board (in the form of an XACK/ signal) is too late in arriving at the iSBC 86/35 board. The TIME OUT INTR/ signal is also made available to the interrupt jumper matrix (E133). The TIME OUT INTR/ signal must be used with the edge-sensitive interrupt latch, or may be connected directly to the PIC if the PIC is in edge mode. TIME OUT INTR/ may not be connected to the PIC if the PIC is in level mode.

When in a HALT condition under iRMX 86 operation, the iSBC 86/35 board could failsafe timeout and reboot the system. TIME OUT INTR/ may be combined with AEN/ (E279) by using the interrupt OR circuitry described in section 2.5.5. This eliminates the possibility of false restarts from the failsafe timer if the software enters a HALT condition.

There are two ways to configure this option; either with the PIC in edge mode, or using the edge sensitive interrupt latch with the PIC in level mode. In the case with the PIC in the edge mode, connect AEN/ and the TIME OUT INTR/ to the interrupt OR by installing E279-E138 and E133-E14Ø, and connect OR output E128 to the desired interrupt level of the PIC. In the case with the edge sensitive interrupt latch, connect E279-E138 and E133-E14Ø as previously listed, but connect OR output E128 to EDGE INTR E135, and connect LEVEL INTR E146 to the desired interrupt level of the PIC. Also, when the edge sensitive interrupt latch is used, ensure that E42-E43 is installed.

Refer to Figure 2-12 for the failsafe stake pin locations and default jumpers. As shipped, the iSBC 86/35 board contains a jumper connecting E38-E39. If you do not require the use of this feature, remove the jumper.

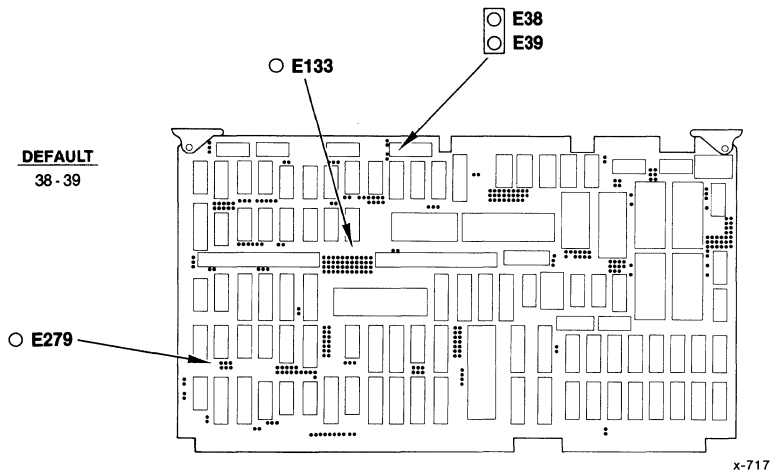

Figure 2-12. Failsafe Stake Pin Locations

2.5.8 STATUS REGISTER JUMPER CONFIGURATION

The Status Register on the iSBC 86/35 board contains 8 programmable functions, 5 of which are user configurable (3 are dedicated). The functions performed are as follows: bit Ø is a user configurable output that may be used to enable the Megabyte Page drivers (U65) or to provide GATE control for timer Ø of the 8253-5 PIT, bit 1 provides GATE control for Counter 1 of the 8253-5 PIT, bit 2 is a user configurable output providing the NMI MASK/ signal, bit 3 is a user configurable output providing the OVERRIDE/ signal, bit 4 is a user configurable output providing the BUS INTR OUT 1 signal as an interrupt request to the MULTIBUS interface, bit 5 is dedicated to generation of BUS INTR OUT 2 (E245) and to driving the LED labeled DS1, bit 6 is dedicated to controlling the LED labeled DS3 on the board, and bit 7 is dedicated to enabling the loading of the Megabyte Page register (U65). Refer to Figure 2-13 for status register stake pin locations and default jumpers. If either the status register or the edge-sensitive interrupt latch is used, jumper E42 to E43 must be installed. If neither is used, this jumper should be removed. The uses of the jumper selectable bits of the Status Register are described in the following paragraphs.

As shipped, the iSBC 86/35 board contains jumpers E28-E32 and E3Ø-E31 which tie the GATE Ø and GATE 1 inputs to the PIT at a HIGH level. If control of the GATE inputs to the PIT is required, connect the GATE input signals (E28 and E31) to the output signals from the status register (jumper stake pins E29 and E35) and program the status register to output the proper signal level. Alternately, bit Ø may be used to control the enabling of the Megabyte page drivers. Refer to paragraph 2.5.1.6 for more information.

The NMI mask enable jumper E26-E27 is installed on the iSBC 86/35 board when shipped. Since the content of the status register bit 2 is Ø initially, the jumper masks the NMI interrupt, thereby disabling the NMI interrupt from reaching the 8Ø86 CPU. By programming a 1 into status register bit 2, you can enable the 8Ø86 to receive an NMI interrupt.

The OVERRIDE/ signal jumper E22-E23 is installed on the iSBC 86/35 board when shipped. The content of status register bit 3 is Ø initially. By programming a 1 into status register bit 3, you can lock the iSBC 86/35 on-board RAM preventing access by other bus masters. If jumper E2Ø4 to E2Ø6 is installed, both the MULTIBUS and the on-board RAM can be locked.

The BUS INTR OUT 1 signal enable jumper E24-E25 is not installed on the iSBC 86/35 board when shipped. Since the content of the status register bit 4 is Ø initially, the jumper must be installed and bit 4 must be programmed to a HIGH if the BUS INTR OUT 1 signal is to generate a MULTIBUS interrupt output (INTØ/ through INT7/). Additional jumper configuration is required at the interrupt jumper matrix to place the BUS INTR OUT 1 signal (E244) on the MULTIBUS interface.

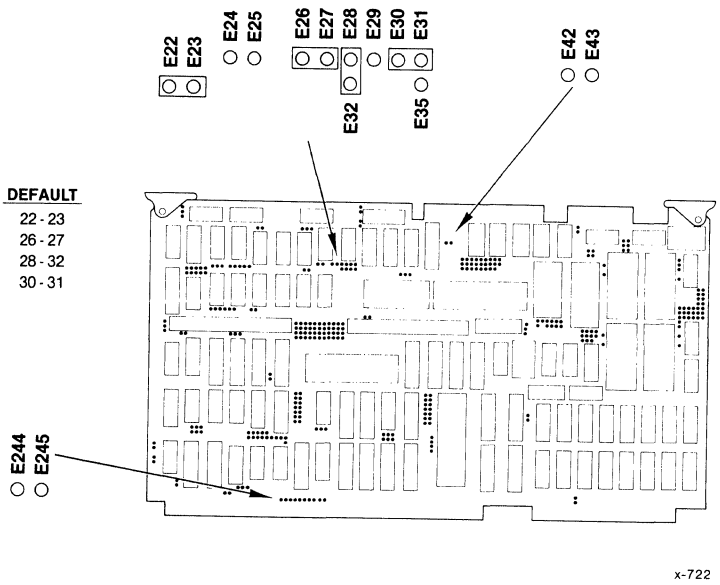

Figure 2-13. Status Register Stake Pin Locations

2.5.9 iSBX™ BUS INTERFACE JUMPER CONFIGURATION

The iSBX bus interfaces on the iSBC 86/35 board each contain four signals that may be configured via user installed jumpers. Those signals are the MULTIMODULE option signals (OPTØ/ and OPT1/) and the MULTIMODULE interrupt signals (MINTRØ/ and MINTR1/) from each iSBX bus connector.

Configuration of the jumpers should take into account the requirements of the MULTIMODULE boards as specified in the respective MULTIMODULE board hardware reference manual.

The interrupt signals are applied to jumper stake pins E137 (SBX 2 INTØ from connector J3), E126 (SBX 2 INT1 from connector J3), E156 (SBX 1 INTØ from connector J4), and E169 (SBX 1 INT1 from connector J4). The option signals are found on jumper stake pins E121 (OPTØ from connector J3), E122 (OPT1 from connector J3), E17Ø (OPTØ from connector J4), E171 (OPT1 from connector J4). The 8-bit or 16-bit interface select jumpers (E172, E173, and E174) allow user selection of either 8-bit or 16-bit operation for each iSBX Bus interface connector (Refer to Table 2-12). Refer to Figure 2-14 for iSBX Bus interface stake pin locations. As shipped from the factory, none of the jumper stake pins are connected.

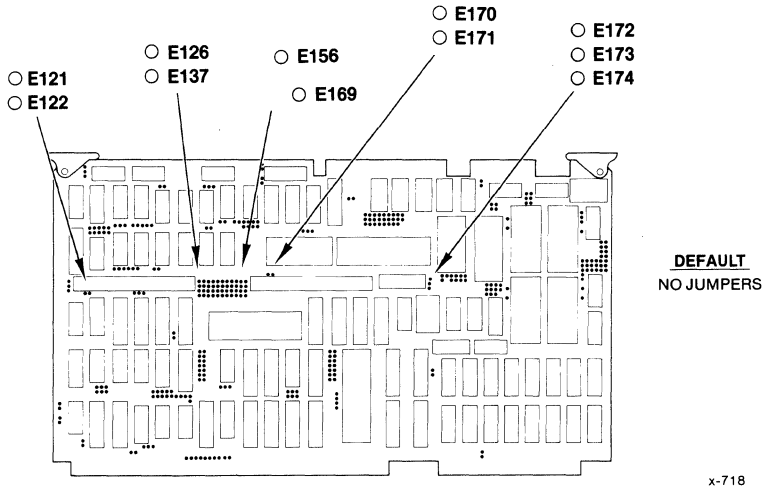

Figure 2-14. iSBX™ Bus Interface Stake Pin Locations

Table 2-12. iSBX™ Bus Decode Options

Jumpers	Operation of Connectors	
	J3	J4
Remove E172 to E173, and E173 to E174	8-bit	8-bit
Install E173 to E174 and remove E172 to E173	8-bit	16-bit
Install E172 to E173 and remove E173 to E174	16-bit	8-bit
Install E172 to E173 and E173 to E174	16 bit	16-bit

2.5.1Ø MULTIBUS® INTERFACE CONTROL JUMPER CONFIGURATION

Jumpers are provided on the iSBC 86/35 board to allow user configuration of the MULTIBUS interface control signals. Refer to Figure 2-15 for MULTIBUS interface control stake pin location and default jumpers. The functions performed by the BCLK/, CCLK/, BPRO/, and LOCK/ jumpers are listed in Table 2-13. The 8Ø86 CPU can lock the on-board RAM by use of the LOCK prefix, preventing other bus masters from accessing on-board RAM. When jumper E2Ø4-E2Ø6 is installed, both the MULTIBUS and the on-board RAM may be locked by the 8Ø86. The status register OVERRIDE signal may be used to lock the on-board RAM (and the MULTIBUS, if E2Ø4-E2Ø6 is installed) even if the 8Ø86 is not requesting LOCK. Refer to section 2.5.8 for more information on configuring the OVERRIDE signal.

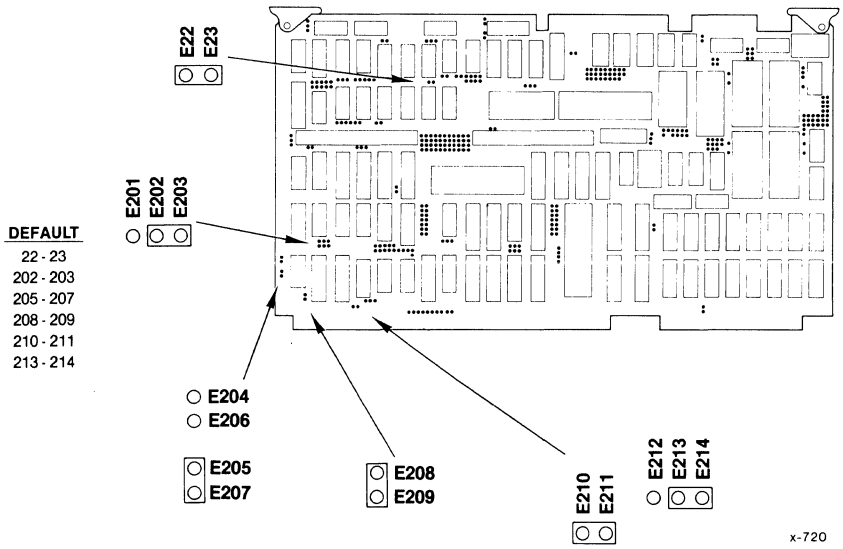

Figure 2-15. MULTIBUS® Interface Control Stake Pin Locations

Table 2-13. MULTIBUS® Interface Control Jumper Options

Jumper	Signal Name	Function
E2Ø5-E2Ø7	BCLK/ Bus Clock	When installed, the iSBC 86/35 board drives BCLK/.
E2Ø8-E2Ø9	CCLK/ Constant Clock	When installed, the iSBC 86/35 board drives CCLK/.
E2Ø4-E2Ø6	LOCK/ Bus Lock	When installed, allows the iSBC 86/35 board to lock the MULTIBUS.
E21Ø-E211	BPRO/ Bus Priority Out	When installed, allows the iSBC 86/35 board to drive BPRO/ in a serial priority resolution scheme.

Table 2-14 lists the jumper configurations for the 8289 Bus Arbiter; i.e., the operation states of the CBRQ/ and ANYRQST signals, and the interfacing modes selected by each.

Table 2-14. MULTIBUS® Interface Arbitration Options

Signal Name	Jumper	Connects	Description
CBRQ/ ANYRQST	E213-E214 E2Ø2-E2Ø1	To BUS Jumpered LOW	Arbitrate to gain access to the MULTIBUS. If needed, the iSBC 86/35 board retains control until a higher priority device requests the bus. Then rearbitrate and surrender to the higher priority device.
CBRQ/ ANYRQST	E213-E214 E2Ø2-E2Ø3	To Bus Jumpered HIGH	Arbitrate to gain access to the MULTIBUS. If needed, the iSBC 86/35 board retains possession until another device asserts CBRQ/. Then rearbitrate and surrender control to any requesting device (higher or lower priority).
CBRQ/ ANYRQST	E212-E213 E2Ø2-E2Ø3	Jumpered LOW Jumpered HIGH	Arbitrate for every bus access.

The ANYRQST and CBRQ/ signals provide the mode select inputs to the 8289 Bus Arbiter. The bidirectional interface signal Common Bus Request (CBRQ/) improves bus access time by allowing a bus master to retain control of the MULTIBUS interface without contending for it on each transfer cycle, as long as no other master is requesting control of the bus. The CBRQ/ signal from the iSBC 86/35 board operates the same in parallel and serial priority resolution schemes.

The Any Request (ANYRQST) signal is an 8289 Bus Arbiter input signal generated either HIGH or LOW, depending on the iSBC 86/35 board jumper configuration. The signal indicates whether the iSBC 86/35 board will allow a lower priority device to gain access to the MULTIBUS interface by the CBRQ/ signal. When ANYRQST is inactive, a lower priority device cannot gain control of the bus until it gains priority via BPRN/. When ANYRQST is active, a lower priority device may gain control of the bus by activating the CBRQ/ signal.

2.6 SYSTEM COMPONENTS

The system components required to configure all intended applications of the iSBC 86/35 board are listed in Table 2-15. Cable configuration information for serial I/O connector J2 and parallel I/O connector J1 are contained in the Appendix E. Figure 2-16 shows the mounting locations on the iSBC 86/35 board for each of the user-provided components. Only those components required to satisfy the application need be installed. When installing the integrated circuit packages into the sockets on the iSBC 86/35 board, make certain that pin 1 of the chip is oriented nearest to the white dot (indicating pin 1 of the socket) that is silk-screened onto the board.

Table 2-15. User-Furnished Components

Item	Description	Remarks
EPROM Chips	Two or four of the following types: EPROM 2764 8 k by 8 bit 27128 16 k by 8 bit 27256 32 k by 8 bit 27512 64 k by 8 bit	Ultraviolet Erasable PROM (EPROM).
Connector (mates with J2)	See Serial Connector cable details in Appendix E.	Provide compatible cables for serial I/O interface to the 8251A PCI device.
Connector (mates with J1)	See Parallel Connector cable details in Appendix E.	Provide compatible cables for parallel I/O signal interface to the 8255A PPI device.
Line Driver SN74Ø3 SN74ØØ SN74Ø8 SN74Ø9	Type Current I, OC 16 mA I 16 mA NI 16 mA NI, OC 16 mA	Interface parallel I/O ports CB and CC with Intel 8255A PPI device. Requires two line drivers for each four parallel output lines.
Line Terminators	Interface parallel I/O ports CB and CC with Intel 8255A PPI device. Requires two MDP 14ØØ-S124 Dividers or two MDP 14ØØ-S93 Pull-Ups for each four parallel input lines.	

Table 2-15. User-Furnished Components (continued)

Item	Description	Remarks
iSBC 3Ø4 RAM MULTIMODULE Board	128 K-bytes of RAM expansion capability.	Provides capability to expand on-board RAM to 64Ø K-bytes.
iSBC 314 RAM MULTIMODULE Board	512 K-bytes of RAM expansion capability.	Provides capability to expand on-board RAM to 1 Mbyte.
iSBC 337 MULTIMODULE Board	Numeric Data Processor	Extends processing capability.
iSBX MULTIMODULE Board		Extends I/O functions.
Notes: I = inverter, OC = Open Collector, NI = Non-inverting The MDP devices listed above are available from Hamilton - Avnet/Dale		

2.7 INSTALLATION

Installation consists of several procedures. The first consists of installing the selected EPROM devices onto the board, refer to 2.7.1. If additional RAM space is required, refer to 2.7.3. If line drivers or terminators are required for your application, refer to 2.7.2. To configure the serial I/O port and parallel I/O ports to your specific application, refer to Appendix E. Once all the jumpers and components have been installed and the backplane configured to implement your system requirements, install the iSBC 86/35 board into place within your system chassis as outlined in paragraph 2.7.5.

Refer to paragraph 2.7.4 if an iSBX MULTIMODULE board is required for your application. Refer to paragraph 2.8 for power fail battery backup provisions.

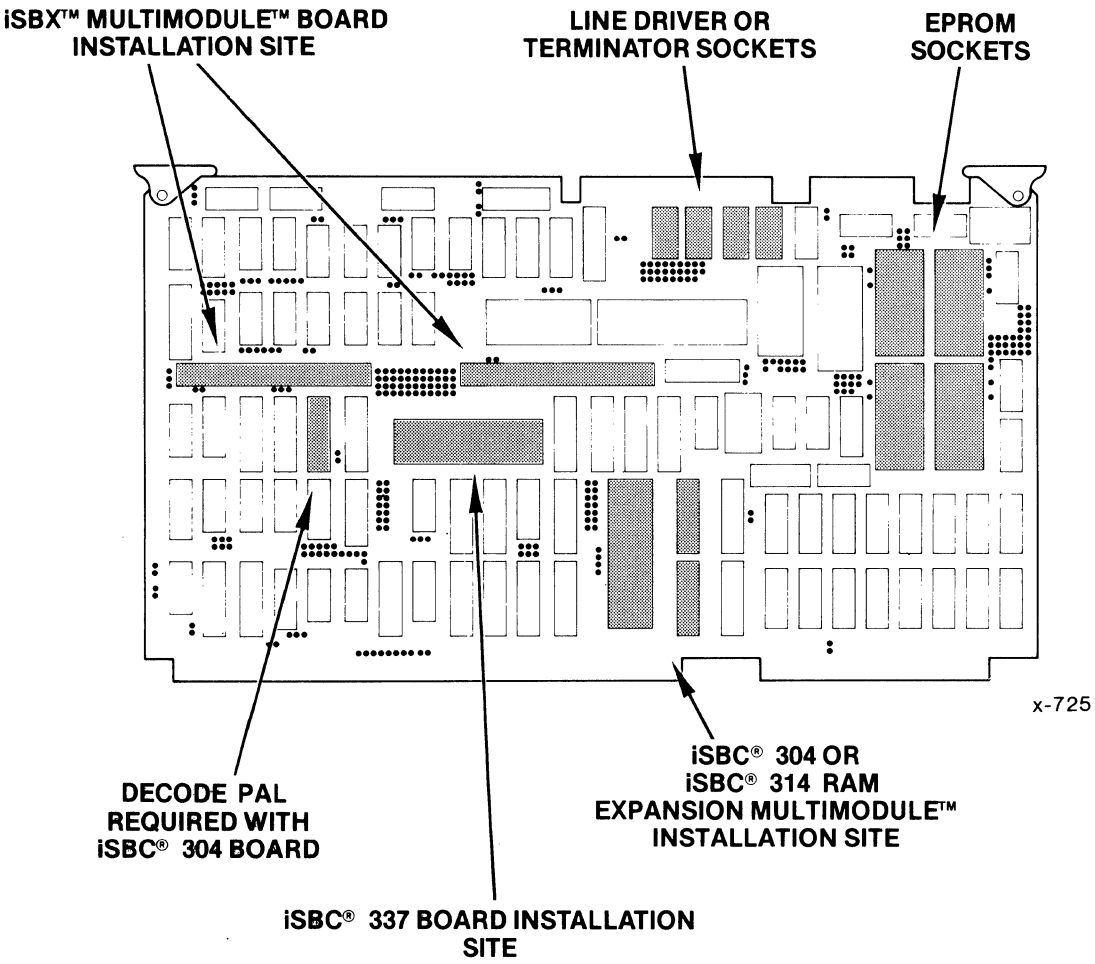

Figure 2-16. iSBC® 86/35 Board User-Furnished Component Locations

2.7.1 EPROM Device Installation

As shipped from the factory, the iSBC 86/35 board contains no EPROM devices. You may install one of several different types of EPROM device into the EPROM sockets on the iSBC 86/35 board. However, the memory address configuration depends on the type of memory device selected. Refer to the jumper configuration section of this chapter for more information.

CAUTION

All MOS devices such as EPROM devices are highly susceptible to damage from static electricity. Use extreme caution when installing MOS devices in a low humidity environment. Always ground yourself before handling MOS devices to ensure that a static charge build-up is not dissipated through or around the MOS devices.

The EPROM devices on the iSBC 86/35 board must be installed into sockets U39, U4Ø, U57, and U58 on the iSBC 86/35 board, as shown in Figure 2-17. Socket U39 accommodates the Bank Ø, high byte memory locations; U57 contains the Bank Ø, low byte memory locations; U4Ø contains the Bank 1, high byte memory locations; and U58 contains the Bank 1, low byte memory locations.

A maximum of 256 K-bytes of EPROM may be installed into sockets U39, U4Ø, U57, and U58 on the iSBC 86/35 board. The sockets must contain only one type of EPROM device; mixture of devices is not allowed. Empty sockets at U39 and U57 are allowed if the memory space is never accessed. After selecting the memory device type to best suit your application, carefully insert each device into its socket.

CAUTION

Never insert MOS devices into a board when power is applied. Doing so could damage the devices.

On power-up, the 8Ø86 CPU jumps to a bootstrap routine located at memory location FFFFØH through FFFFFH in the top-most portion of the on-board EPROM address space. These EPROM locations are contained in the memory devices in sockets U58 and U4Ø.

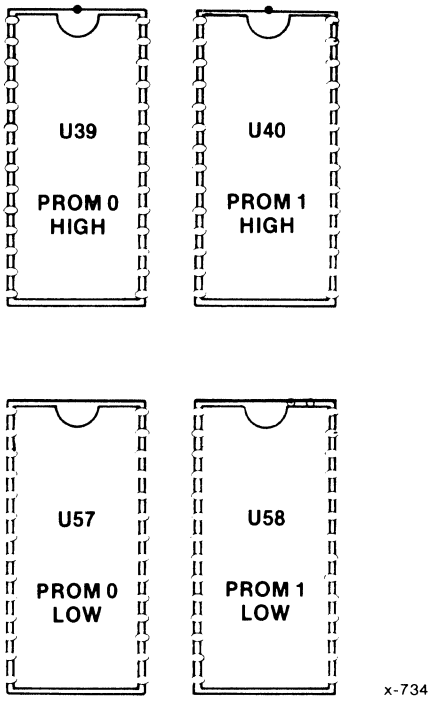

Figure 2-17. EPROM Device Installation

2.7.2 Line Driver Installation

The J1 connector interface includes four 14-pin device sockets (U18, U19, U2Ø, and U21) for installation of user provided line drivers or terminators in configuring the parallel I/O port signals for Port B and Port C of the 8255A PPI device. Table 2-15 lists some of the common types of line drivers and terminators that may be installed into device sockets U18, U19, U2Ø, and U21 for the parallel I/O interface.

As shipped, the iSBC 86/35 board includes an 8287 Octal Bus Transceiver device (U17) that interfaces the parallel I/O port signals for Port A of the 8255A PPI.

2.7.3 iSBC® MULTIMODULE™ BOARD INSTALLATION

The iSBC 86/35 board accepts the iSBC 3Ø4 RAM Expansion MULTIMODULE Board, the iSBC 314 RAM Expansion MULTIMODULE Board, or the iSBC 337 Numeric Data Processor. More information on the iSBC 3Ø4 and iSBC 314 MULTIMODULE boards is contained in Appendices B and C of this manual.

The iSBC 337 Numeric Data Processor is a high-speed, floating-point math board that allows a quick and easy upgrade to floating-point math for the iSBC 86/35 board.

The iSBC 337 Numeric Data Processor is designed to be mounted in the existing 8Ø86 CPU machine socket (U48) of the iSBC 86/35 board. Connect the MINT signal (E166 from connector J5) to the appropriate interrupt level of the 8259A PIC. Refer to Figure 2-9 for stake pin location. Refer to the iSBC 337 Numeric Data Processor Board Hardware Reference Manual for information to install the iSBC 337 Numeric Data Processor.

2.7.4 iSBX™ MULTIMODULE™ BOARD INSTALLATION

The iSBC 86/35 board provides two iSBX MULTIMODULE connectors (J3 and J4). When an iSBX MULTIMODULE board is installed, the iSBC 86/35 board power requirement will increase by the amount specified in the hardware reference manual for the specific iSBX MULTIMODULE board used. Using the hardware supplied with the iSBC MULTIMODULE board, install the MULTIMODULE board(s) as described in the appropriate hardware reference manual.

2.7.5 FINAL INSTALLATION

In an iSBC single board computer based system, install the iSBC 86/35 board in any card slot that has not been wired for a dedicated function. Make certain that auxiliary edge connector P2 (if used) is correctly installed. Attach the appropriate cable assemblies to parallel and serial connectors J1 and J2.

CAUTION

Always turn off the computer system power supply before installing or removing the iSBC 86/35 board and before installing or removing interface cables. Failure to do so can result in damage to the iSBC 86/35 board.

2.8 POWER FAIL BATTERY BACKUP PROVISIONS

In an optional mode, the iSBC 86/35 board may be configured for battery backup operation. This means you may connect a dc battery to the board to preserve memory during an ac power failure. In order for the battery backup scheme to function, your power supply must provide the following signals:

a. PFIN/ Power Fail Interrupt.

b. MPRØ/ Memory Protect.

c. PFSN/ Power Fail Sense.

To implement a typical battery backup scheme on the iSBC 86/35 board, the following connections are required:

a. Connect +5 Volt battery positive leads to auxiliary connector pins P2-3 and P2-4.

b. Connect battery return leads to auxiliary connector pins P2-1, P2-2, P2-21, and P2-22.

c. Remove jumper connections E114-E115 and E277-E278.

d. Connect the power supply PFIN/ line to auxiliary connector P2-19.

e. Remove interrupt jumper E144-E145 and install jumper E145-E168. This routes PFIN/ input to the NMI input on the 8Ø86 CPU.

f. Make certain that the NMI signal is not masked by programming 1 into the Status Register, bit 2.

g. Connect the power supply MPRO/ line to auxiliary connector P2-2Ø.

h. Connect PFSN/ line to auxiliary connector P2-17.

In this typical battery backup configuration, if a power failure occurs, the power supply asserts PFIN/, which in turn initiates the NMI interrupt. The interrupt request could cause the 8Ø86 CPU to store the contents of the various internal registers into RAM, and your interrupt software could store other information that must be saved. When the MPRO/ signal is asserted, all accesses to the RAM are disabled. When the power is restored, the PFSN/ signal still indicates that a power failure had occurred. Your power-on routine could then read the contents of RAM before executing, thereby minimizing data loss.

Refer to Figure 2-18 for power fail battery backup stake pins and default jumpers.

Refer to the MULTIBUS Specification for a complete description of power fail signals and battery backup operation.

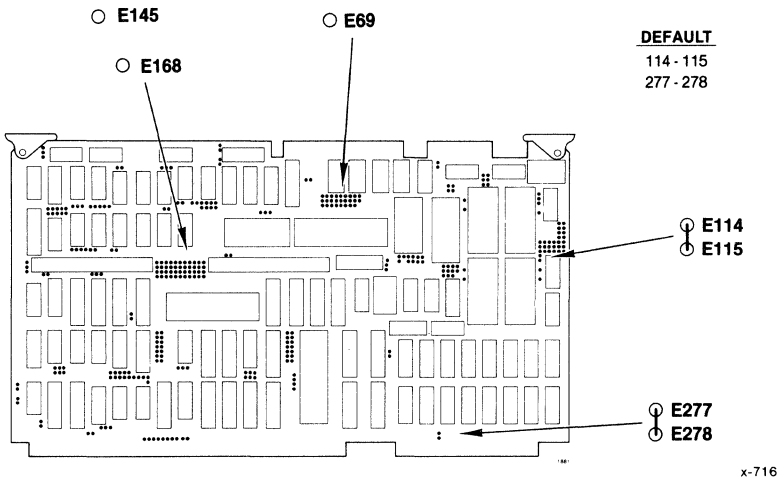

Figure 2-18. Power Fail Battery Backup Stake Pin Locations

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CHAPTER 3. PROGRAMMING INFORMATION

3.1 INTRODUCTION

The Intel iSBC 86/35 Single board computer contains several programmable devices, including an 8255A Programmable Peripheral Interface (PPI), an 8251A Programmable Communications Interface (PCI), an 8253-5 Programmable Interrupt Timer (PIT), and an 8259A Programmable Interrupt Controller (PIC). This chapter provides pertinent board-related programming information. I/O port addresses are provided in tabular form.

3.2 MEMORY ADDRESSING

There are four aspects of memory addressing: EPROM addressing, on-board RAM addressing by the local CPU, on-board RAM addressing by the MULTIBUS, and MULTIBUS addressing by the iSBC 86/35 board.

For the EPROM addressing range, which is determined by jumpers, refer to Table 2-2.

For the on-board RAM addressing by the local CPU, which is determined by jumpers, refer to Table 2-3.

For the on-board RAM addressing by the MULTIBUS interface, which is determined by jumpers, refer to Tables 2-4 and 2-5.

For the MULTIBUS interface addressing by the iSBC 86/35 board, refer to paragraph 2.5.1.6.

3.3 I/O ADDRESSING

The on-board 8Ø86 CPU communicates with the programmable devices and other I/O devices via I/O READ and I/O WRITE commands that are issued to the I/O port address assigned to that particular device. Each I/O device is assigned one (and in some cases, more than one) I/O port address through which data, commands, and status are transferred. Table 3-1 lists all of the legal I/O port addresses for the iSBC 86/35 board. In addition to the programmable devices, the iSBC 86/35 board contains some other devices, such as a status latch and an edge-sensitive interrupt sensing circuit, that are also assigned I/O port addresses.

Those I/O addresses not listed in Table 3-1 are decoded as off-board addresses. Also when an iSBX connector (J3 or J4) is not used, the addresses assigned to it are decoded as off-board addresses.

Table 3-1. I/O Port Addresses

I/O Port Addresses	Device Selected	Function Performed	
CØ or C4	Edge Triggered Latch & 8259A PIC.	Word write	Clear latch & access ICW1, OCW2, or OCW3
	8259A PIC	Byte Read	Status and Poll
	8259A PIC	Byte Write	ICW1, OCW2, or OCW3
C2 or C6	Edge Triggered Latch & 8259A PIC.	Word write	Unpredictable results
	8259A PIC	Byte Read	OCW1
	8259A PIC	Byte Write	ICW2, ICW3, ICW4, OCW1
C8	8255A PPI	Read	Port A
		Write	Port A
CA	8255A PPI	Read	Port B
		Write	Port B
CC	8255A PPI	Read	Port C
		Write	Port C
CE	8255A PPI	Read	Control Word
		Write	none
DØ	8253 PIT	Read	Counter Ø
		Write	Counter Ø
D2	8253 PIT	Read	Counter 1
		Write	Counter 1
D4	8253 PIT	Read	Counter 2
		Write	Counter 2
D6	8253 PIT	Read	Control Word
		Write	none
D8 or DC	8251A PCI	Read	Data
		Write	Data
DA or DE	8251A PCI	Read	Mode or command Word
		Write	Status
C9,CB,CD, CF,D1,D3, D5,D7,D9, DB,DD,DF	Status Latch/ Megabyte Reg	Read	none
		Write	Load upper 4-bit Address, Override, NMI mask, MULTIBUS interrupts, gate control. Megabyte page driver control.

Table 3-1. I/O Port Addresses (continued)

I/O Port Addresses	Device Selected	Function Performed	
8Ø,82,84, 86,88,8A, 8C,8E	iSBX Connector J4	Read/Write	Low byte transfer (both 8-bit and 16-bit boards), or word transfer (16-bit boards only). Activates MCSØ/ for MULTIMODULE boards.
81,83,85, 87,89,8B, 8D,8F	iSBX Connector J4	Read/Write	High byte transfer (16-bit boards only). Activates MCS1/ for MULTIMODULE boards.
9Ø,92,94, 96,98,9A, 9C,9E	iSBX Connector J4	Read/Write	Byte transfer (8-bit boards only). Activates MCS1/ for MULTIMODULE boards.
AØ,A2,A4, A6,A8,AA, AC,AE	iSBX Connector J3	Read/Write	Low byte transfer (both 8-bit and 16-bit boards), or word transfer (16-bit boards only). Activates MCSØ/ for MULTIMODULE boards.
A1,A3,A5, A7,A9,AB, AD,AF	iSBX Connector J3	Read/Write	High byte transfer (16-bit boards only). Activates MCS1/ for MULTIMODULE boards.
BØ,B2,B4, B6,B8,BA, BC,BE	iSBX Connector J3	Read/Write	Byte transfer (8-bit boards only). Activates MCS1/ for MULTIMODULE boards.

3.4 8253 PIT PROGRAMMING

The 8253 Programmable Interval Timer (PIT) includes three independently controlled counters that are used for on-board I/O timing and CPU interrupts. Each counter has its own input and output and can be programmed to operate in any of six different modes. In addition, the iSBC 86/35 board PIT configurations provide several jumper selectable clock rates that can be used for the counter inputs. The default (factory connected) and optional jumpers for selecting the clock inputs to the three counters send a 1.23-MHz clock to counter Ø and counter 2

(CLKØ and CLK2), and a 153.6-kHz to counter 1 (CLK1). The output from counter Ø is routed to IR2 input of the interrupt controller to be used as the CPU interrupt interval timer. It also can be jumpered as an input to counter 1. The output from counter 1 can be routed either to the interrupt jumper matrix or off board via the jumpers of the parallel interface jumper matrix. The output from counter 2 is used exclusively for the baud rate timer, clocking the 8251A serial interface controller. Refer to MICROSYSTEM COMPONENTS HANDBOOK for complete information on programming the 8253 PIT.

3.5 8251A PCI PROGRAMMING

The 8251A Programmable Communications Interface (PCI) converts parallel output data into virtually any serial output data format (including IBM Bi-Synchronous) for half- or full-duplex operation. The PCI also converts serial input data into parallel data format.

Prior to transmitting or receiving data, the PCI must be loaded with a set of control words. These control words, which define the complete functional operation of the PCI, must immediately follow a reset (internal or external). The control words include a Mode instruction and Command instructions. Refer to the INTEL MICROSYSTEM COMPONENTS HANDBOOK for complete information on programming the 8251A PCI.

3.6 8255A PPI PROGRAMMING

The iSBC 86/35 board has a total of 24 parallel I/O lines, grouped into three ports: A, B, and C. All lines exit the board via connector J1. One 8255A PPI device is used to control all three ports.

Each of the three parallel I/O ports may be programmed independently. Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces software requirements in control-based applications.

Refer to the MICROSYSTEM COMPONENTS HANDBOOK for complete information on programming the 8255A.

3.7 8259A PIC PROGRAMMING

The 8259A PIC functions as an overall manager in an interrupt-driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and may issue an interrupt to the CPU based on this determination.

The on-board master 8259A PIC handles up to eight vectored priority interrupts and has the capability of expanding the number of priority interrupts by cascading one or more of its interrupt input lines with slave 8259A PIC's.

The basic functions of the PIC are to (1) resolve the priority of interrupts requests, (2) issue a single interrupt request to the CPU based on that priority, and (3) send the CPU an interrupt type number for servicing the interrupting device.

NOTE

The master PIC in an iSBC 86/35 board with or without slaves, must be operated in the buffered mode.

3.7.1 8Ø86 INTERRUPT HANDLING

The 8Ø86 CPU has two interrupt input request lines: Interrupt Request (INTR) and Non-Maskable Interrupt Request (NMI). All of the interrupt requests handled by the 8259A PIC are passed to the 8Ø86 CPU via the INTR line. The NMI input on the iSBC 86/35 board is not used in the factory default configuration, but can be reconfigured. Refer to Chapter 2 for complete jumper instructions.

3.7.2 NON-MASKABLE INTERRUPT (NMI)

The NMI interrupt request input to the 8Ø86 CPU is of a higher priority than the INTR input. A low-to-high transition on the NMI input will be serviced at the end of the current instruction or between whole moves of a block type instruction. The worst case response to NMI is during a multiply, divide, or variable shift instruction.

When the NMI input is active, the CPU performs the following:

a. Pushes the flag registers into the stack (same as PUSHF)

b. Clears the Interrupt Flag (same as CLI). This disables all maskable interrupts.

c. Transfers control with an indirect call through vector location ØØØØ8.

The NMI input is intended mainly for catastrophic error handling, such as a system power failure interrupt. Upon completion of the service routine, the CPU automatically restores the flags and returns to the main program.

3.7.3 MASKABLE INTERRUPT (INTR)

The INTR input has a lower priority than that of the NMI interrupt input. A high level on the INTR input will be serviced at the end of the current instruction or at the end of a whole move for a block-type instruction.

When INTR goes active, the CPU performs the following (assuming the Interrupt Flag is set):

a. Issues two acknowledge signals; upon receipt of the second acknowledge signal, the interrupting device (master or slave PIC) will respond with a one-byte interrupt identifier.

b. Pushes the Flag registers onto the stack (same as a PUSHF instruction).

c. Clears the Interrupt Flag, thereby disabling further maskable interrupts.

d. Multiplies by four (4) the binary value (X) contained in the one-byte identifier from the interrupting device.

e. Transfers control with an indirect call through location 4X.

Upon completion of the service routine, the CPU automatically restores its flags and returns to the main program.

3.7.4 MASTER PIC BYTE IDENTIFIER

The master (on-board) PIC responds to the second acknowledge signal from the CPU only if the interrupt request is from a non-slaved device; i.e., a device that is reporting through another PIC device. The master PIC has eight IR inputs numbered IRØ through IR7, which are identified by a 3-bit binary number. ICW2 determines the five most significant bits of the interrupt type passed to the 8Ø86 CPU. Thus, if an interrupt request occurs on IR5, and ICW2 was written with a value of 2ØH, the master PIC responds to the second acknowledge signal from the CPU by outputting the byte ØØ1ØØ1Ø1B (25H). The CPU multiplies this value by four and transfers control with an indirect call through 1ØØ1Ø1ØØB (94H).

3.7.5 SLAVE PIC BYTE IDENTIFIER

Each slave PIC is initialized with a 3-bit identifier (ID) in ICW3. The slave PIC requests an interrupt by driving the associated master PIC IR line. The master PIC, in turn, drives the CPU INTR input high and the CPU outputs the first of two acknowledge signals. In response to the first acknowledge signal, the master PIC outputs a 3-bit binary code to the slave PIC via the cascade lines; this 3-bit code allows the appropriate slave PIC to respond to the second acknowledge signal from the CPU.

Assume that the slave PIC has the ID code 1Ø1B (assigned in ICW3) that the ICW2 was programmed with a value of 4ØH, and that the device requesting service is driving the IR2 line of the slave PIC (Ø1Ø). Thus, in response to the second acknowledge signal, where the slave PIC has previously put its ID code 1Ø1B on its cascade lines, the slave PIC outputs Ø1ØØØØ1ØB (42H). The CPU multiplies this value by four and transfers control with an indirect call through 1ØØØØ1ØØØB (1Ø8H).

Refer to the MICROSYSTEM COMPONENTS HANDBOOK for complete information on programming the 8259A. For a complete discussion of 8Ø86 CPU interrupt handling, refer to the INTEL APPLICATION NOTE AP-59.

3.8 STATUS REGISTER PROGRAMMING

The status register is a write-only 8-bit latch accessible at I/O port addresses C9H through DFH (odd addresses only). The Megabyte page register is a 4-bit latch accessible simultaneously with the status register at the same addresses. The four bits in the Megabyte page register control the Megabyte page address that may be driven on the MULTIBUS interface at connector P2. The functions of the status register bits are described in paragraph 2.5.8.

The eight bits of the status register are accessible only one at a time by writing a byte as specified in Figure 3-1, except that the upper four bits are don't cares. Bits Ø through 2 of this byte specify the status bit to be accessed. Bit 3 of this byte specifies whether the bit is to be loaded with a 1 or a Ø. For example, loading a 1 into status register bit 2 is performed by writing the byte xxxx1Ø1Ø. At power up, or re-initialization, all status register bits contain zeros.

The Megabyte page register is accessible simultaneously with a status register access. Bit 7 of the status register is used to enable loading of the Megabyte page register. Note that this differs from bit Ø of the status register which may be used to enable the Megabyte page drivers, not the Megabyte page register. When bit 7 of the status register is a Ø, the upper four bits of any byte written to the I/O addresses of the status register and the Megabyte page register will be loaded into the Megabyte page register. This includes the byte written to make bit 7 a Ø. When bit 7 of the status register is a 1, the upper four bits of any byte written to these I/O addresses are don't cares. This includes the byte written to make bit 7 a 1.

To load the Megabyte page register typically takes two I/O writes. The first write loads a Ø into status register bit 7 (in order to enable loading the Megabyte page register) and loads the Megabyte page register. All eight bits of this write are significant, as specified in Figure 3-1. The second write is to make bit 7 of the status register a 1, so that future I/O writes to the status register will not corrupt the Megabyte page register. Only the lower four bits of this byte (and all future bytes written to change status register bits Ø through 6) are significant as specified in Figure 3-1. This second write may be omitted if the upper four bits of any future byte contain the bits corresponding to the desired Megabyte page.

Note that the bits written to the Megabyte page register are the binary complement of the desired Megabyte page. Also note that at power up or re-initialization, the Megabyte page register contains zeros, which corresponds to page F.

For example, to load the Megabyte page register with page A, the following two bytes would be written. The first byte, Ø1Ø1Ø111, enables the loading of the Megabyte page register and loads the Megabyte page register with 5, which corresponds to page A. The second byte, xxxx1111, disables loading of the Megabyte page register to prevent other status register writes from affecting the Megabyte page register.

3.9 EDGE-TRIGGERED INTERRUPT LATCH PROGRAMMING

The iSBC 86/35 board contains an edge to level converter to allow the mixture of one edge sensitive interrupt request with as many as seven other level sensitive interrupt requests. The 8259A PIC is programmable to recognize up to eight inputs of either edge triggered interrupts or level type interrupts. This edge to level converter (implemented by a latch) permits you to program the 8259A PIC as a level interrupt detector for seven interrupting sources while the eighth one is an edge sensitive interrupting source. This edge-sensitive latch senses the edge-type interrupt, latches it, and converts it to a level-type interrupt signal for the interrupt sensing logic. After sensing the edge interrupt request, the latch remains set until reset by the CPU. The flip-flop is reset by the 8Ø86 CPU as part of the applicable interrupt service routine. The CPU resets the latch by issuing an ØCW2 to the 8259A as a word write to I/O port address CØ or C4. If a specific end of interrupt is not required by the 8259A programming (e.g. automatic end of interrupt is programmed), then the value from AL should be 4ØH which selects the no-op end of interrupt in ØCW2.

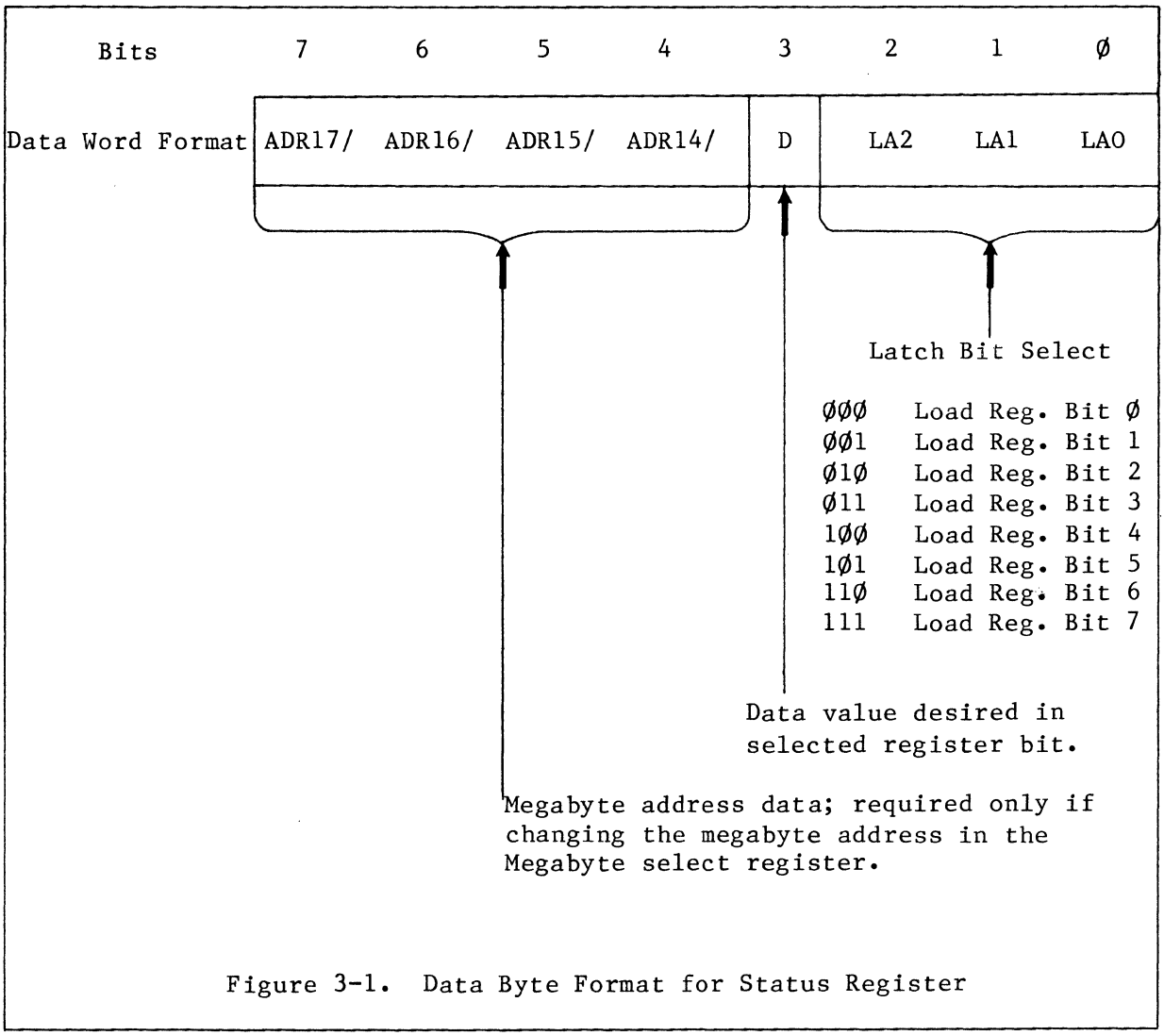

Figure 3-1. Data Byte Format for Status Register

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CHAPTER 4. PRINCIPLES OF OPERATION

4.1 INTRODUCTION

This chapter provides a functional description and a detailed circuit analysis for the iSBC 86/35 board. The description of the iSBC 86/35 board begins by presenting a brief functional description of each of the major components within the block diagram (Figure 4-1). In addition to the functional descriptions, the text presents a detailed circuit analysis of some of the more complex operations performed by the board, including: local memory accessing, MULTIBUS memory accessing, local I/O accessing, interrupt handling, and bus timeout circuit operation.

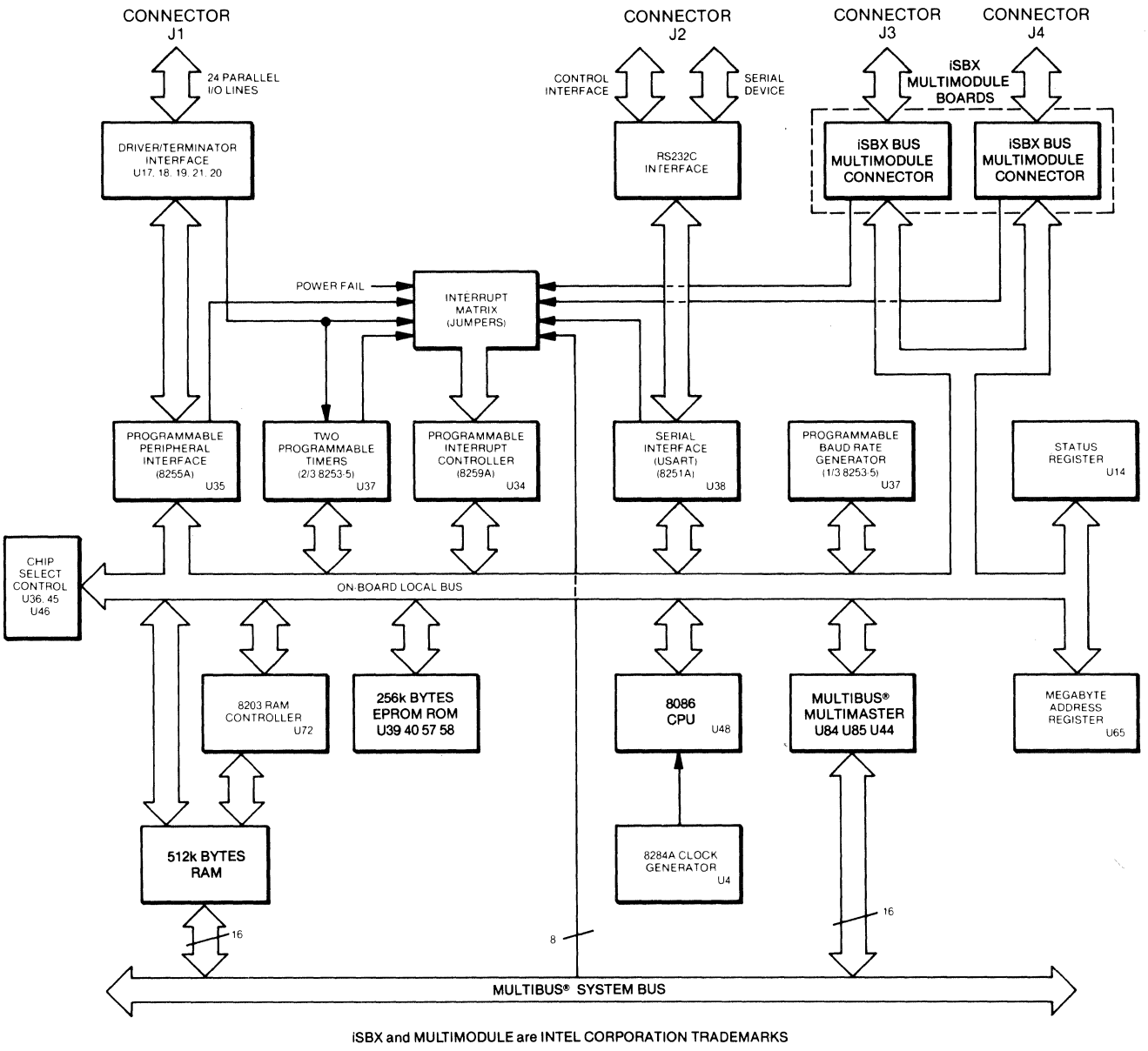
4.2 FUNCTIONAL DESCRIPTION

Figure 4-1 shows the major functional blocks of the iSBC 86/35 board. Each functional block is described in paragraphs 4.2.1 through 4.2.12.2. A detailed circuit analysis for the more complex portions of the iSBC 86/35 board begins at paragraph 4.3.

4.2.1 8Ø86 MICROPROCESSOR

The central processor for the iSBC 86/35 board is Intel's 8Ø86 Microprocessor (referred to hereafter as the CPU) operating at either 5 or 8 MHz. The CPU architecture includes four 16-bit memory base pointer registers, and two 16-bit index registers. All registers are accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for high level language and assembly language data structure support.

The 8Ø86 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions. Additional information on CPU timing and instruction set is available in the INTEL 8Ø86 FAMILY USER'S MANUAL and the INTEL MICROSYSTEM COMPONENT HANDBOOK.



iSBX and MULTIMODULE are INTEL CORPORATION TRADEMARKS

x-723

Figure 4-1. iSBC® 86/35 Board Block Diagram

4.2.2 ON-BOARD TIMING

The CPU may be clocked at a frequency of either 8 MHz or 5 MHz. The latter provides the ability for the iSBC 86/35 board to operate compatibly with the iSBC 337 Numeric Data Processor and with the ICE 86 products. If neither is required in the system, the iSBC 86/35 should be configured for 8 MHz operation.

On-board timing for the CPU is provided by an 8284A Clock Generator device (U4). This device provides either a 8 or 5 MHz clock output for the CPU clock input. The RESET and READY functions for the CPU are also generated by the 8284A device.

Another timing circuit (consisting of a crystal oscillator and two 4-bit counter devices) generates the clock signals for the 8253-5 Programmable Interval Timer and produces the BCLK/ and CCLK/ MULTIBUS clock signals and the MCLK/ iSBX bus clock signal at a frequency of 9.83 MHz.

The 8253-5 Programmable Interval Timer generates timing for the serial port (RxC and TxC baud rate clock) and generates inputs to the interrupt controller.

4.2.3 RANDOM ACCESS MEMORY (RAM) ARRAY

As shipped from the factory, the iSBC 86/35 board contains sixteen 256k x 1 RAM devices with 512 K-bytes enabled as dual port RAM. The local address of the dual port RAM (as-shipped configuration) for the iSBC 86/35 board is ØØØØØH through 7FFFFH (512 K-bytes). When the iSBC 3Ø4 RAM Expansion MULTIMODULE Board is installed, the local address range is ØØØØØH through 9FFFFH (64Ø K-bytes). When the iSBC 314 RAM Expansion MULTIMODULE Board is installed, the local address range is ØØØØØH through DFFFFH (896k) or ØØØØØH through EFFFFH (96Øk).

The dual port control logic interfaces the RAM with the MULTIBUS interface and the on-board bus. This allows the MULTIBUS interface resources to access the dual port RAM when not in use by the iSBC 86/35 board. The dual port logic is designed to maximize the on-board CPU throughput by defaulting control of the dual port RAM to the local CPU when not being accessed via the MULTIBUS interface. Each time a bus master generates a memory request to the dual port RAM via the MULTIBUS interface, control of the RAM must be taken away from the on-board CPU. When the memory request is completed, the control of the RAM returns to the on-board CPU.

The dual port logic consists of CPU address and data buffers and decoders; bidirectional address and data bus (MULTIBUS interface) drivers; slave RAM address decoder/translator; control logic; and the RAM array.

The dual port RAM can be accessed in a word-wide fashion from the MULTIBUS interface; byte-swap logic allows both 8-bit and 16-bit product compatibility. The dual port RAM is inhibited when another memory device generates INH1/ (which causes an overlay of the dual port RAM by another System resource).

The dual port bus can be locked to either the local bus or the MULTIBUS interface; this is typically required in a read-modify-write semaphore operation to prevent the other processor(s) from accessing the dual port memory between the read and write. The iSBC 86/35's CPU locks the dual port to the local bus via the LOCK prefix facility of the 8Ø86 instruction set. When a LOCK XCHG instruction is being executed on a byte in dual port RAM, the dual port bus will be locked to the local bus, blocking MULTIBUS interface access. Conversely, when the MULTIBUS interface LOCK/ line is active during a MULTIBUS interface access to the iSBC 86/35 dual port RAM, the dual port bus will be locked to the MULTIBUS interface, blocking local bus access.

4.2.4 ERASEABLE PROGRAMMABLE READ ONLY MEMORY (EPROM) ARRAY

The iSBC 86/35 board has four sockets for use with EPROM. The board is compatible with four sizes of EPROM devices; either 8k, 16k, 32k or 64k by 8-bit. These are summarized in Chapter 2. The default configuration is for installation of 8 K-byte by 8-bit EPROM devices. EPROM addressing ranges depend on the size of the device and the number of devices installed. Table 2-2 specifies the address range for each socket, according to device size.

4.2.5 ADDRESS DECODING

When the CPU issues an address it outputs three status bits (SØ, S1, and S2) which are latched by the 74S373 Octal Three state Buffer. This generates the MEM/IO signal to indicate whether the address should be examined by the memory decode circuitry or by the I/O decode circuitry. When MEM/IO is a "1", the memory decode circuitry (devices U45 and U46) is enabled; conversely, when MEM/IO is a "Ø", the I/O decode circuitry (device U36) is enabled.

When enabled, the Programmable Array Logic (PAL) devices U45 and U46 decode the address and activate one of the RAM or EPROM chip select signals for the memory array. The PAL device U36 decodes the address and generates the chip select terms for the iSBX bus interfaces, for the status register, and for each of the LSI devices on the board, including the 8255A PPI, the 8253-5 PIT, the 8259A PIC, and the 8251A PCI device.

4.2.5.1 Memory Address Decoding

Memory addressing on the iSBC 86/35 board takes 3 general forms: local addressing for access to MULTIBUS resources, local addressing for access to local resources, and MULTIBUS address decoding for access to local resources.

Local Address to MULTIBUS® Resource

During a local CPU access to a MULTIBUS resource, the local CPU places a 2Ø-bit address (optionally 24-bit when the Megabyte page register is enabled) on the MULTIBUS interface. When the 24-bit address is sent, the upper 4-bits of address (ADR14/, ADR15/, ADR16/, and ADR17/) are programmed into the Megabyte Page Register via the Status Register (U65). After the local CPU acquires MULTIBUS interface control, a signal labeled BUS AEN/ from the Bus Arbiter (U84) routes the upper 4-bit address with the ADRØ/ through ADR13/ lines from U9Ø, U91, and U92 to the MULTIBUS System Bus interface, if enabled.

Local Address to Local Resource

During a local CPU access of on-board RAM or EPROM, the local CPU outputs status onto SØ, S1, and S2, and a local RAM address onto ADØ through AD13. The status and address are decoded by PAL devices U45 (EPROM) and U46 (RAM) to generate the required chip select terms. The PAL devices generate PROM ACCESS and RAM ACCESS signals required for the local operations.

The RAM ACCESS and MEM CMD signals start arbitration for local access to the dual port RAM. The dual port control logic activates the ON BD CMD/ and DP ACCESS/ signals required during a local RAM accessing sequence. The ON BD CMD/ signal gates the local commands (LOCAL DP RD/ or LOCAL DP WT/) from PAL U46 to the RAM controller. The RAM controller then multiplexes the address to the RAM array and completes the operation.

The PROM ACCESS and PROM chip enable signals (PROM Ø HIGH, PROM Ø LOW, PROM 1 HIGH, and PROM 1 LOW) start the local access to the selected EPROM cell. The PROM ACCESS signal generates an enable (via CENPR) to 8288 Bus Controller U44, allowing it to decode the status lines from the CPU. The MRDC/ signal from U44 is sent to the EPROM array, enabling the array to decode address lines A1 through AF.

MULTIBUS® Address to Local Resource

During a MULTIBUS interface access of on-board RAM, the MULTIBUS interface master can address the iSBC 86/35 board as a slave RAM device. The bus master first places the address onto the MULTIBUS interface and then asserts MRDC/ or MWTC/. Address bits ADR1Ø/ through ADR13/ and jumpers E23Ø to E237 and E24Ø to E243 present a 1Ø-bit address to a PROM (U66); address bits ADR14/ through ADR17/ are decoded by a series of exclusive OR gates (U87). ADRF/ and the output signals from U66 ATRØ/ through ATR2/ are enabled by U7Ø (14ZB3) into memory address bits ABF-AB13 when the OFF BD ADR EN/ signal is subsequently activated by the dual port control logic. The pin-11 output from U66 is driven through U29 (when the megabyte address matches) to develop the OFF BD ADR REQ signal to the dual port control logic. If no CPU access is in progress, the dual port control logic enters the slave mode and develops the DP ACCESS/ and SLAVE CMD/ signals. DP ACCESS/ enables RAM controller U72 and SLAVE CMD/ gates the BUS RD CMD/ or BUS MWTC/ signal (11ZB8) to the RAM controller. The RAM controller then multiplexes the address to the RAM array and completes the required operation.

NOTE

Local EPROM is not accessible by another Bus Master.

4.2.5.2 I/O Address Decoding

The I/O decode circuitry consists of PAL device U36, and logic gates U13, U16, U29, U53, and U59. The I/O decode circuitry examines address lines AØ and A3-AF to determine if the address is a valid on-board I/O address and to enable the proper chip select signal. If the address is valid, the I/O decode circuitry activates the I/O ACCESS signal; conversely if not a valid on-board address, the ON BD ADDR/ signal is deactivated.

I/O addressing is discussed in Chapter 3. When the CPU issues an I/O address, one of nine chip select signals is enabled. Each signal corresponds to one of the on-board I/O devices:

8251 CS/ to the PCI device
8253 CS/ to the PIT device
8255 CS/ to the PPI device
8259 CS/ to the PIC device
SBX2 CSO/ to iSBX bus connector J3
SBX2 CS1/ to iSBX bus connector J3
SBX1 CSO/ to iSBX bus connector J4
SBX1 CS1/ to iSBX bus connector J4
PIO CS/ to Status Register and Edge-sensitive Interrupt Latch

Notice that each iSBX bus connector has two chip select signals associated with it. Both signals may not necessarily be used on all iSBX MULTIMODULE boards. Refer to the iSBX board reference manual for exact addressing.

4.2.6 INTERVAL TIMER

The iSBC 86/35 board contains an 8253-5 Programmable Interval Timer (PIT) at chip location U37. The PIT device contains three software selectable counters. Each counter has its own input pin and output pin. Input frequencies are determined by jumper selection. The boards default configuration for the inputs is as follows:

CLKØ Input	1.23 MHz
CLK1 Input	153.6 KHz
CLK2 Input	1.23 MHz

Chapter 2 provides instructions for alternative jumper input selections. All inputs must be 2.5 MHz or less.

The complete functional definition of the interval timer is programmed by system software. A set of control words must be sent out by the CPU to initialize each counter with the desired mode and count information. Each counter consists of a single, 16-bit, presettable, down-counter. The counter can operate in either binary or BCD and its input gate and output are configured by the selection of modes stored in the control word register. Refer to the INTEL MICROSYSTEM COMPONENT HANDBOOK for additional programming information.

4.2.7 SERIAL I/O CONTROL CIRCUITRY

The iSBC 86/35 board uses an Intel 8251A Programmable Communications Interface (PCI) device (U38) to handle serial communications via connector J2. On-board jumpers are used to select the clock source for transmission and reception of data. The RS232C interface may be configured with jumpers as described in section 2.4.6.

The complete functional definition of the PCI is programmed by system software. A set of control words must be sent out by the CPU to initialize the PCI to support the desired communications format. These control words program the baud rate, character length, number of stop bits, synchronous or asynchronous operation, even/odd parity and other parameters. In the synchronous mode, options are also provided to select either internal or external character synchronization.

Once programmed, the PCI is ready to perform its communication functions. The TxRDY signal indicates that the PCI is ready to receive a data character from the CPU. The TxRDY signal is reset automatically when the CPU writes a character into the PCI. When the PCI receives serial data from a modem or I/O device, the RxRDY signal indicates that the PCI has a complete character for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation. The PCI cannot begin transmission until the Tx Enable bit is set in the Command Instruction byte, and it has received a Clear-To-Send (CTS/) input. The TxD output is held in the marking state upon reset.

Refer to the INTEL MICROSYSTEM COMPONENT HANDBOOK for complete PCI programming information.

4.2.8 PARALLEL I/O CONTROL CIRCUITRY

The iSBC 86/35 board provides 24 programmable parallel I/O lines implemented with a single Intel 8255A-5 Programmable Peripheral Interface (PPI) device (U35). These lines are grouped into three software programmable 8-bit I/O ports. On-board usage of each line is variable, depending on mode selection and jumper status. Chapter 2 provides parallel port jumper configurations. Device programming is discussed in the INTEL MICROSYSTEM COMPONENT HANDBOOK.

There are three basic modes of operation which can be selected by system software:

Mode Ø - Basic Input/Output

Mode 1 - Strobed Input/Output

Mode 2 - Bi-Directional Bus

When the reset input gate goes high all ports in the 8255A PPI are set to the input mode (i.e., all 24 lines enter the high impedance state). After the reset is removed, the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any other mode may be selected using a single output instruction.

The modes for Port A and B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, are reset whenever the mode is changed. Modes may be combined so that their functional definition is tailored to almost any I/O structure.

Any of the eight Port C bits can be set or reset using a single output instruction. When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the bit set/reset operation just as if they were data output ports.

For additional 8255A PPI information refer to the INTEL MICROSYSTEM COMPONENT HANDBOOK.

4.2.9 INTERRUPT CONTROL AND TIMING CIRCUITRY

Interrupt circuitry on the iSBC 86/35 board consists of an interrupt source jumper matrix, an 8259A Programmable Interrupt Controller (PIC), and the interrupt acknowledge logic. The 8259A Programmable Interrupt Controller (PIC) handles up to eight bus vectored or non-bus vectored priority interrupts. Interrupt requests to the iSBC 86/35 board can originate from 28 sources without external hardware.

The board can experience three basic types of interrupts: a direct CPU input non-maskable interrupt (NMI); an on-board or off-board (non-bus vectored) interrupt through the PIC; and an off-board (bus vectored) interrupt. Bus vectored interrupts are cascaded from another (slave) PIC device. Bus vectored (BV) interrupts require additional response time as compared to non-bus vectored interrupts. Bus vectored interrupts from the MULTIBUS interface are enabled when the iSBC 86/35 board is in its factory default configuration.

When operating in bus vectored mode, the iSBC 86/35 board must gain control of the MULTIBUS interface for each interrupt; this causes the CPU to execute additional wait-states and may create system contention for

use of the MULTIBUS interface. Remove jumper connection E33-E34 to enable only NBV operation (refer to Chapter 2 for more information). If enabled, the bus vectoring sequence inserts wait-states into the CPU instruction execution timing automatically.

4.2.1Ø 82Ø3 DYNAMIC RAM CONTROLLER

The iSBC 86/35 board contains an 82Ø3 Dynamic RAM Controller that provides multiplexed addresses, address strobes, and refresh/access arbitration for the on-board RAM array. The operation of the 82Ø3 Dynamic RAM Controller is configured at the factory before shipment and should not be changed. The memory refresh cycles are internally requested and internally generated by the 82Ø3 device.

In response to chip select terms and an address, the 82Ø3 Dynamic RAM Controller generates the ROW address strobe signal (RAS/), the COLUMN address strobe signal (CAS/), and the 8-bit cell address required to access the memory array during READ, WRITE, and REFRESH operations. Multiplexer U1Ø5 uses addresses 11 and 12, and CAS/ from the 82Ø3 to produce the ninth address bit required by 256k dynamic RAM's. U1Ø5 also delays the CAS/ signal to allow time for multiplexing the ninth bit.

At any given instant, the 82Ø3 Dynamic RAM Controller may be found in one of the following states: IDLE, WRITE cycle, READ cycle, or REFRESH cycle. In IDLE, the Dynamic RAM Controller monitors internal and external cycle requests and counts toward generation of an internal refresh cycle for the RAM chips.

4.2.11 DUAL PORT ADDRESS RANGE DECODE PROM

The address range of the dual port RAM on the iSBC 86/35 board is defined via U66, a 3625A decode PROM. This PROM device combines address bits ADR1Ø/ through ADR13/ with the user selected dual-port address range (as determined by the placement of jumpers E23Ø through E237 and E24Ø through E243). The resulting output signals from the 3625A PROM provide the high order address bits (ADR1Ø/ through ADR13/) for all RAM accesses. The PROM device also generates the off-board address indication (the OFF BD ADD REQ signal) to indicate whether the address is located in the dual port RAM or located elsewhere in the MULTIBUS address space. The OFF BD ADD REQ signal allows the off-board CPU to begin dual port arbitration.

4.2.12 BUS STRUCTURE

The iSBC 86/35 board architecture is organized around a three-bus hierarchy: the local bus, the dual port bus, and the MULTIBUS interface (refer to Figure 4-2). Each bus communicates only within itself or to an adjacent bus. Performance of the iSBC 86/35 board is inversely related to distance it must go to perform an operation; that is, the closer the instruction execution is to the local bus, the better the performance.

The iSBC 86/35 board operates at either a 5- or 8-MHz CPU clock frequency and requires wait-states for all on-board system accesses (exception: EPROM accesses can be jumpered for zero, one, two, or three wait states). However, the pipeline effect of the CPU instruction queue effectively hides these wait-states.

The core of the iSBC 86/35 board bus architecture is the local bus (AD$\emptyset$ through ADF), which connects the CPU to all on-board I/O devices, EPROM, RAM, iSBX bus interfaces, and the dual port RAM bus. Activity on this bus does not require control of the outer busses, thus permitting independent execution of on-board activities. Activities on the local bus require no bus overhead and provide maximum board performance.

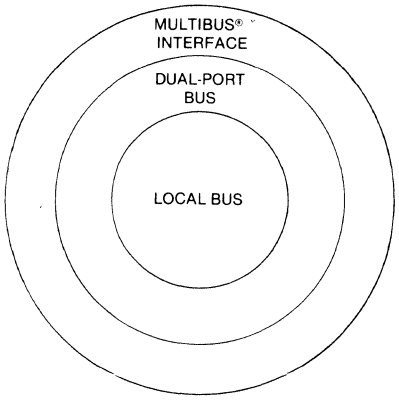
The next bus in the hierarchy is the dual port bus (AB$\emptyset$ through AB13). This bus controls the dynamic dual port RAM and communicates with the local bus and the MULTIBUS interface. The dual port bus can be in one of three states:

a. State 1 - The local bus is controlling the dual port bus but not using it (the dual port bus is considered to be not busy).

b. State 2 - The local bus is controlling the dual port bus and using it (the dual port bus is considered to be busy).

c. State 3 - The system bus is controlling the dual port bus and using it (the dual port bus is considered to be busy).

State 1, as described above, is the idle state of the dual port bus. The dual port bus is left in control of the local bus to minimize delays when the on-board CPU needs the dual port bus. When the local bus requires the dual port bus in order to access dual port RAM, the dual port bus control logic moves from state 1 to state 2 (if the dual port bus is busy, the local bus waits until it is available). Activity at this level requires a minimum bus-overhead and the RAM performance is designed to equal that of protected RAM accesses (when the dual port bus is not found to be busy). The dual port bus control logic returns to state 1 when the on-board CPU completes its operation. This level of bus activity operates independently of the MULTIBUS interface activity (if the MULTIBUS interface does not need the dual port bus).



x-729

Figure 4-2. Internal Bus Structure

When the MULTIBUS interface requests the dual port bus, the control logic goes from state 1 to state 3 (it will wait if busy). Activity at this level requires a minimum of 15Ø nanoseconds and, upon completion, the MULTIBUS interface returns the dual port bus to state 1. The use of the dual port bus by the MULTIBUS interface is independent of the local bus activity.

When the local bus needs the MULTIBUS interface, it must gain access through the dual port bus. In this way the local bus uses the dual port bus only to communicate with the MULTIBUS interface and leaves the dual port bus in state 1. Activity at this level requires a minimum of 2ØØ nanoseconds of overhead for MULTIBUS interface exchanges.

4.2.12.1 MULTIBUS® Interface

The MULTIBUS interface is the system interface. The iSBC 86/35 board communicates with other boards in the system over the MULTIBUS lines. The MULTIBUS lines adhere to a design standard, as specified in the IEEE 796 SPECIFICATION.

Three 8286 Octal Bus Transceivers (U93, U71, and U94) provide the data line interface buffering to the MULTIBUS interface. Two 8287 Octal Bus Transceivers and a bus driver (U9Ø, U91, and U92) provide the address line interface.

In a typical application, the iSBC 86/35 board would be a master board in the system. This means the iSBC 86/35 board could perform MULTIBUS arbitration with all bus master boards in the system. Each board would have a specific priority as controlled by board placement and jumper selection.

MULTIBUS control circuitry includes the 8289 Bus Arbiter device (U84), the 8288 Bus Controller, bi-directional data bus and address bus drivers (U9Ø, 91, 92, 93, 94, and 71), and interrupt driver/receiver (U89). The Bus Arbiter allows the iSBC 86/35 board to operate as a bus master in the system in which the CPU can request the MULTIBUS lines when a resource is required.

4.2.12.2 iSBX™ Bus Interface

Essentially, the iSBX bus is an extension of the local internal bus. This bus interfaces optional plug-in modules via a single iSBX connector. Two such connectors reside on the iSBC 86/35 board (J3 and J4). All necessary power lines, data lines, address lines, and control lines are routed through the two iSBX connectors. The CPU treats the iSBX board as another on-board I/O location. Addressing is discussed in Chapter 3. Pin assignments and signal descriptions for the iSBX bus connectors are given in Appendix E. For additional iSBX MULTIMODULE information, refer to the Intel iSBX SPECIFICATION.

4.3 DETAILED CIRCUIT ANALYSIS

The circuit analysis presented in the following text provides more detailed information on the internal operation of the iSBC 86/35 board. The schematic diagram for the iSBC 86/35 board is provided as Figure 5-3. The schematic diagram consists of 16 sheets, each of which includes grid coordinates. When a logic term is referenced, its grid coordinates on the schematic diagram are presented in parenthesis.

Both active HIGH and active LOW signals are used. A signal mnemonic that ends with a virgule (e.g., DAT7/) denotes that the signal is active LOW (less than Ø.4 volts). Conversely, a signal mnemonic without a virgule (e.g., ALE) denotes that the signal is active HIGH (greater than 2.Ø volts).

4.3.1 POWER-ON INITIALIZATION OPERATION

When power is applied in a start up sequence, the 8284A Clock Generator device generates a reset pulse that provides the reset signal (RST) for several devices on the iSBC 86/35 board. The characteristics of the RST pulse are determined by the time constant created via C62, R33, and CR1. The pulse is typically 1ØØ milliseconds in duration.

The RST and RST/ signals provide the reset function for the resettable devices on the iSBC 86/35 board, including the CPU, the 8289 Bus Arbiter, the 8251A PCI, the 8255A-5 PPI, the interrupt control logic, the iSBX bus connectors, the status register, and the Megabyte page select register. The net effect of a power-up sequence is to set the CPU, Bus Arbiter, I/O ports, and any iSBX modules attached to the iSBC 86/35 board to a known internal state from which orderly operation can commence.

When power is initially applied to the iSBC 86/35 board, capacitor C62 (1ZB7) maintains the Schmitt trigger input at U4 pin-11 (1ZB6) in the logic low state, which causes an active high reset output on U4 pin 1Ø. This active high reset level is inverted by the open-collector driver U3 (2ZB6), generating INIT/ out to the MULTIBUS interface (via connector P1, pin-14) to set the entire system to a known state. The output of U3 is inverted by U11 to generate the RESET signal.

The initialization just described can be performed at any time by activating the AUX RESET/ signal via auxiliary connector P2 pin-38.

After the power-on sequence, the Status Register (U14) and the Megabyte page Register (U65) both contain zeros. Note that zeros in the Megabyte page register corresponds to page F.

4.3.2 CPU OPERATION

The CPU is internally divided into two processors, the Bus Interface Unit (BIU) and an Execution Unit (EU). The BIU is used to constantly monitor the EU and an internal queue for memory or I/O operations. Each time the BIU accesses the iSBC 86/35 internal bus, the CPU executes at least four major cycles, called T-States. The timing required for each T-State is discussed in the following sub-sections. Refer to the INTEL MICROSYSTEM COMPONENT HANDBOOK for more information on CPU operation.

T1 STATE: The first T-State indicates the type of access and the location of the transfer participant. The CPU first activates its status lines SØ/, S1/, and S2/ indicating the type of operation to be performed for the bus cycle, as listed in Table 4-1. When the status lines become active, the 8288 controller activates its Address Latch Enable (ALE) signal and enables the address buffers. While ALE is active, the address is presented on the 8Ø86 multiplexed address/data bus lines.

Before the end of T1, ALE goes inactive latching the address. ALE is also inverted and used to clear the wait state generator. The ALE/ term is used to disable commands from the 8288 controller until the rising edge of T2. The only exception to this sequence occurs if the board is executing an Interrupt Acknowledge (INTA/) cycle. In this case, the 8288 Bus Controller (U44) activates signal MCE. Signals MCE and ALE generate the INT CYCLE signal which activates the off-board address enable term (OFF BD AEN/ on 1ØZA6). The MCE signal is deactivated early in T2.

Table 4-1. 8Ø86 Status Bit Decodes

S2/	S1/	SØ/	CPU Machine Cycle
Ø	Ø	Ø	Interrupt Acknowledge
Ø	Ø	1	Read I/O Port
Ø	1	Ø	Write I/O Port
Ø	1	1	Halt
1	Ø	Ø	Code Access
1	Ø	1	Read Memory
1	1	Ø	Write Memory
1	1	1	Passive

Note: Ø = LOW signal.
1 = HIGH signal.

T2 STATE: During T2 the address presented during T1 is removed from the CPU's address/data bus. There are four types of subsequent bus cycles during T2 following address removal: read cycle, write cycle, interrupt acknowledge cycle, and halt or passive cycles.

If the CPU requests a read cycle, one of the 8288 bus controllers activates either MRDC/ or IORC/. The CPU removes its address from the bus and sets the lines to the receive mode. If the address is valid, the PAL device activates the appropriate chip enable term. After the rising edge of the CPU clock, the commands become active. After the clock's rising edge, the 8288 Bus Controller enables the data buffers by setting the DEN line high (the DT/R line is set low in state T2).

During a write operation, the CPU drives the data lines. After removing the address, the CPU places data on the multiplexed bus. The command, AMWTC/, and AIOWC/, and the chip enable terms become active as during a read cycle. The 8288 Bus Controller activates the DEN signal for the transfer.

An interrupt acknowledge cycle is initiated in the CPU whenever it senses an interrupt request on the INTR line from the 8259A PIC and interrupts are enabled. The CPU generates an interrupt acknowledge status on SØ, S1, and S2, that begins the interrupt acknowledge cycle. The status bits allow the 8288 Bus Controller to activate the INTA/ signal in a series of two pulses. The first INTA/ pulse causes the 8259A PIC to freeze the state of the interrupts for priority resolution and, if performing a bus vectored interrupt cycle, places the slave ID onto the CASØ through CAS2 lines. The second pulse causes the CPU to retrieve the interrupt ID byte (an 8-bit pointer) from the 8259A PIC. The CPU uses the pointer as an address at which to begin the interrupt service routine.

If a HALT or PASSIVE state is indicated on the status lines, no commands are issued. Chip enable terms are still generated and data integrity is maintained.

T3 STATE: During this state, the data transfer consummates when the access time of the peripheral device is met. A READY signal is sent to the 8284A Clock Generator to indicate acknowledgment. If the peripheral does not send an acknowledgment by the rising edge of the previous clock, the CPU enters wait-states until the CPU receives a READY signal via the 8284A.

There are two sources for READY signals. The wait-state generator (U6 on schematic sheet 1ØZC6) is the source for the on-board ready signal. The PAL (PAL device U25 on 1ØZC3) is the source for the off-board ready signal receiving either an XACK/ signal from an off-board resource or the TIMEOUT signal from the timeout generator (U15 on 1ØZA5). When the CPU receives the synchronized 8284A READY output, the status lines are forced to an inactive mode and the CPU is allowed to proceed to state T4.

T4 STATE: During the T4 state all command lines are placed in their inactive mode. All control and direction lines also become inactive, until the CPU status lines are asserted.

HOLD SEQUENCES: The CPU enters a hold sequence by activating the HOLD line or by a co-processor pulsing the RQ/GT line. Typically, this is only done by a co-processor device such as the 8Ø87 on the iSBC 337 Numeric Data Processor. The co-processor pulses the RQ/GT line to obtain control of the local bus. The CPU then sends a return pulse on the same RQ/GT line to indicate that it is ready to relinquish control of the local bus, and places its address and data lines in the inactive state. When the co-processor is finished, it issues a third pulse which enables the CPU to resume normal operation.

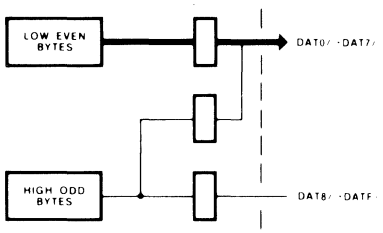
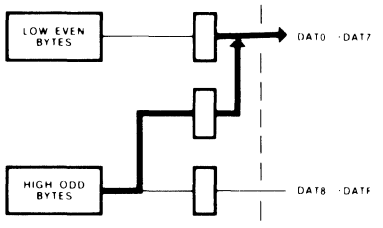
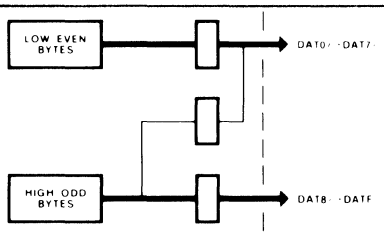
4.3.3 MULTIBUS® DATA TRANSFER MODES

Each iSBC 86/35 board contains three 8286 bidirectional Octal Bus Transceiver devices at chip locations U71, U93, and U94 to buffer the input and output data. As Table 4-2 shows, the transceiver devices provide the interface between the MULTIBUS structure and the on-board memory. The transceiver devices also provide a buffer for performing a data swap operation; i.e., they place the HIGH order data byte from memory onto the LOW order MULTIBUS interface lines during an odd byte output operation, and place the LOW order data byte from the MULTIBUS interface onto the HIGH order memory during an odd byte input operation. When not in use, the transceivers are held in a high impedance state to minimize the loading effects on the MULTIBUS interface.

The bidirectional transceivers are enabled via the WORD EN/, SWAP EN/, and DT/R BUS signals generated by PAL device U25. When the pin-9 input to the transceiver is HIGH, the transceiver is held in a high impedance state (inactive). When the pin-9 input (WORD EN/ or SWAP EN/) is LOW, the pin-11 (DT/R Bus) input to each transceiver controls the direction in which the device passes data. If pin-11 (DT/R Bus) is HIGH, the transceivers transmit data onto the MULTIBUS structure; if pin-11 is LOW the transceivers receive data from the MULTIBUS interface.

The three 8286 octal transceivers provide the iSBC 86/35 board with the flexibility to operate in any of three types of data transfer mode; even byte transfer, odd byte transfer, or 16-bit transfer. Table 4-2 lists the modes selected by the ADØ and BHE/ signals from the CPU and shows a typical transfer path for each type of operation.

Table 4-2. Data Transfer Modes

Transfer Description Master MULTIBUS®	BHE/ Signal	ADØ Signal	Enable Terms and Operations Performed
	HIGH	HIGH	Not used.
	HIGH	LOW	8-bit transfer, low byte to/from even addresses (via DATØ/ through DAT7/). The signal WORD EN/ is low; the signal SWAP EN/ is high.
	LOW	HIGH	8-bit transfer, high byte (swap byte) to/from odd addresses (via DATØ/ through DAT7/). The signal WORD EN/ is high; the signal SWAP EN/ is low.
	LOW	LOW	16-bit transfer, 2 bytes on DATØ/ through DATF/. The signal WORD EN/ is low; the signal SWAP EN/ is high.
Note: The signal DT/R BUS = low for input, = high for output.			

x-735

4.3.3.1 Even Byte Transfer Operation

To transfer a byte to or from an even memory location, the CPU must deactivate AD$\emptyset$ (AD$\emptyset$ is always low for an even byte) and raise BHE/ (for 8-bit operations, BHE/ is always false). The AD$\emptyset$ and BHE/ signals from the CPU generate the write enable terms for the RAM memory array (WE1/ and WE2/). AD$\emptyset$ enters PAL U25 as AB$\emptyset$ to generate the required data transfer buffer control terms (WORD EN/, and SWAP EN/ on 1$\emptyset$ZC3) and enters into the chip select logic to generate the chip select terms. Refer to Table 4-2.

In performing an even byte READ or WRITE operation, the iSBC 86/35 board uses the low order data buffer (U71 on 13ZC6) to transfer the even data byte via MULTIBUS data lines DAT$\emptyset$/ through DAT7/.

4.3.3.2 Odd Byte (Swap) Transfer Operation

To transfer a byte to or from an odd memory location, the CPU must activate both AD$\emptyset$ and BHE/. In performing an odd byte operation, the iSBC 86/35 board uses the swap buffer (U94 on 13ZC6) to transfer the odd data byte to/from MULTIBUS data lines DAT$\emptyset$/ through DAT7/.

4.3.3.3 16-Bit Transfer Operation

The 16-bit word transfer is initiated when the CPU deactivates the AD$\emptyset$ signal and activates the BHE/ signal. This condition transfers the odd byte of data on the DAT8/ through DATF/ data lines and transfers an even byte of data via DAT$\emptyset$/ through DAT7/.

In performing a 16-bit operation, the iSBC 86/35 board uses both 1) the high order data buffer (U93 on 13ZD6) to transfer the odd data byte across MULTIBUS data lines DAT8/ through DATF/ and 2) the low order buffer (U71 on 13ZC6) to transfer the even data byte across MULTIBUS data lines DAT$\emptyset$/ through DAT7/.

4.3.4 DUAL PORT RAM ACCESS CONTROL LOGIC

The dual port RAM access control logic (schematic sheet 12) allows the dual port RAM on the iSBC 86/35 board to be shared by both the local CPU and another bus master operating on the MULTIBUS interface. When accessing the dual port RAM, the local CPU request is granted priority over an off-board CPU's request for access. In a situation where both CPU's issue a request for dual port RAM access at the same instant, the off-board CPU access is held off until the local CPU has completed its particular read or write operation. When an off-board CPU access is in progress, the dual port control logic enters the slave mode and any subsequent local CPU request will be held off until the slave mode is terminated. Figures 4-3 and 4-4 show timing diagrams of the signal

sequences occurring within the dual port control logic for slave mode operation (off-board CPU access) and master mode operation (local CPU access).

4.3.5 DUAL PORT RAM ACCESS OPERATION

The iSBC 86/35 board is designed to handle on-board RAM cycles asynchronous to the operation of the CPU (via the 82Ø3 RAM Controller). When the CPU attempts to access on-board RAM, it can be found in one of two states; either not busy or busy. Both sequences are described in the following paragraphs.

4.3.5.1 Dual Port RAM Access Cycle Without Contention (Not Busy)

If the CPU attempts to access the RAM and finds it not being used by another bus master and not being requested for use, then the Bus Arbitration logic grants the access to the local CPU immediately.

The RAM access cycle begins when the CPU outputs the status and address. The 8288 decodes the status bits and generates the ALE signal which strobes the address into the address latches. The address decode logic (PAL U46 on 4ZB4) decodes the status bits and provides a memory READ or memory WRITE command (LOCAL DP RD/ or LOCAL DP WT/) to the memory array, and also decodes the address bits on ADF through AD13 to activate the RAM ACCESS signal and the ON BD ADDR/ signal from U22 (4ZC3).

The ON BD ADDR/ signal allows the CPU to enter a wait-state cycle (either one or two required for an on-board RAM access) and disables the 8289 Bus Arbiter from arbitrating for access to the MULTIBUS interface.

The RAM ACCESS signal enters the dual port arbitration logic (schematic sheet 12) and locks the dual port RAM into an on-board access condition. As such, the dual port logic asserts the ON BD CMD/ signal and the DP ACCESS/ signal and disables the SLAVE CMD/ signal. The DP ACCESS/ signal enables the 82Ø3 RAM Controller to accept a READ or WRITE command. Both commands are derived from PAL device U46 and routed to the 82Ø3 RAM Controller via U86 (11ZB7).

When the 82Ø3 RAM controller completes the RAM access cycle, the 82Ø3 activates the dual port transfer acknowledge signal (DP XACK/). The DP XACK/ signal generates a RAM XACK/ signal that enters the on-board ready control circuitry on schematic sheet 1Ø. The RAM XACK/ signal and the ON BD CMD/ signal generate ON BD RDY to the 8284A allowing the CPU to continue processing data.

4.3.5.2 Dual Port RAM Access Cycle With Contention

When the CPU attempts to access the on-board RAM and finds it being used by another bus master, then the Bus Arbitration logic enters an arbitration cycle to gain access to the dual port RAM.

The bus arbitration begins when the dual port logic recognizes that another bus master is presently accessing the dual port RAM. In this condition, the remote bus master is asserting its commands to the dual port RAM via the BUS MRDC/ and BUS MWTC/ signals from the MULTIBUS interface. When either command is active and the iSBC 86/35 board is being addressed, the result is the generation of an off-board RAM request signal (OFF BD RAM REQ on schematic sheet 14ZC3) to the dual port RAM arbitration logic. The OFF BD RAM REQ signal locks the dual port arbitration logic (schematic sheet 12) into an off-board access mode in which the local command and grant signals (ON BD CMD/ and ON BD GNT/) are inactive, and the SLAVE DEN signal, the SLAVE CMD signal, the OFF BD ADR EN/ signal, and the DP ACCESS/ signal are active. Each of the signals is instrumental in inhibiting an on-board access to dual port RAM while an off-board access is occurring.

When the on-board CPU requires access to on-board dual port RAM resources that are being accessed by another bus master, the on-board CPU must begin the access by asserting the status and address as for other types of operations. PAL U46 decodes the address as before, and activates the ON BD ADR/ signal to the 8289 Bus Arbiter (U84 on 3ZA4). The ON BD ADR/ signal prevents the 8289 Bus Arbiter from requesting the MULTIBUS interface.

The local CPU does not gain access to the dual port RAM until the remote bus master has completed its operation. At that time, the 82Ø3 RAM Controller asserts the DP XACK/ signal and the remote bus master deactivates the bus command signals (BUS MRDC/ and BUS MWTC/). The inactive OFF BD RAM REQ signal enters the dual port arbitration logic and allows the pending on-board request to acquire the dual port RAM access rights.

The latched status lines from the CPU are decoded through PAL U46 to activate the local commands (LOCAL DP RD/ OR LOCAL DP WT/), the on-board RAM access signal (RAM ACCESS), the dual port request signal (DP REQ/), and the memory command signal (MEM CMD) to the dual port arbitration logic.

The RAM ACCESS, DP REQ/, and MEM CMD signals enter the dual port arbitration logic (schematic sheet 12) and lock the dual port arbitration logic into an on-board CPU access condition. In this state, the dual port logic asserts the ON BD CMD/ signal, the DP ACCESS/ signal and disables the SLAVE CMD/ signal.

The ON BD CMD/ signal routes the local commands from PAL U46 to the 82Ø3 RAM Controller. The DP ACCESS/ signal enables the 82Ø3 RAM Controller to accept a READ or WRITE command.

When the local CPU completes its RAM access cycle, the 82Ø3 RAM Controller activates the dual-port transfer acknowledge signal (DP XACK/). The DP XACK/ signal generates the RAM XACK/ signal. The RAM XACK/ signal and the ON BD CMD/ signal generate ON BD RDY to the 8284A Clock Generator. ON BD RDY allows the local CPU to continue processing as soon as the RAM Controller completes the RAM cycle. The number of wait states required for any RAM access cycle depends on the current dual port activity and depends on whether a refresh cycle is in process. A typical RAM access operation at 8 MHz requires 2 wait states; at 5 MHz, it requires 1 wait state.

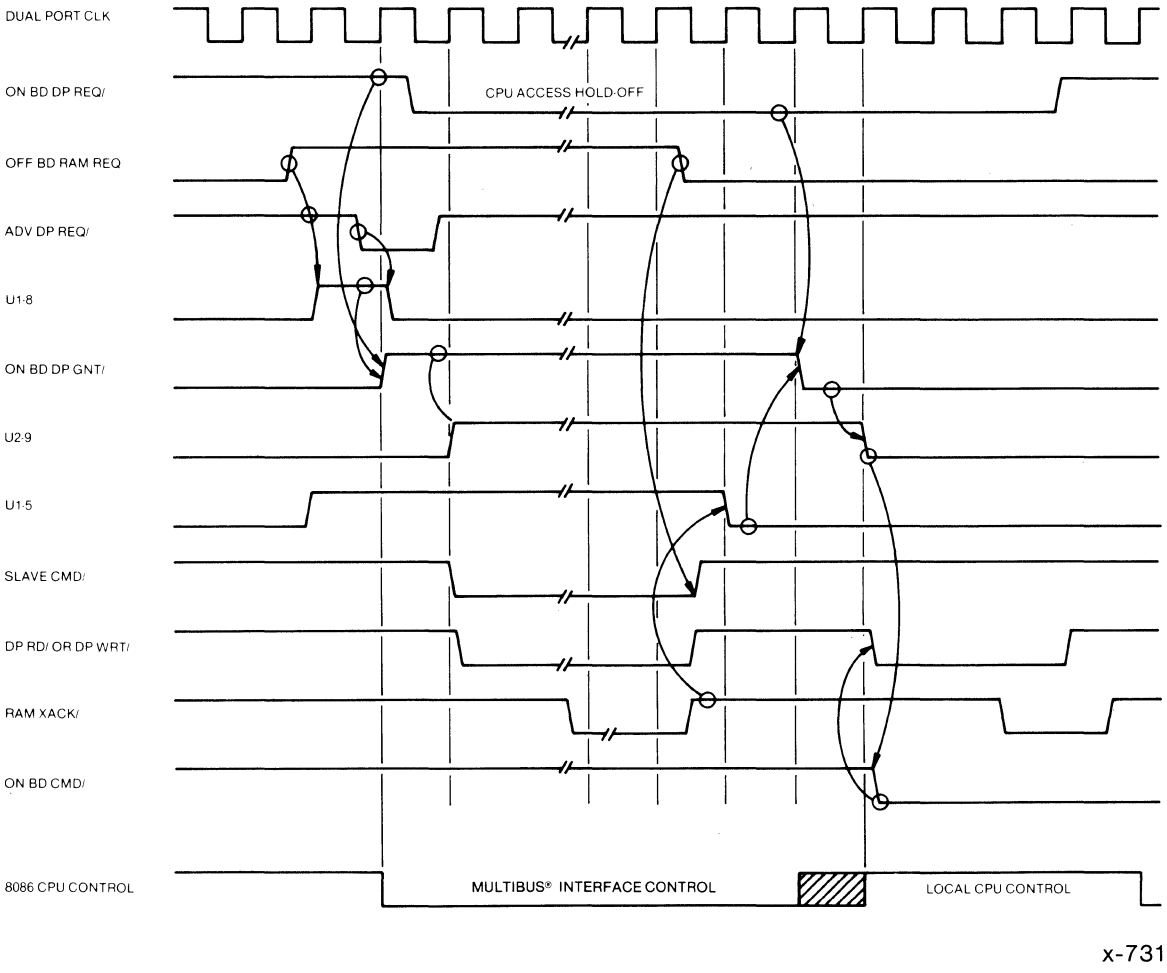


Figure 4-3. Slave Mode Dual-Port Access (CPU Lockout)

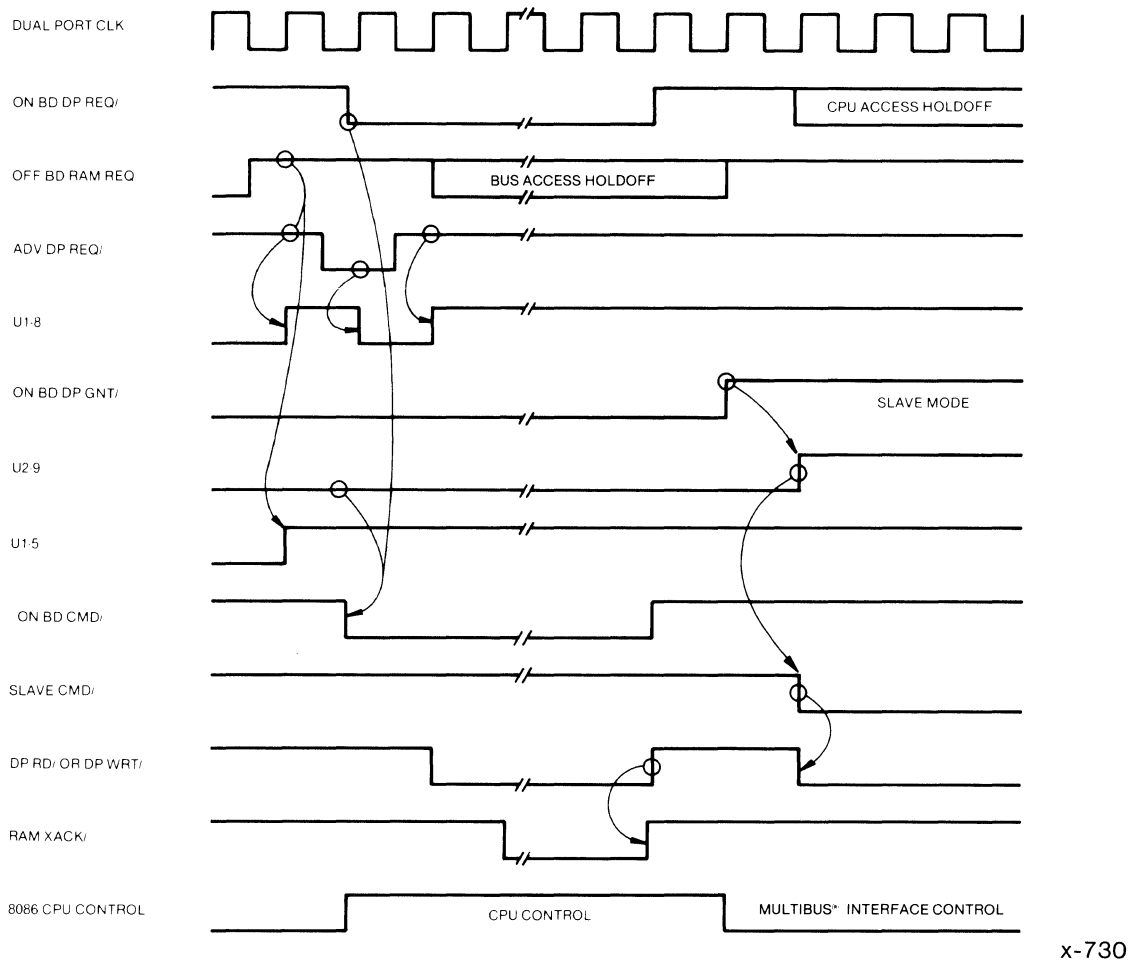


Figure 4-4. Master Mode Dual-Port Access (MULTIBUS® Lockout)

4.3.5.3 RAM Controller Operation Timing

The iSBC 86/35 board 82Ø3 Dynamic RAM Controller provides multiplexed addresses, address strobes, and refresh/access arbitration for the on-board RAM array. The operation of the 82Ø3 Dynamic RAM Controller is configured at the factory and must not be changed. The memory refresh cycles are internally requested and internally generated by the 82Ø3 device.

In response to chip select terms, commands, and addresses, the 82Ø3 Dynamic RAM Controller generates the Row address strobe signal (RAS/), the Column address strobe signal (CAS/), and the 8-bit cell address required to access the memory array during read and write operations.

Multiplexer U1Ø5 uses addresses 11 and 12 and CAS/ from the 82Ø3 Dynamic RAM Controller to produce the ninth address bit required by the 256 K-byte dynamic RAM's. U1Ø5 also delays CAS/ to allow time for multiplexing the ninth bit. The ninth bit is not used for refresh operations.

A write cycle starts when the WT/ input to the 82Ø3 Dynamic RAM Controller (pin 31) goes LOW. During the write cycle, an address on AB1 through AB1Ø and AB13 is routed to the 82Ø3 device which, in turn, generates the row and column addresses for the memory array. The 82Ø3 Dynamic RAM Controller generates row and column address strobe signals (RAS/ and CAS/) when the address on OUTØ/ through OUT7/ is valid. With the assertion of RAS/, CAS/, WE1/, and WE2/ signals, the RAM array begins the data storage operation. After completing the data storage operation, the Dynamic RAM Controller generates XACK/. Receipt of a refresh cycle request during a write operation causes the refresh cycle to occur immediately following the write cycle.

The read cycle operation within the 82Ø3 Dynamic RAM Controller is the same as that of the write cycle except that the RD/ signal is asserted and the write enable signals (WE1/ and WE2/) on the RAM board are disabled, implying a read operation. Receipt of a refresh cycle request during a read operation causes the refresh cycle to occur immediately following the read cycle.

The 82Ø3 Dynamic RAM Controller contains an internal Refresh Timer that performs the refresh cycle automatically. In generating a refresh cycle, the 82Ø3 device activates the RAS/ signal to enable access to the memory array as for the read or write operation; however, neither the CAS/ signal nor the column address is generated. The timing required for an internal refresh cycle is the same as that of a read or write cycle, as shown in Figure 4-5. More information on the operation of the 82Ø3 Dynamic RAM Controller is available in the MICROSYSTEM COMPONENTS HANDBOOK.

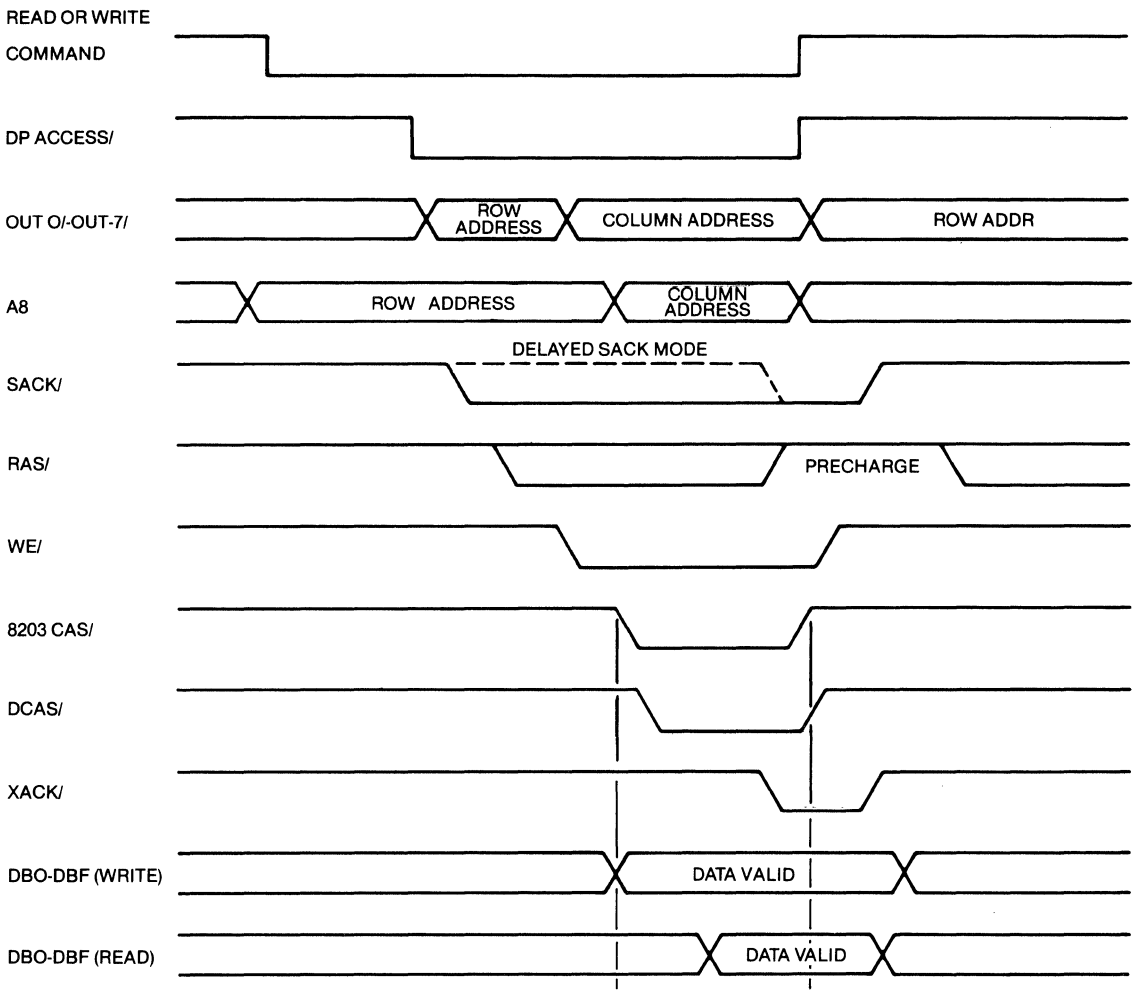


Figure 4-5. Typical Dynamic RAM Operation Sequence x-727

4.3.6 ON-BOARD EPROM ACCESS SEQUENCE

Accesses to the EPROM devices begin when the CPU asserts the status on SØ through S2. The 8288 Bus Controller decodes the status from the CPU and initiates the memory read operation. For an EPROM access, the 8288 decodes a memory read operation and the CPU places the address onto the local bus (ADØ through AD15). As a result of decoding the status bits, the 8288 Bus Controller (U44 at 3ZD4) generates the ALE signal which strobes the address into the address latches (U47, U51, and U52 on 3ZB3). The 8288 device also generates a MRDC/ or an AMWTC command. The Programmable Array Logic (PAL) device (U45 on 4ZD5) decodes address bits ADC through AD13 to generate three signals: one signal, (PROM ACCESS), defines the memory address as an EPROM access so the wait state generator can produce READY at the proper time. The other two signals are used to produce the appropriate chip enable term (either PROM Ø LOW/, PROM 1 LOW/, PROM Ø HIGH/, or PROM 1 HIGH/). The operation is further defined

via the ADØ and BHE/ signals from the CPU. These signals enable the 2-to-4 line decoders (U56 at 4ZD3), effectively providing an 8- or 16-bit operation selection (refer to Table 4-2).

Logic devices U43 and U42 delay the CEN (command Enable) signal to the 8288 Bus Controller (U44 on 3ZD4). The various types of EPROM devices have standard access times that may, in some cases, require insertion of wait-states into the instruction execution cycles of the CPU. Depending on the clock frequency selected for operation of the board, the EPROM access times could vary from 228 ns to 1Ø54 ns, as listed in Table 4-3. The jumper configuration required for each condition is listed in Chapter 2.

Table 4-3. EPROM Access Time Verses Wait-State Selection

CPU Clock Frequency	Access Time Required	Number of Wait-States Required
8 MHz	228 ns	None
8 MHz	353 ns	One wait-state.
8 MHz	478 ns	Two wait-states.
8 MHz	6Ø3 ns	Three wait-states.
5 MHz	454 ns*	None
5 MHz	654 ns*	One wait-state.
5 MHz	854 ns*	Two wait-states.
5 MHz	1Ø54 ns*	Three wait-states.

Note: * These figures are for 8-MHz 8Ø86-2 CPU running at 5-MHz. In-circuit emulators may have different access time requirements.

4.3.7 ON-BOARD I/O ACCESS OPERATION

I/O access operations are similar to EPROM read operations; that is, the CPU provides the status and the addresses and the 8288 Bus Controller (U44 at 3ZD4) provides either an IORC/ signal for an I/O read cycle or an AIOWC/ signal for an I/O write cycle. Both IORC/ and AIOWC/ are delayed as was the MRDC/ signal for the EPROM read operation. The PAL device (U36 on 4ZA4) decodes the address on ADØ through ADF and activates the I/O ACCESS signal from U29 (4ZB3) and the on-board address (ON BD ADDR/ signal from U22 at 4ZC3). The PAL device also generates a specific chip select signal for the device being accessed. Upon receiving the select signal, an address, and a command, the selected I/O device begins the operation.

The iSBC 86/35 board must allow a specific number of wait states to occur during which the I/O device is allowed to complete its cycle. After the period elapses, the iSBC 86/35 board resumes CPU operation by activating the ON BD RDY signal which releases the CPU from its wait state execution. Chapter 2 contains the wait-state jumper selection configuration. Table 4-4 defines the relationship between the I/O access time and the number of wait states inserted into the I/O operation for each clock rate on the iSBC 86/35 board.

NOTE

The as-shipped configuration of the wait state jumpers assumes that the board operates at 8 MHz. If you reconfigure the board to operate at 5 MHz, reconfigure the wait state jumpers also.

Table 4-4. I/O Access Time Verses Wait-State Selection

CPU Clock Frequency	Access Time Required	Number of Wait-States Required
8 MHz	438 ns	2
5 MHz	538 ns*	1

Note: * This figure is for 8-MHz 8Ø86-2 CPU running at 5-MHz. In-circuit emulators may have different access time requirements.

4.3.8 iSBX™ BUS ACCESS OPERATION

Accesses to devices on the iSBX bus interface are similar to I/O cycles in that the CPU provides status and address and the 8288 Bus Controller provides the command decode (either IORC/ or AIOWC/). PAL device U36 decodes the address on ADØ through ADF to activate one of the chip select terms for one of the iSBX bus connectors. The iSBC 86/35 board must be configured to allow a specific number of wait states to occur, during which the iSBX bus device is allowed to complete its cycle.

After the period elapses, the iSBC 86/35 board resumes CPU operation by activating the ON BD RDY signal which releases the CPU from its wait state execution. Chapter 2 contains the wait state jumper selection configuration. Table 4-4 defines the relationship between the wait states and the access time.

4.3.9 TYPICAL LOCAL ACCESS TO MULTIBUS® RESOURCE

MULTIBUS accesses by the local CPU are performed asynchronously to CPU operations. The local CPU places status onto the SØ through S2 lines and an address onto ADØ through ADF. The activation of ALE strobes the address (on AØ through A13) into the address buffers (U47, U51, and U52; see schematic sheet 2ZC3). The address decode logic decodes the addresses and drives ON BD ADR/ high if the address is not a valid local address.

The 8289 Bus Arbiter decodes the status bits (SØ, S1, and S2) and, since signal ON BD ADR/ is high, a MULTIBUS access cycle is requested. When the iSBC 86/35 board obtains priority (BPRN/ is low) and the MULTIBUS interface is not busy (BUSY/ is high), the 8289 Bus Arbiter assumes control of the MULTIBUS interface. After acquiring the MULTIBUS interface, the iSBC 86/35 board transmits the address and data. The accessed device signals completion of the operation by asserting the XACK/ signal.

If the MULTIBUS interface is found to be busy when the iSBC 86/35 board attempts to perform a MULTIBUS access operation, the 8289 Bus Arbiter (U84; see schematic sheet 3ZA4) asserts the BREQ/ and CBRQ/ signals to begin arbitrating for use of the bus. One effect that assertion of BREQ/ has on the iSBC 86/35 board is to unLOCK the on-board dual port RAM immediately. This eliminates the possibility that another bus master is holding the MULTIBUS interface while waiting to gain access to the LOCKed on-board dual port RAM.

If the LOCK/ or OVERRIDE/ signals are active, or if the BPRN/ signal is active and the CBRQ/ signal is inactive, the local CPU will retain control of the MULTIBUS interface on completion of the access. The MULTIBUS interface remains in this condition until: 1) LOCK is deactivated, or 2) CBRQ/ goes active and the CPU completes a MULTIBUS cycle. Refer to paragraph 2.5.1Ø for more information on CBRQ operation.

4.3.1Ø INTERRUPT OPERATION

The iSBC 86/35 board supports both bus-vectored and non-bus-vectored interrupt generation through the use of an 8259A PIC device. In both types of operation, the on-board PIC (U34; see schematic sheet 8ZC3) must be the master PIC in the configuration.

When an interrupt request is sensed by the master PIC, it activates the INTR line to initiate an interrupt cycle in the CPU. Figure 4-7 provides the timing for a typical bus-vectored interrupt and for a typical non-bus-vectored interrupt cycle. The following paragraphs describe the operation of a bus-vectored (BV) and a non-bus-vectored (NBV) interrupt on the iSBC 86/35 board.

4.3.1Ø.1 NBV Interrupt Sequence

An NBV interrupt is one in which the interrupt vector is generated by the on-board PIC. An NVB interrupt does not require sending an interrupt vector across the MULTIBUS interface. Assume for explanation purposes that an NBV interrupt is initiated by an on-board device activating the IR5 interrupt request signal to the PIC. The interrupt sequence occurs as follows.

If no other higher priority interrupt is currently being serviced, the IR5 input causes the PIC to activate the INTR signal. The INTR signal suspends the current code execution in the CPU. The CPU then executes an interrupt acknowledge cycle that places status onto SØ, S1, and S2 (all bits LOW); the status initiates the interrupt acknowledge cycle in the 8288 Bus Controller.

The 8288 Bus Controller decodes the status lines and activates the MCE and INTA/ signal outputs, then activates the MCE signal, which asserts the INTA CYCLE signal. The active INTA CYCLE signal, along with jumper E33-E34, either enables or disables the 8289 Bus Arbiter from arbitrating for control of the MULTIBUS interface.

For an NBV interrupt with jumper E33-E34 installed, the 8288 Bus Controller (external bus, U85) decodes the status lines from the CPU and activates the BUS INTA/ signal when the board gains control of the MULTIBUS interface. During the local operation, the ON BD ADR/ signal is high; the BUS AEN/ and BUS INTA/ signals cause the LOCAL INTA signal to go active; and the CPU activates the LOCK/ signal to the MULTIBUS interface to ensure that the MULTIBUS interface is controlled throughout the interrupt cycle.

For an NBV interrupt with jumper E33-E34 removed, the 8288 Bus Controller (local bus, U44) decodes the status lines from the CPU and activates the local INTA/ signal. The acquisition of the MULTIBUS interface is not required. During the local operation, the ON BD ADR/ signal is LOW. The ON BD ADR/ and local INTA signals cause the LOCAL INTA signal to go active.

On receipt of an INTA/ signal from one of the 8288 Bus Controllers, the on-board PIC freezes the state of its internal priority resolution logic. PAL device U25 (1ØZC3) uses the first INTA/ signal to activate the LOCAL INTA signal. This signal generates a FIRST INTA/ signal to indicate that this is the first of two INTA cycles and to prepare for the next INTA cycle. The FIRST INTA/ signal and the input to pin 19 from the wait-state shift register U6 activate the OFF BD RDY signal from the PAL device to allow the CPU to complete the first INTA cycle.

On receipt of the second INTA/ pulse from the 8288 Bus Controller, the PIC places an 8-bit interrupt ID for IR5 onto the local data bus (DØ through D7) and activates its EN/ output. The EN/ signal activates signal 59 DEN to the PAL device (U25 on 1ØZC3) indicating that the INTA cycle is a local one. The PAL device generates an OFF BD RDY signal as a result of the 59 DEN signal input and the input to pin 19 from the wait-state shift register U6. At that time the CPU reads the interrupt vector from the 8259A PIC. The CPU must then multiply the vector by 4 to obtain an interrupt service routine address for IR5.

After the interrupt service routine is completed, the CPU automatically restores the affected flags and returns to normal program execution.

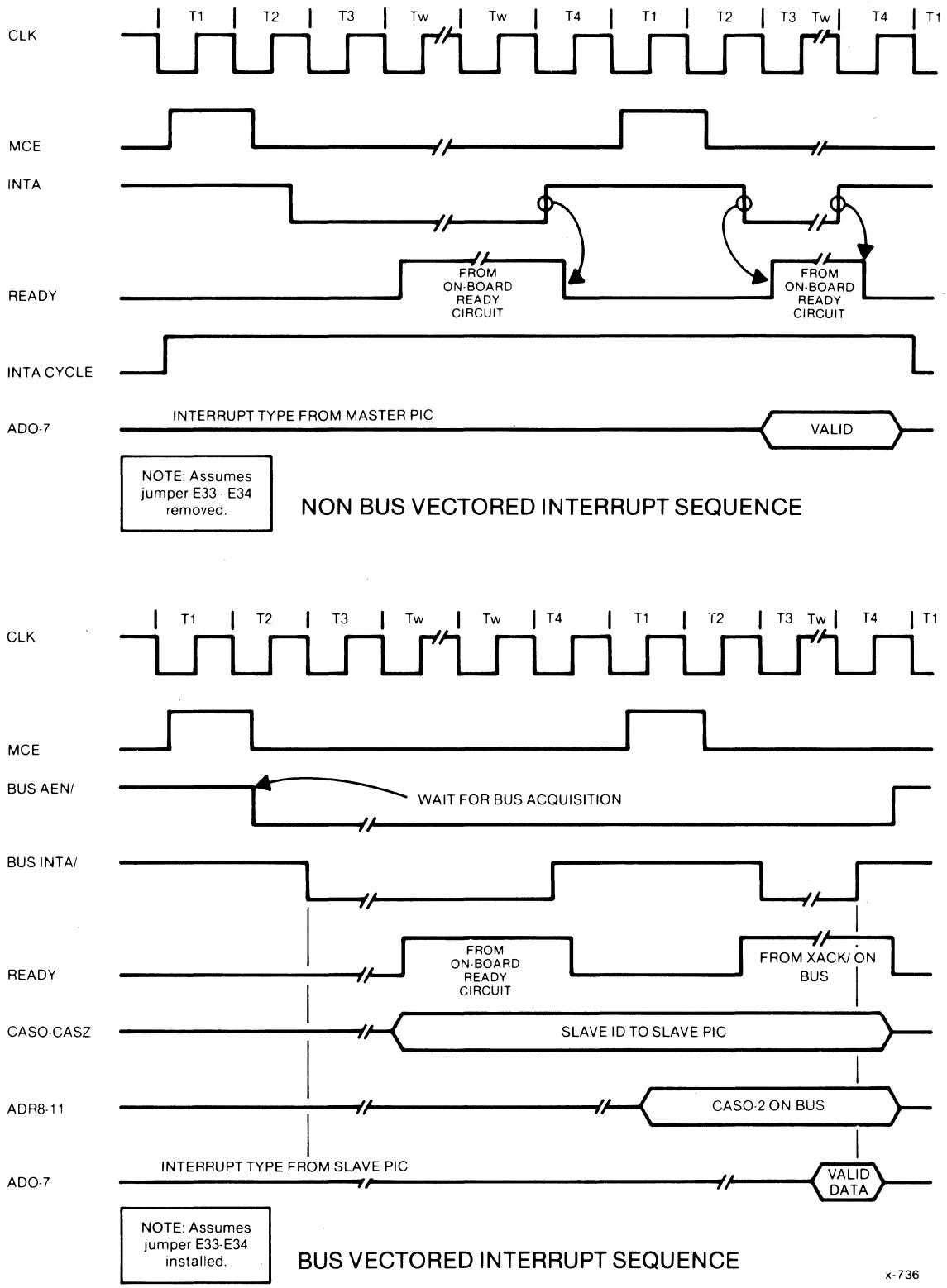


Figure 4-6. MULTIBUS® Access Timing

4.3.1Ø.2 BV Interrupt Sequence

The BV interrupt sequence appears to the 8Ø86 CPU to be similar to the NBV interrupt sequence except that the interrupt vector is applied to the CPU from a slave PIC rather than from the master (on-board) PIC. Assume for explanation purposes that the master PIC receives an IR6 interrupt request from a slave PIC. The interrupt sequence occurs as follows.

A typical BV sequence begins when an interrupt request is sensed on interrupt line (IR6). Providing that no other higher priority request is being serviced, the master PIC responds by generating an interrupt request signal (INTR) to the CPU. The CPU responds by executing an interrupt acknowledge cycle that places status onto its status lines (SØ, S1, and S2).

The 8288 Bus Controller (U85) decodes the status lines and activates the MCE signal which activates the INTA CYCLE signal. Jumper E33 to E34 being installed disables the ON BD ADR/ signal. The inactive ON BD ADR/ signal enables the 8289 Bus Arbiter to begin arbitration for control of the MULTIBUS interface.

When the 8289 Bus Arbiter obtains control of the bus, it activates BUS AEN/, which generates a BUS INTA/ signal from the 8288 Bus Controller (U85). The BUS INTA/ signal is applied to the MULTIBUS interface and causes the slave PIC to freeze the internal state of its priority resolution logic. Locally, the BUS INTA/ signal generates the FIRST INTA/ and 8259A INTA/ signals to perform the following functions:

- The 8259A INTA/ signal allows the master PIC to place the interrupt ID byte on the CASØ through CAS2 lines.

- The FIRST INTA/ signal and the input to pin 19 from the wait-state shift register U6 generate the OFF BD RDY signal to provide a READY input to the CPU, allowing the CPU to complete the first interrupt acknowledge bus cycle.

The second interrupt acknowledge bus cycle activates the MCE signal again and generates the second INTA/ pulse from the 8288 Bus Controller (U85) to the MULTIBUS interface. The functions performed by each are as follows:

- The MCE signal enables the slave ID byte (on CASØ through CAS2) and gates the byte on AD address lines ADR8/ through ADRA/.

- The INTA/ pulse causes the slave PIC to recognize its slave ID on AD8 through ADA, read the interrupt ID byte, place an interrupt vector onto MULTIBUS data lines DATØ/ through DAT7/, and activate the XACK/ line on the MULTIBUS interface.

By activating the XACK/ signal, the slave device indicates that the interrupt vector is available on the MULTIBUS data lines. The XACK/ signal generates another READY signal (OFF BD RDY) to the CPU via PAL device U25, allowing the CPU to read the interrupt vector, terminate the interrupt, and begin servicing the interrupt request.

4.3.11 FAILSAFE TIMER OPERATION

The iSBC 86/35 board contains a Failsafe Timer that generates a bus timeout signal (TIME OUT INTR/) when an expected response from another device (in the form of an XACK/ signal) is too late in arriving back to the iSBC 86/35 board.

When the timeout interval has elapsed with jumper E38-E39 installed, single-shot U15 activates the TIME OUT INTR/ signal which enables the generation of the local interrupt (LOCAL INTA) signal. The LOCAL INTA signal to PAL device U25 generates the ready (OFF BD RDY) signal to the CPU.

The duration of the timeout interval results from the time constant created by components R13 and C7 (1ØZB5) and the occurrence of the ALE signal. The ALE signal occurs every instruction cycle, which retriggers single-shot device U15. If the ALE signal does not occur within approximately 4 milliseconds, the U15 output pulse activates the TIME OUT INTR/ signal. Jumper connections on the iSBC 86/35 board allow use of the TIME OUT INTR/ signal (if jumpered properly within the interrupt logic) to interrupt the CPU, indicating that a timeout condition has occurred.

4.3.12 PAL OPERATION

The iSBC 86/35 board contains Programmable Array Logic (PAL) devices which provide address and command decoding to generate the required chip select terms for the operation to be performed. The PAL devices are fused program devices whose output signals are dependent on the factory programming performed before shipping the board. The iSBC 86/35 board contains four PAL devices that provide several functions required for board operation.

The internal operation of the PAL devices, to this point, has been handled as though the device where a black box; that is, when a certain input signal combination occurs, a predefined output results. However, in certain cases, the internal operation of the PAL devices must be known. Appendix G contains the Boolean equations that describe the operation of these devices.

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CHAPTER 5. SERVICE INFORMATION

5.1 INTRODUCTION

This chapter contains the service and repair assistance instructions, connector dimensioning diagram, jumper post location diagram, parts location diagram, and schematic diagram.

5.2 SERVICE DIAGRAMS

The connector dimensioning diagram, jumper location diagram, parts location diagram, and schematic diagram for the iSBC 86/35 board are shown in Figures 5-1, 5-2, 5-3, and 5-4, respectively.

The schematic diagram is current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides a photocopy of the current schematic diagram with the board, when it is shipped from the factory. This diagram should be inserted into this manual for future reference.

On the schematic diagram, a signal mnemonic that is followed by a virgule (slash) (for example, ALE/) is active low. Conversely, a signal mnemonic without a virgule (for example, ALE) is active high.

5.3 SERVICE AND REPAIR ASSISTANCE

Customers within the United States can obtain service and repair assistance by contacting the Intel Product service Marketing Administration in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for detailed service information and repair assistance.

Before calling the Product Service Marketing Administration, you should have the following information available:

1. The date on which you received the product.
2. The complete model number (including the dash number) and serial number for the product. These numbers are stamped onto Intel printed circuit boards.
3. Your shipping and billing addresses.
4. A purchase order number, for billing purposes if your Intel product warranty has expired.
5. Any applicable extended warranty agreement information.

Use the following numbers for contacting the Intel Product Service Marketing Administration group:

Regional Telephone Numbers:

Western Region:	6Ø2-869-4951
Midwestern Region:	6Ø2-869-4392
Eastern Region:	6Ø2-869-4Ø45
International:	6Ø2-869-4862

TWX Numbers:

91Ø - 951 - 133Ø
91Ø - 951 - Ø687

Always contact the Product Service Marketing Administration group before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information that will help Intel to provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment, or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to Intel, use the original factory packing material, if possible. If this material is not available, wrap the product in cushioning material such Air Cap TH-24Ø, manufactured by Sealed Air Corporation, Hawthorne, N. J. Then, pack it in a heavy corrugated paper shipping carton, and label it "FRAGILE" to ensure careful handling. Ship it only to the address specified by the Intel Product Service Marketing Administration personnel.

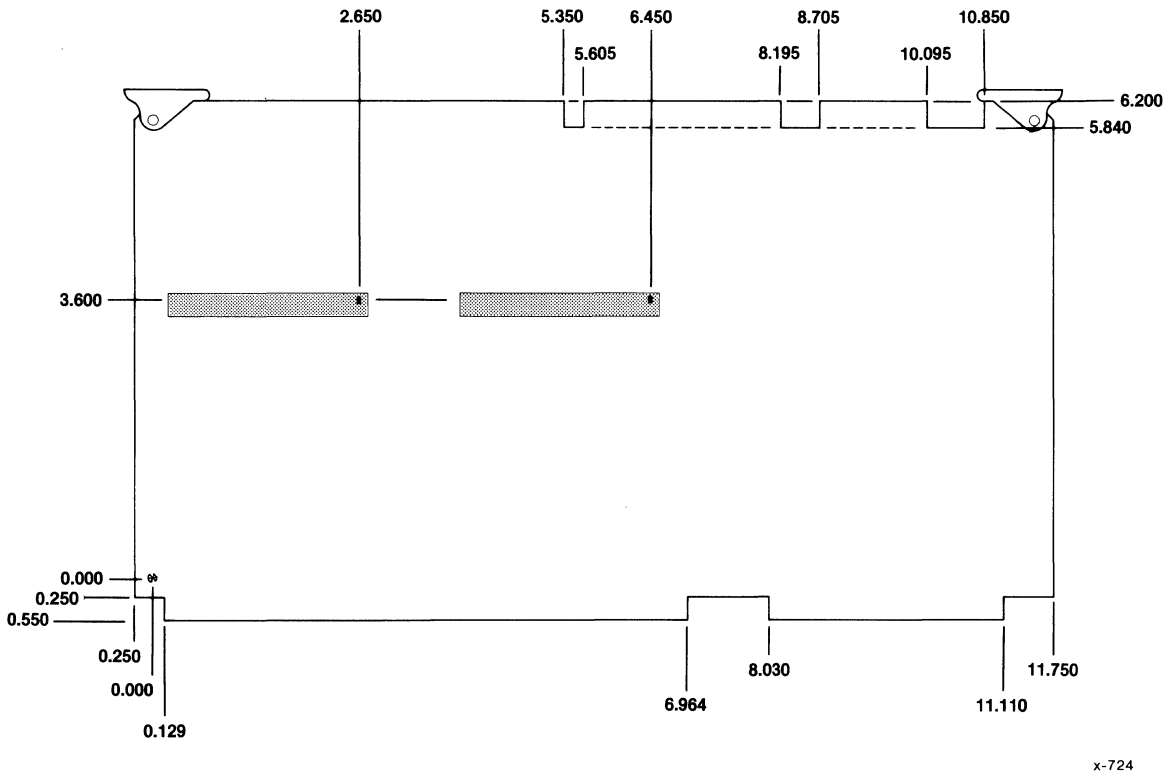


Figure 5-1. Connector Dimensioning Diagram

Jumper Number		Jumper Number	
From	To	From	To
E2	E3	E112	E113
E7	E11	E114	E115
E13	E14	E144	E145
E15	E16	E147	E158
E17	E18	E151	E152
E22	E23	E175	E176
E26	E27	E178	E179
E28	E32	E184	E185
E3Ø	E31	E189	E193
E33	E34	E19Ø	E194
E38	E39	E191	E195
E42	E43	E2Ø2	E2Ø3
E44	E53	E2Ø5	E2Ø7
E45	E54	E2Ø8	E2Ø9
E46	E55	E21Ø	E211
E47	E56	E213	E214
E48	E57	E238	E239
E49	E58	E254	E255
E5Ø	E59	E258	E259
E51	E6Ø	E261	E262
E52	E61	E265	E266
E84	E85	E267	E269
E88	E89	E27Ø	E272
E9Ø	E91	E275	E276
E92	E93	E277	E278
E94	E95	E283	E284
E96	E97	E286	E287
E96	E1Ø2	E292	E293
E98	E99	E294	E295
E98	E1Ø4		

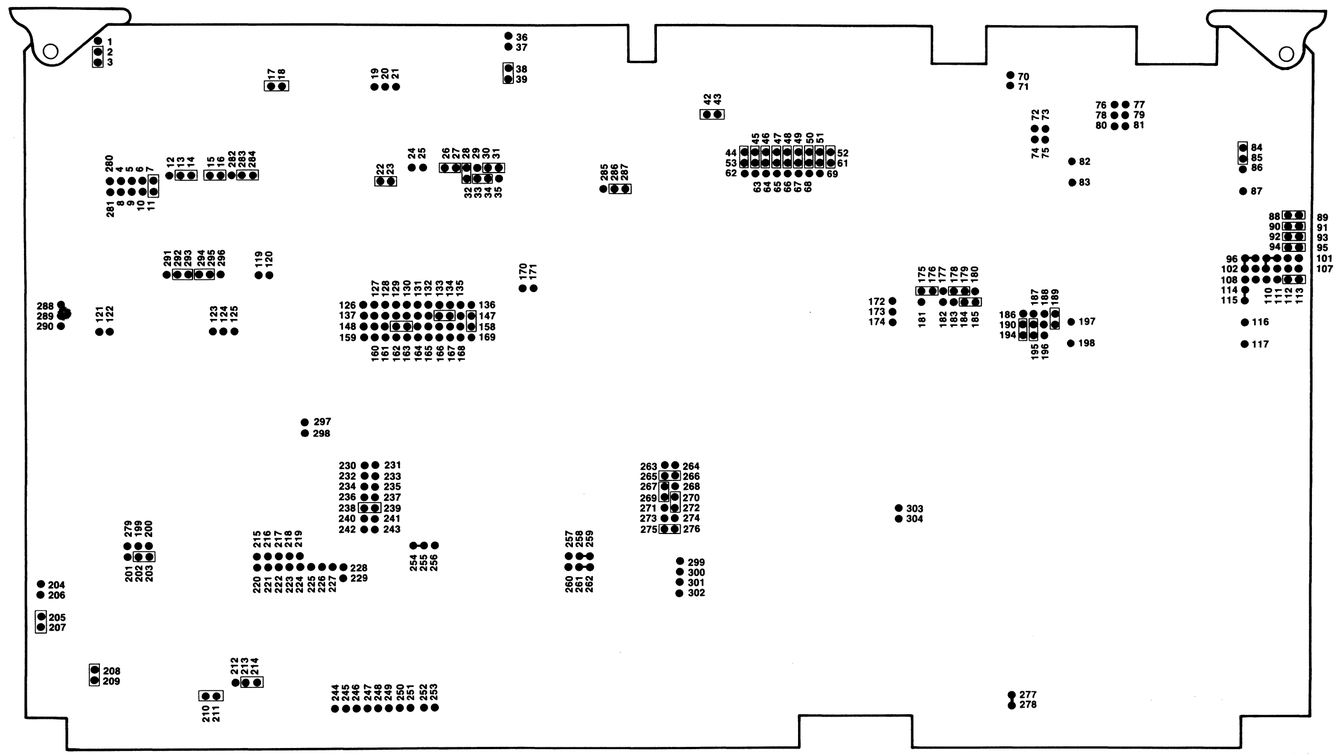


Figure 5-2. Jumper Location Diagram

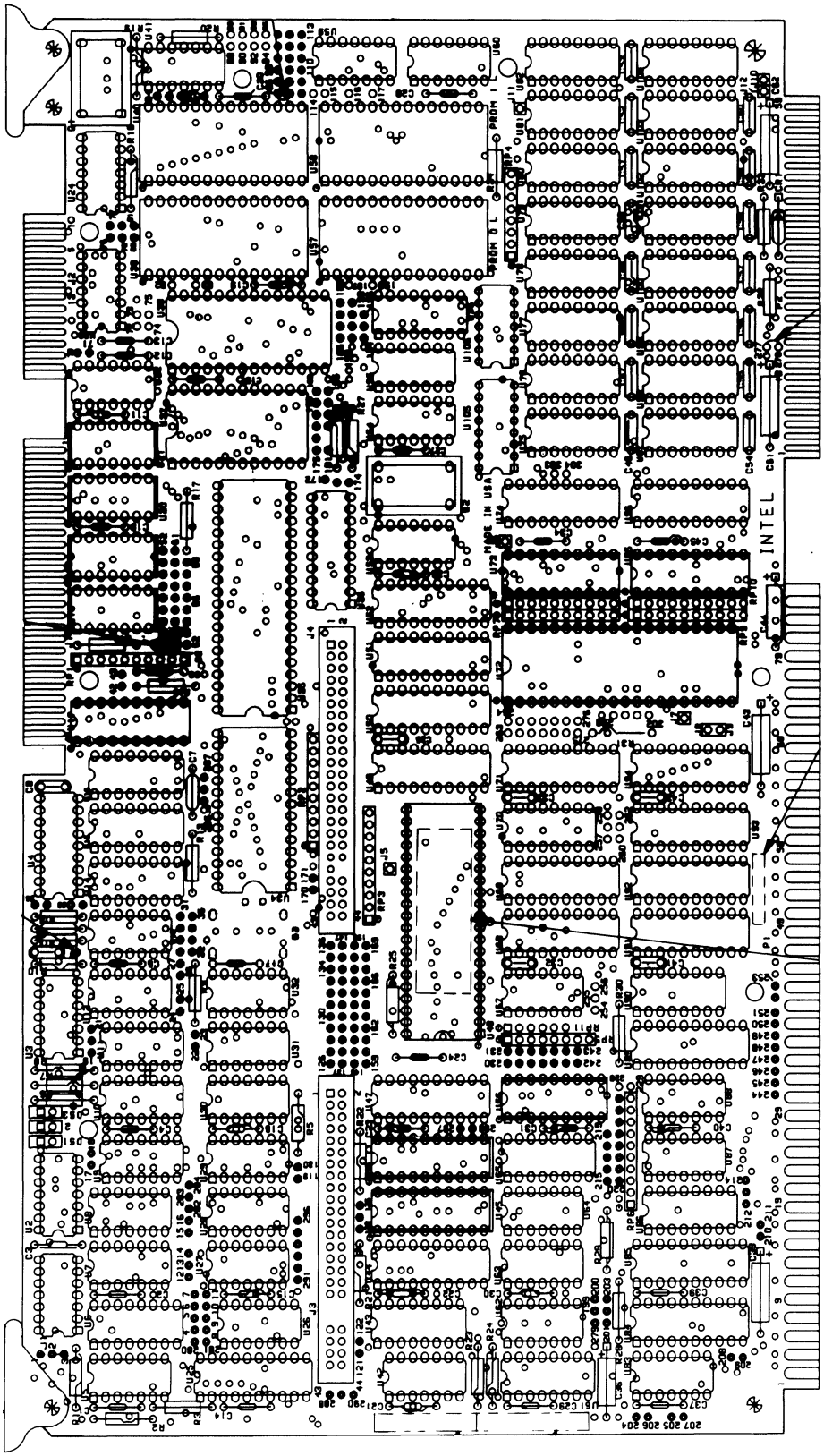


Figure 5-3. Parts Location Diagram

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-4187	R.T.	3/1/84	[illegible]	3/2/84	[illegible]	3/5/84

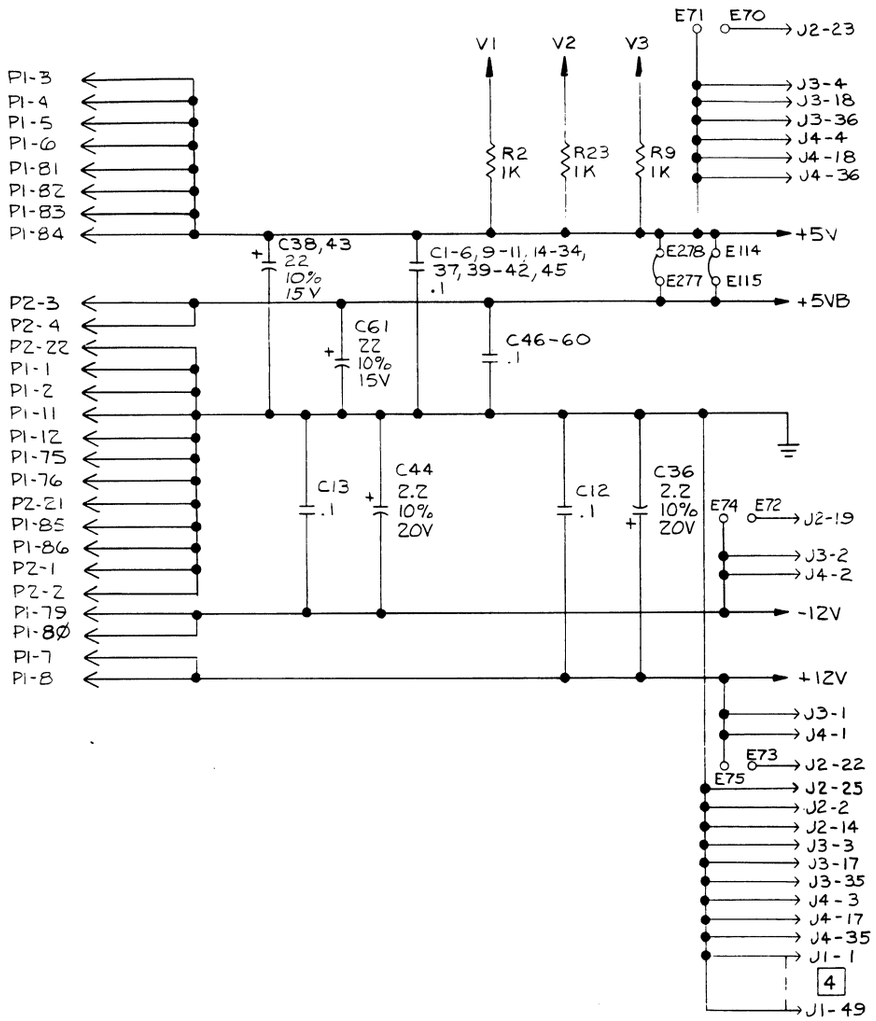


TABLE 1

DEVICE TABLE

REFERENCE DESIGNATION	DEVICE TYPE	POWER PINS GND	+5V	+12V	-12V	+5VB	UNUSED LOGIC ELEMENT OUTPUT PINS
U10,30,42	74S00	7	14				
U59	74S00	7				14	
U29	74S02	7	14				
U28,62	74S04	7	14				
U11,55	74LS04	7	14				U55-6
U3	7406	7	14				
U12,27	74S08	7	14				U12-8
U54	74LS08	7	14				U54-11
U7,8,9	74S10	7	14				
U13,26,63	74S32	7	14				
U31	74LS32	7	14				
U60	74LS32	7				14	U60-11
U83	74128	7	14				U83-1,13
U1,2,5	74S74	7	14				
U32	74LS74	7	14				
U43	74S112	8	16				
U15	74LS123	8	16				U15-13
U67,106	74125	7	14				U106-11
U64	74LS132	7	14				
U16,56	74S139	8	16				
U6	74S174	8	16				U6-12
U89	74LS240	10	20				
U14	74LS259	8	16				
U53	74S260	7	14				
U87,88	74LS266	7	14				
U70,90	74LS366	8	16				U70-13
U61,86	74367	8	16				
U47,51,52,73,95	74S373	10	20				
U41	74LS393	7	14				
U22	74S64	7	14				
U65	74LS173	8	16				
U23	75189A	7	14				
U24	75188	7		14	1		
U66 [6]	3625A	9	18				
U48	8086-2	1,20	40				
U72	8203	20				40	
U38	8251A	4	26				
U37	8253-5	12	24				
U35	8255A-5	7	26				
U34	8259A	14	28				
U4	8284A	9	18				
U71,93,94	8286	10	20				
U17,91,92	8287	10	20				
U44,85	8288	10	20				
U84	8289	10	20				
U36 [6]	12L6	10	20				
U25,45 [6]	14H4	10	20				
U68,69	74LS373	10	20				
U49,U50	8304	10	20				
U105	74F157	8				16	
U74,96	8303	10	20				
U46 [6]	16L8A	10	20				

TABLE 3

PROM DECODE OPTIONS

		JUMPERS FROM	TO	
	2764	—	—	3
	27128	E124	E125	
	27256	E123	E124	
	27512	E124	E125	
		E123	E124	

TABLE 4

RAM DECODE OPTIONS

BOARD CONFIGURATION	JUMPERS [illegible]	ADDRESS RANGE	
86/35	[illegible]	0-FFFFH	3
86/35+304	[illegible]	0-3FFFFH	
86/35+314	[illegible]	0-3FFFFH	
86/35+314	[illegible]	0-FFFFFH	

TABLE 5

iSBX DECODE OPTIONS

iSBX CONNECTOR	DATA BUS SIZE	JUMPERS FROM	TO	
iSBX 1 (J4)	8 BIT	—	—	3
	16 BIT	E173	E174	
iSBX 2 (J3)	8 BIT	—	—	3
	16 BIT	E172	E173	

TABLE 6

PROM JUMPER TABLE

DEVICE TYPE	START ADDRESS BANK Ø	BANK 1	JUMPERS FROM	TO	
2764	F8ØØØ	FCØØØ	E98	E99	3
			E98	E104	
27128	FØØØØ	F8ØØØ	E98	E99	
			E98	E104	
			E109	E110	
27256	EØØØØ	FØØØØ	E98	E99	
			E98	E104	
			E109	E110	
			E100	E10	
			E100	E105	
27512	CØØØØ	EØØØØ	E99	E104	
			E99	E105	
			E109	E110	
			E100	E101	
			E100	E106	

NOTES: UNLESS OTHERWISE SPECIFIED:

1. [illegible] ARE IN MICROFARADS, +80%, -20%, 50V.
2. [illegible] ARE IN OHMS 1/4 W, ± 5%.
3. [illegible] REFER TO [illegible].
4. [illegible] NUMBERED PINS OF J ARE CONNECTED TO GROUND.
5. [illegible]
6. [illegible]
7. THESE PARTS NOT INSTALLED.

TABLE 2

RESISTOR PACK CHART

REFERENCE DESIGNATION	RESIST. VALUE	NUMBER OF PINS	UNUSED PIN NUMBERS
RP1	5.6 K	10	
RP2,3,6, 8, 10	2.2 K	10	RP2-10, RP3-4
			RP5-2
			RP10-2
RP4,5	10 K	8	RP4-7,8
RP7,9	1 K	10	
RP11	2.2K	6	RP11-2

REF DESIGNATIONS LAST USED	NOT USED
C62	C35
CR1	
DS3	
E304	E40,41,118
G3	
J12	
P2	
R34	R4,14
U106	U33
Y1	
RP11	

QUANTITY PER DASH NO.
UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ± XX ± XXX ±

ITEM NO.	DESCRIPTION
	PARTS LIST

SIGNATURE	DATE
DRN BY [illegible] Johnson	3/1/84
CHK BY [illegible]	3/2/84
ENGR APVD [illegible]	3/5/84
APVD	
APVD	

intel® 3065 BOWERS AVE SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC DIAGRAM iSBC 86/35

SIZE	DCLC	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	0.00		146073	A

SCALE NONE SHEET 1 OF 16

Figure 5-4. Schematic Diagram (Sheet 1 of 16)

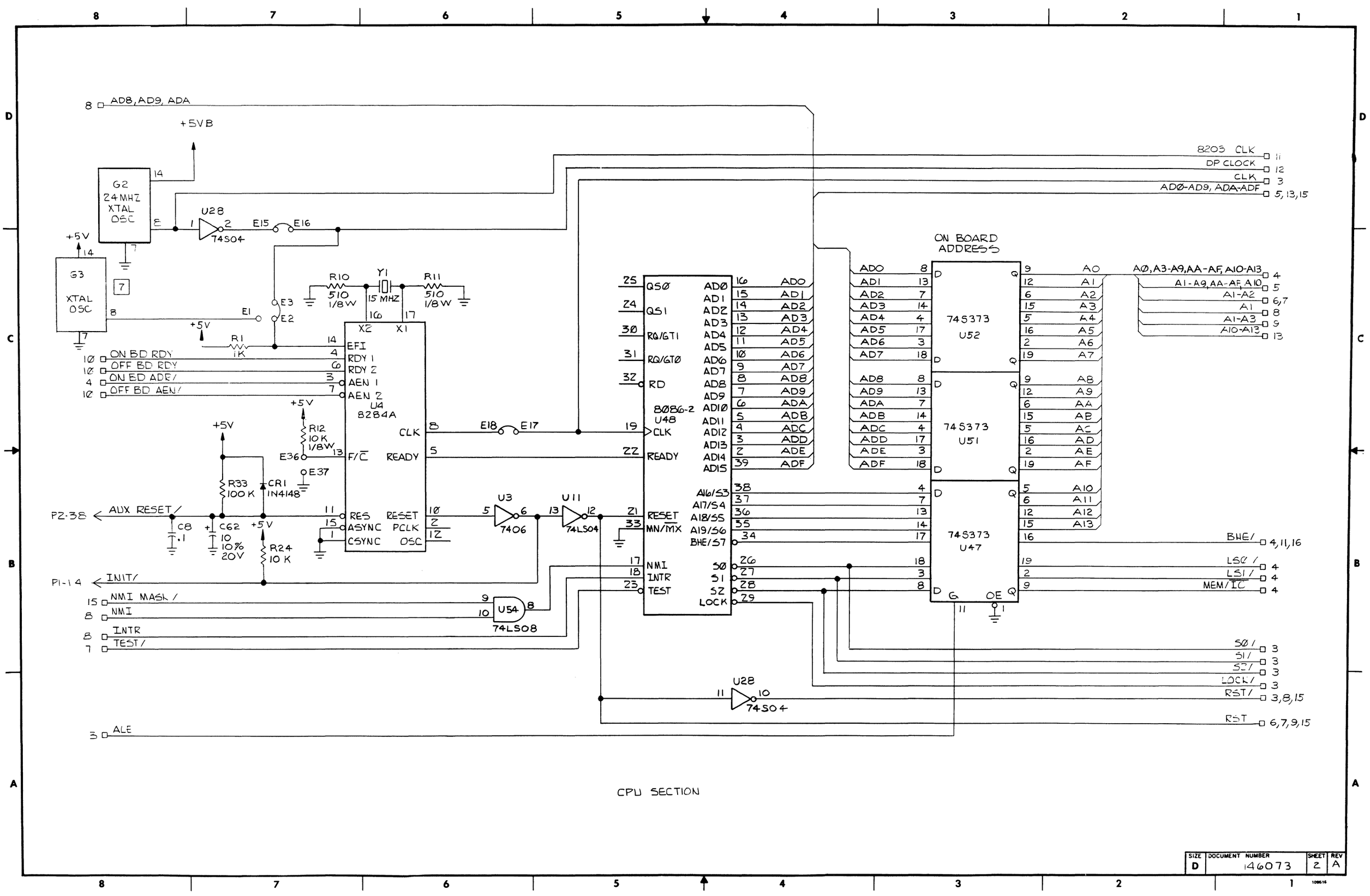


Figure 5-4. Schematic Diagram (Sheet 2 of 16)

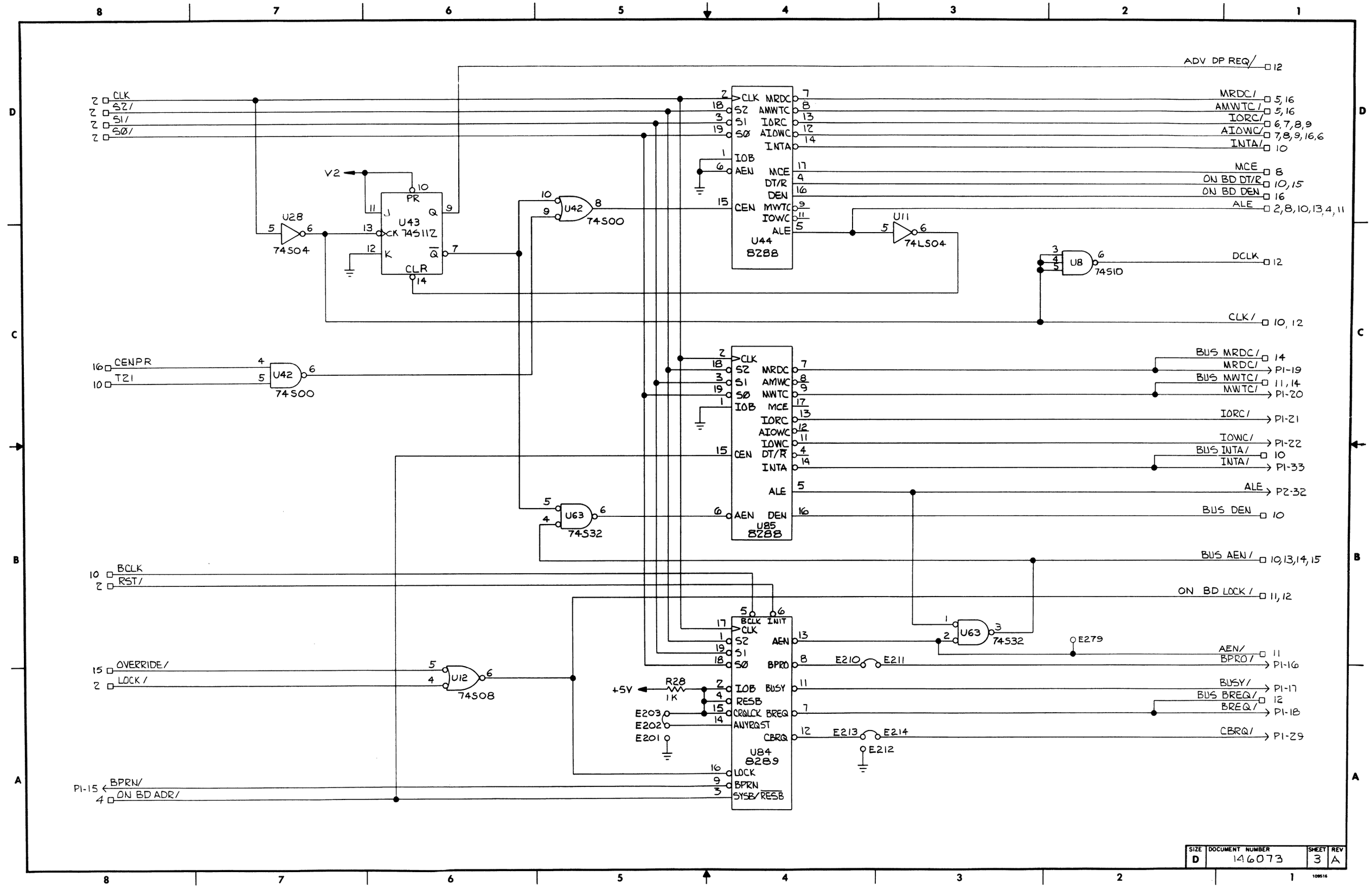
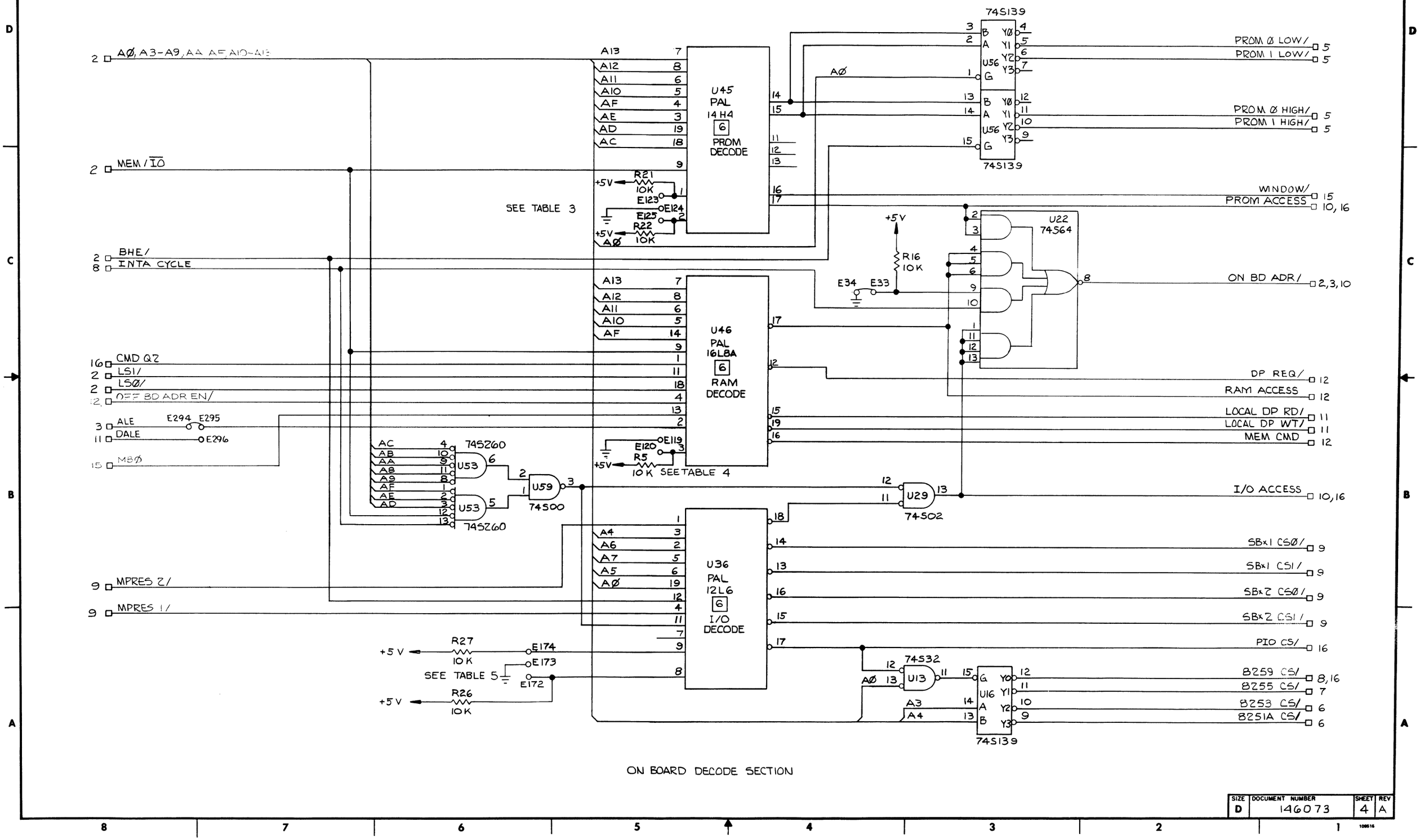


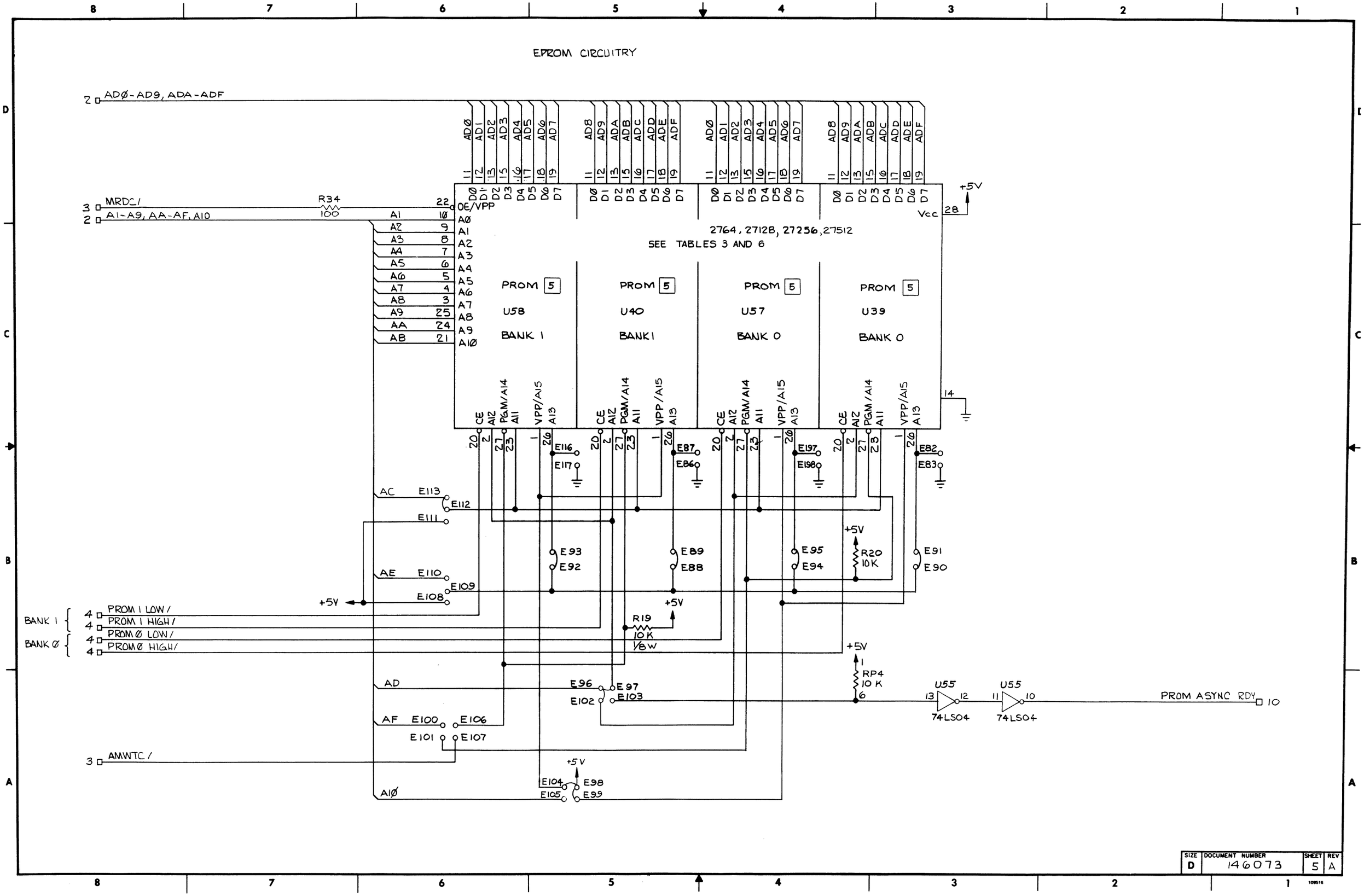
Figure 5-4. Schematic Diagram (Sheet 3 of 16)



ON BOARD DECODE SECTION

SIZE	DOCUMENT NUMBER	SHEET	REV
D	146073	4	A

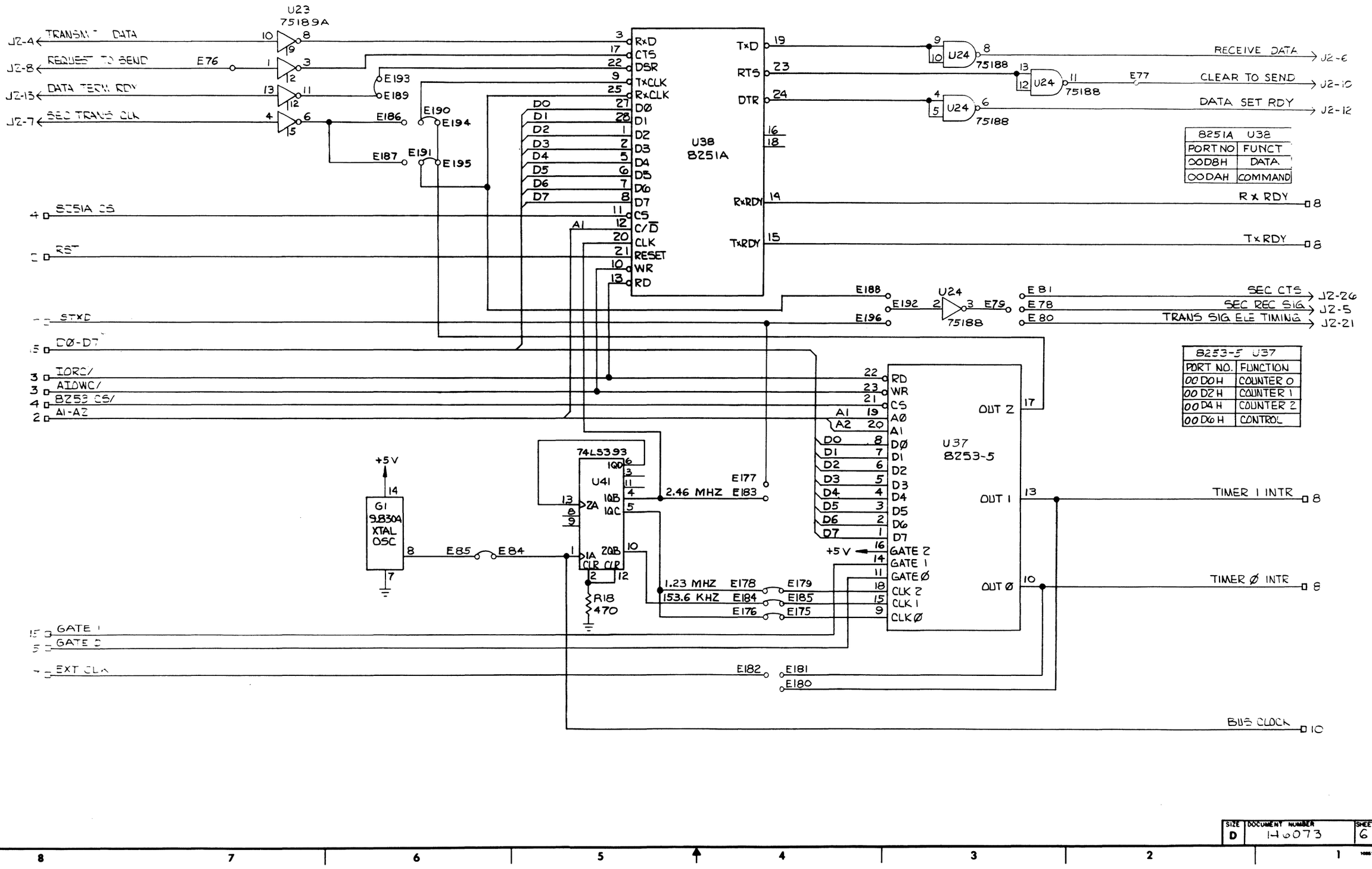
Figure 5-4. Schematic Diagram (Sheet 4 of 16)



SIZE	DOCUMENT NUMBER	SHEET	REV
D	146073	5	A

Figure 5-4. Schematic Diagram (Sheet 5 of 16)

SERIAL COMMUNICATIONS SECTION



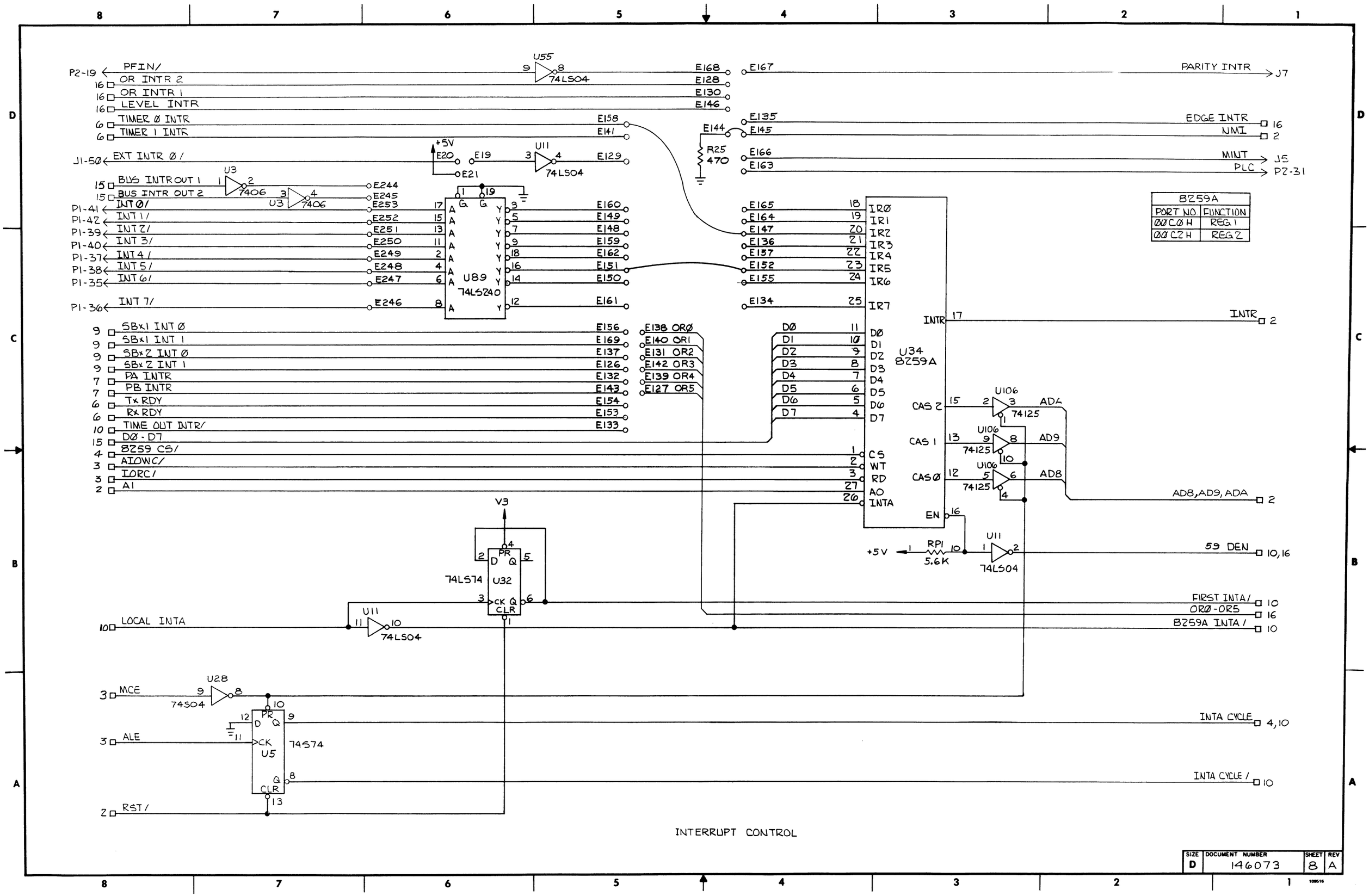
SIZE	DOCUMENT NUMBER	SHEET	REV
D	146073	6	A

Figure 5-4. Schematic Diagram (Sheet 6 of 16)

PARALLEL COMMUNICATIONS

8255A-5 U35	
PORT NO	FUNCTION
00C8H	PORT A
00CAH	PORT B
00CCH	PORT C
00CEH	CONTROL

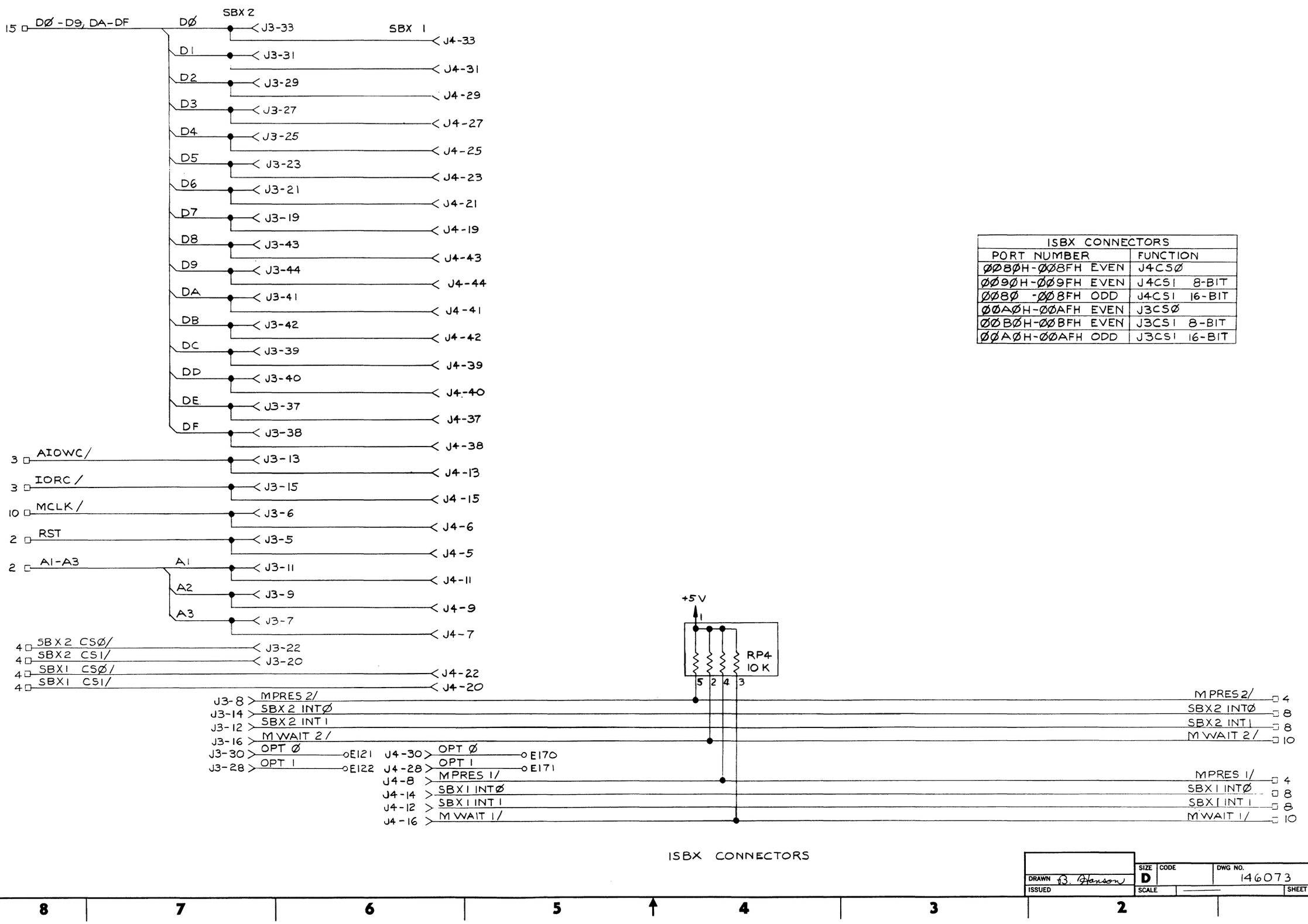
Figure 5-4. Schematic Diagram (Sheet 7 of 16)



8259A	
PORT NO	FUNCTION
ØØCØH	REG 1
ØØC2H	REG 2

SIZE	DOCUMENT NUMBER	SHEET	REV
D	146073	8	A

Figure 5-4. Schematic Diagram (Sheet 8 of 16)



ISBX CONNECTORS	
PORT NUMBER	FUNCTION
ØØ8ØH-ØØ8FH EVEN	J4CSØ
ØØ9ØH-ØØ9FH EVEN	J4CS1 8-BIT
ØØ8Ø -ØØ8FH ODD	J4CS1 16-BIT
ØØAØH-ØØAFH EVEN	J3CSØ
ØØBØH-ØØBFH EVEN	J3CS1 8-BIT
ØØAØH-ØØAFH ODD	J3CS1 16-BIT

Figure 5-4. Schematic Diagram (Sheet 9 of 16)

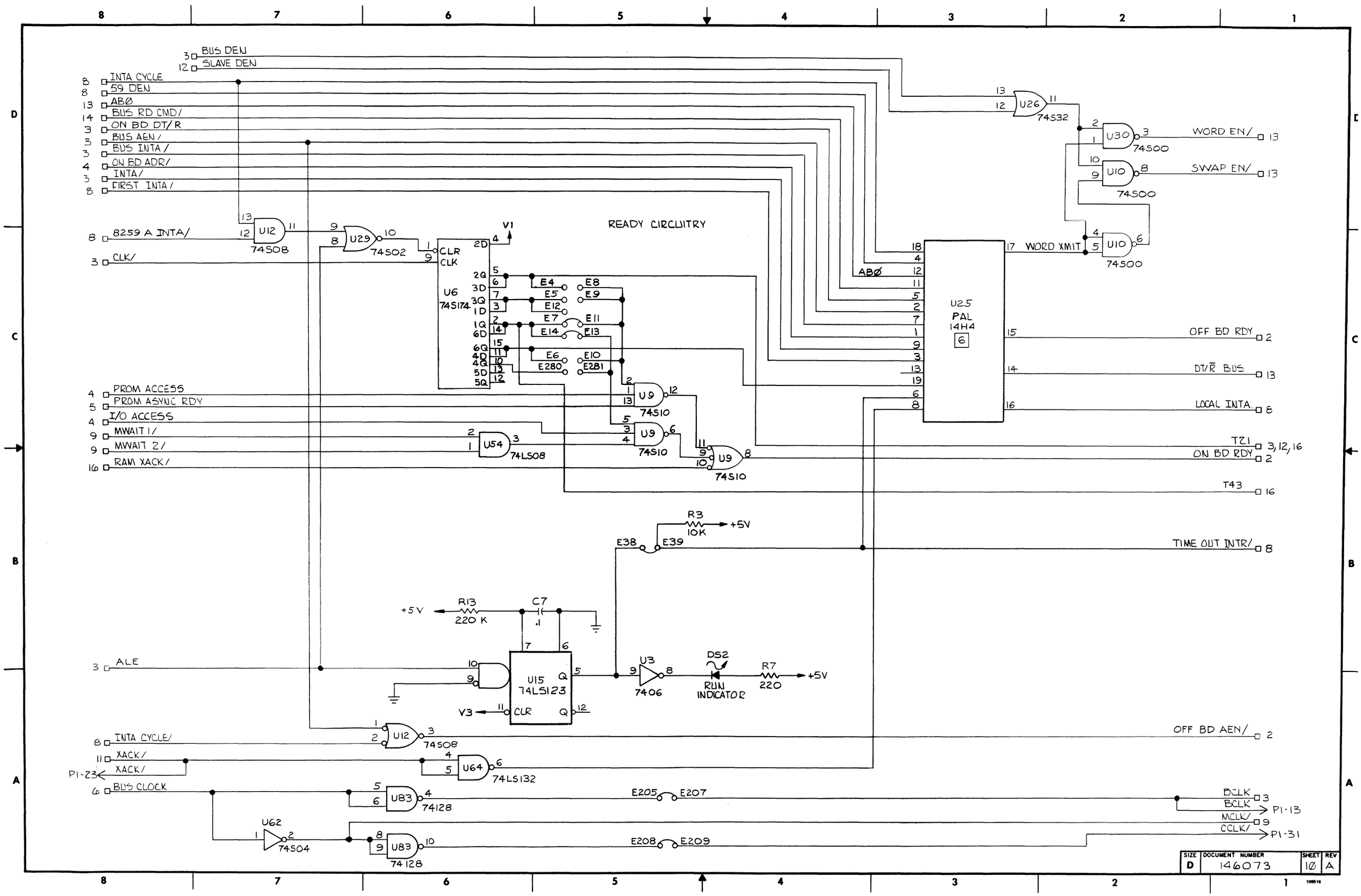


Figure 5-4. Schematic Diagram (Sheet 1Ø of 16)

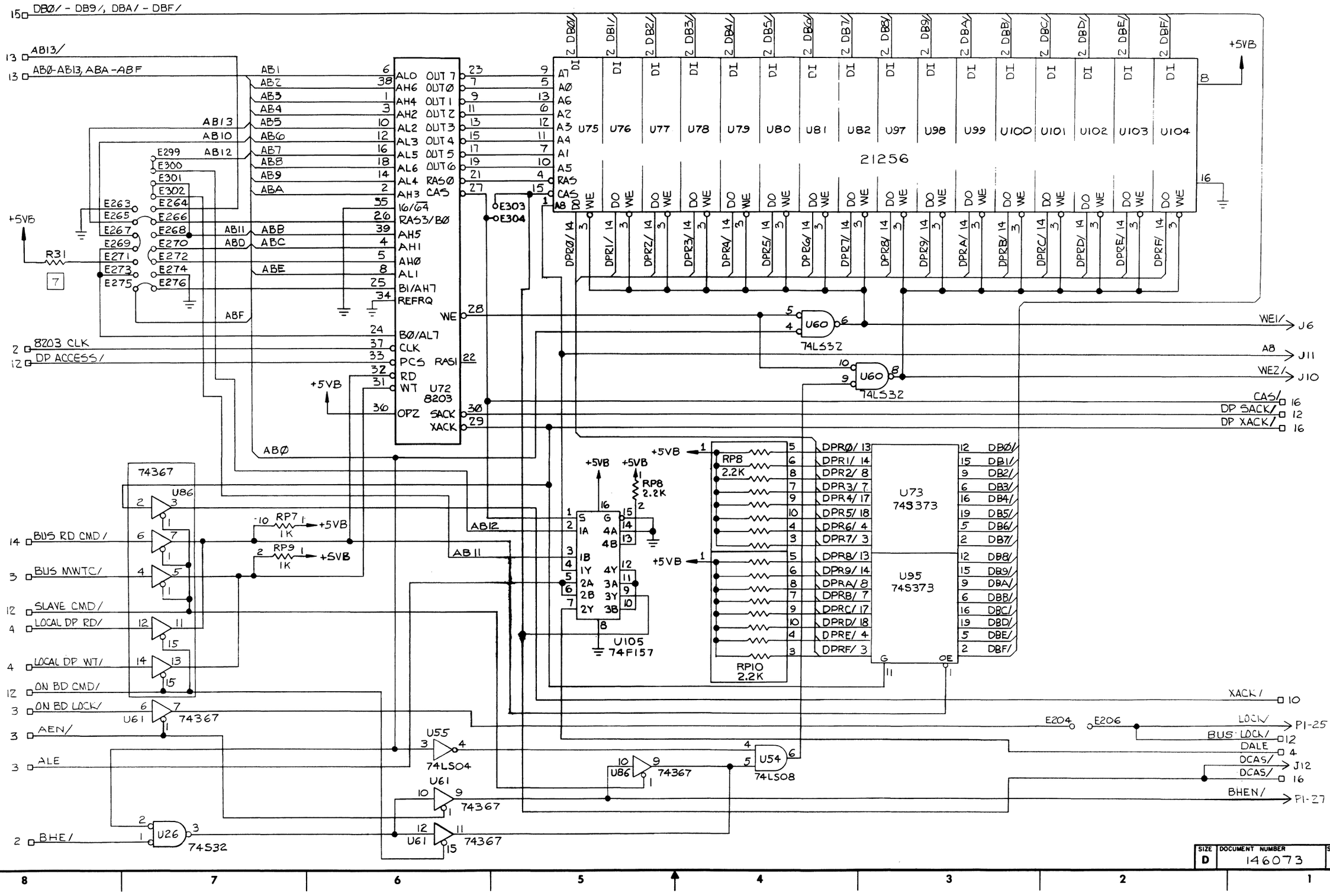


Figure 5-4. Schematic Diagram (Sheet 11 of 16)

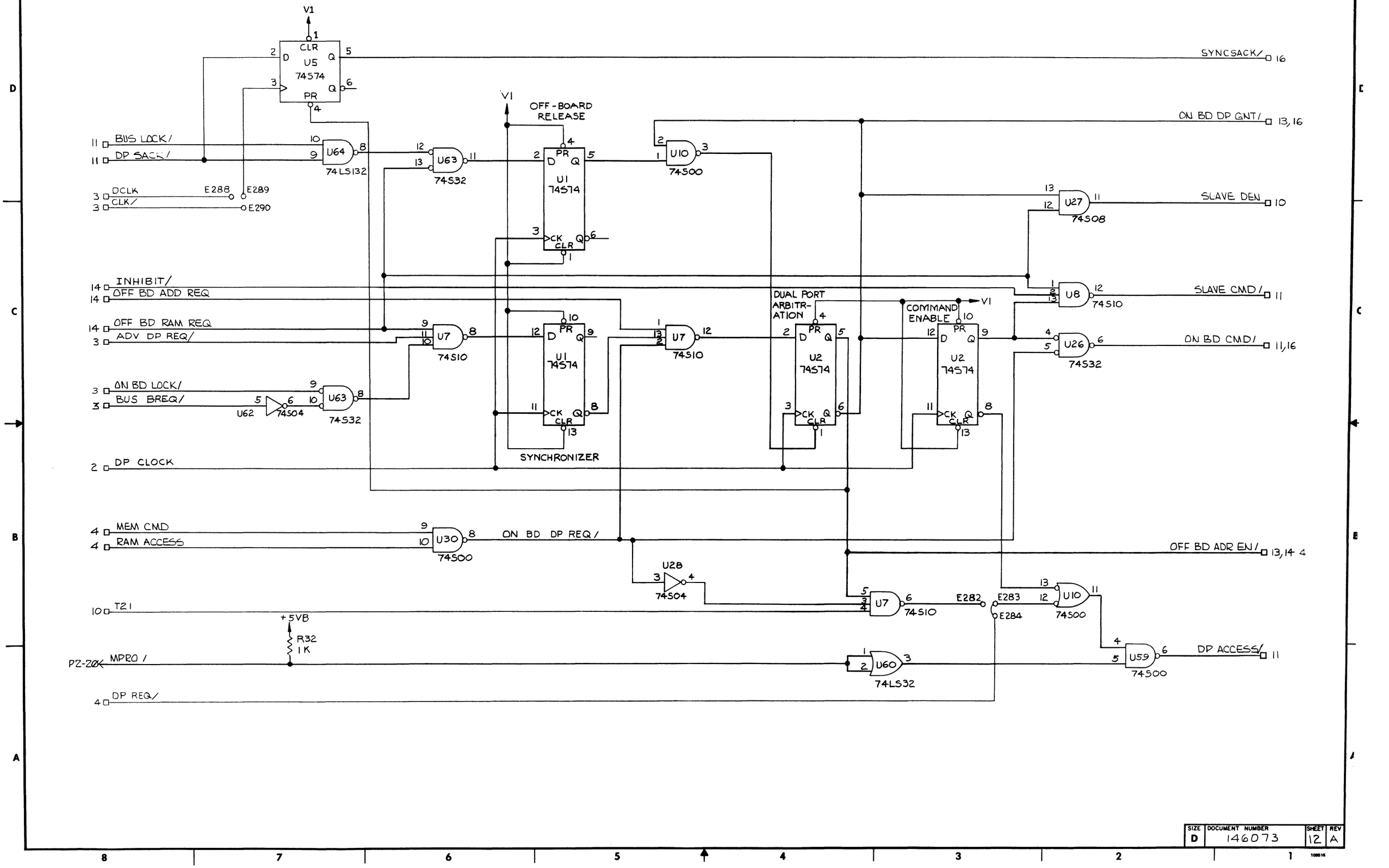


Figure 5-4. Schematic Diagram (Sheet 12 of 16)

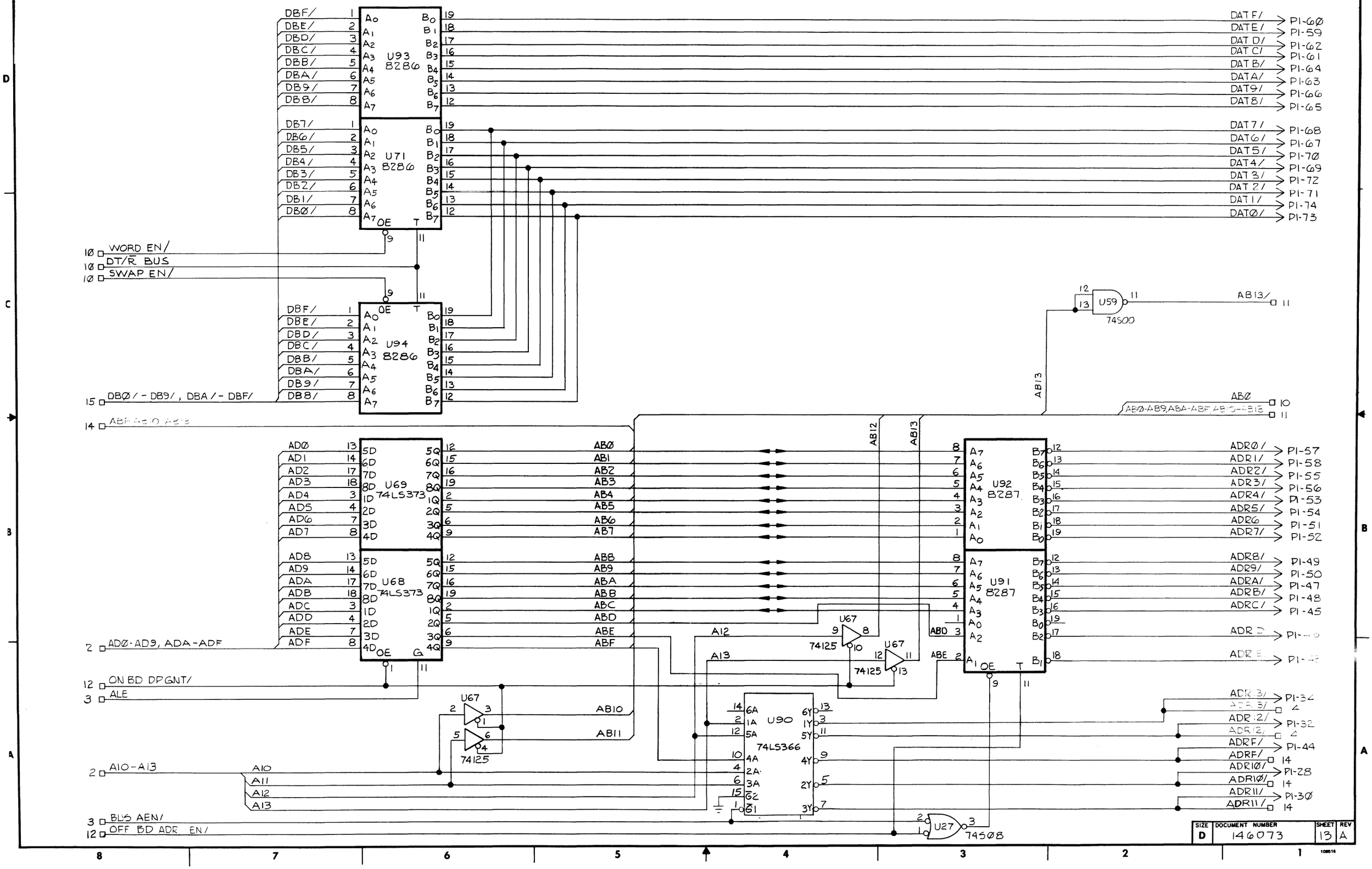


Figure 5-4. Schematic Diagram (Sheet 13 of 16)

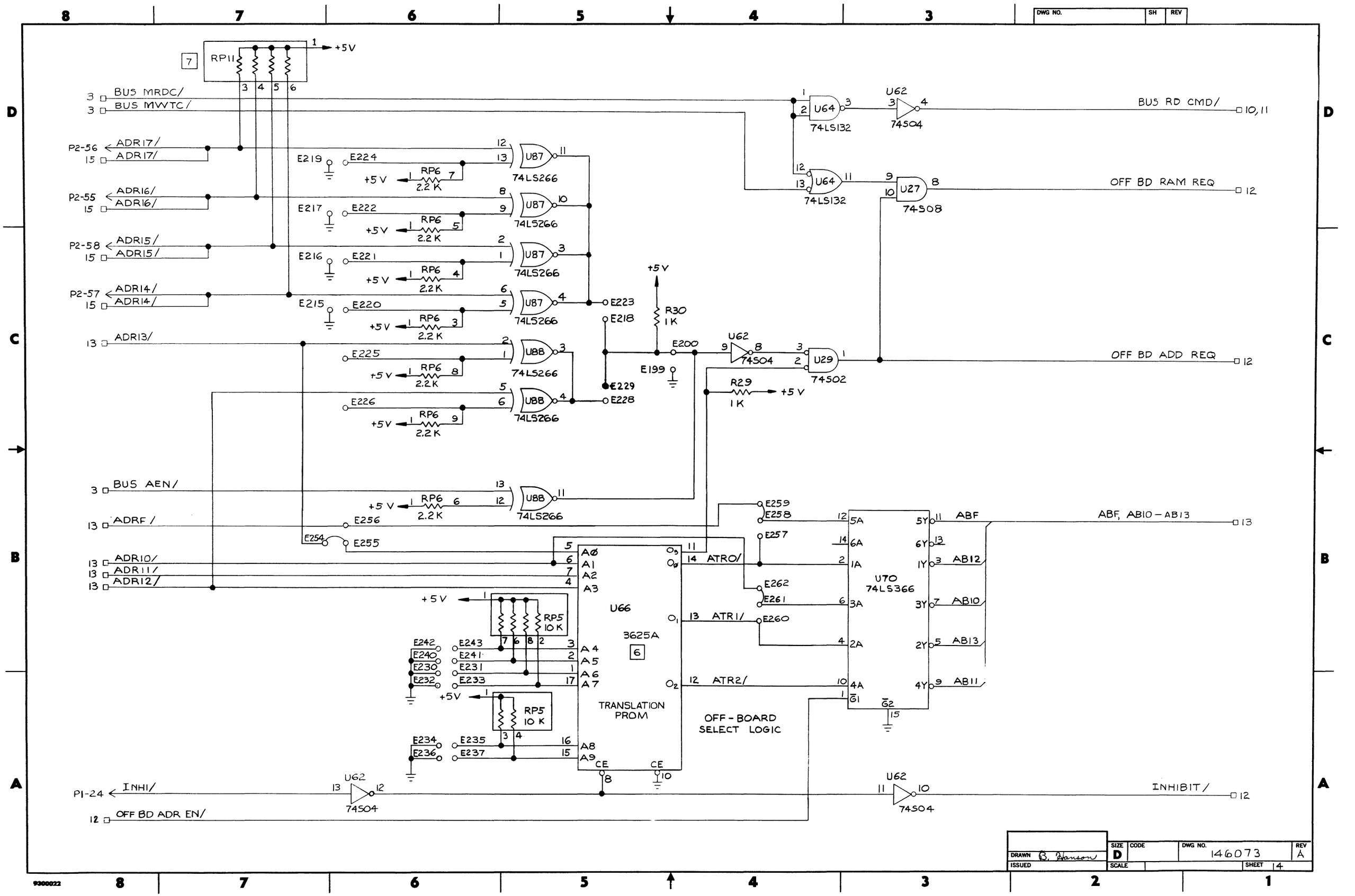


Figure 5-4. Schematic Diagram (Sheet 14 of 16)

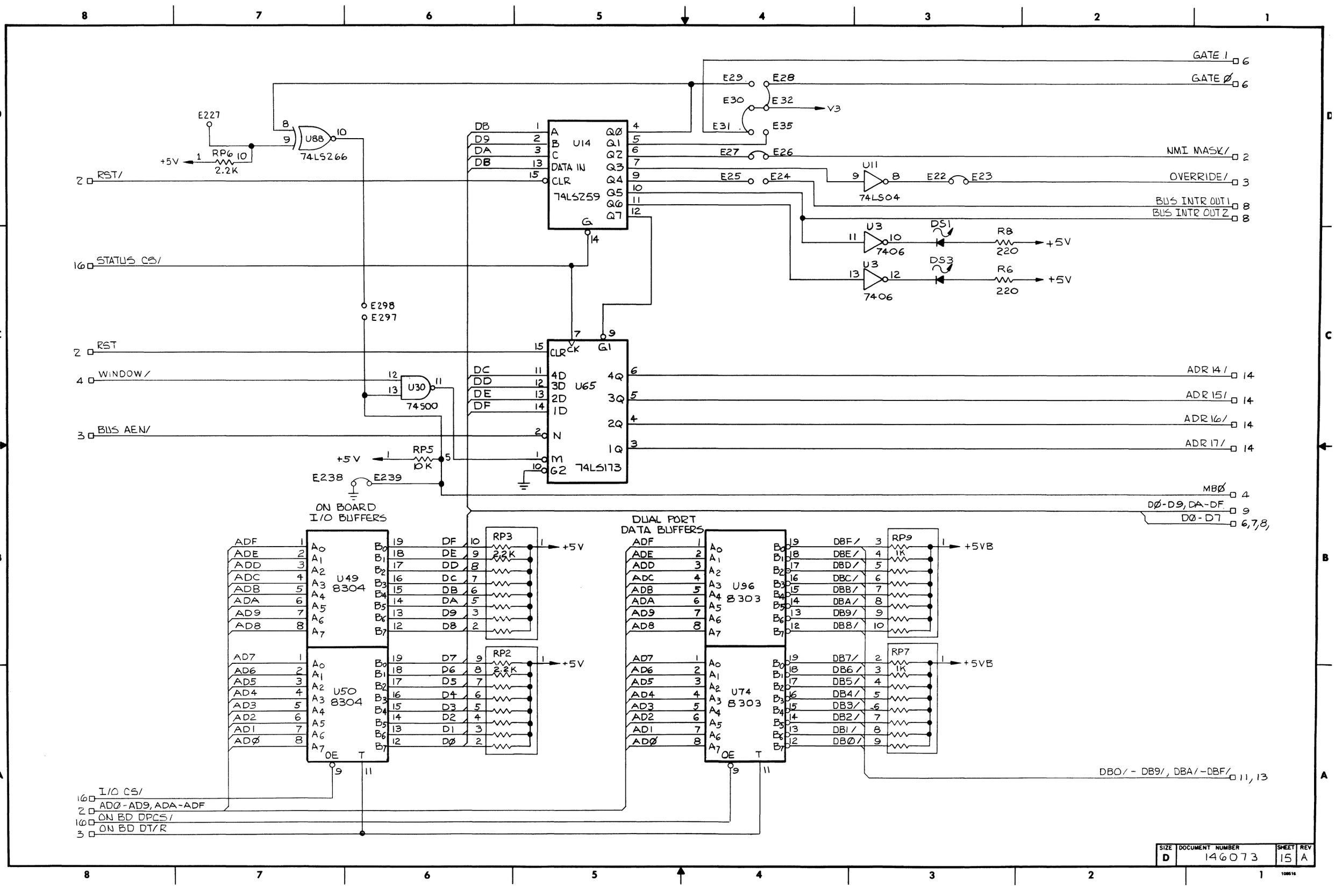


Figure 5-4. Schematic Diagram (Sheet 15 of 16)

DWG NO.	SH	REV

REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED

8 ORØ-OR5

ORØ, OR1, OR2, OR3, OR4, OR5 → U31 (74LS32) → OR INTR 2 (8), OR INTR 1 (8)

V3 → U32 74LS74 (PR, D, CK, CLR, Q) → LEVEL INTR (8)

8 EDGE INTR

2 BHE/
4 8259 CS/
4 PIO CS/
3 AIOWC/ (U28 74S04)
10 T43
→ U16 74S139 (A, B, G, Ø, 1, 2, 3)
→ U13 74S32, U8 74S10
E43, E42
+5V → R15 10K
→ STATUS CS/ (15)

4 I/O ACCESS
8 59 DEN
→ U13 74S32, U30 74S00
→ I/O CS/ (15)

3 ON BD DEN
→ U42 74S00
→ ON BD DPCS/ (15)

12 ON BD DP GNT/
4 PROM ACCESS
→ U13 74S32, U29 74S02
→ CENPR (3)

11 CAS/
11 DP XACK/
12 ON BD CMD/
→ U27 74S08, U26 74S32
→ RAM XACK/ (10)

E287 E286
11 DCAS/ E285
E293 E292
12 SYNCSACK/ E291

10 T21
3 AMWTC/
3 MRDC/
→ U42 74S00
→ U43 74S112 (PR, J, CK, K, CLR, Q)
V2
→ CMD Q2 (4)

DRAWN G. Hanson	SIZE D	CODE	DWG NO. 146073	REV A
ISSUED	SCALE		SHEET 16	

9300022

Figure 5-4. Schematic Diagram (Sheet 16 of 16)

***

APPENDIX A. JUMPER LISTS FOR THE iSBC® 86/35 BOARD

This appendix provides quickly retrievable information concerning the jumpers on the iSBC 86/35 board. Table A-1 is a numerical listing of all jumpers on the iSBC 86/35 board. Table A-2 is a listing of all default jumpers as configured by the factory.

Table A-1. Jumper Listing by Numerical Order

Jumper Number	Reference Section	Schematic Sheet No.	Description
E1		2	Not used.
E2-E3		2	Not user configurable.
E4 through E14	2.5.2	1Ø	Wait-state selection jumpers for ready circuitry.
E15-E16		2	Not user configurable.
E17-E18		2	Not user configurable.
E19	2.5.5	8	Input pin of interrupt signal inverter U11 in the interrupt jumper matrix.
E2Ø	2.5.5	8	Provides access to EXT INTRØ/ on J1-5Ø.
E21	2.5.5	8	+5 Volt signal for general use.
E22-E23	2.5.8	15	When installed, provides programmable control of the OVERRIDE/ signal via the status register to control the locking of dual port RAM and optionally the MULTIBUS.
E24-E25	2.5.8	15	Provides programmable control of the BUS INTR OUT 1 signal via the status register to the interrupt jumper matrix.
E26-E27	2.5.8	15	Provides programmable control of the NMI mask signal via the status register to control the NMI interrupt input to the 8Ø86 CPU.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E28-E32	2.5.8	15	Provides continuous enable of the GATE input to 8253 PIT timer Ø.
E28-E29	2.5.8	15	Provides programmable control of the GATE signal via the status register to 8253 PIT timer Ø.
E3Ø-E31	2.5.8	15	Provides continuous enable to the GATE input to 8253 PIT timer 1.
E31-E35	2.5.8	15	Provides programmable control of the GATE signal via the status register to 8253 PIT timer 1.
E33-E34	2.5.5.1	4	Selects operation of the interrupt circuitry in a bus vectored system when installed; remove for exclusively non-bus-vectored operation.
E36-E37	2.5.2	2	Selects either 5-MHz clock (installed) or 8 MHz clock (removed) operation for the 8Ø86 CPU.
E38-E39	2.5.7	1Ø	Enables generation of the failsafe timeout interrupt request to the 8259A PIC when installed. It is also routed to PAL U25 to truncate the current operation.
E42-E43	2.5.8	16	Enables status register and edge triggered latch. If these devices are not required, remove jumper.
E44-E53, E45-E54, E46-E55, E47-E56, E48-E57, E49-E58, E5Ø-E59, E51-E6Ø	2.5.4	7	Connect the 8255A PPI Port C I/O signals to the J1 connector.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E52-E61	2.5.4	7	Connects the direction control for the 8255A PPI port A I/O signal buffer to ground, selecting output mode when installed.
E62	2.5.4	7	TEST signal to 8Ø86 CPU.
E63	2.5.4	7	PA INTR signal from the parallel port to the interrupt jumper matrix.
E64	2.5.4	7	PB INTR signal from the parallel port to the interrupt jumper matrix.
E65, E66	2.5.4	7	Reserved signals.
E67	2.5.4	7	EXT CLK signal from the 8253 PIT device to the parallel interface.
E68	2.5.4	7	STXD signal from the clock generator circuitry to either the serial or parallel interface.
E69	2.5.4	7	PFSN/ (power fail sense) signal input from the P2 connector to the parallel interface.
E7Ø-E71	2.5.6	1	Enables +5 volts to connector J2 at pin 23 when installed.
E72-E74	2.5.6	1	Enables -12 volts to connector J2 at pin 19 when installed.
E73-E75	2.5.6	1	Enables +12 volts to connector J2 at pin 22 when installed.
E76-E77	2.5.6	6	Enables generation of CTS signal from RTS signal on the serial interface.
E78	2.5.6	6	Provides access to J2 -5.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E79	2.5.6	6	Output of signal line driver; for use when configuring an output onto the serial interface.
E8Ø	2.5.6	6	Provides access to J2 - 21.
E81	2.5.6	6	Provides access to J2 - 26.
E82-E83		5	Not used.
E84-E85		6	Not user configurable.
E86-E87		5	Not used.
E88 through E113	2.5.1.3	5	EPROM address and control.
E114-E115	2.8	1	Connects +5 volt battery back-up to +5 volt supply.
E116-E117		5	Not used.
E119-E12Ø	2.5.1.4	4	Selects the RAM Local address range.
E121	2.5.9	9	OPTØ option signal from the iSBX bus connector J3.
E122	2.5.9	9	OPT1 option signal from the iSBX bus connector J3.
E123,E124,E125	2.5.1.3	4	Select the on-board EPROM capacity.
E126	2.5.9	8	SBX2 INT 1 interrupt signal from iSBX connector J3.
E127	2.5.5	8	OR5 input signal to the interrupt OR function in the interrupt jumper matrix.
E128	2.5.5	8	OR INTR2 OR gate output signal from the interrupt ORing function. OR's together ORØ and OR1.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E129	2.5.5	8	Output pin from interrupt signal inverter U11.
E13Ø	2.5.5	8	OR INTR1 OR gate output signal from the interrupt ORing function. OR's together OR2 through OR5.
E131	2.5.5	8	OR2 input signal to the interrupt OR function.
E132	2.5.4	8	PA INTR interrupt signal from the parallel interface.
E133	2.5.7	8	TIMEOUT INTR signal from the failsafe timer.
E134	2.5.5	8	Input to IR7 interrupt level of PIC.
E135	2.5.5	8	Input to edge-interrupt latch U32.
E136	2.5.5	8	Input to IR3 interrupt level of PIC.
E137	2.5.9	8	SBX2 INTØ interrupt signal from iSBX connector J3.
E138	2.5.5	8	ORØ input signal to the interrupt OR function.
E139	2.5.5	8	OR4 input signal to the interrupt OR function.
E14Ø	2.5.5	8	OR1 input signal to the interrupt OR function.
E141	2.5.3	8	TIMER 1 INTR interrupt signal from PIT counter 1.
E142	2.5.5	8	OR3 input signal to the interrupt OR function.
E143	2.5.4	8	PB INTR interrupt signal to the interrupt jumper matrix from the parallel port.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E144-E145	2.5.5	8	Disables NMI interrupt input to 8Ø86 CPU when installed.
E146	2.5.5	8	LEVEL INTR interrupt signal from the edge-to-level interrupt conversion latch U32.
E147	2.5.5	8	Input to IR2 interrupt level of PIC.
E147-E158	2.5.3	8	Connects PIT timer Ø output to IR2 interrupt level of the PIC.
E148	2.5.5	8	MULTIBUS interrupt input INT2.
E149	2.5.5	8	MULTIBUS interrupt input INT1.
E15Ø	2.5.5	8	MULTIBUS interrupt input INT6.
E151	2.5.5	8	MULTIBUS interrupt input INT5.
E151-E152	2.5.5	8	Connects INT5 interrupt signal from the MULTIBUS to IR5 interrupt level of PIC.
E153	2.5.6	8	RxRDY interrupt signal from the 8251A PCI device.
E154	2.5.6	8	TxRDY interrupt signal from the 8251A PCI device.
E155	2.5.5	8	Input to IR6 interrupt level of PIC.
E156	2.5.9	8	SBX1 INTØ interrupt signal from iSBX connector J4.
E157	2.5.5	8	Input to IR4 interrupt level of PIC.
E158	2.5.3	8	TIMER Ø INTR interrupt signal from PIT counter Ø.
E159	2.5.5	8	MULTIBUS interrupt input INT 3.
E16Ø	2.5.5	8	MULTIBUS interrupt input INT Ø.
E161	2.5.5	8	MULTIBUS interrupt input INT 7.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E162	2.5.5	8	MULTIBUS interrupt input INT 4.
E163	2.5.5	8	POWER LINE CLOCK signal from P2 connector pin 31.
E164	2.5.5	8	Input to IR1 interrupt level of PIC.
E165	2.5.5	8	Input to IRØ interrupt level of PIC.
E166	2.7.3	8	MINT interrupt signal input from the iSBC 337 Numeric Data Processor.
E167	2.5.5	8	Reserved interrupt signal.
E168	2.8	8	Power Fail Interrupt (PFI) input signal from the external power fail sense circuitry.
E169	2.5.9	8	SBX1 INT1 interrupt signal from iSBX connector J4.
E17Ø	2.5.9	9	OPTØ option signal from the iSBX bus connector J4.
E171	2.5.9	9	OPT1 option signal from the iSBX bus connector J4.
E172,E173,E174	2.5.9	4	Select either 8-bit or 16-bit operation of the iSBX bus interfaces at MULTIMODULE connectors J3 and J4.
E175-E176	2.5.3	6	Selects 1.23-MHz clock input frequency for counter Ø of the 8253 PIT device.
E177	2.5.6	6	Provides connection to either the input of driver U24 or to the parallel interface.
E178-E179	2.5.3	6	Selects 1.23-MHz clock input frequency for counter 2 of the 8253 PIT device.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E18Ø	2.5.3	6	Output from counter 1 of the 8253 PIT.
E181	2.5.3	6	Output from counter Ø of the 8253 PIT device.
E182	2.5.3	6	EXT CLK signal to the parallel interface.
E183	2.5.6	6	2.46-MHz clock signal.
E184-E185	2.5.3	6	Selects 156.3-KHz clock input frequency for counter 1 of the 8253 PIT device.
E186,E187	2.5.6	6	Secondary Transmit Clock input signal to the serial I/O logic from the serial interface connector J2.
E188	2.5.6	6	Provides access to the Receive Clock (RxC) signal at the 8251A PCI device.
E189-E193	2.5.6	6	Connects the Data Terminal Ready signal from the serial interface to the Data Set Ready input on the 8251A PCI.
E19Ø-E194	2.5.6	6	Selects the output from counter 2 of the PIT as the Transmit Clock (TxC) input to the 8251A PCI.
E191-E195	2.5.6	6	Selects the output from counter 2 of the PIT as the Receive Clock (RxC) input to the 8251A PCI.
E192	2.5.6	6	Input to the signal amplifier U24 for the serial interface.
E196	2.5.6	6	Provides general purpose access to the serial I/O port either from a clock signal or from the parallel interface.
E197-E198		5	Not used.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E199-E2ØØ	2.5.1.5	14	Inhibits access to all RAM from the MULTIBUS; no on-board RAM is allowed to be dual port memory when installed.
E2Ø1,E2Ø2,E2Ø3	2.5.1Ø	3	Configure ANY REQUEST signal for MULTIBUS arbitration scheme.
E2Ø4-E2Ø6	2.5.1Ø	11	Provides the ability to drive the on board LOCK/ signal onto the MULTIBUS interface if required.
E2Ø5-E2Ø7	2.5.1Ø	1Ø	Provides BCLK/ system clock to the MULTIBUS interface when installed.
E2Ø8-E2Ø9	2.5.1Ø	1Ø	Provides CCLK/ system clock to the MULTIBUS interface when installed.
E21Ø-E211	2.5.1Ø	3	Connect BPRO/ signal generated on-board to the MULTIBUS interface when installed.
E212,E213,E214	2.5.1Ø	3	Configure CBRQ/ signal for MULTIBUS arbitration scheme.
E215-E22Ø, E216-E221, E217-E222, E219-E224	2.5.1.5	14	Select the Megabyte page of the RAM MULTIBUS address.
E218-E223	2.5.1.5	14	Enables Megabyte page decoders.
E225		14	Not used.
E226		14	Not used.
E219-E227	2.5.1.6	15	Determines whether a 1 or a Ø in status register bit Ø enables the Megabyte page drivers and disables the on-board RAM above 1FFFFH.
E228-E229		14	Not used.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E23Ø-E231, E232-E233, E234-E235, E236-E237	2.5.1.5	14	Select the RAM MULTIBUS Address range.
E238-E239	2.5.1.6	15	Disables the upper 4-bits of a 24-bit address to the MULTIBUS when installed.
E24Ø-E241, E242-E243	2.5.1.5	14	Select the RAM MULTIBUS address range.
E244	2.5.8	8	Provides the BUS INTR OUT 1 signal output from the status register to the MULTIBUS interrupt jumper matrix.
E245	2.5.8	8	Provides the BUS INTR OUT 2 signal output from the status register to the MULTIBUS interrupt jumper matrix.
E246	2.5.5	8	MULTIBUS interrupt output INT 7/.
E247	2.5.5	8	MULTIBUS interrupt output INT 6/.
E248	2.5.5	8	MULTIBUS interrupt output INT 5/.
E249	2.5.5	8	MULTIBUS interrupt output INT 4/.
E25Ø	2.5.5	8	MULTIBUS interrupt output INT 3/.
E251	2.5.5	8	MULTIBUS interrupt output INT 2/.
E252	2.5.5	8	MULTIBUS interrupt output INT 1/.
E253	2.5.5	8	MULTIBUS interrupt output INT Ø/.
E254 through E262		14	Not user configurable.
E263 through E276		11	Not user configurable.
E277-E278	2.8	1	Connects the +5V bus to the +5V battery backup bus when installed.

Table A-1. Jumper Listing by Numerical Order (continued)

Jumper Number	Reference Section	Schematic Sheet No.	Description
E279	2.5.7	3	Provides more conditions on generation of the TIME OUT INTR/ signal for use with iRMX 86 software. The OR-ing of E279 and E133 via the OR function provided in the interrupt jumper matrix disables a failsafe timeout restart when executing a HALT instruction under iRMX 86 software.
E28Ø,E281		1Ø	Not used.
E282		12	Not Used.
E283-E284		12	Not user configurable.
E285		16	Not used.
E286-E287		16	Reserved.
E288 through E29Ø		12	Not used.
E291		16	Not Used.
E292-E293		16	Not user configurable.
E294-E295		4	Not user configurable.
E296		4	Not used.
E297-E298	2.5.1.6	15	Routes bit Ø from the status register to programmatically enable or disable the drivers for the upper 4 bits of the 24-bit address. This jumper is mutually exclusive with jumper E238 to E239.
E299 through E3Ø2		11	Not user configurable.
E3Ø3, E3Ø4		11	Not used.

Table A-2. Default Jumper List

Jumper Number		Jumper Number	
From	To	From	To
E2	E3	E112	E113
E7	E11	E114	E115
E13	E14	E144	E145
E15	E16	E147	E158
E17	E18	E151	E152
E22	E23	E175	E176
E26	E27	E178	E179
E28	E32	E184	E185
E3Ø	E31	E189	E193
E33	E34	E19Ø	E194
E38	E39	E191	E195
E42	E43	E2Ø2	E2Ø3
E44	E53	E2Ø5	E2Ø7
E45	E54	E2Ø8	E2Ø9
E46	E55	E21Ø	E211
E47	E56	E213	E214
E48	E57	E238	E239
E49	E58	E254	E255
E5Ø	E59	E258	E259
E51	E6Ø	E261	E262
E52	E61	E265	E266
E84	E85	E267	E269
E88	E89	E27Ø	E272
E9Ø	E91	E275	E276
E92	E93	E277	E278
E94	E95	E283	E284
E96	E97	E286	E287
E96	E1Ø2	E292	E293
E98	E99	E294	E295
E98	E1Ø4		

***

APPENDIX B. iSBC® 3Ø4 RAM EXPANSION MULTIMODULE™ BOARD INSTALLATION

B.1 INTRODUCTION

This appendix provides information for installing the iSBC 3Ø4 RAM Expansion MULTIMODULE board onto the iSBC 86/35 board.

B.2 iSBC® 3Ø4 RAM EXPANSION MULTIMODULE BOARD INSTALLATION

The iSBC 86/35 board is shipped with 512 K-bytes of RAM (in locations U75 through U82 and U97 through U1Ø4). The iSBC 86/35 board contains sixteen devices (256 k by 1-bit capacity each). To expand total on-board memory to 64Ø K-bytes, install the iSBC 3Ø4 RAM Expansion MULTIMODULE board onto the iSBC 86/35 board in accordance with the following procedure:

CAUTION

Always turn off power before removing or installing any board.

1. Turn power off and remove the iSBC 86/35 board from its system.
2. Place the iSBC 86/35 board on a soft surface (preferably a piece of foam), component side up.
3. Discard the PROM device supplied with the iSBC 3Ø4 RAM Expansion Module. Carefully remove the 82Ø3 RAM Controller from socket U72 and remove the two latch devices from sockets U73 and U95.

NOTE

Save these devices, they are reinstalled at a later step.

4. Install the mating pins of the iSBC 3Ø4 MULTIMODULE onto the socket U72 of the iSBC 86/35 board, orienting the module as shown in Figure B-1. The iSBC 3Ø4 module connector pins fit directly into board sockets U72, U73, and U95. It also fits into board connectors J6, J1Ø.
5. Ensure that all the mating pins are aligned and carefully press the MULTIMODULE into place by applying pressure at U1.
6. Place nylon spacer between the base board and the iSBC 3Ø4 MULTIMODULE at one of the holes.

7. Insert screw from the solder side through the baseboard, the spacer, and the iSBC 3Ø4 MULTIMODULE.

8. Attach a nut and tighten finger tight.

9. Repeat steps 6 through 8 for the other holes.

1Ø. Install the 82Ø3 RAM Controller device into iSBC 3Ø4 socket U1 and the two latch devices into sockets U3 and U12. Make certain that pin 1 of each device aligns with pin 1 of each socket.

11. You will need to configure both the local and the MULTIBUS® RAM addresses. See sections 2.5.1.4, 2.5.1.5 and 2.5.1.6.

12. Installation is complete. The iSBC 86/35 board is now ready to be installed into your system cardcage. Refer to section 2.7.5.

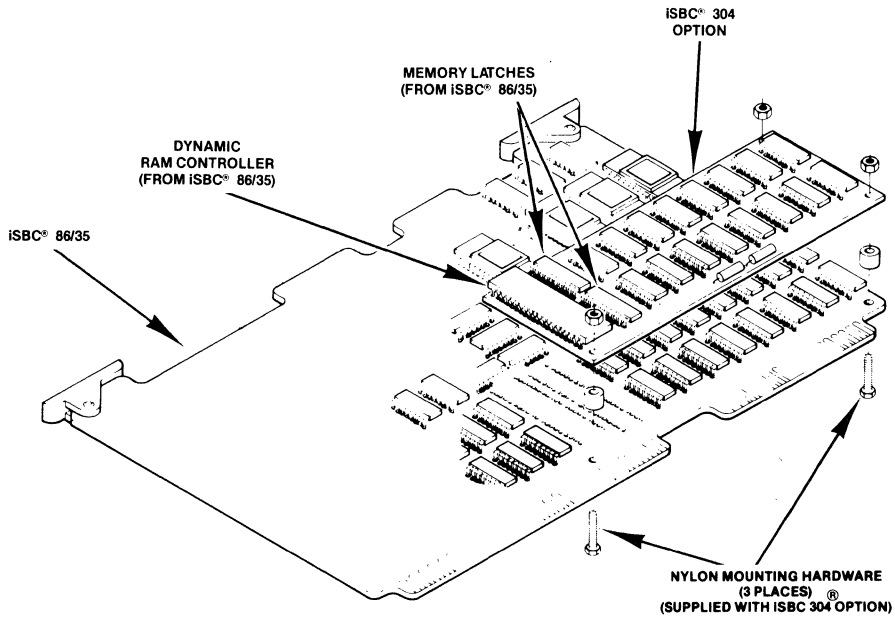


Figure B-1. iSBC® 3Ø4 RAM Expansion MULTIMODULE™ Board Installation

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-2747	D.M.	7/28/81	J.J.S.	8/17/81	J.A.C.	9/17/81
B	ECO 40-3015	N.G.	12/28/81	K. Langrick	12/28/81	K. Langrick	4/5/82

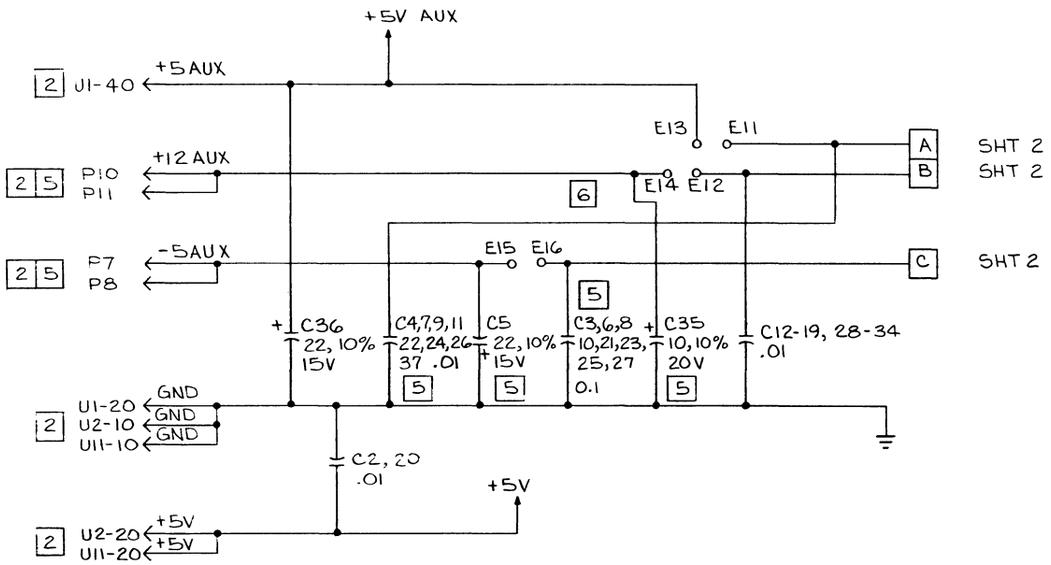


TABLE 1

PRODUCT		300		300A		304	
BOARD CAPACITY		32K		32K		128K	
MEMORY DEVICE		2117-4		2118-4		2164-20	
PIN NUMBER U3-10, U11-19	1	-5V AUX		N.C.		N.C.	
	8	+12V AUX		+5V AUX		+5V AUX	
	9	+5V AUX		N.C.		A7	
	16	GND		GND		GND	
JUMPERS		FROM	TO	FROM	TO	FROM	TO
		E15	E16	E12	E13	E12	E13
		E12	E14			E5	E10
		E11	E13				
MEMORY CONTROLLER		8202A		8202A		8203	
MEMORY CONTROLLER PIN	23	$\overline{RAS2}$		$\overline{RAS2}$		$\overline{OUT7}$	
	24	BØ		BØ		AL7	
	25	BI/OPI		BI/OPI		AH7	
	26	RAS3		RAS3		BØ	
	35	TNK		TNK		16K/$\overline{64K}$	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITOR VALUES ARE IN MICROFARADS, +80%, -20%, 50V.
2. THESE PIN CONNECTIONS MATE WITH SOCKETS ON iSBC HOST BOARD.
3. U1, U2 AND U11 ARE NOT SUPPLIED.
4. FOR $\overline{RAS}$-TO-RAM JUMPERS SEE TABLE 2.
5. THESE COMPONENTS NOT INSTALLED ON 300A, OR 304.
6. FOR VOLTAGE JUMPERS SEE TABLE 1.
7. FOR PIN OUTS SEE TABLE 1.

TABLE 2

$\overline{RAS}$ TO RAM	JUMPER TABLE			
	MEMORY DEVICE U3-U10		MEMORY DEVICE U12-U19	
	FROM	TO	FROM	TO
$\overline{RAS1}$	E2	E3	E6	E7
$\overline{RAS2}$	E1	E2	E5	E6
$\overline{RAS3}$	E2	E4	E6	E8

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C37	P1-4, 9
U19	
E16	
P11	

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ±, XX ±, XXX ±

ITEM NO.	DESCRIPTION
	PARTS LIST

SIGNATURE		DATE
DRN BY	D. Moore	11/24/81
CHK BY	H. Baker	9/17/81
ENGR / APVD	Alan Kirkwood	9/17/81
APVD		
APVD		

intel® 3065 BOWERS AVE SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC iSBC 300/300A/304 RAM MODULE

SIZE	DCLC	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	01		143844	5

SCALE NONE SHEET 1 OF 2

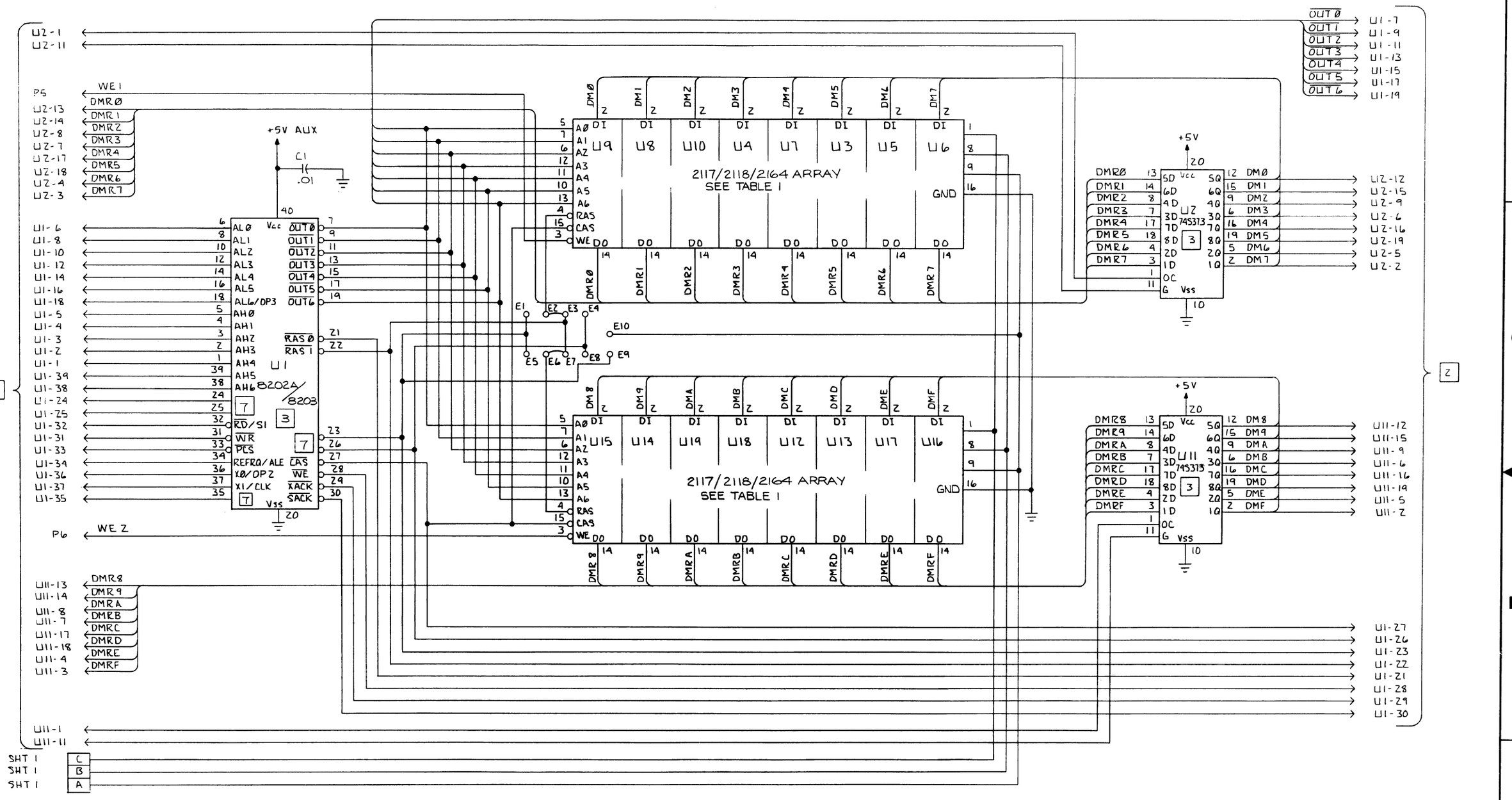
109515

Figure B-2. Schematic Diagram (Sheet 1 of 2)

DWG NO. 143844	SH 2	REV B

REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
	B	SEE SHEET 1				



DRAWN D. MOORE	SIZE D	CODE 40 01	DWG NO. 143844	REV B
ISSUED	SCALE NONE			SHEET 2

9300022

Figure B-2. Schematic Diagram (Sheet 2 of 2)

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APPENDIX C. iSBC® 314 RAM EXPANSION MULTIMODULE™ BOARD INSTALLATION

C.1 INTRODUCTION

This appendix provides information for installing the iSBC 314 RAM Expansion MULTIMODULE board onto the iSBC 86/35 board.

C.2 iSBC® 314 RAM EXPANSION MULTIMODULE™ BOARD INSTALLATION

The iSBC 86/35 board is shipped with 512 K-bytes of RAM (in locations U75 through U82 and U97 through U1Ø4). The iSBC 86/35 board contains sixteen devices (256k by 1-bit capacity each). To expand total on-board memory to 1 Megabyte, install the iSBC 314 RAM Expansion MULTIMODULE board onto the iSBC 86/35 board in accordance with the following procedure:

CAUTION

Always turn off power before removing or installing any board.

1. Turn power off and remove the iSBC 86/35 board from its system.
2. Place the iSBC 86/35 board on a soft surface (preferably a piece of foam), component side up.
3. Carefully remove the 82Ø3 RAM Controller from socket U72 and remove the two latch devices from sockets U73 and U95.

NOTE

Save these devices, they are reinstalled at a later step.

4. Install the mating pins of the iSBC 314 MULTIMODULE onto the socket U72 of the iSBC 86/35 board, orienting the module as shown in Figure C-1. The iSBC 314 module connector pins fit directly into board sockets U72, U73, and U95. It also fits into board connectors J6, J1Ø, J11, J12.

5. Ensure that all the mating pins are aligned and carefully press the MULTIMODULE into place by applying pressure at U1.

6. Place nylon spacer between the base board and the iSBC 314 MULTIMODULE at one of the holes.

7. Insert screw from the solder side through the baseboard, the spacer, and the iSBC 314 MULTIMODULE.

8. Attach a nut and tighten finger tight.

9. Repeat steps 6 through 8 for the other holes.

1Ø. Install the 82Ø3 RAM Controller device into iSBC 314 socket U1 and the two latch devices into sockets U3 and U12. Make certain that pin 1 of each device aligns with pin 1 of each socket.

11. Remove U46 from the iSBC 86/35 board and replace with the PAL device supplied with the iSBC 314 board.

12. You will need to configure both the local and the MULTIBUS RAM addresses. See section 2.5.1.4, 2.2.1.5, and 2.2.1.6.

13. Installation is complete. The iSBC 86/35 board is now ready to be installed into your system cardcage. Refer to section 2.7.5.

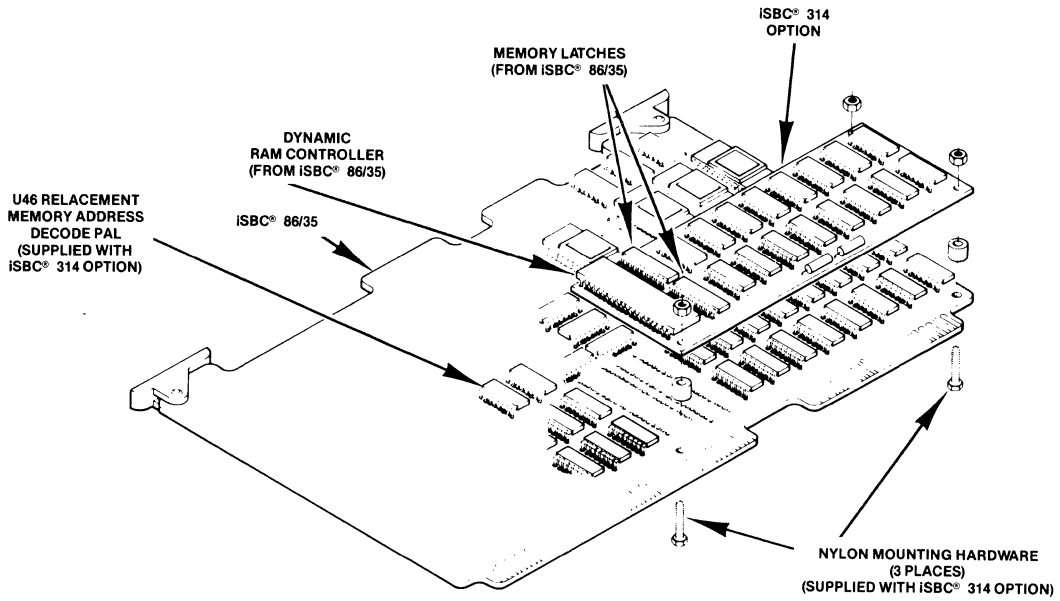

Figure C-1. iSBC® 314 RAM Expansion MULTIMODULE™ Board Installation

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-4291	R.Thong	3/27/84	KA	3/27/84	(illegible)	3/27/84

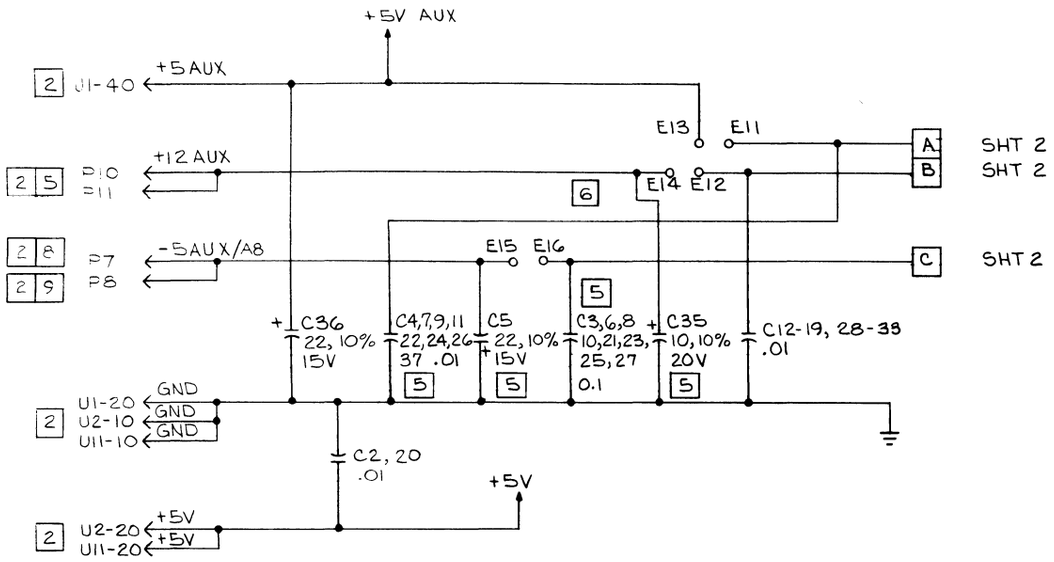

TABLE 1

PRODUCT		300		300A		304		314	
BOARD CAPACITY		32K		32K		128K		512 K	
MEMORY DEVICE		2117-4		2118-4		2164-20		21256-20	
PIN NUMBER U3-U10 U11-U19	1	-5V AUX		N.C.		N.C.		A8	
	8	+12V AUX		+5V AUX		+5V AUX		+5V AUX	
	9	+5V AUX		N.C.		A7		A7	
	16	GND		GND		GND		GND	
JUMPERS		FROM	TO	FROM	TO	FROM	TO	FROM	TO
		E15 E12 E11 E17	E16 E14 E13 E18	E12 E17	E13 E18	E12 E9 E17	E13 E10 E18	E12 E9 E15 E19	E13 E10 E16 E20
MEMORY CONTROLLER		8202A		8202A		8203		8203	
MEMORY CONTROLLER PIN	23	$\overline{RAS2}$		$\overline{RAS2}$		$\overline{OUT7}$		$\overline{OUT7}$	
	24	BØ		BØ		AL7		AL7	
	25	BI/OPI		BI/OPI		AH7		AH7	
	26	$\overline{RAS3}$		$\overline{RAS3}$		BØ		BØ	
	35	TNK		TNK		16K/$\overline{64K}$		16K/$\overline{64K}$	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITOR VALUES ARE IN MICROFARADS, +80%, -20%, 50V.
2. THESE PIN CONNECTIONS MATE WITH SOCKETS ON LSBC HOST BOARD.
3. U1, U2 AND U11 ARE NOT SUPPLIED.
4. FOR $\overline{RAS}$-TO-RAM JUMPERS SEE TABLE 2.
5. THESE COMPONENTS NOT INSTALLED ON 300A, 304 OR 314.
6. FOR JUMPERS SEE TABLE 1.
7. FOR PIN OUTS SEE TABLE 1.
8. P7 IS NOT INSTALLED ON THE 300A OR 304.
9. P8 AND P12 ARE NOT INSTALLED ON 300, 300A OR 304.

TABLE 2

$\overline{RAS}$ JUMPER TABLE				
$\overline{RAS}$ TO RAM	MEMORY DEVICE U3-U10		MEMORY DEVICE U12-U19	
	FROM	TO	FROM	TO
$\overline{RAS1}$	E2	E3	E6	E7
$\overline{RAS2}$	E1	E2	E5	E6
$\overline{RAS3}$	E2	E4	E6	E8

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C37	P1-4, 9
U19	C34
E20	
P12	

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ±, XX ±, XXX ±

SIGNATURE	DATE
DRN BY R. Thong	11/29/83
CHK BY Engvick	11/1/83
ENGR APVD (illegible)	11/1/83
APVD	
APVD	

ITEM NO. | DESCRIPTION

PARTS LIST

intel® 3065 BOWERS AVE SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC, RAM MODULE LSBC 300/300A/304/314

SIZE	DCLC	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	0100		146170	A

SCALE NONE | SHEET 1 OF 2

109513

Figure C-2. Schematic Diagram (Sheet 1 of 2)

DWG NO.	SH	REV

REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
		SEE SHEET 1			11/4/87	

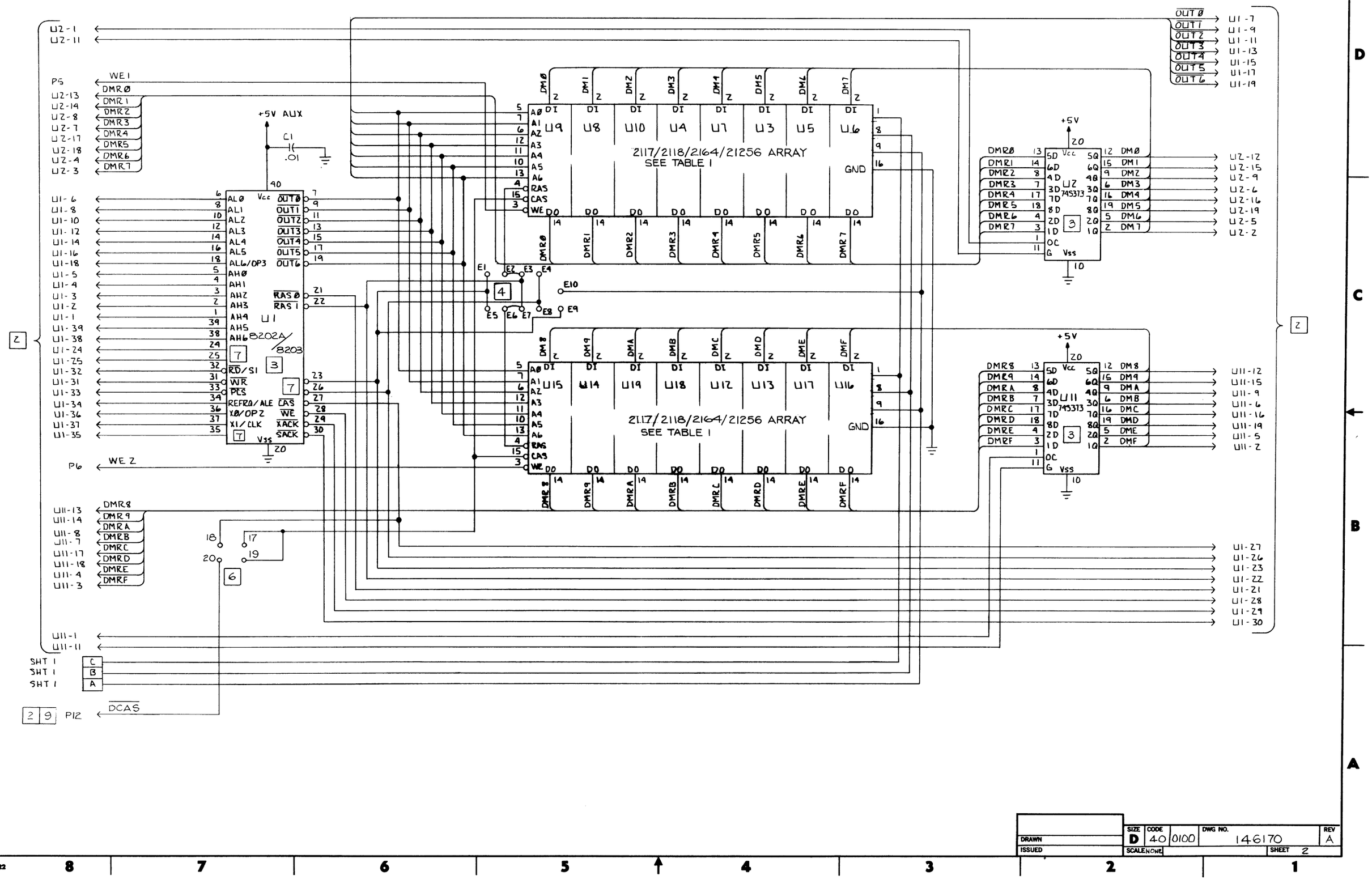

Figure C-2. Schematic Diagram (Sheet 2 of 2)

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APPENDIX D. DIFFERENCES BETWEEN THE iSBC® 86/35 AND THE iSBC® 86/3Ø

The differences between the iSBC 86/35 board and the iSBC 86/3Ø board are as follows:

RAM

The iSBC 86/35 board has 512 K-bytes of on-board RAM expandable to 1Mbyte, compared to the iSBC 86/3Ø board which has 128 K-bytes expandable to 256 K-bytes. Because of this, different jumpering options are available for determining RAM local address range and RAM MULTIBUS address range. Refer to paragraphs 2.5.1.4 and 2.5.1.5 for more information on RAM options.

EPROM

The iSBC 86/35 board supports 2764, 27128, 27256, and 27512 EPROM devices, while the iSBC 86/3Ø board supports 2716, 2732, 2764 and 27128 EPROM's. Because of this EPROM jumpering requirements are different than those on the iSBC 86/3Ø board. Also, VPP from connector P2 pin 6 is no longer connected to the EPROM jumper matrix. Neither the iSBC 86/35 nor the iSBC 86/3Ø board supports programming of EEPROM's. Refer to paragraph 2.5.1.3 for more information on EPROM options.

MULTIBUS® Addressing (24 Address Line Systems)

Bit Ø of the status register on the iSBC 86/35 board may now be used to control enabling of the Megabyte page register, and to temporarily disable local access to on-board RAM above 1FFFFH, in order to allow greater access to other MULTIBUS resources. Also, a PAL reprogramming option can be used to reduce the number of status register I/O writes in a system with both a 2Ø address line board and 24 address line boards. Refer to paragraph 2.5.1.6 for more information on MULTIBUS Addressing options.

***

APPENDIX E. CONNECTOR INFORMATION

E.1 CONNECTOR P1 INFORMATION

MULTIBUS connector P1 interfaces the iSBC 86/35 board signals and power lines to other boards in your system and to the power supply. These signals conform to the Intel MULTIBUS SPECIFICATION. Connector P1 pin assignments are listed in Table E-1.

Table E-1. Connector P1 Pin Assignments

	(Component Side)			(Solder Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5 V	+5 V supply	4	+5 V	+5 V supply
	5	+5 V	+5 V supply	6	+5 V	+5 V supply
	7	+12 V	+12 V supply	8	+12 V	+12 V supply
	9		Not Used	10		Not Used
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 Disable RAM
BUS CONTROLS AND ADDRESS	25	LOCK/	Bus Lock	26		No Connection
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA	Interrupt Ack	34	AD13/	
INTERRUPTS	35	INT6/		36	INT7/	
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	

Table E-1. Connector P1 Pin Assignments (continued)

	(Component Side)			(Solder Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
ADDRESS	43	ADRE/	Address Bus	44	ADRF/	Address Bus
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/		5Ø	ADR9/	
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2		56	ADR3/	
	57	ADRØ/		58	ADR1/	
DATA	59	DATE/	Data Bus	6Ø	DATF/	Data Bus
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/		66	DAT9/	
	67	DAT6/		68	DAT7/	
	69	DAT4/		7Ø	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DATØ/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12 V	-12 V supply	8Ø	-12 V	-12 V supply
	81	+5 V	+5 V supply	82	+5 V	+5 V supply
	83	+5 V	+5 V supply	84	+5 V	+5 V supply
	85	GND	Signal Gnd	86	GND	Signal GND

E.2 CONNECTOR P2 INFORMATION

The iSBC 86/35 board makes use of lines designated as reserved by IEEE 796 MULTIBUS SPECIFICATION. Table E-2 lists the pin assignments for the P2 connector. Refer to the INTEL MULTIBUS SPECIFICATION for more information on interfacing to auxiliary connector P2.

Table E-2. Auxiliary Connector P2 Pin Assignments

(Component Side)			(Solder Side)		
Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	GND	Ground	2	GND	Ground
3	+5V AUX	+5 volt battery	4	+5V AUX	+5 volt battery
5		Reserved	6		No Connection
7		No Connection	8		No Connection
9		Reserved	1Ø		Reserved
11		No Connection	12		No Connection
13		No Connection	14		Reserved
15		No Connection	16		No Connection
17	PFSN/	Power Fail Sense	18		No Connection
19	PFIN/	P Fail Interrupt	2Ø	MPRO/	Memory Protect
21	GND	Ground	22	GND	Ground
23		No Connection	24		No Connection
25		No Connection	26		No Connection
27		No Connection	28		No Connection
29		No Connection	3Ø		No Connection
31	PLC	Power Line Clock	32	ALE	Bus Master ALE
33		Reserved	34		Reserved
35		Reserved	36		No Connection
37		Reserved	38	AUX RESET/	Reset Switch
39		Reserved	4Ø		Reserved
41		Reserved	42		Reserved
43		Reserved	44		Reserved
45		Reserved	46		Reserved
47		Reserved	48		Reserved
49		Reserved	5Ø		Reserved
51		Reserved	52		Reserved
53		Reserved	54		Reserved
55	ADR16/	Addrss Bus	56	ADR17/	Address Bus
57	ADR14/	Address Bus	58	ADR15/	Address Bus
59		Reserved	6Ø		Reserved

Notes: 1. All odd-numbered pins (1, 3, 5, etc.) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top.

2. Cable connector numbering convention may not agree with board connector numbering convention.

E.3 PARALLEL I/O INTERFACE

The 8255A PPI device (U35) controls the parallel I/O interface at the J1 connector on the iSBC 86/35 board. Table E-3 provides a list of the parallel I/O interface pin assignments. The pin assignments on port C of connector J1 can be readily modified via the jumpers included on the iSBC 86/35 board; refer to table 2-7.

Table E-3. Parallel I/O Connector J1 Pin Assignments

Pin Number	Function	Pin Number	Function
1	Ground	2	Port B, bit 7
3	Ground	4	Port B, bit 6
5	Ground	6	Port B, bit 5
7	Ground	8	Port B, bit 4
9	Ground	1Ø	Port B, bit 3
11	Ground	12	Port B, bit 2
13	Ground	14	Port B, bit 1
15	Ground	16	Port B, bit Ø
17	Ground	18	Port C, bit 3
19	Ground	2Ø	Port C, bit 2
21	Ground	22	Port C, bit 1
23	Ground	24	Port C, bit Ø
25	Ground	26	Port C, bit 4
27	Ground	28	Port C, bit 5
29	Ground	3Ø	Port C, bit 6
31	Ground	32	Port C, bit 7
33	Ground	34	Port A, bit 7
35	Ground	36	Port A, bit 6
37	Ground	38	Port A, bit 5
39	Ground	4Ø	Port A, bit 4
41	Ground	42	Port A, bit 3
43	Ground	44	Port A, bit 2
45	Ground	46	Port A, bit 1
47	Ground	48	Port A, bit Ø
49	Ground	5Ø	EXT INTRØ/or +5 volts if required.

Note: Cable and connector pin numbering conventions may not agree with the pin numbering conventions used on the board edge connectors.

Refer to INTEL MULTIBUS SPECIFICATION for part numbers and the types of cable that may be used to interface the parallel port I/O to a user application. Any functional and electrical equivalent may be substituted. To obtain maximum reliability, limit the length of the parallel I/O cable to 3 meters (about 1Ø feet) or less.

E.4 SERIAL I/O INTERFACE

The serial I/O interfaces on the iSBC 86/35 board at connector J2 provide EIA RS232C standard interfacing capability. Connector J2 is a 13/26-pin connector providing an RS232C-compatible interface. The iSBC 86/35 board requires a serial I/O cable and connectors for the J2 connector. The configuration of the cable and connectors depends on the type of interfacing application. However, an RS232C interface requires a 26-pin edge connector, a 25-conductor flat ribbon cable, and a 25-pin RS232C connector.

When assembling the RS232C interface cable, ensure that pin-26 of the edge connector is not connected to a conductor in the flat cable, and ensure that pin 2 of the edge connector is connected to pin 1 of the J2 connector on the iSBC 86/35 board. Table E-4 lists the pin assignments of the serial I/O connector. Refer to INTEL MULTIBUS SPECIFICATION for part numbers and types of cable that may be used to interface the serial I/O port to a user application..

E.5 iSBX™ BUS INTERFACE

The iSBC 86/35 board contains two iSBX (single board expansion) bus connectors (J3 and J4) that allow on-board expansion using iSBX MULTIMODULE boards.

Table E-5 provides the iSBX bus connector pin assignments as found on both J3 and J4. The connectors have identical pin assignments, functions, and physical layout.

Table E-4. Serial I/O Connector J2 Pin Assignments

Pin Number J2	RS232C	RS232C Function	8251 PCI Function
1	14	Not Used	Not Used
2	1	Ground	Ground
3	15	Not Used	Not Used
4	2	Transmit Data	RxD input
5	16	Sec Receive	Selectable
6	3	Receive Data	TxD Output
7	17	External Clock	TxC/RxC Input
8	4	Request To Send	CTS/ Input
9	18	Not Used	Not Used
1Ø	5	Clear To Send	RTS/ Output
11	19	Not Used	Not Used
12	6	Data Set Ready	DTR/ Output
13	2Ø	Data Terminal Ready	DSR/ Input
14	7	Ground	Ground
15	21	Not Used	Not Used
16	8	Not Used	Not Used
17	22	Not Used	Not Used
18	9	Not Used	Not Used
19	23	-12 volts DC	Not Connected
2Ø	1Ø	Not Used	Not Used
21	24	Tran Sig Ele Timing	Selectable
22	11	+12 volts DC	Not Connected
23	25	+5 volts DC	Not Connected
24	12	Not Used	Not Used
25	N/C	Ground	Not Connected
26	13	Secondary CTS	Selectable

Note: Board edge connector pin numbering and external connector pin numbering conventions may not agree.

Table E-5. iSBX™ Bus Connector J3 and J4 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+12V	+12 volts	2	-12V	-12 volts
3	GND	Ground	4	+5V	+5 volts
5	MRESET	Module Reset	6	MCLK	Module Clock
7	MA2	Address Bit 2	8	MPST/	Module Present
9	MA1	Address Bit 1	1Ø		Reserved
11	MAØ	Address Bit Ø	12	MINTR1	Module Interrupt 1
13	IOWRT/	I/O Write Command	14	MINTRØ	Module Interrupt 2
15	IORD/	I/O Read Command	16	MWAIT/	Wait-state Request
17	GND	Ground	18	+5V	+5 volts
19	MD7	Module Data Bit 7	2Ø	MCS1/	Module Chip Select 1
21	MD6	Module Data Bit 6	22	MCSØ/	Module Chip Select Ø
23	MD5	Module Data Bit 5	24		Reserved
25	MD4	Module Data Bit 4	26		No Connection
27	MD3	Module Data Bit 3	28	OPT1	Option Line 1
29	MD2	Module Data Bit 2	3Ø	OPTØ	Option Line Ø
31	MD1	Module Data Bit 1	32		No Connection
33	MDØ	Module Data Bit Ø	34		No Connection
35	GND	Ground	36	+5V	+5 volts
37	MDE	Module Data Bit E	38	MDF	Module Data Bit F
39	MDC	Module Data Bit C	4Ø	MDD	Module Data Bit D
41	MDA	Module Data Bit A	42	MDB	Module Data Bit B
43	MD8	Module Data Bit 8	44	MD9	Module Data Bit 9

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APPENDIX F. RAM MULTIBUS® ADDRESS DECODE PROM

Table F-1 lists the contents of the RAM MULTIBUS Address decode PROM. The first three HEX digits represent the address to the PROM.

Table F-1. PROM Memory Map

Starting Address 4ØØØØH																
SPARE			ØØØ	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			Ø1Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			Ø2Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			Ø3Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
86/35 AND 3Ø4			Ø4Ø	F	2	F	2	F	6	F	6	F	F	F	F	5	F	5	F
86/35 AND 3Ø4			Ø5Ø	F	2	F	2	F	6	F	6	F	F	F	F	5	F	5	F
86/35 AND 3Ø4			Ø6Ø	F	2	F	2	F	6	F	6	F	F	F	F	5	F	5	F
86/35 AND 3Ø4			Ø7Ø	F	2	F	2	F	6	F	6	F	F	F	F	5	F	5	F
SPARE			Ø8Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
86/35 AND 314.	END	DFFFFH.	Ø9Ø	F	2	F	2	4	6	4	6	1	F	1	F	5	F	5	F
86/35 AND 314.	END	EFFFFH.	ØAØ	F	2	Ø	2	4	6	4	6	1	F	1	F	5	F	5	F
86/35 AND 314.	END	FFFFFH.	ØBØ	Ø	2	Ø	2	4	6	4	6	1	F	1	F	5	F	5	F
86/35 ALONE			ØCØ	F	2	F	2	F	6	F	6	F	F	F	F	F	F	F	F
86/35 ALONE			ØDØ	F	2	F	2	F	6	F	6	F	F	F	F	F	F	F	F
86/35 ALONE			ØEØ	F	2	F	2	F	6	F	6	F	F	F	F	F	F	F	F
86/35 ALONE			ØFØ	F	2	F	2	F	6	F	6	F	F	F	F	F	F	F	F
Starting Address 1ØØØØH																
SPARE			1ØØ	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			11Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			12Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			13Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
86/35 AND 3Ø4			14Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	7	5	F
86/35 AND 3Ø4			15Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	7	5	F
86/35 AND 3Ø4			16Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	7	5	F
86/35 AND 3Ø4			17Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	7	5	F
SPARE			18Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
86/35 AND 314.	END	DFFFFH.	19Ø	F	2	F	2	4	6	4	6	1	3	1	3	5	7	5	F
86/35 AND 314.	END	EFFFFH.	1AØ	F	2	Ø	2	4	6	4	6	1	3	1	3	5	7	5	F
86/35 AND 314.	END	FFFFFH.	1BØ	Ø	2	Ø	2	4	6	4	6	1	3	1	3	5	7	5	F
86/35 ALONE			1CØ	F	2	F	2	F	6	F	6	F	3	F	3	F	7	F	F
86/35 ALONE			1DØ	F	2	F	2	F	6	F	6	F	3	F	3	F	7	F	F
86/35 ALONE			1EØ	F	2	F	2	F	6	F	6	F	3	F	3	F	7	F	F
86/35 ALONE			1FØ	F	2	F	2	F	6	F	6	F	3	F	3	F	7	F	F

Table F-1. PROM Memory Map (continued)

Starting Address 2ØØØØH																
SPARE			2ØØ	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			21Ø	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			22Ø	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			23Ø	F	F	F	F	F	F	F	F	F	F	F	F	F
86/35 AND 3Ø4			24Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	F	5	F
86/35 AND 3Ø4			25Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	F	5	F
86/35 AND 3Ø4			26Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	F	5	F
86/35 AND 3Ø4			27Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	F	5	F
SPARE			28Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
86/35 AND 314.	END	DFFFFH.	29Ø	F	2	F	2	4	6	4	6	1	3	1	3	5	F	5	F
86/35 AND 314.	END	EFFFFH.	2AØ	F	2	Ø	2	4	6	4	6	1	3	1	3	5	F	5	F
86/35 AND 314.	END	FFFFFH.	2BØ	Ø	2	Ø	2	4	6	4	6	1	3	1	3	5	F	5	F
86/35 ALONE			2CØ	F	2	F	2	F	6	F	6	F	3	F	3	F	F	F	F
86/35 ALONE			2DØ	F	2	F	2	F	6	F	6	F	3	F	3	F	F	F	F
86/35 ALONE			2EØ	F	2	F	2	F	6	F	6	F	3	F	3	F	F	F	F
86/35 ALONE			2FØ	F	2	F	2	F	6	F	6	F	3	F	3	F	F	F	F
Starting Address ØØØØØH																
SPARE			3ØØ	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			31Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			32Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SPARE			33Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
86/35 AND 3Ø4			34Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	7	5	7
86/35 AND 3Ø4			35Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	7	5	7
86/35 AND 3Ø4			36Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	7	5	7
86/35 AND 3Ø4			37Ø	F	2	F	2	F	6	F	6	F	3	F	3	5	7	5	7
SPARE			38Ø	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
86/35 AND 314.	END	DFFFFH.	39Ø	F	2	F	2	4	6	4	6	1	3	1	3	5	7	5	7
86/35 AND 314.	END	EFFFFH.	3AØ	F	2	Ø	2	4	6	4	6	1	3	1	3	5	7	5	7
86/35 AND 314.	END	FFFFFH.	3BØ	Ø	2	Ø	2	4	6	4	6	1	3	1	3	5	7	5	7
86/35 ALONE			3CØ	F	2	F	2	F	6	F	6	F	3	F	3	F	7	F	7
86/35 ALONE			3DØ	F	2	F	2	F	6	F	6	F	3	F	3	F	7	F	7
86/35 ALONE			3EØ	F	2	F	2	F	6	F	6	F	3	F	3	F	7	F	7
86/35 ALONE			3FØ	F	2	F	2	F	6	F	6	F	3	F	3	F	7	F	7

***

APPENDIX G. PAL EQUATIONS

The iSBC 86/35 board is equipped with four Programmable Array Logic (PAL) devices U25, U36, U45, and U46. These devices are programmed at the factory to perform specific functions. The tables in this appendix give the equations used to determine the function of the devices. Table G-1 lists the equations for Bus decode PAL U25, Table G-2 lists the equations for I/O decode PAL U36, Table G-3 lists the equations for PROM decode PAL U45, Table G-4 lists the equations for the standard RAM Decode PAL U46, and Table G-5 lists the equations for optional RAM decode PAL U46 as used with the iSBC 314 RAM Expansion MULTIMODULE board. This PAL is shipped from the factory with the iSBC 314 RAM Expansion MULTIMODULE board.

EPROM decode PAL U45 and RAM decode PAL U46 are socketed, allowing you to replace them with differently programmed PALs to meet special requirements. Examples of some of these are presented in this appendix.

For the correct syntax of PAL equations for your PAL programmer, refer to its reference manual.

Table G-1. Bus Decode PAL U25 Equations

```
BUS DECODE PAL FOR iSBC 86/35

NONBD NBSAEN NFINTA DEN59 DTR NTMOUT NBINTA XACK NINTA GND
NBMRDC ABØ 13 BDTR BUSACK LINTA WORD INTAC T54 VCC

LINTA  =   /NBSAEN * /NBINTA +
           /NONBD * /NINTA
BDTR   =   NBSAEN * /NBMRDC +
           /NBSAEN * DTR
BUSACK =   XACK * /NBSAEN +
           DEN59 * T54 +
           /NFINTA * T54 +
           /NTMOUT
WORD   =   /ABØ + INTAC * /DEN59 * /NBSAEN
```

Table G-2. I/O Decode PAL U36 Equations

```
I/O DECODE PAL FOR THE iSBC 86/35

NMPRES2 A6 A4 NMPRES1 A7 A5 7 SBX28 SBX18 GND
IOADDR NBHE /SBX11 /SBX1Ø /SBX21 /SBX2Ø /IO12 /IOACCT AØ VCC

IØ12    =  A7 * A6 * /A5 * /IOADDR

SBX21   =  A7 * /A6 * A5 * /A4 * /NBHE * /IOADDR * /SBX28 * /NMPRES2 +
           A7 * /A6 * A5 * A4 * /AØ * /IOADDR * SBX28 * /NMPRES2

SBX2Ø   =  A7 * /A6 * A5 * /A4 * /AØ * /IOADDR * /NMPRES2

SBX11   =  A7 * /A6 * /A5 * /A4 * /NBHE * /IOADDR * /SBX18 * /NMPRES1 +
           A7 * /A6 * /A5 * A4 * /AØ * /IOADDR * SBX18 * /NMPRES1

SBX1Ø   =  A7 * /A6 * /A5 * /A4 * /AØ * /IOADDR * /NMPRES1

IOACCT  =  A7 * A6 * /A5 +
           A7 * /A6 * /A5 * /NMPRES1 +
           A7 * /A6 * A5 * /NMPRES2
```

Table G-3. PROM Decode PAL U45 Equations

```
PROM DECODE PAL FOR THE iSBC 86/35


SZ1 SZØ AE AF A1Ø A11 A13 A12 MEM GND
11 12 13 BANK1 BANKØ WINDOW PRMACC AC AD VCC

PRMACC =   MEM * A13 * A12 * A11 * A1Ø * AF * SZ1 * SZØ +
           MEM * A13 * A12 * A11 * A1Ø * SZ1 * /SZØ +
           MEM * A13 * A12 * A11 * /SZ1 * SZØ +
           MEM * A13 * A12 * /SZ1 * /SZØ

BANKØ =    MEM * A13 * A12 * A11 * A1Ø * AF * /AE * SZ1 * SZØ +
           MEM * A13 * A12 * A11 * A1Ø * /AF * SZ1 * /SZØ +
           MEM * A13 * A12 * A11 * /A1Ø * /SZ1 * SZØ +
           MEM * A13 * A12 * /A11 * /SZ1 * /SZØ

BANK1 =    MEM * A13 * A12 * A11 * A1Ø * AF * AE * SZ1 * SZØ +
           MEM * A13 * A12 * A11 * A1Ø * AF * SZ1 * /SZØ +
           MEM * A13 * A12 * A11 * A1Ø * /SZ1 * SZØ +
           MEM * A13 * A12 * A11 * /SZ1 * /SZØ

WINDOW = VCC
```

Example 1: Changing the EPROM sizes that the iSBC 86/35 accepts.

You can make the iSBC 86/35 board accept 2716, 2732, 2764, or 27128 EPROM devices by replacing the PRMACC, BANKØ, and BANK1 equations in PAL U45 with the following:

```
PRMACC =  MEM * A13 * A12 * A11 * A1Ø * AF * AE * AD * SZ1 * SZØ +
          MEM * A13 * A12 * A11 * A1Ø * AF * AE * SZ1 * /SZØ +
          MEM * A13 * A12 * A11 * A1Ø * AF * /SZ1 * SZØ +
          MEM * A13 * A12 * A11 * A1Ø * /SZ1 * /SZØ

BANKØ =   MEM * A13 * A12 * A11 * A1Ø * AF * AE * AD * /AC * SZ1 * SZØ +
          MEM * A13 * A12 * A11 * A1Ø * AF * AE * /AD * SZ1 * /SZØ +
          MEM * A13 * A12 * A11 * A1Ø * AF * /AE * /SZ1 * SZØ +
          MEM * A13 * A12 * A11 * A1Ø * /AF * /SZ1 * /SZØ

BANK1 =   MEM * A13 * A12 * A11 * A1Ø * AF * AE * AD * AC * SZ1 * SZØ +
          MEM * A13 * A12 * A11 * A1Ø * AF * AE * AD * SZ1 * /SZØ +
          MEM * A13 * A12 * A11 * A1Ø * AF * AE * /SZ1 * SZØ +
          MEM * A13 * A12 * A11 * A1Ø * AF * /SZ1 * /SZØ
```

The jumpering to select the EPROM type would then be as follows:

	Jumper	
Device	FROM	TO
2716	-	-
2732	E124	E125
2764	E123	E124
27128	E124	E125
	E123	E124

Table G-4. RAM Decode PAL U46 Equations

```
RAM DECODE PAL WITH COMMANDS FOR 86/35 AND FOR 86/35 + 3Ø4

CMDQ ALE SZ ADEN A1Ø A11 A13 A12 MEM GND
LS1 DPREQ MBØ AF NDPRD MEMCMD RAMACC LSØ NDPWT VCC

IF (VCC) /MEMCMD =   /CMDQ +
                     /MEM +
                     LS1 * LSØ
IF (VCC) /NDPWT =    CMDQ * MEM * LS1 * /LSØ
IF (VCC) /NDPRD =    CMDQ * MEM * /LS1
IF (VCC) /RAMACC =   /MEM +
                     A13 * A12 +
                     A13 * /A12 * A11 +
                     A13 * /A12 * /A11 * SZ +
                     MBØ * A13 +
                     MBØ * A12 +
                     MBØ * A11


IF (VCC) /DPREQ = MEMCMD * /ALE * ADEN * /A13 * /A12 * /A11 +
                  MEMCMD * /ALE * ADEN * /MBØ * /A13 +
                  MEMCMD * /ALE * ADEN * /MBØ * A13 * /A12 * /A11 * /SZ
```

Table G-5. Optional RAM Decode PAL U46 Equations

```
RAM DECODE PAL WITH COMMANDS FOR 86/35 + 314 ONLY

CMDQ ALE SZ ADEN A1Ø A11 A13 A12 MEM GND
LS1 DPREQ MBØ AF NDPRD MEMCMD RAMACC LSØ NDPWT VCC

IF (VCC) /MEMCMD =   /CMDQ +
                     /MEM +
                     LS1 * LSØ
IF (VCC) /NDPWT =    CMDQ * MEM * LS1 * /LSØ
IF (VCC) /NDPRD =    CMDQ * MEM * /LS1
IF (VCC) /RAMACC =   /MEM +
                     A13 * A12 * A11 * A1Ø +
                     A13 * A12 * A11 * SZ +
                     MBØ * A13 +
                     MBØ * A12 +
                     MBØ * A11


IF (VCC) /DPREQ = MEMCMD * /ALE * ADEN * /A13 * /A12 * /A11 +
                  MEMCMD * /ALE * ADEN * /MBØ * /A13 +
                  MEMCMD * /ALE * ADEN * /MBØ * /A12 +
                  MEMCMD * /ALE * ADEN * /MBØ * /A11 +
                  MEMCMD * /ALE * ADEN * /MBØ * /A1Ø * /SZ
```

Example 2: Using the signal designated as WINDOW to reduce the number of I/O writes when a 2Ø-bit address board is used in a 24-bit address system.

Assume, for the purpose of this example, that the system consists of three boards; the iSBC 86/35 board (RAM local address range of ØØØØØ to 7FFFFH), a 512 K-byte memory board that recognizes 24-bit addresses and is located on Mbyte page 4 at addresses 8ØØØØ to FFFFFH, and a peripheral board with 64 K-byte of RAM that recognizes only 2Ø-bit addresses and is located at address 9ØØØØH to 9FFFFH. Note that if the iSBC 86/35 board were to access Mbyte page 4 in the range 9ØØØØ to 9FFFFH, both boards could respond, resulting in a failure. A likely tradeoff is to consider the 64 K-byte address range between 9ØØØØH and 9FFFFH on the 512 K-byte memory board to be inaccessible. This can be accomplished by setting the Megabyte page register to something other than 4 whenever the 64 K-byte peripheral board is accessed. There are three ways to implement this:

1. Using I/O writes to the status register and Megabyte page register, you can change the contents of the Megabyte Page register before and after every access to the 512 K-byte memory board.

2 Using I/O writes to the status register, you can disable the Megabyte page register drivers whenever the 512 K-byte memory board is accessed. Because the passive state of the upper four address lines on MULTIBUS connector P2 corresponds to page Ø, the 512 K-byte memory board will not respond.

3. Replace PAL U45 with a PAL programmed to drive the WINDOW signal low whenever the range 9ØØØØ to 9FFFFH is addressed. This automatically disables the Megabyte page drivers, preventing the 512 K-byte memory board from responding, all without using I/O writes before and after every access to the 512 K-byte memory board. The contents of the Megabyte page register still requires initializing.

In all three cases, it would be beneficial to modify PAL U46 to prevent the MBØ signal from disabling local access to some on-board RAM. This modification is described in Example 3 of this appendix. The replacement equation for the WINDOW term in PAL U45 to implement the specific example previously described is as follows:

```
WINDOW = /A13 + A12 + A11 + /AlØ
```

Example 3: Preventing MBØ from disabling on-board RAM.

As explained in Chapter 2, enabling the Megabyte page drivers automatically disables local access to on-board RAM between addresses 2ØØØØH and 7FFFFH (in the case of the iSBC 86/35 board without an expansion MULTIMODULE). MBØ is the input to PAL U46 that disables this range of memory. In some cases, it may be desirable to enable the Megabyte page drivers permanently (by removing jumpers E297 to E298 and E238 to E239) without disabling local access to any on-board RAM. PAL U46 could be replaced with a PAL that implements the RAMACC and DPREQ equations as follows:

```
IF (VCC) /RAMACC =   /MEM +
                     A13 * A12 +
                     A13 * /A12 * A11 +
                     A13 * /A12 */A11 * SZ

IF (VCC) /DPREQ =    MEMCMD * /ALE * ADEN * /A13 * /A12 * /A11 +
                     MEMCMD * /ALE * ADEN * /A13 +
                     MEMCMD * /ALE * ADEN * A13 * /A12 * /A11 + /SZ
```

A similar modification could be made to the PAL that is used at U46 when the iSBC 314 RAM Expansion MULTIMODULE is installed.

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