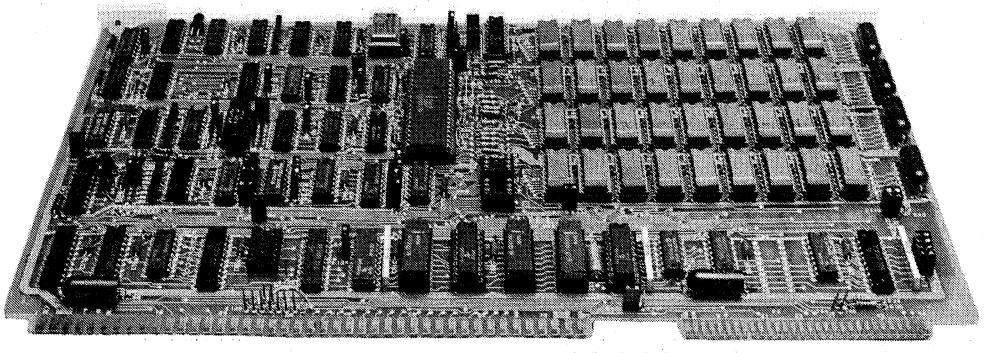
iSBC® 028A/056A RAM MEMORY BOARDS

- **iSBC 86, iSBC 88 and iSBC 80 Board RAM Expansion through Direct MULTIBUS® Interface**
- **128K or 256K Bytes of Read/Write Memory**
- **On-Board Parity Generator/Checker and Error Status Register**
- **Requires a Single +5V Power Supply**
- **Assignable Anywhere within a 16 Megabyte Address Space**
- **Jumper Selectable Base Address on Any 4K Byte Boundary**
- **Auxiliary Power Bus and Memory Protect Control Logic for Battery Backup RAM Requirements**

The iSBC 028A and iSBC 056A RAM memory boards are members of Intel's complete line of iSBC memory and I/O expansion boards. Each board interfaces directly to any iSBC 80, iSBC 88 or iSBC 86 Single Board Computer via the MULTIBUS interface to expand system RAM capacity. The iSBC 028A and iSBC 056A boards contain 128K, or 256K bytes of read/write memory implemented using dynamic RAM components. An on-board LSI dynamic RAM controller refreshes a portion of these components every 14 microseconds. Each refresh cycle utilizes memory for 480 nanoseconds (maximum).

The iSBC 028A and iSBC 056A boards generate byte oriented parity during all write operations and perform parity checking during all read operations. When a parity error is detected, these boards can generate an interrupt on the MULTIBUS interface. In addition, the row and bank of the RAM array containing the error are stored in a Parity Flag Register (see Figure 1). This register is accessible as a MULTIBUS I/O port. An on-board LED also provides a visual indication that a parity error has occurred. To facilitate testing of these boards, parity generation and checking can be changed from even to odd under software control.



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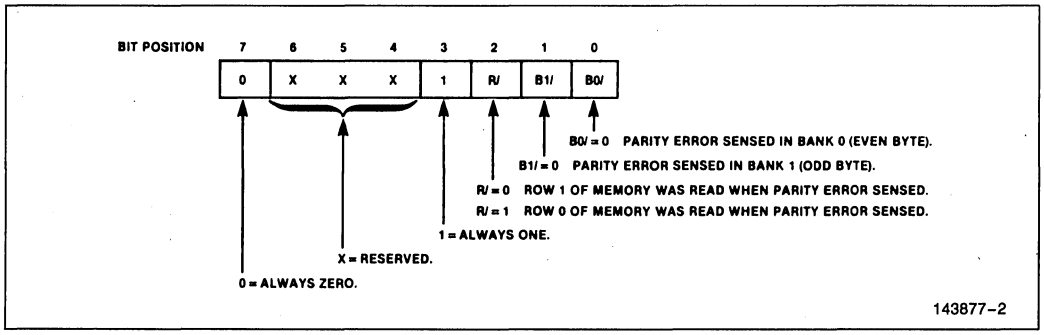

Figure 1. Parity Flag Register Format

SPECIFICATIONS

Word Size

8 bits and 16 bits

Memory Size

131,072 bytes (iSBC 028A); or 262,144 bytes (iSBC 056A)

Access Time

iSBC 028A
500 ns max. (worst case)
460 ns max. (typical)

iSBC 056A
570 ns max. (worst case)
530 ns max. (typical)

Cycle Times (Worst Case)

Read
iSBC 028A—600 ns max.
iSBC 056A—650 ns max.

Write
iSBC 028A—600 ns max.
iSBC 056A—650 ns max.

Refresh
iSBC 028A—480 ns max.
iSBC 056A—600 ns max.

Interface

All address, data and command signals are TTL compatible.

Address Selection

Memory—Base address is jumper selectable on any 4K byte boundary in a 16 megabyte address space. On-board RAM cannot cross a megabyte address boundary.

Parity Flag Register—The I/O address of the Parity Flag Register is jumper selectable to be between 00H to 0FH or 40H to 4FH.

Connector

Edge connector—86 pin double-sided PC edge connector with 0.156 in. contact centers.

Mating connector—Viking 3KH43/9AMK12 or equivalent.

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM array for system requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz. (397 gm)

Electrical Characteristics

D.C. POWER REQUIREMENTS

All configurations require only +5V ±5%.

Normal System Operation (max.)
iSBC 028A/056A—4.57A (worst case)
3.66A (typical)

Auxiliary Power No RAM Access (max.)
iSBC 028A/056A—0.55A (worst case)
0.45A (typical)

Environmental Characteristics

Operating Temperature: 0°C to +55°C
Relative Humidity: to 90% (without condensation)

Reference Manual

143572-001— iSBC 032A/064A/028A/056A Hardware Reference Manual (not supplied)

Manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Dept., 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 028A	128K-Byte RAM Board with Parity
SBC 056A	256K-Byte RAM Board with Parity